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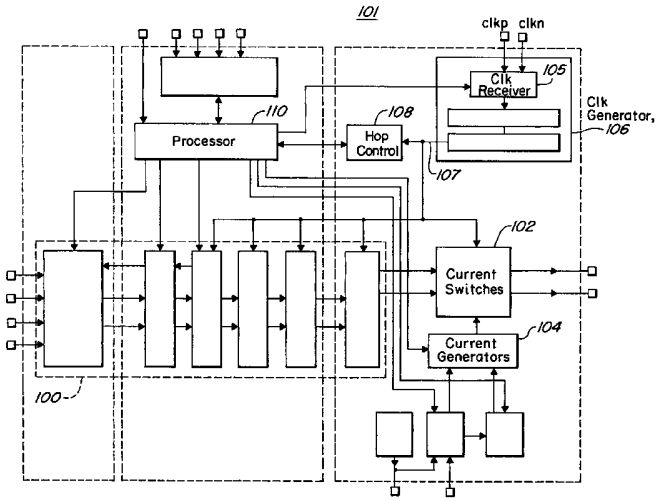
(54) Title: CONTROL LOOP FOR MINIMAL TAILNODE EXCURSION OF DIFFERENTIAL SWITCHES



(57) Abstract: A system and method are provided for controlling the on/off timing relationship between two transistors in a differential that are connected at a tail node to a common current generator. The on/off timing relationship is controlled by on/off signals that control the state of the transistors such that one transistor turns one while the other is turning off. An overlap signal is derived from the tail node excursion and is indicative of whether the on/off signals are overlapping too much or too little. A control signal is generated based on the overlap signal. The timing of driver signals used to drive the on/off signals is adjusted based on the control signal. When more overlap is needed, the timing of the driver signals is adjusted such that there is more overlap of the derived on/off signals. When less overlap is needed, the timing of the driver signals is adjusted such that there is less overlap of the derived on/off signals. An embodiment that adjusts the voltage of the on/off signals to control the on/off timing is also disclosed.

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CONTROL LOOP FOR MINIMAL TAILNODE EXCURSION OF DIFFERENTIAL SWITCHES

PRIORITY INFORMATION

This application claims priority to U.S. Patent Application Serial Number 10/217,842 filed August 13, 2002, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

The invention relates to the field of control loops, and in particular to a control loop to control the on/off timing of differential switches.

Differential switches in which one transistor is turned off while the other is turned on so as to steer a common current along a particular path are used in a number of devices. One such device is a differential current steering digital-to-analog converter (DAC). Generally, a differential current steering DAC is a device that converts a digital value into a differential current by steering an amount of current out one or the other output of a differential output pair depending on the value of each bit in the digital word. When using such differential switches in a differential current steering DAC or other device, it is important to control the on/off timing relationship between the two transistors.

SUMMARY OF THE INVENTION

In one aspect, the present invention provides a control loop for controlling the on/off timing relationship between two transistors in a differential switch that are connected at a tail node to a common current generator. The on/off timing relationship is controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off. The control loop comprises a controller and a clock generator. The controller receives an overlap signal indicative of whether the on/off signals are overlapping too much or too little. The overlap signal is derived from the tail node excursion. The clock generator receives a control signal from the controller. The control signal is based on the overlap signal and causes the clock generator to adjust the timing of driver signals used to derive the

on/off signals. When more overlap of the on/off signals is needed, the control signal causes the clock generator to adjust the timing of the driver signals such that there is more overlap of the derived on/off signals. When less overlap of the on/off signals is needed, the control signal causes the clock generator to adjust the timing of the driver signals such that there is less overlap of the derived on/off signals.

Another aspect of the present invention provides a method of controlling the on/off timing relationship between two transistors in a differential switch that are connected at a tail node to a common current generator. The on/off timing relationship is controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off. An overlap signal is derived from the tail node excursion. The overlap signal is indicative of whether on/off signals are overlapping too much or too little. A control signal is generated based on the overlap signal. The timing of driver signals used to derive the on/off signals is adjusted based on the control signal. When more overlap of the on/off signals is needed, the timing of the driver signals is adjusted such that there is more overlap of the derived on/off signals. When less overlap of the on/off signals is needed, the timing of the driver signals is adjusted such that there is less overlap of the derived on/off signals.

An alternative way to control the on/off timing relationship between transistors 202 is to adjust the voltage levels of the on/off signals. In this embodiment, the present invention provides a control loop to control the on/off timing relationship between two transistors in a differential switch that are connected at a tail node to a common current generator. The on/off timing relationship of the transistors is controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off. The control loop comprises a controller and at least one switch driver. The controller receives an overlap signal indicative of whether the on/off timing of the transistors is overlapping too much or too little. The overlap signal is derived from the tail node excursion. The switch driver receives a control signal from the controller, wherein the control signal is based on the overlap signal and causes the switch driver to adjust the voltage of the on/off signals. When more on/off overlap is needed, the control signal causes the switch driver to adjust the voltage of the on/off signals such that there is more overlap

of the transistors' on/off timing. When less on/off overlap is needed, the control signal causes the switch driver to adjust the voltage of the on/off signals such that there is less overlap of the transistors' on/off timing.

In another aspect of this embodiment, the present invention provides a method of controlling the on/off timing relationship between two transistors in a differential switch that are connected at a tail node to a common current generator. The on/off timing relationship is controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off. An overlap signal is derived from the tail node excursion. The overlap signal is indicative of whether on/off timing is overlapping too much or too little. A control signal is generated based on the overlap signal. The voltage of the on/ff signals is adjusted based on the control signal. When more overlap of the on/off timing is needed, the voltage of the on/off signals is adjusted such that there is more overlap of the transistors' on/off timing. When less overlap of the on/off timing is needed, the voltage of the on/off signals is adjusted such that there is less overlap of the transistors' on/off timing.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a block diagram of the control loop according to the present invention as used in a differential current steering DAC;

Figure 2a illustrates one embodiment of the present invention that determines the overlap quality by comparing the tail node to a DC reference;

Figure 2b illustrates one embodiment of the present invention that determines the overlap quality from the peak-to-peak excursion of the tail node; and

Figures 3a-3e, collectively, illustrate simulations of various nodes for the embodiment of figure 2a when different values of up_del and dn_del are applied.

DETAILED DESCRIPTION OF THE INVENTION

There is depicted in the drawings, and will herein be described in detail, a differential switch control loop according to the present invention as used with a current steering DAC. The present disclosure, however, is to be considered as an exemplification of the principles of the invention and the associated functional

specifications for its construction, and is not intended to limit the invention to the embodiment(s) illustrated. Those skilled in the art will envision many other possible variations within the scope of the present invention.

Figure 1 illustrates a block diagram of the control loop according to the present invention as used in a differential current steering DAC 101. DAC 101 comprises a matrix of differential current switches 102 that steer current from current generators 104 to output IP or output IN (which form a differential output pair) based on the digital value from pre-processing circuitry 100. Pre-processing circuitry processes digital data into a digital value that is applied to the cells of current switches 102. Each bit of the digital value is latched into the correct cell decoder, and the corresponding transistors are switched as appropriate, based on the timing of a differential clock. While the particular implementation shown uses a differential clock, any type of clock signal can be used.

Generally, a clock generator 106 receives the differential clock as signal clkp and clkn. Clock generator 106 uses the differential clock to generate the driver signals 107 from which the transistor on/off signals in a cell are derived. Clock generator 106 derives the driver signals from output signals output by a clock receiver 105 in clock generator 106. Clock receiver 105 receives the differential clock signal and generates the output signals from the clock signal. Clock receiver 105 is preferably implemented according to the teachings of the copending application entitled "Differential Clock Receiver with Adjustable Output Crossing Point", (Atty. docket no. 6715) filed by common assignee on even date herewith, and incorporated herein by reference.

Driver signals 107 are received by both the current switches 102 (so that the transistor on/off signals can be derived) and by a hop control circuit 108. Hop control circuit 108 determines whether the on/off timing of the transistors is overlapping too much or not enough. The present invention uses the excursion of the tail node (i.e., the common current source node for the transistors of the differential switch) as an indicator of whether the on/off timing is overlapping too much or too little. An overlap signal that is indicative of whether the on/off timing is overlapping too much or too little is derived from the tail node excursion. This signal is sent to processor 110. If the on/off timing is overlapping too much, processor 110 sends a

signal to clock generator 106 that causes it to generate driver signals that result in on/off timing with less overlap. If the on/off timing is not overlapping enough, processor 110 sends a signal to clock generator 106 that causes it to generate driver signals that result in on/off timing with more overlap. This continues until an optimal point is reached.

Figure 2a illustrates one embodiment of the present invention that determines the overlap quality by comparing the tail node to a DC reference. As shown, hop control circuit 108 comprises transistors 202 that form a differential current switch. The differential current switch is a replica of the current switches in the matrix of current switches 102. On/off signals are provided to the gates of transistors 202 by cell decoder 200. The on/off signals control the state of transistors 202 such that one transistor turns on while the other is turning off. The on/off signals are derived from the driver signals, dn and up, supplied by clock generator 106. Transistors 202 are connected at a tail node 207 to a cascoded current generator comprising a current source transistor 204 and cascode transistor 206. While a cascoded current generator has been shown, one of skill in the art would appreciate the present invention is not limited thereto. Also, while the cascoded current generator is shown located in hop control 108, it could be implemented elsewhere, such as with other current generators 104.

A DC reference is set up using transistor 208 and another cascoded current generator comprising transistors 210 and 212. The DC reference is taken at the node 209 and is equivalent to the value that node 207 would be when there is an appropriate amount of overlap between the on/off signals, i.e. when the overlap of the on/off signals is neither too big or too little.

Tail node 207 is compared to DC reference node 209 by comparator 214. A first input 211 of comparator 214 is connected to tail node 207, while a second input 213 of comparator 214 is connected to DC reference node 209. An output 215 of comparator 214 provides an overlap signal indicative of whether the average of tail node 207 is greater than or less than DC reference node 209. When the on/off signals are overlapping too much, the average of tail node 207 is greater than DC reference node 209. Conversely, when the on/off signals are not overlapping enough, the average of tail node 207 is less than DC reference node 209. The output of

comparator 214 is provided to a controller 218 in processor 110. While not necessary, hysterisis 216 is preferably used to provide a "clean" digital signal to controller 118.

Based on output 215, controller 218 determines whether the on/off signals should be overlapped more or less. Controller 218 sends a control signal to clock generator 106 that causes clock generator 106 to adjust the timing of the driver signals, dn and up, that are used by cell decoder 200 to derive the on/off signals. When more overlap is needed, the control signal causes clock generator 106 to adjust the timing such that there is more overlap. Conversely, when less overlap is needed, the control signal causes clock generator 106 to adjust the timing such that there is less overlap. After a preset settling period following the clock generator's adjustment of the timing, controller 218 again determines from output 215 whether the on/off signals should be overlapped more or less, and adjusts the control signal again as appropriate. This cycle is continued until an optimal point is reached.

In the embodiment shown, the control signal comprises two digital words, dn_del and up_del. Decreasing the value of dn_del causes clock generator 106 to decrease the overlap of the driver signals, dn and up, while increasing the value of dn_del increases the overlap of the driver signals. Conversely, decreasing the value of up_delay causes clock generator 106 to increase the overlap of the driver signals, while increasing the value of up_del decreases the overlap of the driver signals. Thus, for example, when the average of tail node 207 is higher than DC reference node 209, the value of dn_del is decreased by one. If the optimal point is not reached, controller 218 continues to decrease dn_del each cycle until dn_del is zero. Controller 218 then increases up_del by one each cycle. While controller 218 has been described as using a particular control algorithm to adjust the timing to an optimal point, it should be noted that other control algorithms can be used. For instance, an alternative control algorithm that can be implemented by controller 218 is a successive approximation algorithm.

Figure 2b illustrates one embodiment of the present invention that determines the overlap quality from the peak-to-peak excursion of the tail node. When the overlap of the on/off timing is at the correct amount, the excursion of the tail node will be at a minimum. As shown, this embodiment is similar to the embodiment of

figure 2a, except that a DC reference is not established and the comparator is replaced by a peak detector 220 followed by an analog-to-digital converter (ADC) 222. Peak detector detects the peak-to-peak swing of tail node 220 in each cycle and outputs an overlap signal indicative of the peak-to-peak value. The overlap signal is converted to a digital value by ADC 222 and provided to controller 218. Based on the current peak value and previous peak value(s), controller 218 attempts to minimize the peak-to-peak excursion of tail node 207 by sending a control signal to clock generator 106 that causes clock generator 106 to adjust the timing of the driver signals, dn and up. Controller 218 continues to cause the timing to be adjusted each cycle until the excursion of tail node 207 is at a minimum. As with the embodiment of figure 2a, clock generator 106 is preferably implemented according to the teachings of the copending application entitled "Differential Clock Receiver with Adjustable Output Crossing Point", filed by common assignee on evendate herewith. Thus, the control signal preferably comprises the two digital words, dn_del and up_del.

Figures 3a-3e illustrate simulations of various nodes for the embodiment of figure 2a when different values of up_del and dn_del are applied. Figure 3a illustrates the values of up_del and dn_del. As shown, from 0 to 450 ns, up_del is being increased, while dn_del is zero. From 450 to about 800 ns, dn_del is being increased, while up_del is zero. Figure 3a shows the corresponding response 300 of tail node 207 along with DC reference node 209. The response 300 of tail node 207 appears as solid black areas and the DC reference can not be seen because of the y-axis is too small in figure 3a. Figure 3e, however, illustrates the response 300 of tail node 207 and response 302 of DC reference node on a time scale that shows the spikes of tail node and DC reference. As shown, DC reference node 209 has a generally static response 302 of about -50 millivolts. When the average of the spikes 302 of tail node is below DC reference 302, comparator 214 has a downward sloping output (illustrated in figure 3c). This occurs until up_del has a value of 20. Then, the average is above DC reference 302 and comparator 214 has an upward sloping output. Once up_del has a value of zero again, the average is below DC reference 302 comparator 214 has an output with a downward slope. As dn_del continues to be increased, the peak of the spikes below DC reference 302 continues to increase,

causing the average to be further below DC reference 302. This causes the downward slope of the comparator output to increase.

An alternative way to control the on/off timing relationship between transistors 202 is to adjust the voltage levels of the on/off signals. In this case, the timing of the on/off signals doesn't change, only the voltage levels, and the current transfer function $I_d = f(V_{gate})$ is used to modulate the on/off timing relation. In this case, controller 218 would receive the overlap signal derived from the tail node excursion and derive a control signal based on the overlap signal. Controller 218 would send the control signal to a switch driver(s) (not shown), which is located within the cell decoder or between cell decoder 200 and transistors 202 (the switch drivers have not been illustrated for simplicity). The control signal would cause the switch driver to adjust the voltage of the on/off signals, such there is more or less overlap of the transistors' on/off timing, as needed. For instance, for the embodiment of figure 2a, if the average of tail node 207 is greater than the DC reference node 209, then the of/off signals' voltage swing is increased. Conversely, if the average of the tail node 207 is less than the DC reference 209, then the on/off signals' voltage swing is decreased.

Although the present invention has been shown and described with respect to several embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A control loop to control the on/off timing relationship between two transistors in a differential switch that are connected at a tail node to a common current generator, the on/off timing relationship of the transistors controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off, the control loop comprising:

a controller to receive an overlap signal indicative of whether the on/off signals are overlapping too much or too little;

wherein the overlap signal is derived from the tail node excursion;

a clock generator to receive a control signal from the controller, wherein the control signal is based on the overlap signal and causes the clock generator to adjust the timing of driver signals used to derive the on/off signals;

wherein when more overlap of the on/off signals is needed, the control signal causes the clock generator to adjust the timing of the driver signals such that there is more overlap of the derived on/off signals; and

wherein when less overlap of the on/off signals is needed, the control signal causes the clock generator to adjust the timing of the driver signals such that there is less overlap of the derived on/off signals.

2. The control loop, as per claim 1, wherein the overlap signal is derived based on a comparison of the tail node to a DC reference node.

3. The control loop, as per claim 2, wherein the comparison is performed using a comparator having a first input connected to the tail node and a second input connected to the DC reference node, wherein an output of the comparator outputs the overlap signal.

4. The control loop, as per claim 3, wherein hysterisis is used with the comparator.

5. The control loop, as per claim 1, wherein the over lap signal is derived based on the peak-to-peak value of the tail node.

6. The control loop, as per claim 5, wherein the peak-to-peak value is measured by a peak detector.

7. The control loop, as per claim 6, wherein the peak-to-peak value measured by the peak detector is converted to a digital value by an analog-to-digital converter and provided to the controller as the overlap signal.

8. The control loop, as per claim 1, wherein the control loop is used in a differential current steering DAC.

9. A system comprising:

a differential switch comprising two transistors that are connected at a tail node to a common current generator, the on/off timing relationship of the transistors controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off;

a comparator having a first input connected to the tail node and a second input connected to a DC reference node;

wherein the value of the DC reference node is equivalent to the value that the tail node would be when there is an appropriate amount of overlap between the on/off signals;

wherein an output of the comparator outputs an overlap signal indicative of whether the average of the tail node is greater than or less than the DC reference node;

a controller having an input connected to the output of the comparator, wherein the controller generates a control signal based on the overlap signal;

a clock generator that generates driver signals from which the on/off signals are derived, wherein the clock generator receives the control signal and adjusts the timing of the driver signals based on the control signal.

10. The system, as per claim 9, wherein hysterisis is used with the comparator.

11. The system, as per claim 9, wherein the control loop is used in a differential current steering DAC.

12. A system comprising:

a differential switch comprising two transistors that are connected at a tail node to a common current generator, the on/off timing relationship of the transistors controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off;

a peak detector having an input connected to the tail node, wherein the peak detector outputs an overlap signal indicative of a peak-to-peak value of the tail node;

an analog-to-digital converter connected to the peak detector to receive the overlap signal and convert the overlap signal to a digital value;

a controller having an input connected to the output of the comparator, wherein the controller generates a control signal based on the overlap signal;

a clock generator that generates driver signals from which the on/off signals are derived, wherein the clock generator receives the control signal and adjusts the timing of the driver signals based on the control signal.

13. The system, as per claim 12, wherein the control loop is used in a differential current steering DAC.

14. A method of controlling the on/off timing relationship between two transistors in a differential switch that are connected at a tail node to a common current generator, the on/off timing relationship controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off, the method comprising:

deriving an overlap signal from the tail node excursion, wherein the overlap signal is indicative of whether on/off signals are overlapping too much or too little;

generating a control signal based on the overlap signal

adjusting the timing of driver signals used to derive the on/off signals based on the control signal;

wherein when more overlap of the on/off signals is needed, the timing of the driver signals is adjusted such that there is more overlap of the derived on/off signals; and

wherein when less overlap of the on/off signals is needed, the timing of the driver signals is adjusted such that there is less overlap of the derived on/off signals.

15. The method, as per claim 14, wherein the overlap signal is derived based on a comparison of the tail node to a DC reference node.

16. The method, as per claim 14, wherein the overlap signal is derived based on the peak-to-peak value of the tail node.

17. The method, as per claim 14, wherein the method is used in a differential current steering DAC.

18. A control loop to control the on/off timing relationship between two transistors in a differential switch that are connected at a tail node to a common current generator, the on/off timing relationship of the transistors controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off, the control loop comprising:

a controller to receive an overlap signal indicative of whether the on/off timing of the transistors is overlapping too much or too little;

wherein the overlap signal is derived from the tail node excursion;

at least one switch driver to receive a control signal from the controller, wherein the control signal is based on the overlap signal and causes the switch driver to adjust the voltage of the on/off signals;

wherein when more on/off overlap is needed, the control signal causes the switch driver to adjust the voltage of the on/off signals such that there is more overlap of the transistors' on/off timing; and

wherein when less on/off overlap is needed, the control signal causes the switch driver to adjust the voltage of the on/off signals such that there is less overlap of the transistors' on/off timing.

19. The control loop, as per claim 1, wherein the overlap signal is derived based on a comparison of the tail node to a DC reference node.

20. The control loop, as per claim 19, wherein the comparison is performed using a comparator having a first input connected to the tail node and a second input connected to the DC reference node, wherein an output of the comparator outputs the overlap signal.

21. The control loop, as per claim 20, wherein hysterisis is used with the comparator.

22. The control loop, as per claim 18, wherein the over lap signal is derived based on the peak-to-peak value of the tail node.

23. The control loop, as per claim 22, wherein the peak-to-peak value is measured by a peak detector.

24. The control loop, as per claim 23, wherein the peak-to-peak value measured by the peak detector is converted to a digital value by an analog–to-digital converter and provided to the controller as the overlap signal.

25. The control loop, as per claim 18, wherein the control loop is used in a differential current steering DAC.

26. A method of controlling the on/off timing relationship between two transistors in a differential switch that are connected at a tail node to a common current generator, the on/off timing relationship controlled by on/off signals that control the state of the transistors such that one transistor turns on while the other is turning off, the method comprising:

deriving an overlap signal from the tail node excursion, wherein the overlap signal is indicative of whether on/off timing is overlapping too much or too little;

generating a control signal based on the overlap signal

adjusting the voltage of the on/ff signals based on the control signal;

wherein when more overlap of the on/off timing is needed, the voltage of the on/off signals is adjusted such that there is more overlap of the transistors' on/off timing; and

wherein when less overlap of the on/off timing is needed, the voltage of the on/off signals is adjusted such that there is less overlap of the transistors' on/off timing.

27. The method, as per claim 26, wherein the overlap signal is derived based on a comparison of the tail node to a DC reference node.

28. The method, as per claim 26, wherein the overlap signal is derived based on the peak-to-peak value of the tail node.

29. The method, as per claim 26, wherein the method is used in a differential current steering DAC.

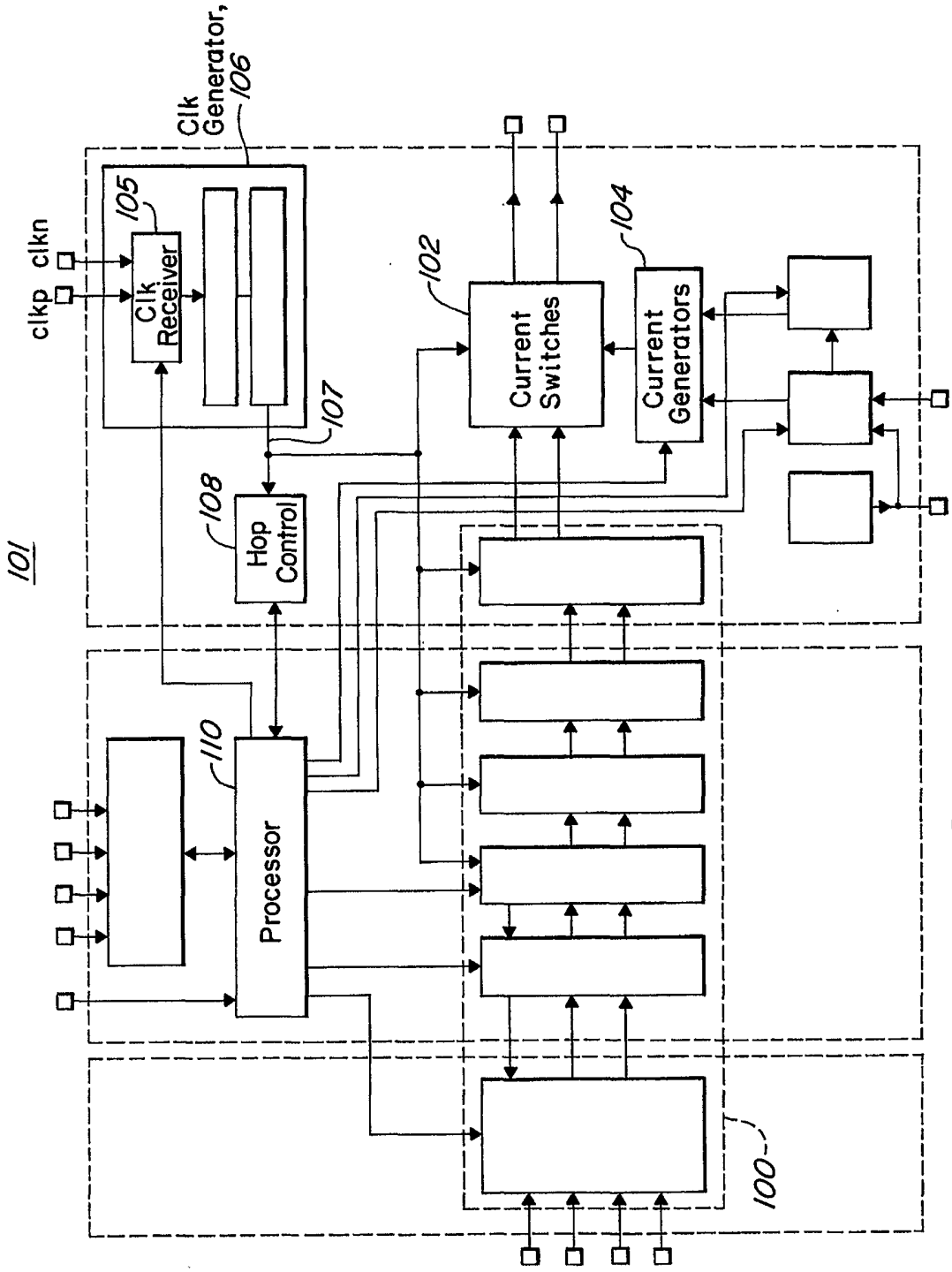
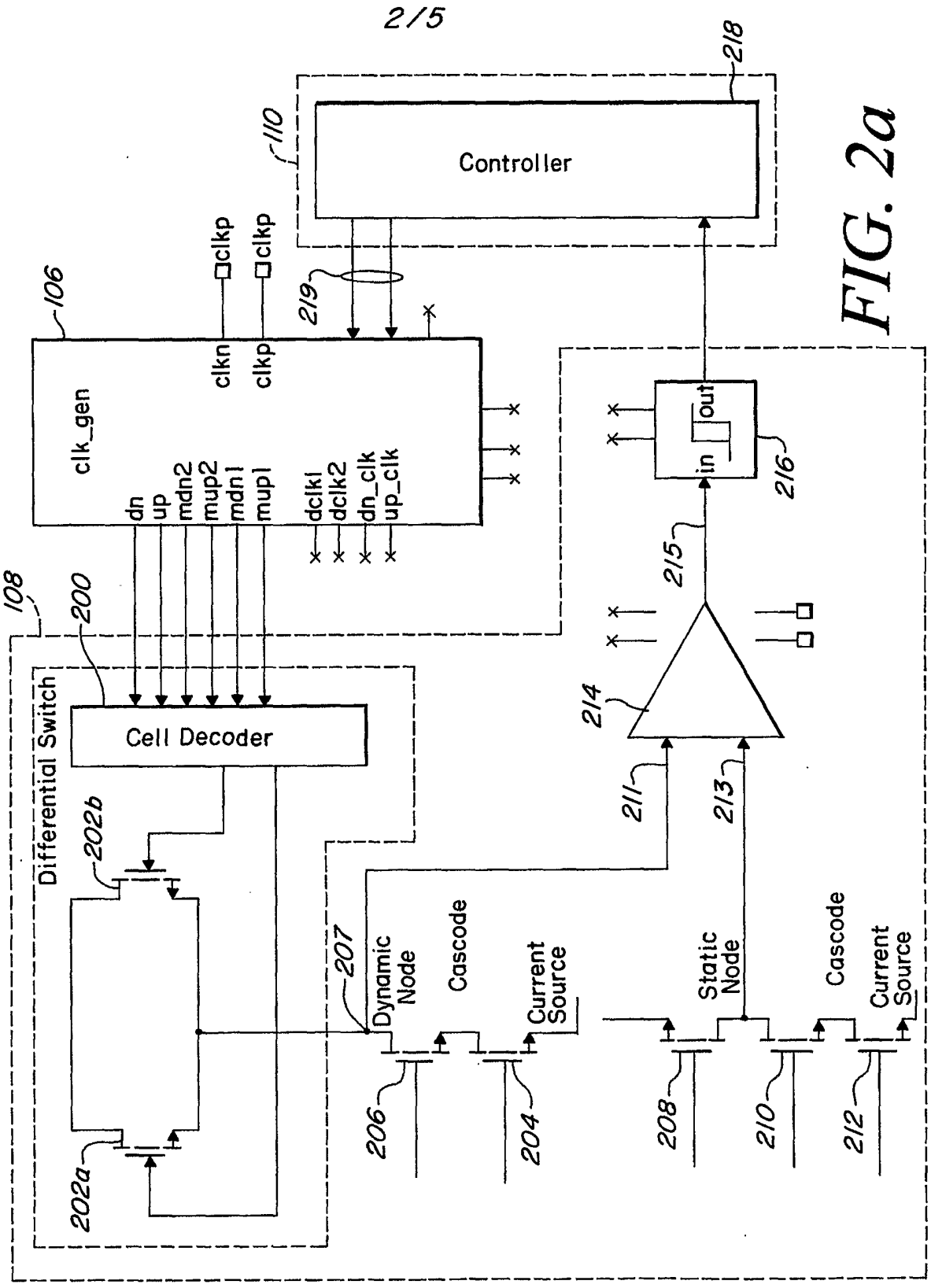

Clk Generator, 106
105
clkp clkn
Clk Receiver
107
102
Current Switches
104
Current Generators
108
Hop Control
101
110
Processor
100

FIG. 1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clkp
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dclk1
dclk2
dn_clk
up_clk
out
in
216
215
108
200
214
Differential Switch
Cell Decoder
211
213
202b
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Dynamic Node
Cascode
Current Source
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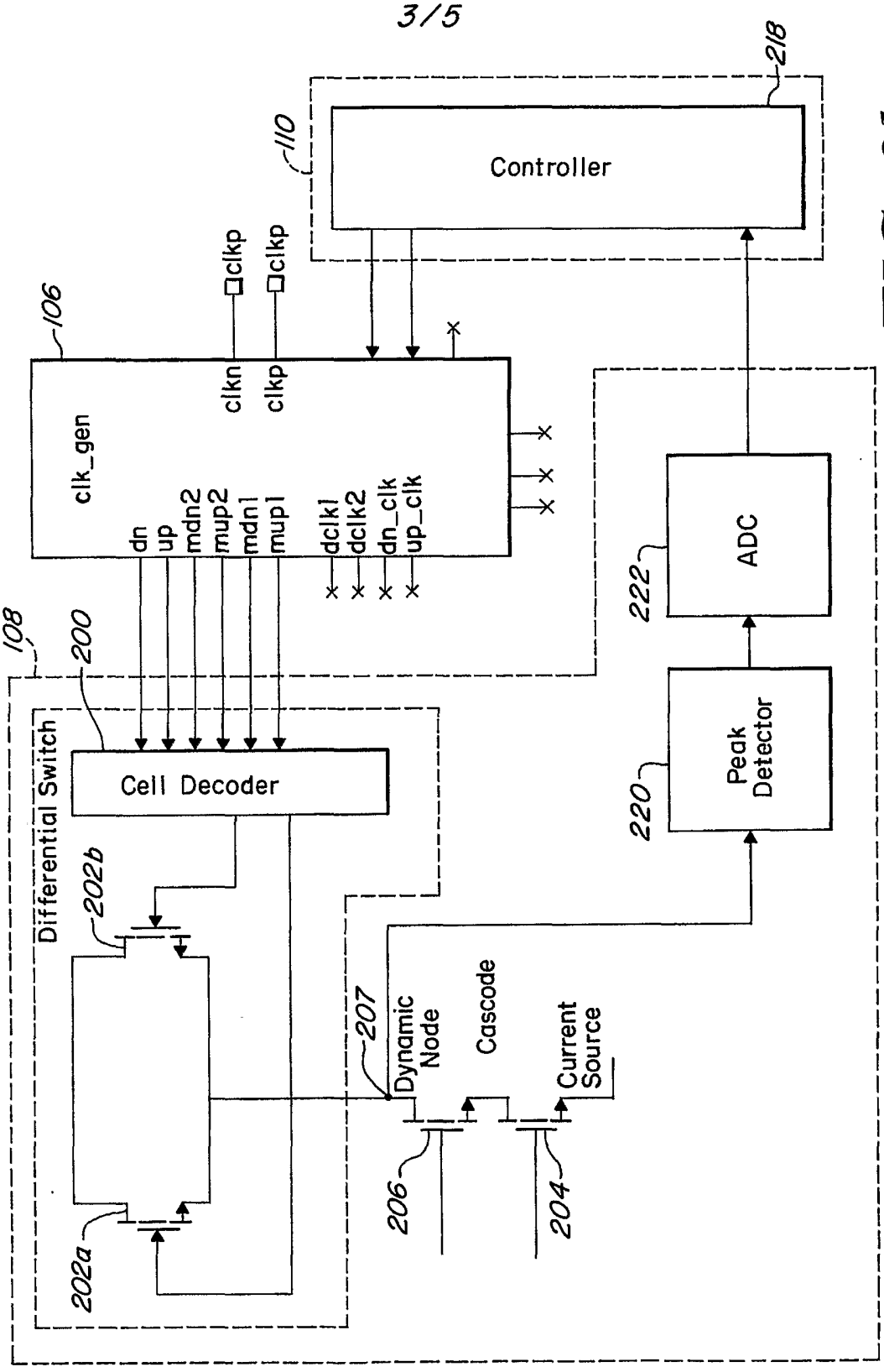
Current Source
206
204
208
210
212
202a

FIG. 2a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clkp
clkp
106
clkn
clkp
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mup2
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dclk1
dclk2
dn_clk
up_clk
222
ADC
108
200
Differential Switch
Cell Decoder
220
Peak Detector
202b
207
Dynamic Node
Cascode
Current Source
206
204
202a

FIG. 2b

FIG. 3a

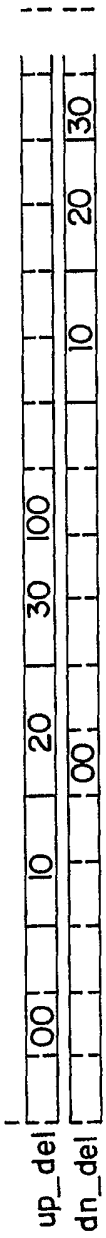


FIG. 3b

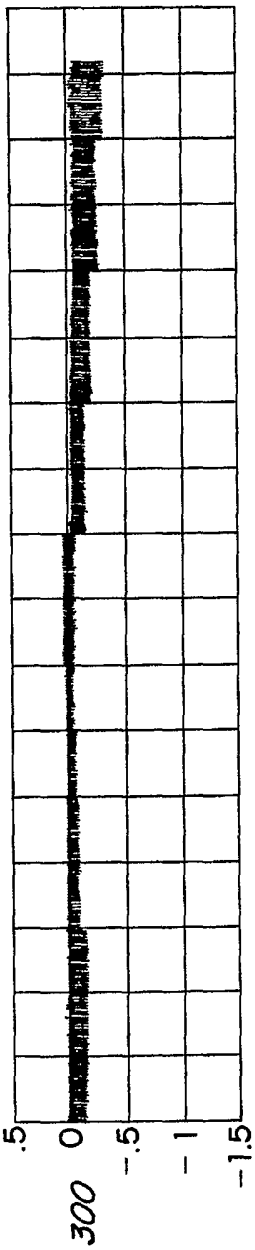


FIG. 3c

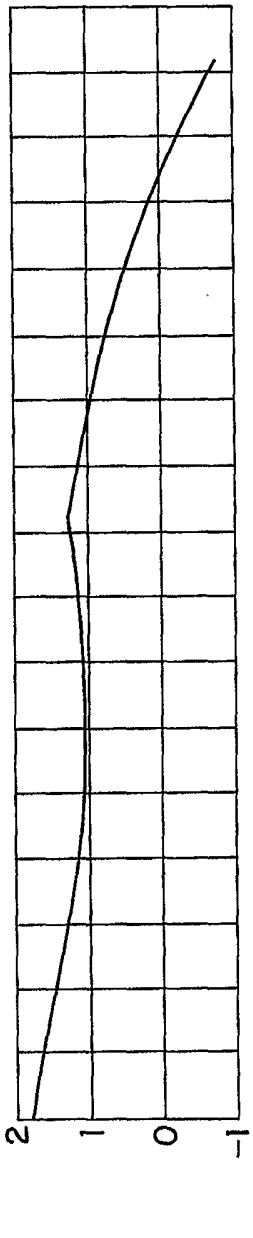
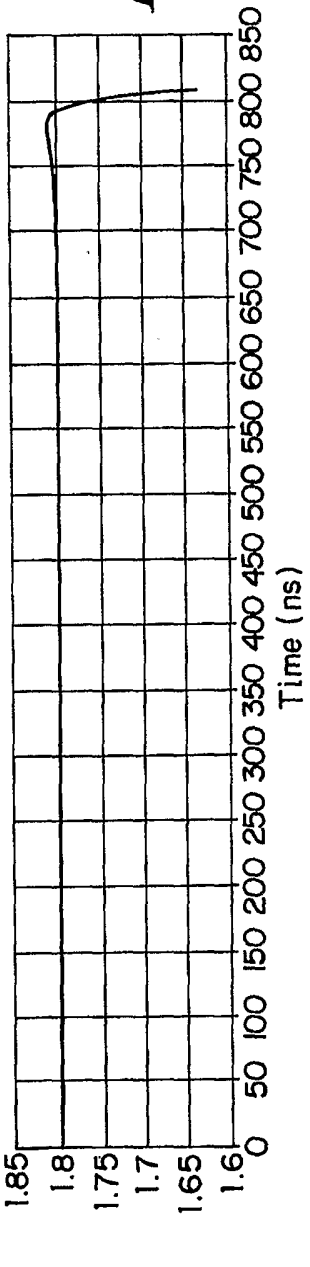
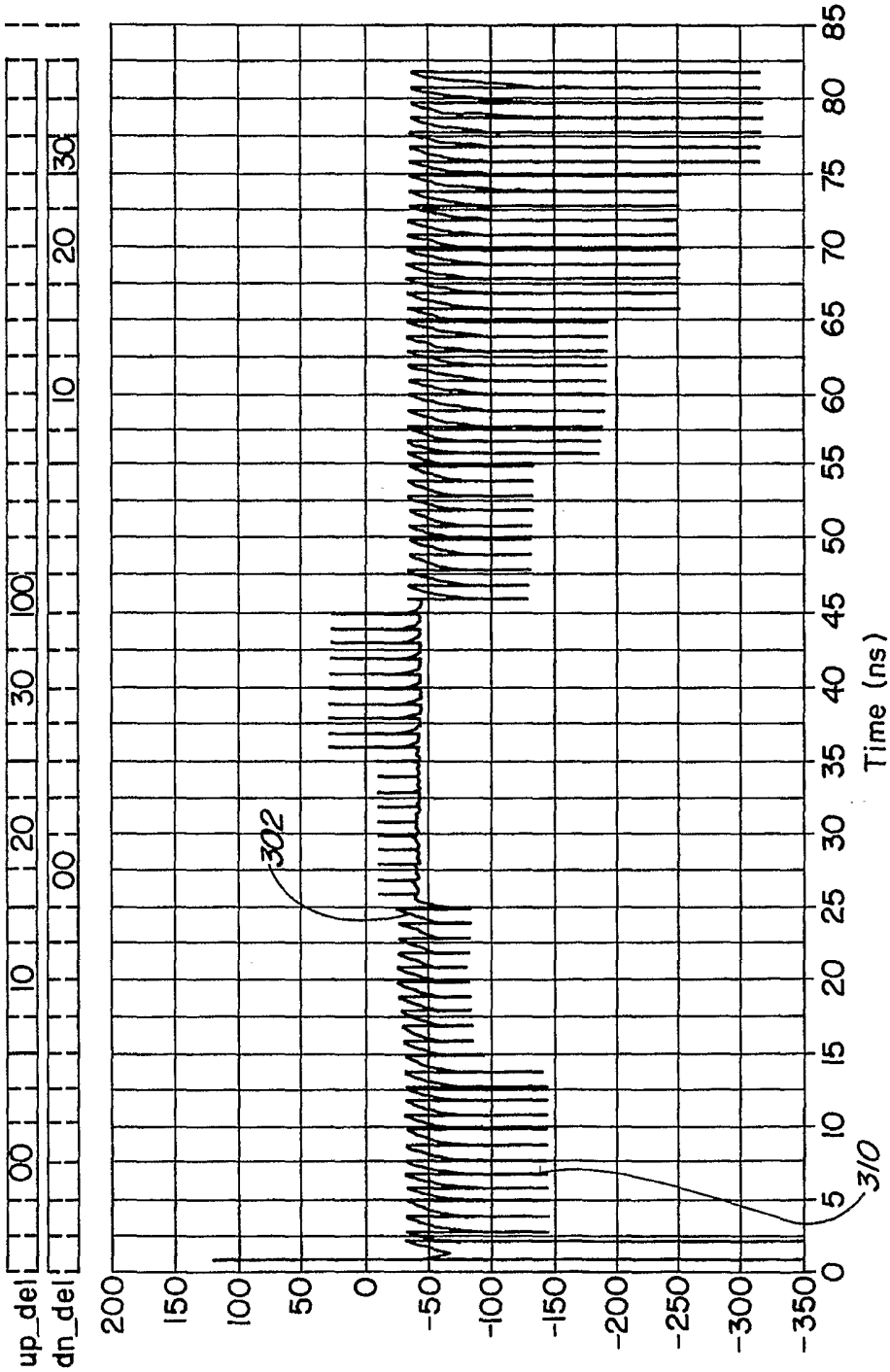


FIG. 3d

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dn_del
00
10
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30
100
00
10
20
30
200
150
100
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-50
-100
-150
-200
-250
-300
-350
0
5
10
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
Time (ns)
302
310

FIG. 3e