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938 O.G. 7

T938,005

PROCESS FOR MAKING LSI CHIPS HAVING BOTH RULES DRIVEN AND FREE FORM DESIGN

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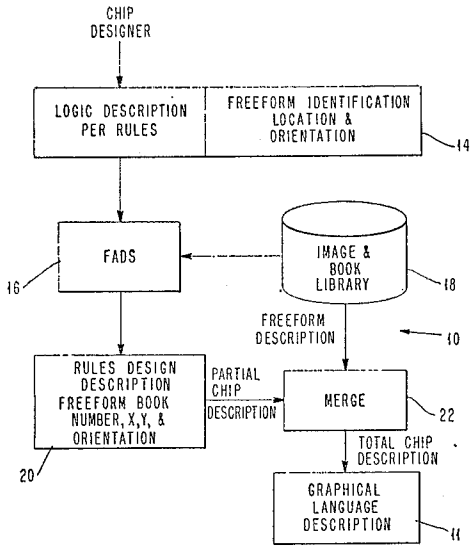
Continuation of abandoned application Ser. No. 401,303, Sept. 27, 1973. This application Aug. 28, 1974, Ser. No. 501,320

Int. Cl. G06f *15/20*
U.S. Cl. 444—1
6 Sheets Drawing. 11 Pages Specification



Stored in a design automation (DA) system is a library of predesigned graphical descriptions that describe circuits designed by the free form technique. A chip designer would layout a chip including both free form and rules driven portions. An input is fed to the DA system which specifies the rules driven design in the established manner and specifies the free form design by defining the library description thereof, and the relative placement of the design on the chip. The system in response to such input generates a graphical description of the rules driven design without doing any automatic checking of the internals of the free form design. The generated description or topology is then merged with the free form description or topology from the library to form a complete chip description from which is derived data for making the masks.

FIG. 1 PRIOR ART & INVENTION

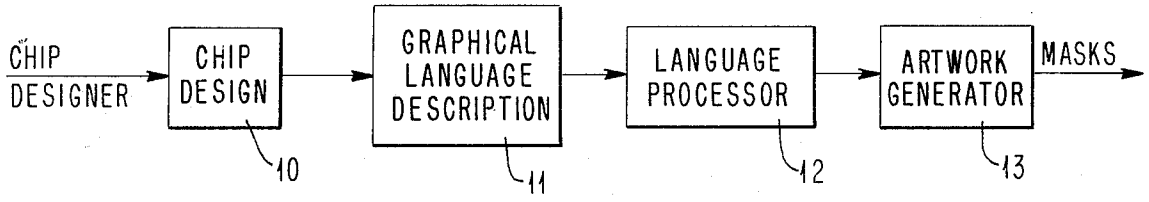


FIG. 2

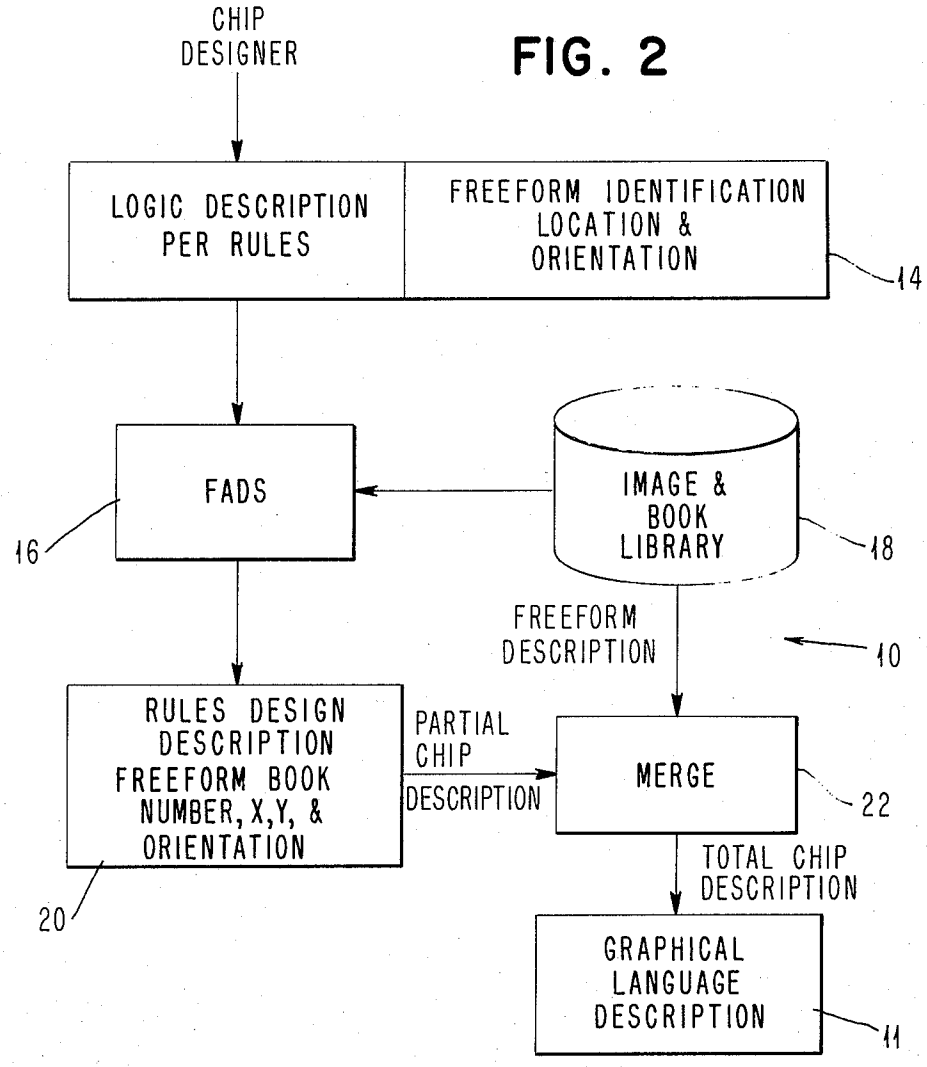


FIG. 3

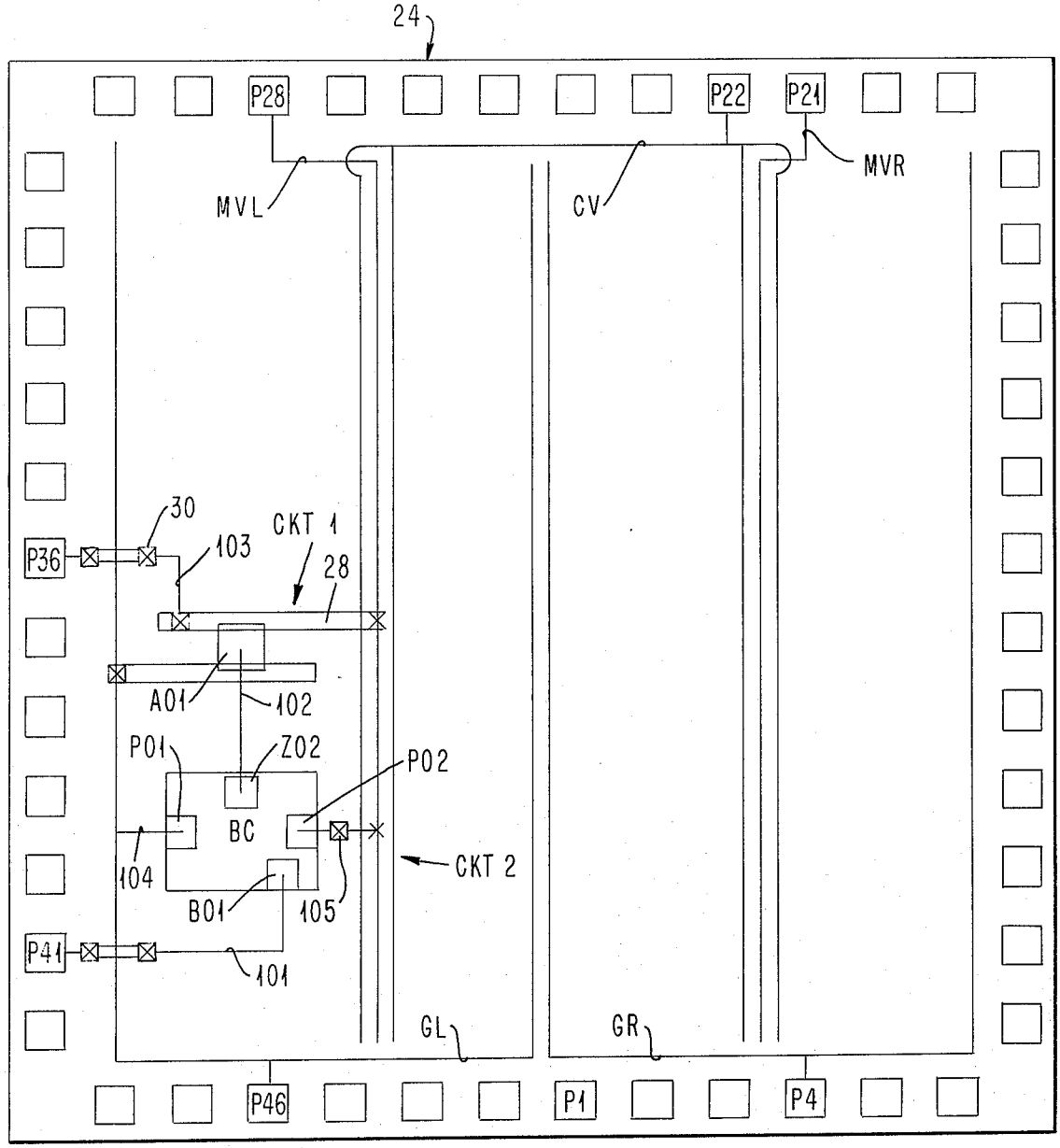

24
P28
P22
P21
MVL
CV
MVR
30
CKT 1
P36
103
28
A01
102
P01
Z02
P02
BC
CKT 2
104
B01
105
P41
101
GL
GR
P46
P1
P4

FIG. 4

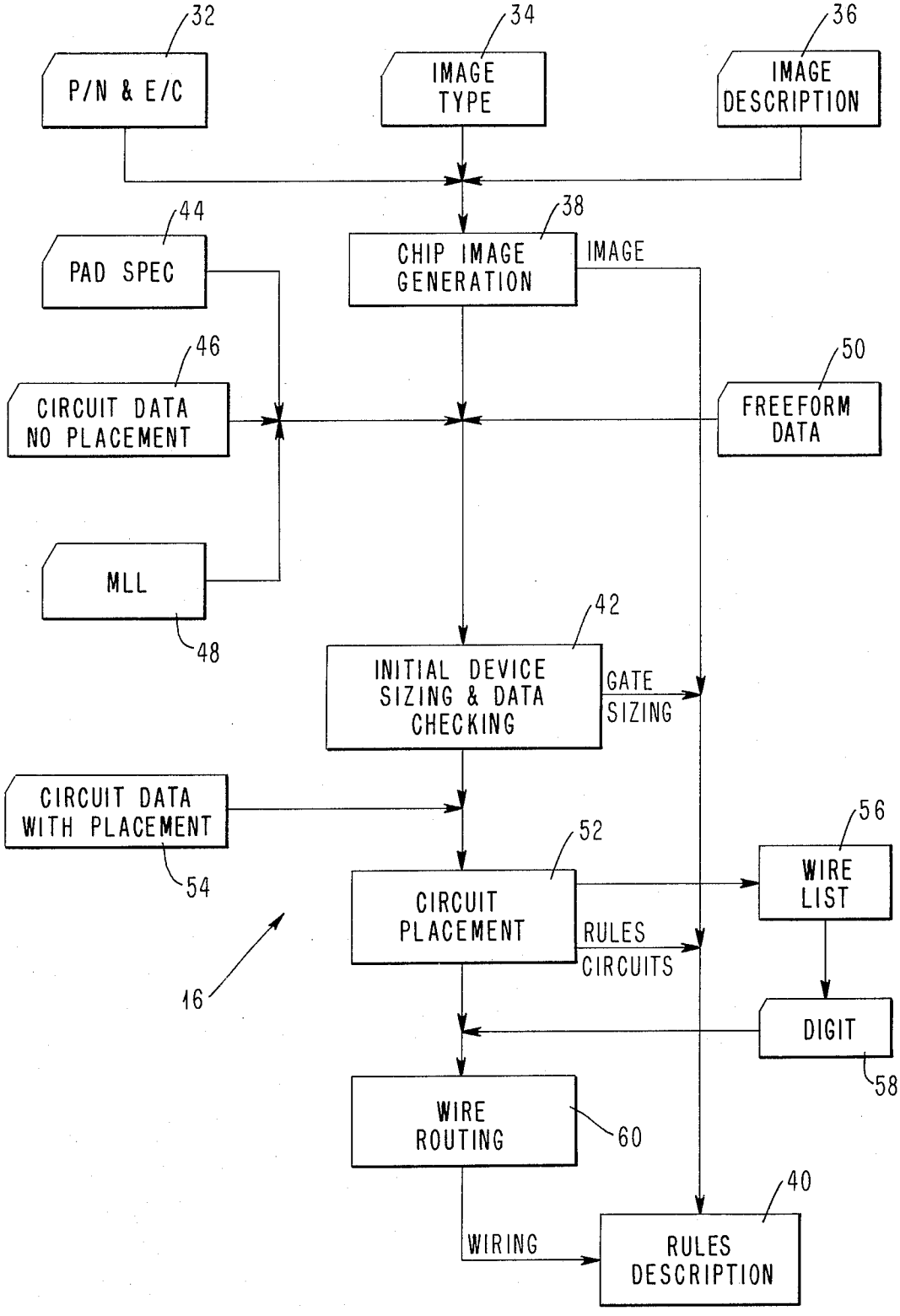

32
P/N & E/C
34
IMAGE TYPE
36
IMAGE DESCRIPTION
44
PAD SPEC
38
CHIP IMAGE GENERATION
IMAGE
46
CIRCUIT DATA NO PLACEMENT
50
FREEFORM DATA
MLL
48
42
INITIAL DEVICE SIZING & DATA CHECKING
GATE SIZING
CIRCUIT DATA WITH PLACEMENT
54
52
CIRCUIT PLACEMENT
56
WIRE LIST
RULES
CIRCUITS
16
DIGIT
58
WIRE ROUTING
60
40
WIRING
RULES DESCRIPTION

FIG. 5d

44

LOGICAL I/O	PHYSICAL I/O	WAVEFORM	RISE TIME	FALL TIME	CAPACITANCE
P41	P41		100	200	
P36	P36				5

PAD DATA

FIG. 5e

58

NET NUMBER	CODE	X START	Y START	Z START	WIDTH	DIRECTION	STEPS
101	1	a	b	c	o		
102	1	d	e	f	o		
103	1	s	n	i	o		

DIGIT DATA

FIG. 5f

34

DEFAULT IMAGE	COLUMNS = N

IMAGE TYPE

FIG. 5a

46 (54)

CIRCUIT NUMBER	BOOK NUMBER	COLUMN	ROW	ORDER	ORIENTATION	LOAD DEVICE	LOAD WIDTH	FUNCTION	SUB-FUNCTION	SPECIFICATION	SPECIFIED LST	DELAY LST
1	1	(1)	(2)	(1)	(1)							

CIRCUIT DATA

FIG. 5b

50

CIRCUIT NUMBER	BOOK NUMBER	X LOCATION	Y LOCATION	ORIENTATION
2	401	10	50	1

FREEFORM DATA

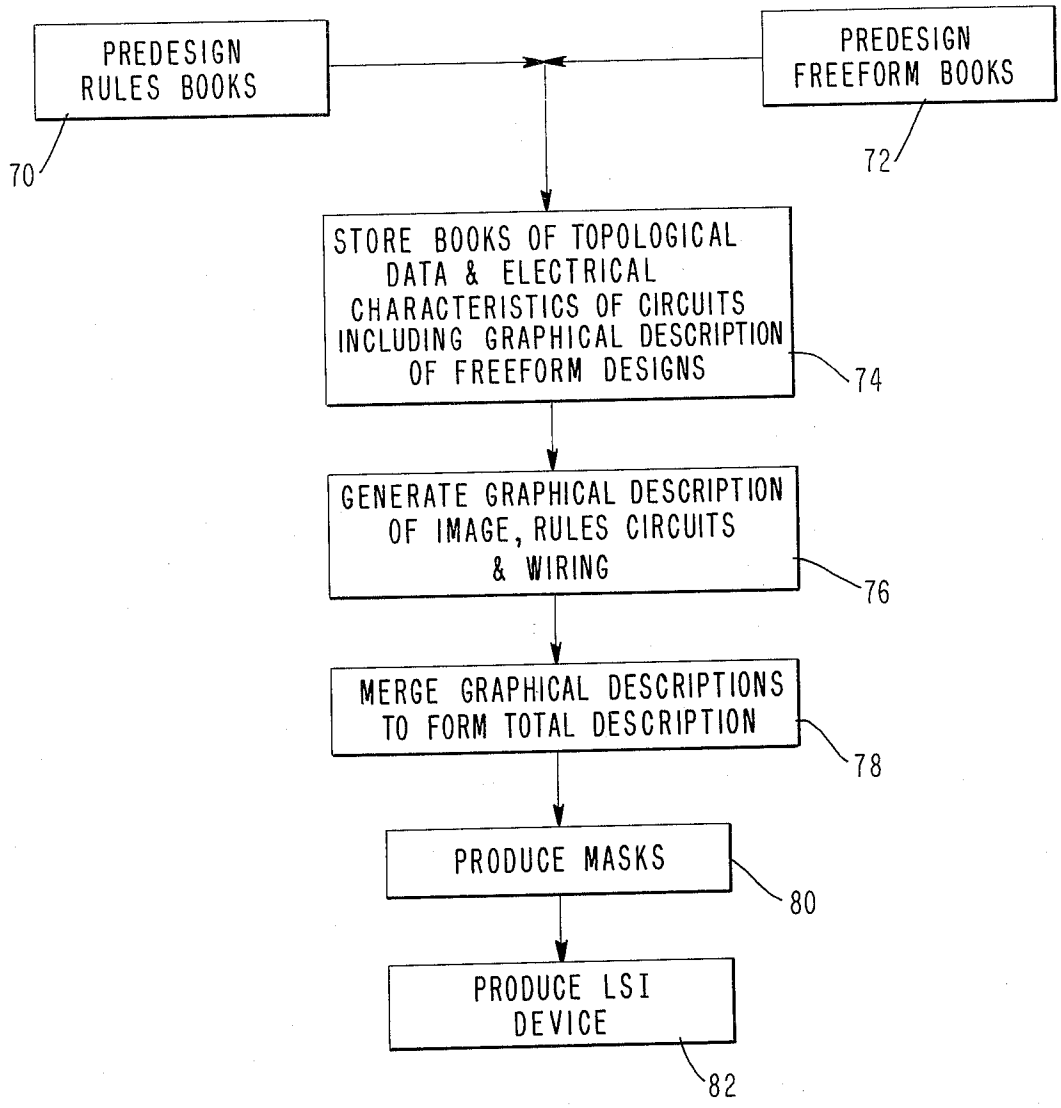
FIG. 5c

48

NET NUMBER	CIRCUIT NUMBER	LST ID	CIRCUIT	LST ID	CIRCUIT	LST ID
101	2	B01	-1	P41		
102	2	Z02	1	A01		
103	1	Z01	-101	P36		

MASTER LOGIC LIST (MLL)

FIG. 6


PREDESIGN RULES BOOKS
70
PREDESIGN FREEFORM BOOKS
72
STORE BOOKS OF TOPOLOGICAL DATA & ELECTRICAL CHARACTERISTICS OF CIRCUITS INCLUDING GRAPHICAL DESCRIPTION OF FREEFORM DESIGNS
74
GENERATE GRAPHICAL DESCRIPTION OF IMAGE, RULES CIRCUITS & WIRING
76
MERGE GRAPHICAL DESCRIPTIONS TO FORM TOTAL DESCRIPTION
78
PRODUCE MASKS
80
PRODUCE LSI DEVICE
82