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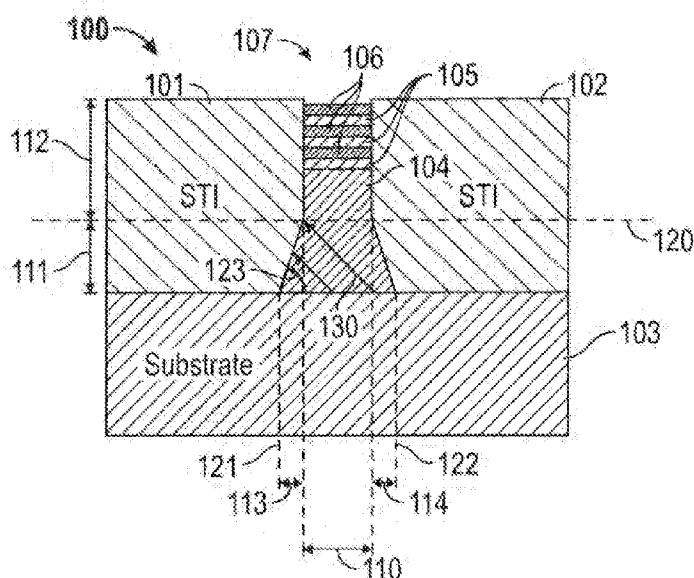


FIG. 12

- (57) Abstract:** An embodiment includes depositing a material onto a substrate where the material includes a different lattice constant than the substrate (e.g., III-V or IV epitaxial (EPI) material on a Si substrate). An embodiment includes an EPI layer formed within a trench having walls that narrow as the trench extends upwards. An embodiment includes an EPI layer formed within a trench using multiple growth temperatures. A defect barrier, formed in the EPI layer when the temperature changes, contains defects within the trench and below the defect barrier. The EPI layer above the defect barrier and within the trench is relatively defect free. An embodiment includes an EPI layer annealed within a trench to induce defect annihilation. An embodiment includes an EPI superlattice formed within a trench and covered with a relatively defect free EPI layer (that is still included in the trench). Other embodiments are described herein.



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EPITAXIAL FILM GROWTH ON PATTERNED SUBSTRATE

Background

[0001] A variety of electronic and optoelectronic devices can be enabled by developing, for example, high quality III-V semiconductors on elemental silicon (Si) substrates or IV semiconductors on Si substrates. Surface layers capable of achieving the performance advantages of III-V or IV materials may host a variety of high performance electronic devices such as CMOS and quantum well (QW) transistors fabricated from extremely high mobility materials such as, but not limited to, indium antimonide (InSb), indium arsenide (InAs), germanium (Ge), and silicon germanium (SiGe). Optical devices such as lasers, detectors and photovoltaics may also be fabricated from various other direct band gap materials, such as, but not limited to, gallium arsenide (GaAs) and indium gallium arsenide (InGaAs). These devices can be further enhanced by monolithically integrating them with conventional devices of Si since use of a Si substrate has the additional advantage of cost reduction.

[0002] The growth of III-V and IV materials upon Si substrates, however, presents many challenges. Crystal defects are generated by lattice mismatch, polar-on-nonpolar mismatch, and thermal mismatch between the III-V semiconductor epitaxial (EPI) layer and the Si semiconductor substrate or the IV semiconductor EPI layer and the Si semiconductor substrate. When the lattice mismatch between the EPI layer and substrate exceeds a few percent, the strain induced by the mismatch becomes too large and defects are generated in the EPI layer by relaxing the EPI film. Once the film thickness is greater than the critical thickness (i.e., film is fully strained below this thickness and partially relaxed above this thickness), the strain is relaxed by creating misfit dislocations at the film and substrate interface as well as in the EPI film. The EPI crystal defects may be in the form of threading dislocations, stacking faults and twins. Many defects, particularly threading dislocations and twins, tend to propagate into the "device layer" where the semiconductor device is fabricated. Generally, the severity of defect generation correlates to the amount of lattice mismatch between the III-V semiconductor and the Si substrate or the IV semiconductor and the Si substrate.

Brief Description Of The Drawings

[0003] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures, in which:

Figures 1(a)-(b) depict a trench with narrowing sidewalls in an embodiment.

Figures 2(a)-(b) depict a trench with an EPI layer and defect barrier in an embodiment.

Figures 3(a)-(b) depict a trench including an annealed EPI layer in an embodiment.

Figures 4(a)-(b) depict a trench with a superlattice and EPI layer in an embodiment.

Figure 5 includes a process in an embodiment.

Figure 6 includes a process in an embodiment.

Figure 7 includes a process in an embodiment.

Figure 8 includes a process in an embodiment.

Detailed Description

[0004] In the following description, numerous specific details are set forth but embodiments of the invention may be practiced without these specific details. Well known circuits, structures and techniques have not been shown in detail to avoid obscuring an understanding of this description. "An embodiment", "various embodiments" and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. "First", "second", "third" and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. "Connected" may indicate elements are

in direct physical or electrical contact with each other and “coupled” may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact. Also, while similar or same numbers may be used to designate same or similar parts in different figures, doing so does not mean all figures including similar or same numbers constitute a single or same embodiment.

[0005] An embodiment includes depositing a material onto a substrate where the material includes a different lattice constant than the substrate (e.g., III-V or IV EPI material on a Si substrate). An embodiment includes an EPI layer formed within a trench having walls that narrow as the trench extends upwards. An embodiment includes an EPI layer formed within a trench using multiple growth temperatures. A defect barrier, formed in the EPI layer when the temperature changes, contains defects within the trench and below the defect barrier. The EPI layer above the defect barrier and within the trench is relatively defect free. An embodiment includes an EPI layer annealed within a trench to induce defect annihilation. An embodiment includes an EPI superlattice formed within a trench and covered with a relatively defect free EPI layer (that is still included in the trench). Other embodiments are described herein.

[0006] A conventional technique for EPI formation includes Aspect Ratio Trapping (ART). ART is based on threading dislocations that propagate upwards at a specific angle. In ART a trench is made with a high enough aspect ratio such that the defects terminate on the sidewall of the trench and any layer above the terminations is defect free. More specifically, ART includes trapping defects along the sidewall of a shallow trench isolation (STI) portion by making the height (H) of the trench larger than the width (W) of the trench such that H/W ratio is at least 1.50. This ratio gives the minimum limit for ART to block defects within a buffer layer.

[0007] Figures 1(a)-(b) depict a trench with narrowing sidewalls in an embodiment of the invention. Figure 5 includes a process in an embodiment of the invention. Figures 1(a) and 5 are first discussed and then Figure 1(b) is discussed.

[0008] In an embodiment trench 107, having a top and a bottom, is included in between insulation portions 101, 102 (Block 505) of device 100. The sidewalls of

trench 107 may be shaped to narrow as they move away from substrate 103 (Block 510, described further below). Such insulation portions may include STI portions but other embodiments are not so limited. Portions 101, 102 are included on substrate 103, which has a first lattice constant. Substrate 103 may contain Si, such as a Si and/or SiGe substrate. One embodiment includes a SiGe common buffer on a Si substrate, but other embodiments are not so limited. Trench 107 extends downwards towards substrate 103. Trench 107 has a lower width 110 adjacent the trench bottom and an upper width above the lower width, and the upper width is narrower than the lower width. The upper width may be along horizontal axis 120, which is located at the narrowest portion of trench 107. The upper width is determined from the differential between width 110 and deviations 113, 114. Deviation 113 is the distance between trench 107 sidewall and axis 121 and deviation 114 is the distance between trench 107 sidewall and axis 122.

[0009] Lower EPI layer 104 has a second lattice constant mismatched with the first lattice constant that corresponds to substrate 103 (or a top layer of substrate 103 if an intermediate layer, such as a buffer layer, is included between the lower portions of substrate 103 and EPI layer 104). EPI layer 104 is formed in trench 107, adjacent the trench bottom, and below the trench upper width located at the narrowest portion of trench 107 (Block 515).

[0010] An upper EPI layer is included in trench 107 above lower EPI layer 104. For example, any of EPI layers 106 may constitute such an upper EPI layer. Further, any of EPI layers 105 may constitute such an upper EPI layer. Any of EPI layers 105, 106 may be included in a device layer that may form, in part, a device such as a channel of a transistor (Block 520). Any of EPI layers 105, 106 may have a lattice constant different from the lattice constants of substrate 103 and/or EPI layer 104. For example, EPI layer 105 may have lattice constant such that a differential between the substrate lattice constant and the lattice constant for EPI layer 105 is greater than a differential between the substrate lattice constant and the lattice constant for EPI layer 104. In one embodiment, substrate 103 includes Si (e.g., Si and/or SiGe), EPI layer 104 includes a III-V or IV material, EPI layer 105 includes a III-V or IV material, and EPI layer 106 includes a III-V or IV material. III-V and IV

materials include, without limitation, Ge, SiGe, GaAs, AlGaAs, InGaAs, InAs, and InSb. Each or any of components 103, 104, 105, 106 may be different materials, such as materials including different compositions such as $\text{Si}_x\text{Ge}_{1-x}$ and $\text{Si}_y\text{Ge}_{1-y}$ where x is unequal to y . In other embodiments, the materials may be completely different such as InP, SiGe, and/or GaAs.

[0011] In an embodiment lower EPI layer 104 includes more defects than upper EPI layers 105 and/or 106. In an embodiment lower EPI layer 104 includes more defects than the portion of EPI layers 104 above axis 120. For example, defect 130 terminates within EPI layer 104. In one embodiment well trench 107 includes a length (not shown in Figure 1(a)) less than the trench overall height, which is composed of height 111 (which extends from the trench bottom to the narrowest portion of the trench) and height 112 (which extends from the narrowest portion of the trench to the top of the trench). In one embodiment the combination of heights 111, 112 is greater than 100 nm and width 110 is less than the combination of heights 111, 112.

[0012] In one embodiment EPI layer 104 may include n-MOS material (e.g., InP, SiGe, GaAs) grown as a buffer layer in trench 107 using various methods (e.g., molecular beam epitaxy, metal-organic chemical vapor deposition (MOCVD), and/or metalorganic vapour phase epitaxy (MOVPE)).

[0013] In an embodiment the width and length of well 107 is maintained much lower than the height of the trench. This helps capture defects (e.g., defect 130) along the sidewalls of STI 101, 102 and prevents defects from reaching the top of trench 107.

[0014] In an embodiment the sidewalls of the trench are shaped as shown in Figure 1(a) (i.e., a hyperbola). The curvature allows defect trapping at a height (combined height from heights 111, 112) that is less than the product of 1.5 and width 110. Subsequently, the device layers (e.g., layers 105, 106) are grown over the buffer layer (e.g., layer 104) and device processing (not shown) is performed. Such an embodiment may reduce the need for a tall aspect ratio for the trench, allowing defects to be captured within thin buffer layers, thus reducing the cost associated

with the process by reducing materials needed (for higher layers of EPI and the like) and process tool time.

[0015] In one embodiment trench 107 has combined heights 111, 112 (extending from the trench top to the trench bottom) less than the product of 1.5 and lower width 110. In one embodiment trench 107 includes a lower portion having sidewalls that narrow as the sidewalls move away from the substrate; the sidewalls stop narrowing at the upper width (located at axis 120); and combined heights 111, 112 are no more than the product of 1.5 and the upper width at axis 120. In one embodiment the upper width at axis 120 is narrower than the lower width 110 by a first differential (deviation 113 + deviation 114) and the combination of heights 111, 112 is no more than the product of 1.5 and width 110 minus one half of the differential (e.g., deviation 113 or deviation 114).

[0016] In an embodiment, either of deviations 113, 114 is 3 to 195 nm, the combination of heights 111, 112 is 5 nm to several microns, and width 110 is 5 to 200 nm. This compares to a conventional ART system where a trench width of 10 nm would require a height of at least 15 nm (height equals the product of 1.5 and the width based on the tangent of 55 degree angle between the trench bottom and a defect). An embodiment includes a height equal to the product of 1.5 and (width 110 – deviation 113, which is 10 nm – 3 nm). Thus, the height is 10.5 nm (instead of 15 nm as would be the case of a classic ART system using a 10 nm width).

[0017] Figure 1(b) includes an embodiment where trench 107 includes a lower portion (bound by the trench bottom, sidewalls, and the width at axis 120) shaped like a trapezoid. In an embodiment, height 111 is equal to the product of 1.5 and deviation 113 for a height equaling 20-750 nm in various embodiments. The addition of widths 110, 113, 114 equals 15 to 500 nm in various embodiments. Width 113 and width 114 may each be 5 nm or more. Height 112 may be 0 nm to several microns. An embodiment includes height 111 equal to the product of 1.5 and (width 110 – deviation 113, which is 10 nm – 3 nm). Thus, height 111 is 10.5 nm (instead of 15 nm as would be the case of a classic ART system using a 10 nm width).

[0018] Both of Figures 1(a) and 1(b) include trench 107 with a lower half that includes a side wall that joins the bottom of the trench at angle 123. Angle 123 may be than 70 degrees. In other embodiments, angle 123 is 60, 55, 50, 45, 40 degrees and the like. Also, while 1.5 has been used as a ratio for determining heights (e.g., the combination of heights 111, 112 for Figure 1(a) and height 111 for Figure 1(b)) other ratios are provided for in various embodiments as may be dictated by the severity of angle 123 and the curvature of trench sidewalls. In an embodiment the trench has a height extending from the trench top to the trench bottom and the height is less than 1.3 times the width 110. In an embodiment the trench has a height extending from the trench top to the trench bottom and the height is less than 1.4 times the width 110. In an embodiment the trench has a height extending from the trench top to the trench bottom and the height is less than 1.1 times the width 110 (e.g., see example where height is 10.5 nm and width is 10 nm).

[0019] Regarding shaping the sidewalls of trench 107, in the embodiment of Figure 1(a) trench 107 may be patterned using, for example, a resist layer and a hard mask. Resist is patterned and then a hard mask is etched using the resist as the mask. The choice of etch chemistry and the amount of the etch depth dictates the curved profile of the sidewalls inside the trench. In Figure 1(b) a hard mask is etched using patterned resist, which is used to generate a fin that gives the straight profile to the upper part of trench 107. Regarding the lower part of trench 107, a portion of substrate 103 below the hard mask is wet etched selectively in (111) direction to give the tapered profile. STI is filled around the patterned hard mask and the underlying fin. This is followed by removal of the hard mask and fin selectively with respect to the STI, yielding trench 107. EPI layer growth may then follow.

[0020] Figures 2(a)-(b) depict device 200 having a trench that includes an EPI layer with a defect barrier in an embodiment of the invention. Figure 6 includes a process in an embodiment of the invention. Figures 2(a) and 6 are first discussed and then Figure 2(b) is discussed.

[0021] In Figure 2(a) trench 207 is included in STI portions 201, 202 and on substrate 203 (Block 605). Substrate 203 may contain Si, such as a Si and/or SiGe substrate but other embodiments are not so limited. One embodiment includes a

SiGe common buffer on a Si substrate, but other embodiments are not so limited. Trench 207 includes a top and a bottom and extends downwards towards substrate 203. Lower EPI layer 204, located in the trench adjacent the trench bottom (Block 610), has a lattice constant mismatched with a lattice constant that corresponds to substrate 203 (or a top layer of substrate 203 if an intermediate layer, such as a buffer layer, is included between the lower portions of substrate 203 and EPI layer 204).

[0022] Upper EPI layer 205 is formed over and in direct contact with lower EPI layer 204, the lower and upper EPI layers 204, 205 being monolithic with one another (Block 615). Further, lower and upper EPI layers 204, 205 directly join one another at barrier 220, which blocks defects (e.g., defect 230) in lower EPI layer 204. In an embodiment upper EPI layer 205 has lattice constant generally equal to the lattice constant of EPI layer 204.

[0023] The embodiment of Figure 2(a) terminates defects by changing temperatures during EPI growth in trench 207. Low growth temperature film 204 is grown first. Subsequently, growth is paused and growth temperature is increased. The pause in growth changes the surface condition such that interface 220 is formed, which blocks defects in underlying layer 204 from propagating up into layer 205. Subsequent growth at a higher temperature is followed through to form layer 205. In one embodiment, the lower temperature is 400 C and the higher temperature is 550 C but other embodiments are not so limited and may include lower temperatures of, for example, 300, 325, 350, 375, 400, 425, 450 C and higher temperatures of 450, 475, 500, 525, 575, 600 C.

[0024] Thus, in an embodiment lower EPI layer 204 includes more defects than upper EPI layer 205. Defect 230 in lower EPI layer 204 grows upwards and then deflects off barrier 220 and grows downwards (see defect portion 231) towards substrate 203 (Block 620). In an embodiment barrier 220 extends from one of the trench sidewalls to another of the sidewalls.

[0025] In one embodiment height 211 equals the product of 1.5 and width 210; however other embodiments are not so limited.

[0026] Figure 2(b) includes an image illustrating trench 207 with defect barrier 220 between layers 204 and 205. Layer 204 has far more defects contained within that layer than layer 205, which shows fewer defects, if any, concentrated near barrier 220 and away from the top of the trench.

[0027] Figures 3(a)-(b) depict device 300 having a trench with an annealed EPI layer in an embodiment of the invention. Figure 7 includes a process in an embodiment of the invention.

[0028] In Figure 3(a) trench 307 is located between STI portions 301, 302 and above substrate 303 (Block 705). EPI layer 304 is formed within trench 307 (Block 710). Due to a lattice mismatch between EPI layer 304 and substrate 303 defects (e.g., defect 330) propagate within layer 304 (Block 715). However, an anneal of layer 304 yields the embodiment of Figure 3(b) (Block 720). In one embodiment height 311 equals the product of 1.5 and width 310; however other embodiments are not so limited.

[0029] Figure 3(b) includes an embodiment with trench 307, having a top and a bottom, between insulation layers 301, 302 and on substrate 303. EPI layer 304 is in the trench adjacent the trench bottom and has no defects. The lack of defects may be due to annealing (Block 720). In an embodiment EPI layer 304 comprises one of a IV and a III-V material and substrate 303 includes silicon (e.g., Si or SiGe). In an embodiment EPI layer 304 and substrate 303 include equal lattice constants (e.g., due to the annealing) and EPI layer 304 directly contacts substrate 303.

[0030] In another embodiment (not shown) EPI layer 304 couples to substrate 303 via an intermediate layer having a lattice constant that equals the EPI layer lattice constant (due to annealing) and the EPI layer directly contacts the intermediate layer.

[0031] Thus, in one embodiment after the growth of an EPI layer in the trench, the device is annealed at a high temperature (e.g., rapid thermal, spike, flash, and/or laser annealing). The high thermal budget melts the EPI film. Once melted, the wafer is cooled down to room temperature. The cooling cycle induces recrystallization of the melted film which then conforms to the lattice constant of the underlying layer

(e.g., substrate or intermediate layer between lower portion of substrate and EPI layer). However, another embodiment does not melt the EPI layer. Instead, the embodiment anneals at temperatures below the melting point for layer 304 while still causing recrystallization. In an embodiment recrystallization occurs at a temperature above the product of 0.6 and the melting point of EPI layer 304; however other embodiments are not so limited and may include, for example, multiplicands of 0.5, 0.7, 0.8 and the like.

[0032] Figures 4(a)-(b) depict device 400 with a trench including a superlattice and an EPI layer in an embodiment of the invention. Figure 8 includes a process in an embodiment of the invention.

[0033] In Figure 4(a) trench 407 is located between STI portions 401, 402 and above substrate 403. Due to a lattice mismatch between EPI layer 406 and substrate 403 defects (e.g., defect 430) propagate within layer 406.

[0034] However, Figure 4(b) includes an embodiment with trench 407 included between insulation layers 401, 402 (Block 805) and formed on substrate 403. Substrate 403 may contain Si, such as a Si and/or SiGe substrate but other embodiments are not so limited. One embodiment includes a SiGe common buffer on a Si substrate, but other embodiments are not so limited. Further, trench 407 includes a superlattice adjacent the trench bottom (Block 810) and axis 420. A superlattice is a periodic structure of layers of two (or more) materials (which may change merely in concentration among elements or may include entirely different elements). The superlattice including EPI layer or layers 404 and EPI layer or layers 405 formed over and in direct contact with any of EPI layers 404. EPI layer 406 is in trench 407 above the superlattice (Block 815). The superlattice may include 2, 3, 4, 5, 6, 7 or more layers. In various embodiments the superlattice includes alternating layers of, for example, Si and SiGe, InGaAs and InP, and combinations of Si, SiGe, InGaAs, and InP.

[0035] In one embodiment the superlattice includes a Ge seed layer contacting an intermediate layer that is directly contacting a Si substrate. The Ge seed layer is followed upwards by $\text{Si}_{50}\text{Ge}_{50}$, Ge, $\text{Si}_{50}\text{Ge}_{50}$, Ge, and then more superlattice layers or

a layer like layer 406. The intermediate layer may include $\text{Si}_{70}\text{Ge}_{30}$ near the substrate and $\text{Si}_{30}\text{Ge}_{70}$ near the Ge seed layer. Another embodiment is the same as above but with no Ge seed layer.

[0036] Any of EPI layers 404, 405, 406, or even EPI layer 408, may include the same lattice constant as one another or a different lattice constant from one or more fellow EPI layers. Also, any of EPI layers 404, 405, 406 may have a lattice mismatch with substrate 403 or some intermediate layer between a lower portion of substrate 403 and the EPI layer in question.

[0037] In the embodiment of Figure 4(b) multilayer growth is used to block or glide defects (e.g., defect 430) from propagating to top layers, such as layer 406. Strain introduced by the superlattice (e.g., layers 404, 405) causes dislocations to bend and annihilate inside the superlattice (Block 820). An embodiment may also include implementation of multilayers in buffer/substrate layer(s). Thus, in an embodiment the superlattice includes more defects than the EPI layer 406.

[0038] In one embodiment height 411 equals the product of 1.5 and width 410; however other embodiments are not so limited. In one embodiment, width 410 is between 5 and 200 nm. In one embodiment the superlattice has a height between 2 and 50 nm. In an embodiment an intermediate layer between the lower substrate and the superlattice is 1.3 microns in height.

[0039] Any of the EPI layers discussed herein may be included in, for example, a channel of a transistor.

[0040] In an embodiment an apparatus comprises: a trench, having a top and a bottom, in an insulation layer that is on a substrate having a first lattice constant; wherein (a) the trench extends downwards towards the substrate; (b) the trench has a lower width adjacent the trench bottom and an upper width above the lower width, and (c) the upper width is narrower than the lower width; and a lower epitaxial (EPI) layer, having a second lattice constant mismatched with the first lattice constant, in the trench adjacent the trench bottom and below the trench upper width. An embodiment comprises an upper EPI layer in the trench above the lower EPI layer. In an embodiment the lower EPI layer includes more defects than the upper EPI

layer. In an embodiment the upper EPI layer is included in a device layer and has a third lattice constant; and a differential between the first and third lattice constants is greater than a differential between the first and second lattice constants. In an embodiment the trench has a height extending from the trench top to the trench bottom and the height is less than 1.5 times the lower width. In an embodiment the trench has a height extending from the trench top to the trench bottom and the height is less than 1.4 times the lower width. In an embodiment the trench has a height extending from the trench top to the trench bottom and the height is less than 1.3 times the lower width. In an embodiment the trench includes a lower portion having sidewalls that narrow as the sidewalls move away from the substrate; the sidewalls stop narrowing at the upper width; the trench has a height extending from the trench bottom to the upper width; and the upper width is narrower than the lower width by a first differential and the height is no more than a product of 1.3 and one half of the differential. In an embodiment the trench has a height extending from the trench top to the trench bottom: the trench includes a lower portion having sidewalls that narrow as the sidewalls move away from the substrate and the sidewalls stop narrowing at the upper width; and the upper width is narrower than the lower width by a first differential and the height is no more than a product of 1.3 and one half of the differential. In an embodiment the trench has a cross-section shaped like a hyperbola. In an embodiment the trench includes a lower portion, extending from the lower width to the upper width, shaped like a trapezoid. In an embodiment the trench includes a lower half and an upper half and the lower half includes a side wall that joins the bottom of the trench at an angle of less than 70 degrees between the side wall and the bottom of the trench.

[0041] An embodiment comprises: a trench included in an insulation layer that is formed on a substrate having a first lattice constant, the trench having a top and a bottom and extending downwards towards the substrate; a lower epitaxial (EPI) layer, having a second lattice constant mismatched with the first lattice constant, in the trench adjacent the trench bottom; an upper EPI layer formed over and in direct contact with the lower EPI layer, the lower and upper EPI layers being monolithic with one another; wherein the lower and upper EPI layers directly join one another at a barrier that blocks defects in the lower EPI layer. In an embodiment the lower EPI

layer includes more defects than the upper EPI layer. An embodiment includes a defect in the lower EPI layer grows upwards and then deflects off the barrier and grows downwards towards the substrate. In an embodiment the upper EPI layer has a third lattice constant generally equal to the second lattice constant. In an embodiment the trench includes opposing sidewalls and the barrier extends from one of the sidewalls to another of the sidewalls. In an embodiment the lower EPI layer is formed at a lower EPI layer growth temperature and the upper EPI layer is formed at an upper EPI layer growth temperature that is higher than the lower EPI growth temperature.

[0042] An embodiment comprises: a trench included in an insulation layer that is formed on a substrate having a substrate lattice constant, the trench having a top and a bottom and extending downwards towards the substrate; a superlattice in the trench adjacent the trench bottom, the superlattice including (a) a first epitaxial (EPI) layer having a first lattice constant mismatched with the substrate lattice constant, and (b) a second EPI layer formed over and in direct contact with the first EPI layer; a third EPI layer in the trench above the superlattice. In an embodiment the superlattice includes more defects than the third EPI layer. In an embodiment defects annihilate in the superlattice. In an embodiment the second EPI layer includes a second lattice constant, the third EPI layer includes a third lattice constant, and a differential between the substrate and third lattice constants is greater than a differential between the substrate and first lattice constants.

[0043] An embodiment comprises: a trench, having a top and a bottom, in an insulation layer that is on a substrate having a first lattice constant; and an epitaxial (EPI) layer, having a second lattice constant, in the trench adjacent the trench bottom; wherein the EPI layer includes no defects. In an embodiment the EPI layer comprises one of a IV and a III-V material and the substrate includes silicon. In an embodiment the first lattice constant equals the second lattice constant and the EPI layer directly contacts the substrate. In an embodiment the EPI layer couples to the substrate via an intermediate layer having a third lattice constant, the second lattice constant equals the third lattice constant, and the EPI layer directly contacts the intermediate layer.

[0044] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

- 1 1. An apparatus comprising:
2 a trench, having a top and a bottom, in an insulation layer that is on a
3 substrate having a first lattice constant; wherein (a) the trench extends downwards
4 towards the substrate; (b) the trench has a lower width adjacent the trench bottom
5 and an upper width above the lower width, and (c) the upper width is narrower than
6 the lower width; and
7 a lower epitaxial (EPI) layer, having a second lattice constant mismatched
8 with the first lattice constant, in the trench adjacent the trench bottom and below the
9 trench upper width.
- 1 2. The apparatus of claim 1 comprising an upper EPI layer in the trench above
2 the lower EPI layer.
- 1 3. The apparatus of claim 2 wherein the lower EPI layer includes more defects
2 than the upper EPI layer.
- 1 4. The apparatus of claim 3, wherein the upper EPI layer is included in a device
2 layer and has a third lattice constant; and a differential between the first and third
3 lattice constants is greater than a differential between the first and second lattice
4 constants.
- 1 5. The apparatus of claim 3, wherein the trench has a height extending from the
2 trench top to the trench bottom and the height is less than 1.3 times the lower width.
- 1 6. The apparatus of claim 3, wherein:
2 the trench includes a lower portion having sidewalls that narrow as the
3 sidewalls move away from the substrate;
4 the sidewalls stop narrowing at the upper width;
5 the trench has a height extending from the trench bottom to the upper width;
6 and

7 the upper width is narrower than the lower width by a first differential and the
8 height is no more than a product of 1.3 and one half of the differential.

1 7. The apparatus of claim 3, wherein:
2 the trench has a height extending from the trench top to the trench bottom:
3 the trench includes a lower portion having sidewalls that narrow as the
4 sidewalls move away from the substrate and the sidewalls stop narrowing at the
5 upper width; and
6 the upper width is narrower than the lower width by a first differential and the
7 height is no more than a product of 1.3 and one half of the differential.

1 8. The apparatus of claim 3, wherein the trench has a cross-section shaped like
2 a hyperbola.

1 9. The apparatus of claim 3, wherein the trench includes a lower portion,
2 extending from the lower width to the upper width, shaped like a trapezoid.

1 10. The apparatus of claim 1, wherein the trench includes a lower half and an
2 upper half and the lower half includes a side wall that joins the bottom of the trench
3 at an angle of less than 70 degrees between the side wall and the bottom of the
4 trench.

1 11. An apparatus comprising:
2 a trench included in an insulation layer that is formed on a substrate having a
3 first lattice constant, the trench having a top and a bottom and extending downwards
4 towards the substrate;
5 a lower epitaxial (EPI) layer, having a second lattice constant mismatched
6 with the first lattice constant, in the trench adjacent the trench bottom;
7 an upper EPI layer formed over and in direct contact with the lower EPI layer,
8 the lower and upper EPI layers being monolithic with one another;
9 wherein the lower and upper EPI layers directly join one another at a barrier
10 that blocks defects in the lower EPI layer.

1 12. The apparatus of claim 11, wherein the lower EPI layer includes more defects
2 than the upper EPI layer.

1 13. The apparatus of claim 12, wherein a defect in the lower EPI layer grows
2 upwards and then deflects off the barrier and grows downwards towards the
3 substrate.

1 14. The apparatus of claim 12, wherein the upper EPI layer has a third lattice
2 constant generally equal to the second lattice constant.

1 15. The apparatus of claim 12, wherein the trench includes opposing sidewalls
2 and the barrier extends from one of the sidewalls to another of the sidewalls.

1 16. The apparatus of claim 12, wherein the lower EPI layer is formed at a lower
2 EPI layer growth temperature and the upper EPI layer is formed at an upper EPI
3 layer growth temperature that is higher than the lower EPI growth temperature.

1 17. An apparatus comprising:
2 a trench included in an insulation layer that is formed on a substrate having a
3 substrate lattice constant, the trench having a top and a bottom and extending
4 downwards towards the substrate;
5 a superlattice in the trench adjacent the trench bottom, the superlattice
6 including (a) a first epitaxial (EPI) layer having a first lattice constant mismatched
7 with the substrate lattice constant, and (b) a second EPI layer formed over and in
8 direct contact with the first EPI layer; and
9 a third EPI layer in the trench above the superlattice.

1 18. The apparatus of claim 17 wherein the superlattice includes more defects
2 than the third EPI layer.

1 19. The apparatus of claim 17 wherein defects annihilate in the superlattice.

1 20. The apparatus of claim 17, wherein the second EPI layer includes a second
2 lattice constant, the third EPI layer includes a third lattice constant, and a differential
3 between the substrate and third lattice constants is greater than a differential
4 between the substrate and first lattice constants.

1 21. An apparatus comprising:
2 a trench, having a top and a bottom, in an insulation layer that is on a
3 substrate having a first lattice constant; and
4 an epitaxial (EPI) layer, having a second lattice constant, in the trench
5 adjacent the trench bottom;
6 wherein the EPI layer includes no defects.

1 22. The apparatus of claim 21, wherein the EPI layer comprises one of a IV and a
2 III-V material and the substrate includes silicon.

1 23. The apparatus of claim 22, wherein the first lattice constant equals the second
2 lattice constant and the EPI layer directly contacts the substrate.

1 24. The apparatus of claim 22, wherein the EPI layer couples to the substrate via
2 an intermediate layer having a third lattice constant, the second lattice constant
3 equals the third lattice constant, and the EPI layer directly contacts the intermediate
4 layer.

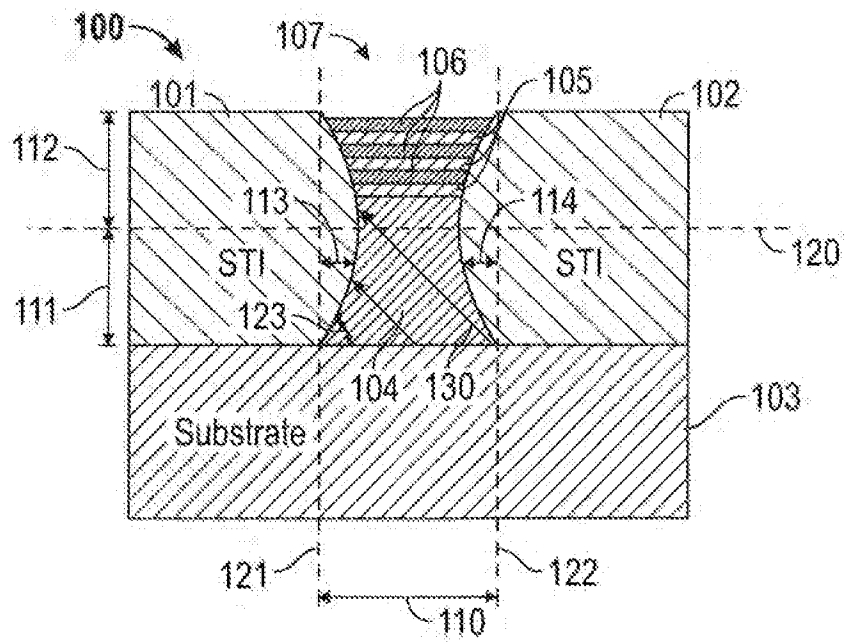


FIG. 1A

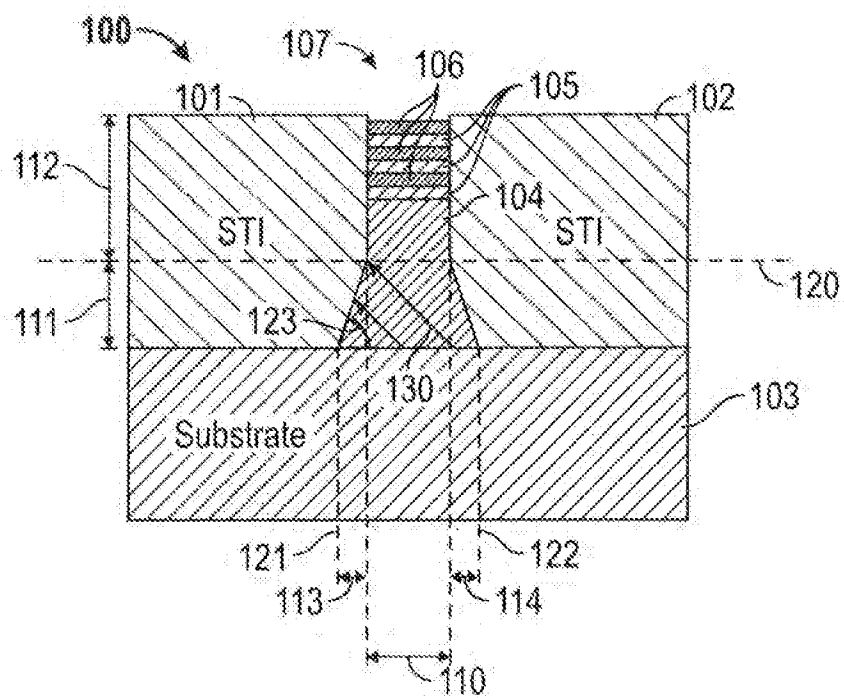


FIG. 18

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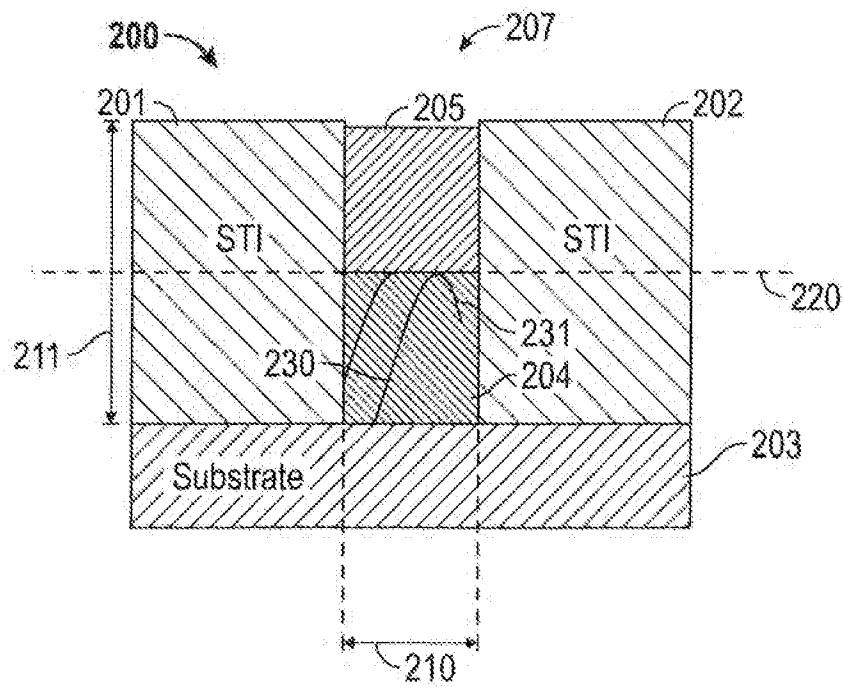


FIG. 2A

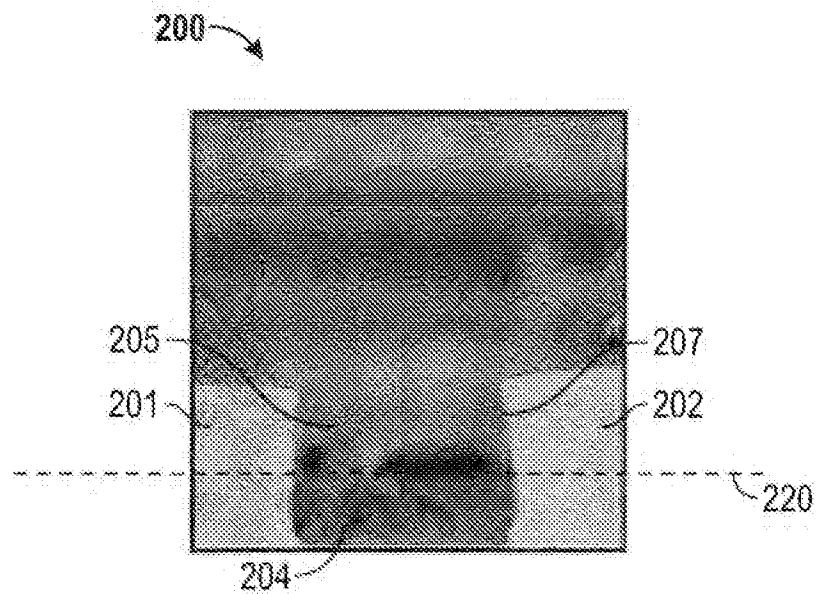


FIG. 2B

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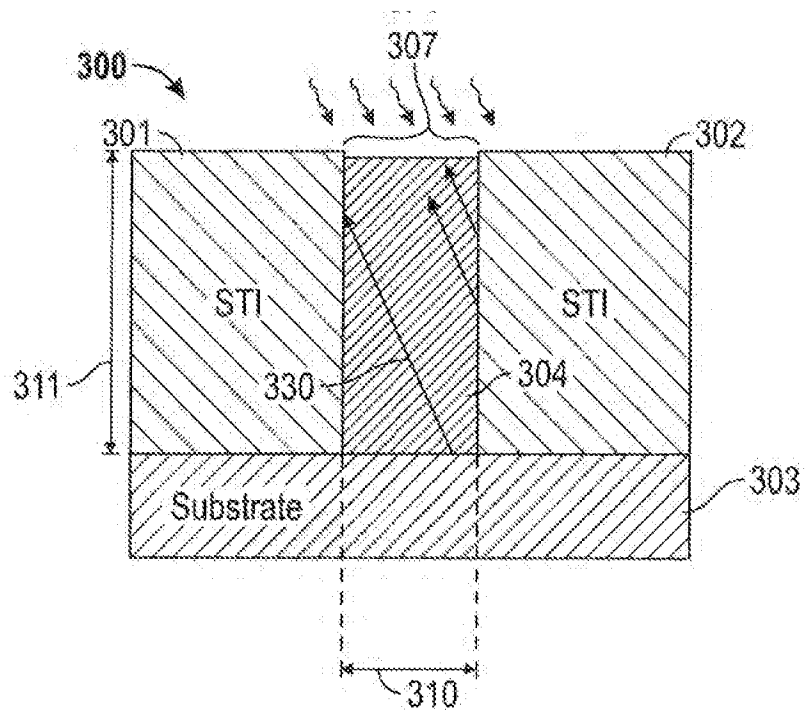


FIG. 3A

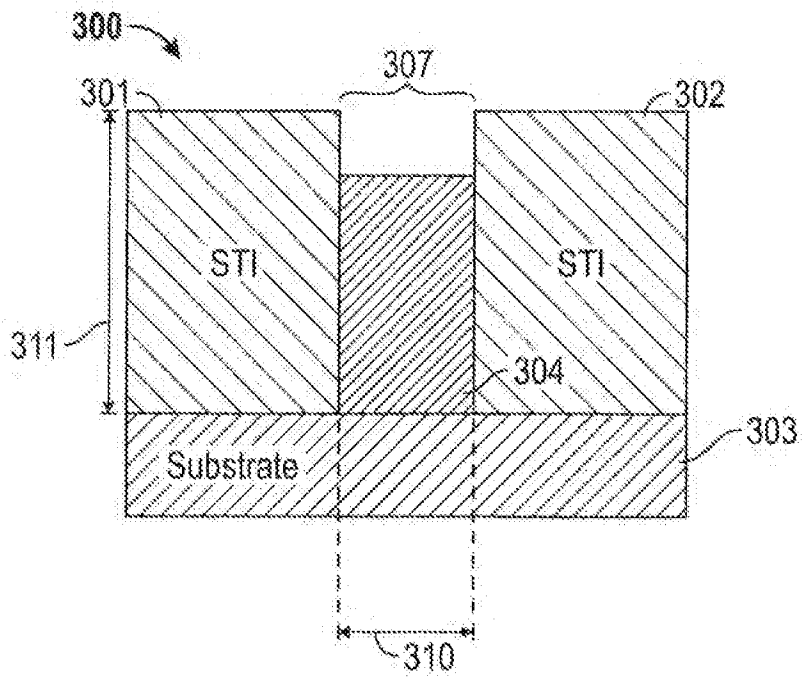


FIG. 3B

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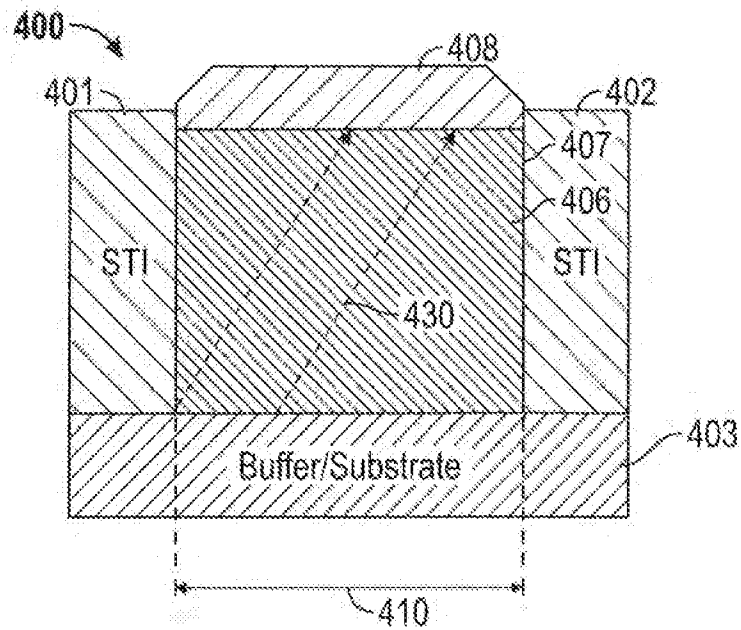


FIG. 4A

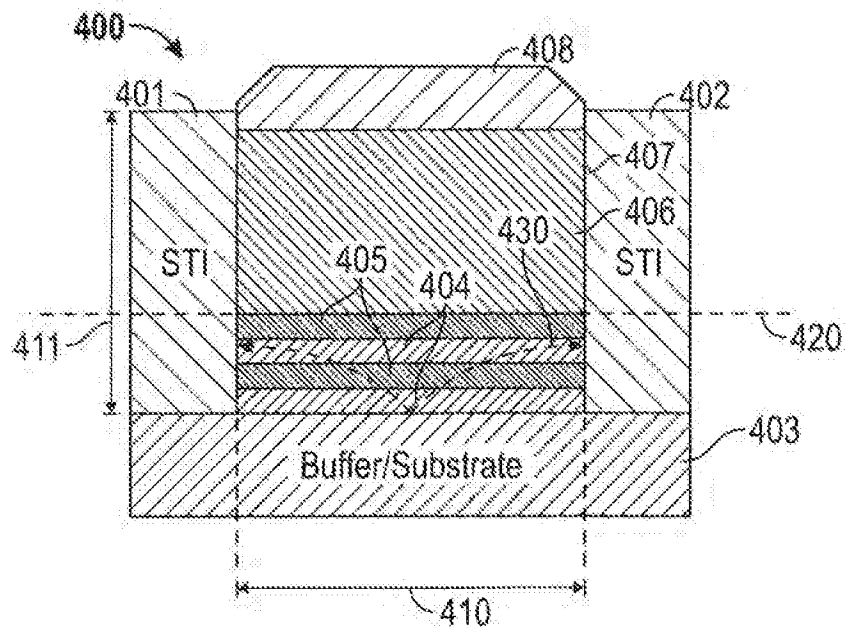


FIG. 4B

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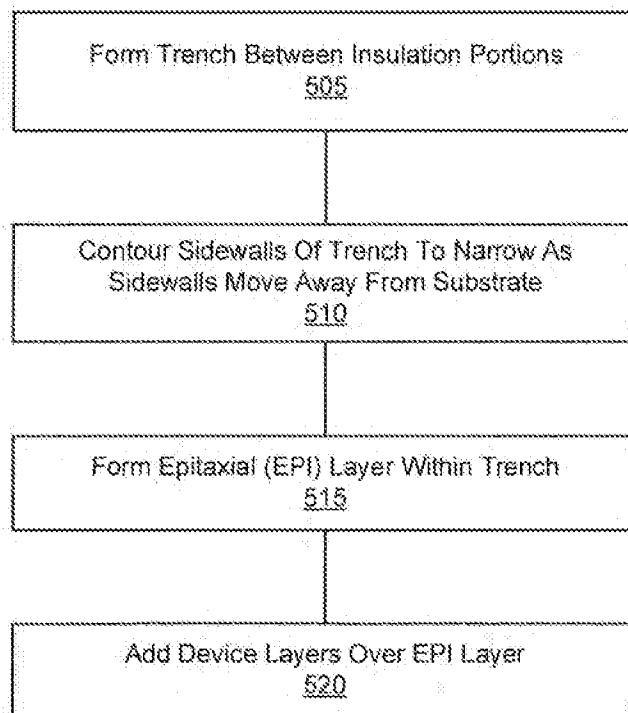
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FIG. 5

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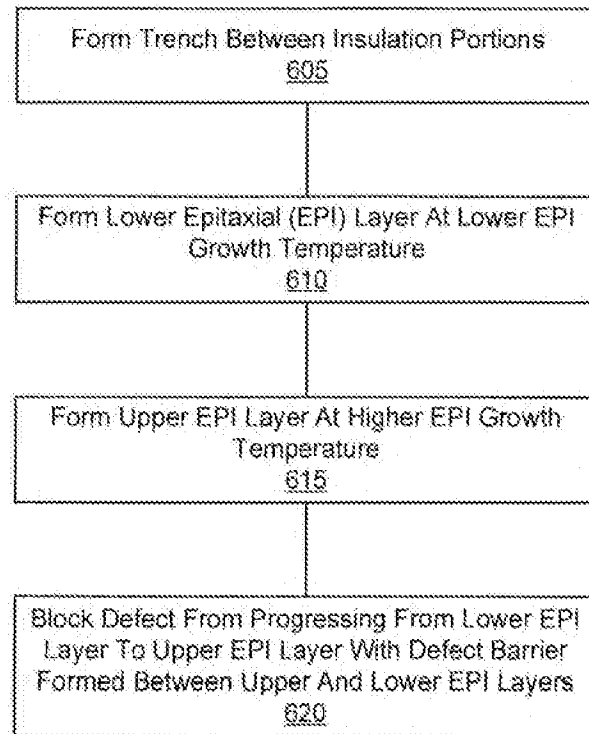
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FIG. 6

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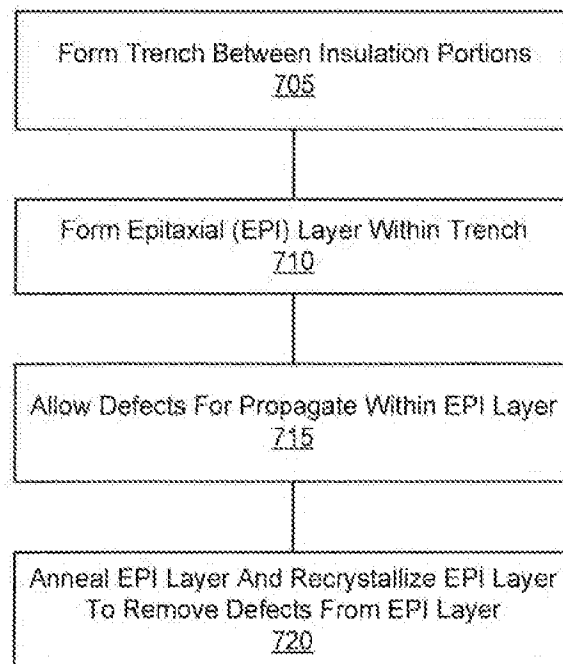
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FIG. 7

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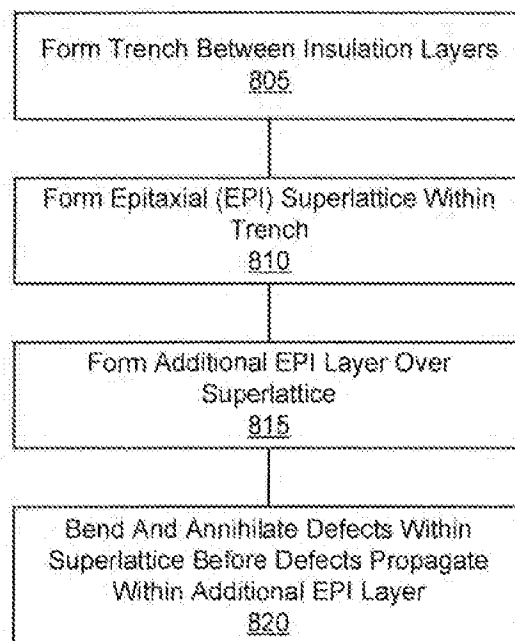
800

FIG. 8

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/20(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/20; H01L 27/088; H01L 21/336; H01L 29/78; H01L 29/04; H01L 29/06; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: trench, width, height, lattice constant and epitaxial

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0088344 A1 (MARK VAN DAL) 12 April 2012 See paragraphs [0011]-[0018], claim 1 and figure 3.	1-3, 5-10, 21-24
A		4, 11-20
Y	US 7682859 B2 (KANGGUO CHENG et al.) 23 March 2010 See column 4, line 62 - column 6, line 4, claims 1-13 and figure 4.	1-3, 5-10, 21-24
A	US 2010-0283108 A1 (MAHITO SAWADA et al.) 11 November 2010 See paragraphs [0048]-[0052], claims 1-12 and figures 1-8.	1-24
A	US 2008-0142880 A1 (RICHARD A. BLANCHARD et al.) 19 June 2008 See paragraphs [0009]-[0010], claims 1-8 and figures 5(a)-5(g).	1-24
A	US 2009-0146263 A1 (XIANGDONG CHEN et al.) 11 June 2009 See paragraphs [0022]-[0029], claim 13 and figures 3C-3H.	1-24



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 October 2013 (28.10.2013)

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/048799

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