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(54) INVERTED MULTIJUNCTION SOLAR CELLS WITH GROUP IV/III-V HYBRID ALLOYS

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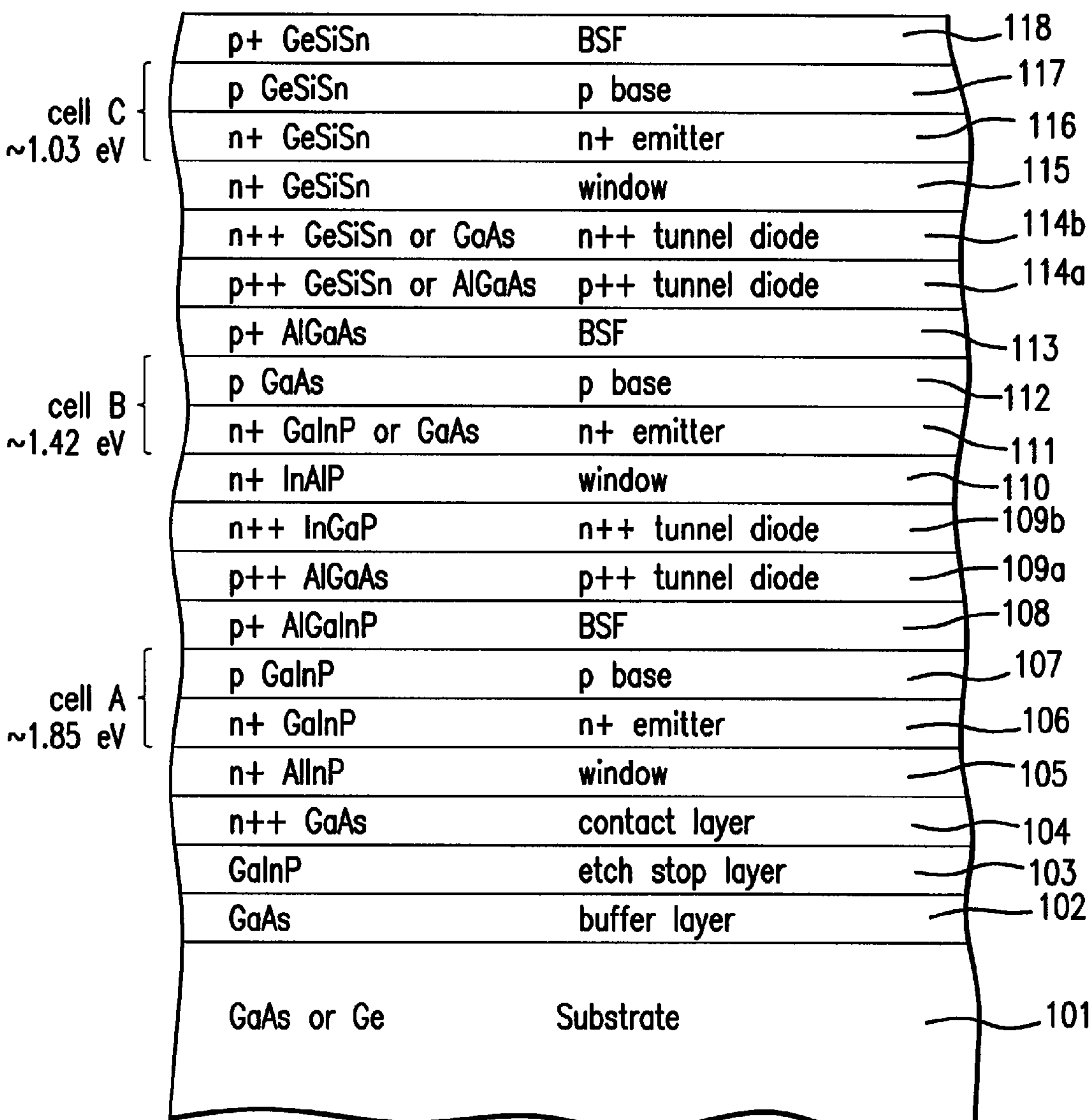
(57) ABSTRACT

A method of manufacturing a solar cell comprising providing a growth substrate; depositing on said growth substrate a sequence of layers of semiconductor material forming a solar cell, including at least one subcell composed of a group IV/III-V hybrid alloy such as GeSiSn; and removing the semiconductor substrate.



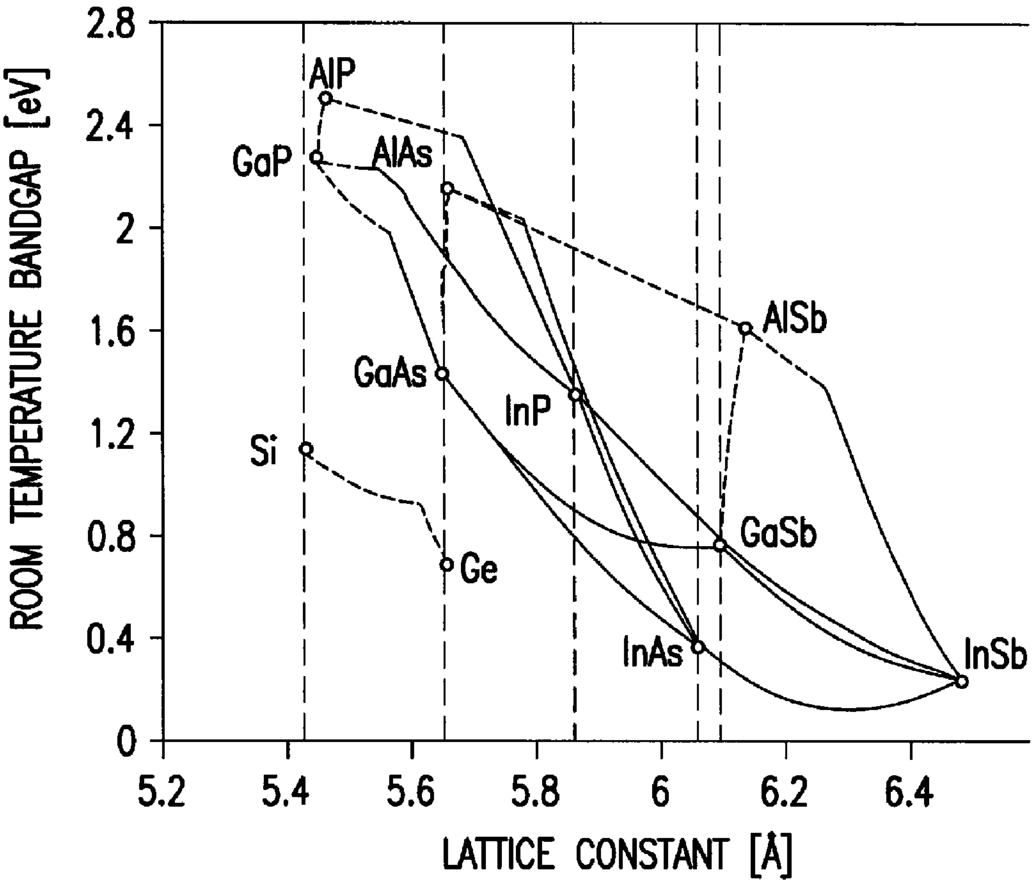

ROOM TEMPERATURE BANDGAP [eV]
2.8
2.4
2
1.6
1.2
0.8
0.4
0
5.2
5.4
5.6
5.8
6
6.2
6.4
LATTICE CONSTANT [Å]
AlP
GaP
AlAs
AlSb
GaAs
InP
Si
Ge
GaSb
InAs
InSb

FIG.1

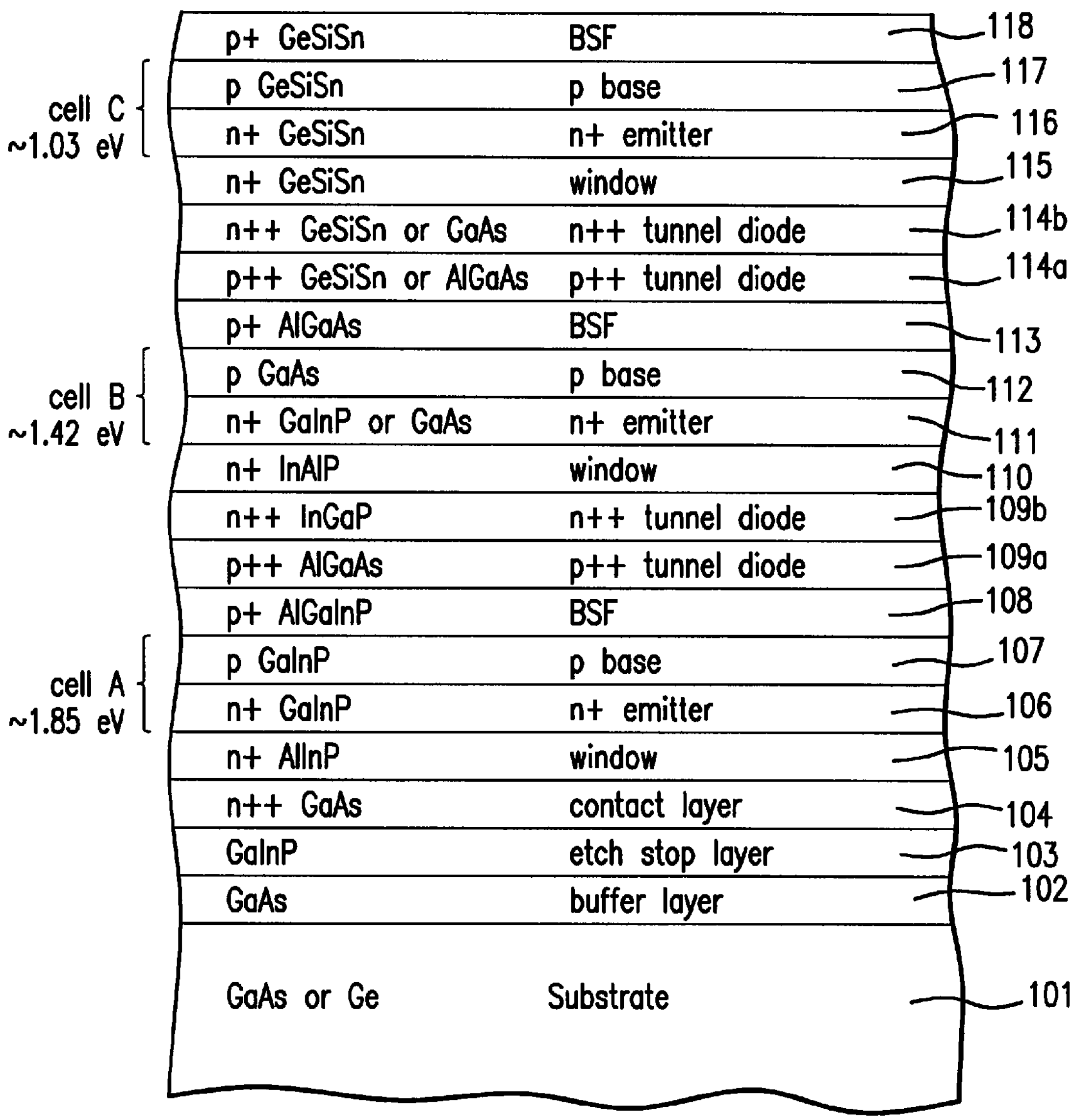

p+ GeSiSn
BSF
118
cell C ~1.03 eV
p GeSiSn
p base
117
n+ GeSiSn
n+ emitter
116
n+ GeSiSn
window
115
n++ GeSiSn or GaAs
n++ tunnel diode
114b
p++ GeSiSn or AlGaAs
p++ tunnel diode
114a
p+ AlGaAs
BSF
113
cell B ~1.42 eV
p GaAs
p base
112
n+ GaInP or GaAs
n+ emitter
111
n+ InAlP
window
110
n++ InGaP
n++ tunnel diode
109b
p++ AlGaAs
p++ tunnel diode
109a
p+ AlGaInP
BSF
108
cell A ~1.85 eV
p GaInP
p base
107
n+ GaInP
n+ emitter
106
n+ AlInP
window
105
n++ GaAs
contact layer
104
GaInP
etch stop layer
103
GaAs
buffer layer
102
GaAs or Ge
Substrate
101

FIG.2A

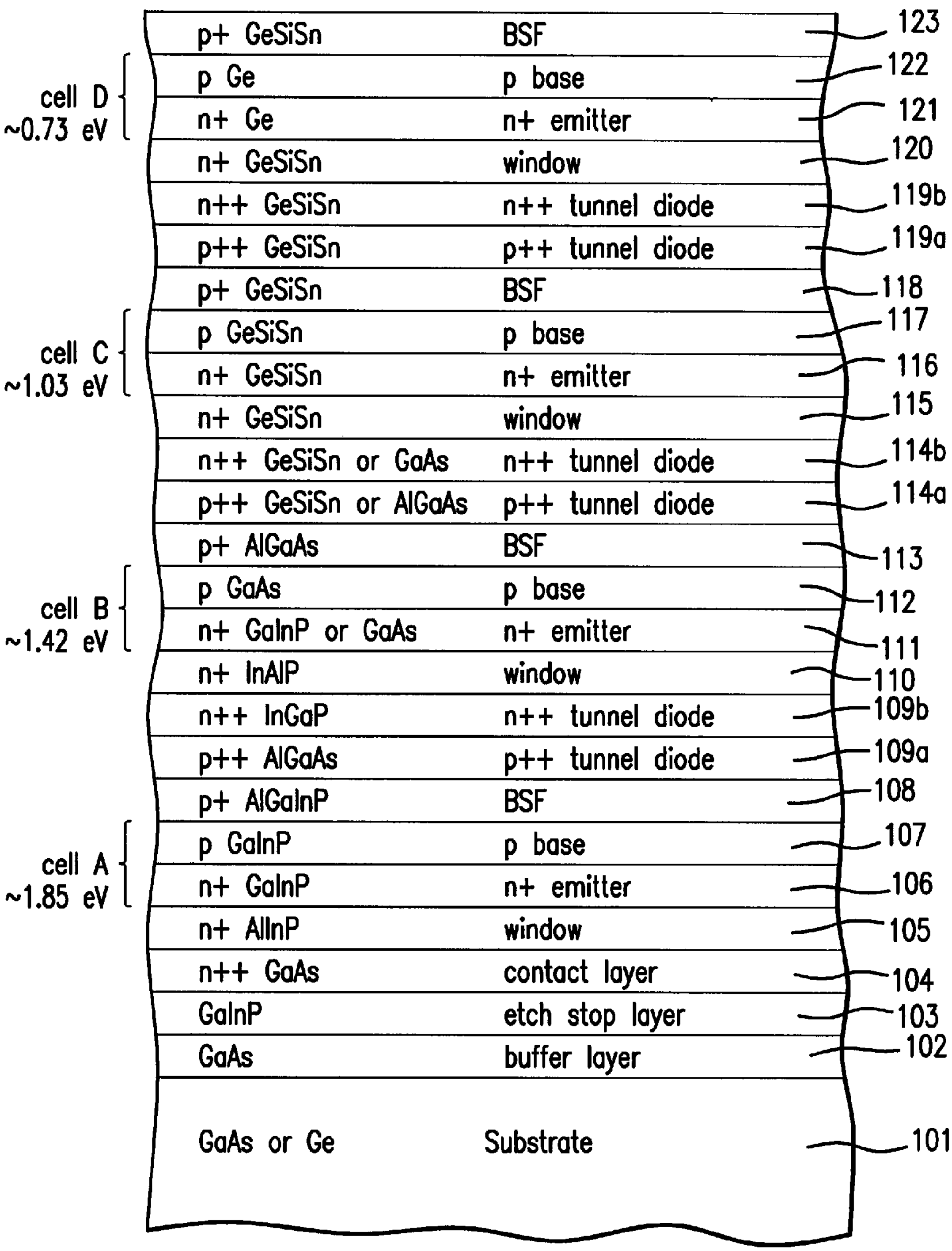
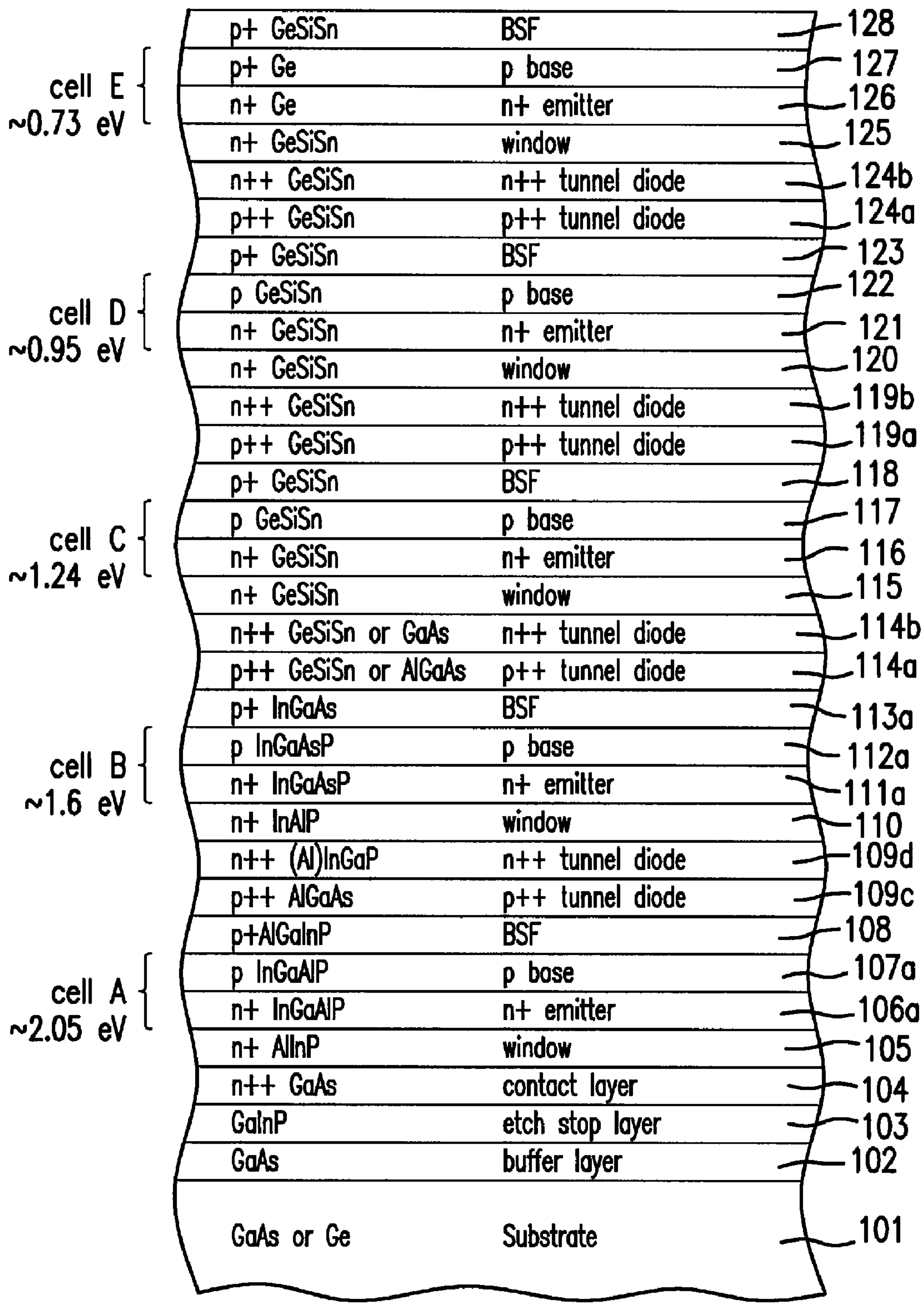

p+ GeSiSn BSF 123
cell D ~0.73 eV
p Ge p base 122
n+ Ge n+ emitter 121
n+ GeSiSn window 120
n++ GeSiSn n++ tunnel diode 119b
p++ GeSiSn p++ tunnel diode 119a
p+ GeSiSn BSF 118
cell C ~1.03 eV
p GeSiSn p base 117
n+ GeSiSn n+ emitter 116
n+ GeSiSn window 115
n++ GeSiSn or GaAs n++ tunnel diode 114b
p++ GeSiSn or AlGaAs p++ tunnel diode 114a
p+ AlGaAs BSF 113
cell B ~1.42 eV
p GaAs p base 112
n+ GaInP or GaAs n+ emitter 111
n+ InAlP window 110
n++ InGaP n++ tunnel diode 109b
p++ AlGaAs p++ tunnel diode 109a
p+ AlGaInP BSF 108
cell A ~1.85 eV
p GaInP p base 107
n+ GaInP n+ emitter 106
n+ AlInP window 105
n++ GaAs contact layer 104
GaInP etch stop layer 103
GaAs buffer layer 102
GaAs or Ge Substrate 101

FIG.2B



p+ GeSiSn BSF 128
p+ Ge p base 127
n+ Ge n+ emitter 126
n+ GeSiSn window 125
n++ GeSiSn n++ tunnel diode 124b
p++ GeSiSn p++ tunnel diode 124a
p+ GeSiSn BSF 123
p GeSiSn p base 122
n+ GeSiSn n+ emitter 121
n+ GeSiSn window 120
n++ GeSiSn n++ tunnel diode 119b
p++ GeSiSn p++ tunnel diode 119a
p+ GeSiSn BSF 118
p GeSiSn p base 117
n+ GeSiSn n+ emitter 116
n+ GeSiSn window 115
n++ GeSiSn or GaAs n++ tunnel diode 114b
p++ GeSiSn or AlGaAs p++ tunnel diode 114a
p+ InGaAs BSF 113a
p InGaAsP p base 112a
n+ InGaAsP n+ emitter 111a
n+ InAlP window 110
n++ (Al)InGaP n++ tunnel diode 109d
p++ AlGaAs p++ tunnel diode 109c
p+AlGaInP BSF 108
p InGaAlP p base 107a
n+ InGaAlP n+ emitter 106a
n+ AlInP window 105
n++ GaAs contact layer 104
GaInP etch stop layer 103
GaAs buffer layer 102
GaAs or Ge Substrate 101
cell E ~0.73 eV
cell D ~0.95 eV
cell C ~1.24 eV
cell B ~1.6 eV
cell A ~2.05 eV

FIG.2C

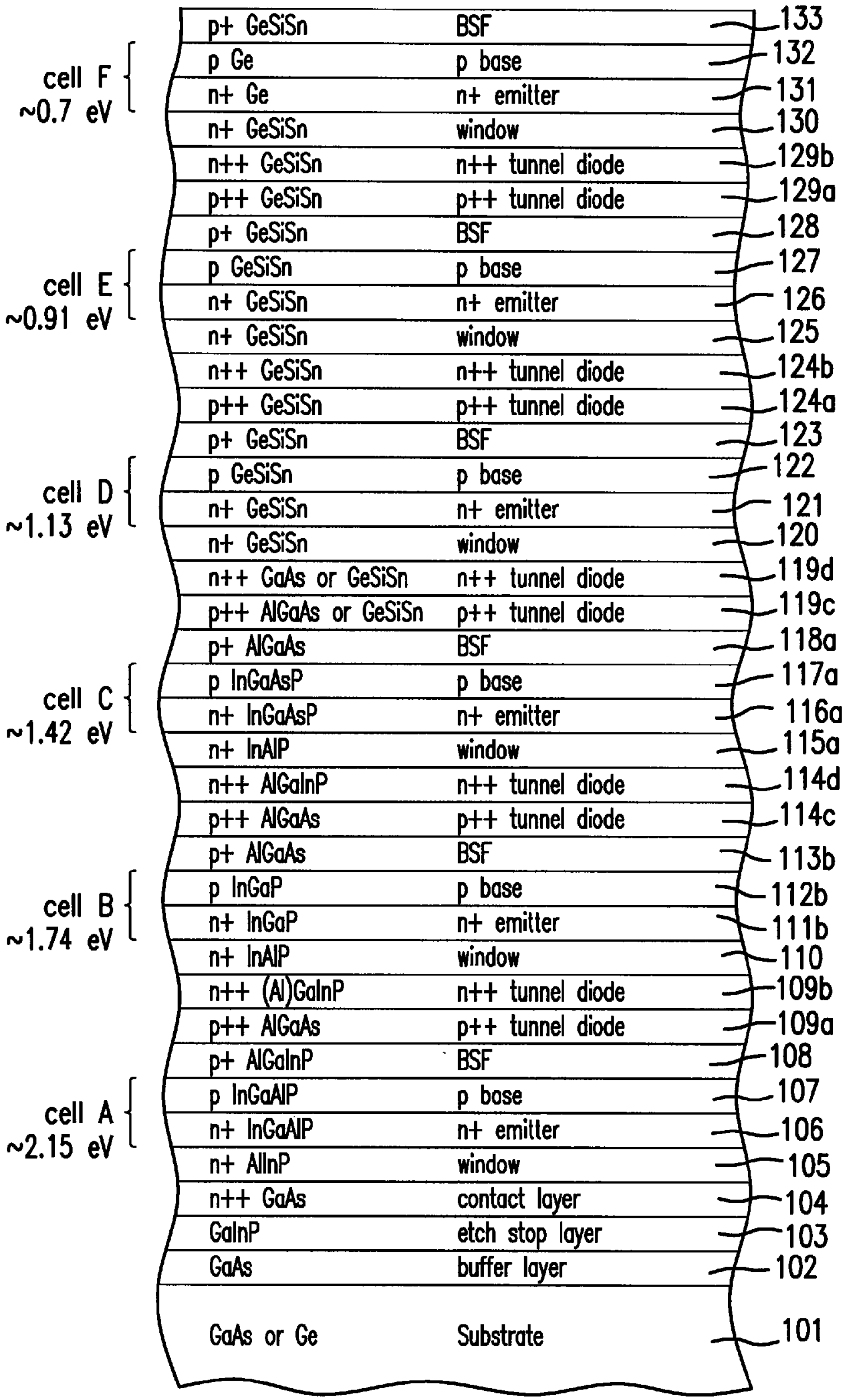
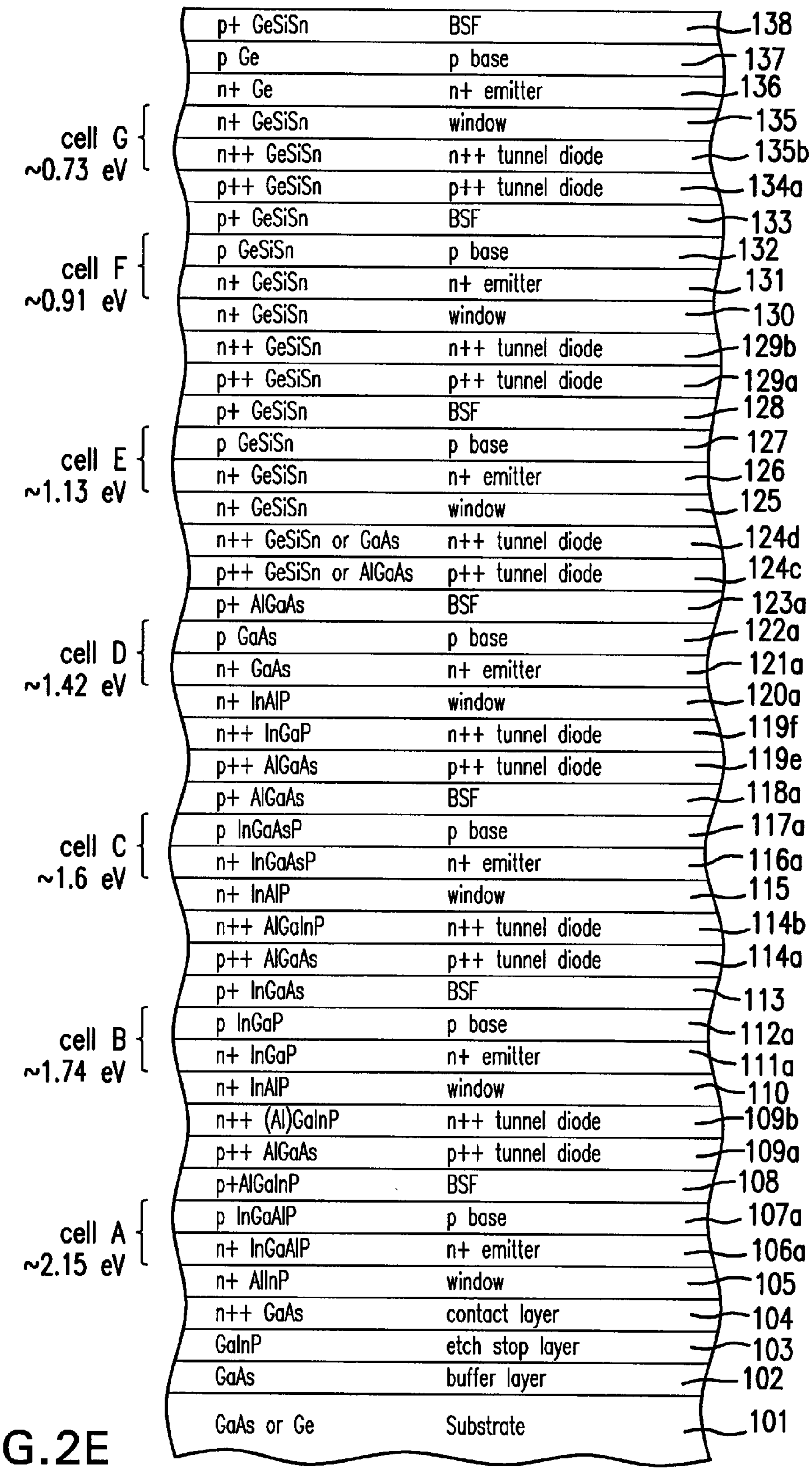

p+ GeSiSn BSF 133
cell F ~0.7 eV
p Ge p base 132
n+ Ge n+ emitter 131
n+ GeSiSn window 130
n++ GeSiSn n++ tunnel diode 129b
p++ GeSiSn p++ tunnel diode 129a
p+ GeSiSn BSF 128
cell E ~0.91 eV
p GeSiSn p base 127
n+ GeSiSn n+ emitter 126
n+ GeSiSn window 125
n++ GeSiSn n++ tunnel diode 124b
p++ GeSiSn p++ tunnel diode 124a
p+ GeSiSn BSF 123
cell D ~1.13 eV
p GeSiSn p base 122
n+ GeSiSn n+ emitter 121
n+ GeSiSn window 120
n++ GaAs or GeSiSn n++ tunnel diode 119d
p++ AlGaAs or GeSiSn p++ tunnel diode 119c
p+ AlGaAs BSF 118a
cell C ~1.42 eV
p InGaAsP p base 117a
n+ InGaAsP n+ emitter 116a
n+ InAlP window 115a
n++ AlGaInP n++ tunnel diode 114d
p++ AlGaAs p++ tunnel diode 114c
p+ AlGaAs BSF 113b
cell B ~1.74 eV
p InGaP p base 112b
n+ InGaP n+ emitter 111b
n+ InAlP window 110
n++ (Al)GaInP n++ tunnel diode 109b
p++ AlGaAs p++ tunnel diode 109a
p+ AlGaInP BSF 108
cell A ~2.15 eV
p InGaAlP p base 107
n+ InGaAlP n+ emitter 106
n+ AlInP window 105
n++ GaAs contact layer 104
GaInP etch stop layer 103
GaAs buffer layer 102
GaAs or Ge Substrate 101

FIG.2D



p+ GeSiSn BSF 138
p Ge p base 137
n+ Ge n+ emitter 136
n+ GeSiSn window 135
n++ GeSiSn n++ tunnel diode 135b
p++ GeSiSn p++ tunnel diode 134a
p+ GeSiSn BSF 133
p GeSiSn p base 132
n+ GeSiSn n+ emitter 131
n+ GeSiSn window 130
n++ GeSiSn n++ tunnel diode 129b
p++ GeSiSn p++ tunnel diode 129a
p+ GeSiSn BSF 128
p GeSiSn p base 127
n+ GeSiSn n+ emitter 126
n+ GeSiSn window 125
n++ GeSiSn or GaAs n++ tunnel diode 124d
p++ GeSiSn or AlGaAs p++ tunnel diode 124c
p+ AlGaAs BSF 123a
p GaAs p base 122a
n+ GaAs n+ emitter 121a
n+ InAlP window 120a
n++ InGaP n++ tunnel diode 119f
p++ AlGaAs p++ tunnel diode 119e
p+ AlGaAs BSF 118a
p InGaAsP p base 117a
n+ InGaAsP n+ emitter 116a
n+ InAlP window 115
n++ AlGaInP n++ tunnel diode 114b
p++ AlGaAs p++ tunnel diode 114a
p+ InGaAs BSF 113
p InGaP p base 112a
n+ InGaP n+ emitter 111a
n+ InAlP window 110
n++ (Al)GaInP n++ tunnel diode 109b
p++ AlGaAs p++ tunnel diode 109a
p+AlGaInP BSF 108
p InGaAlP p base 107a
n+ InGaAlP n+ emitter 106a
n+ AlInP window 105
n++ GaAs contact layer 104
GaInP etch stop layer 103
GaAs buffer layer 102
GaAs or Ge Substrate 101
cell G ~0.73 eV
cell F ~0.91 eV
cell E ~1.13 eV
cell D ~1.42 eV
cell C ~1.6 eV
cell B ~1.74 eV
cell A ~2.15 eV

FIG.2E

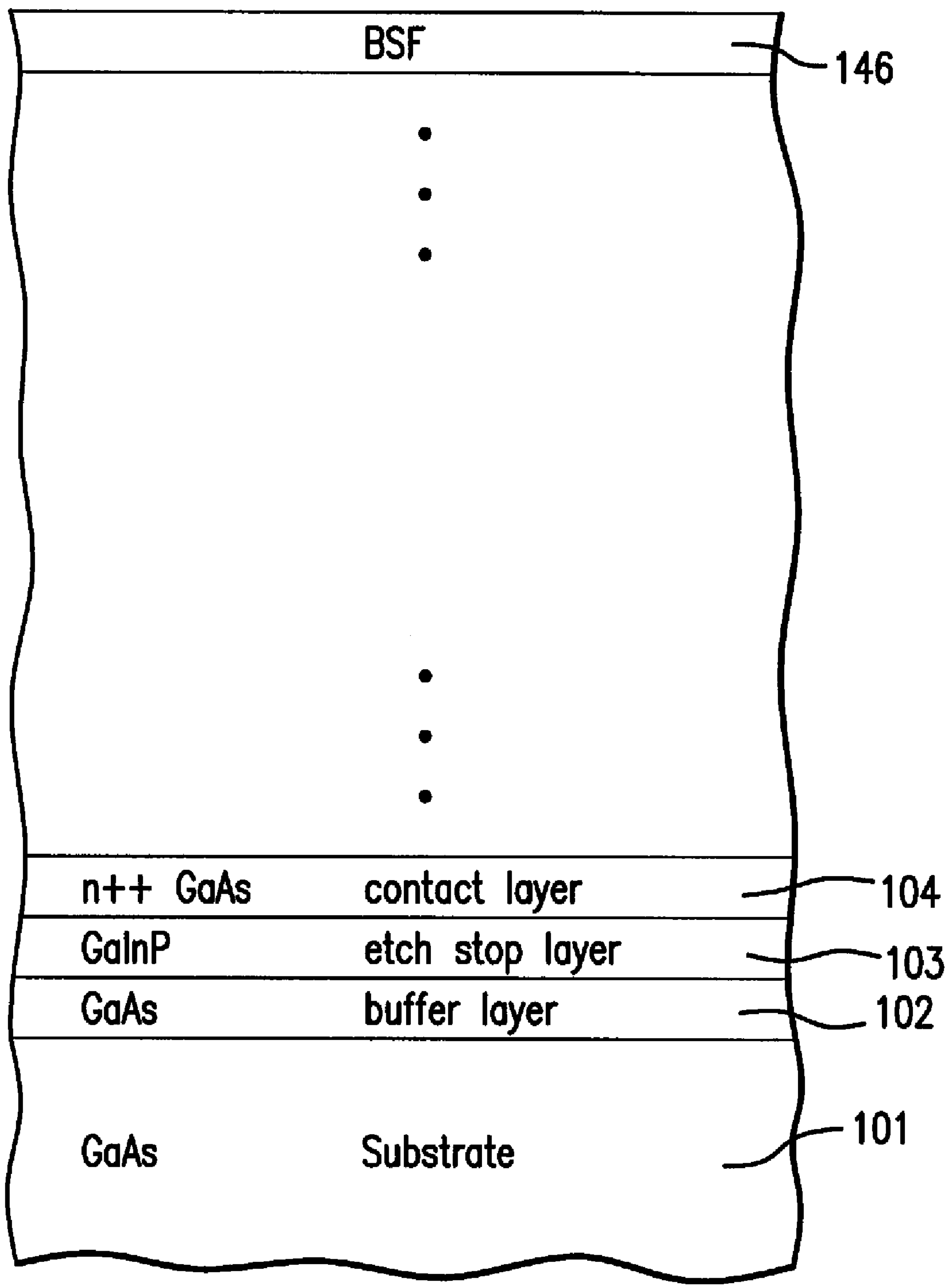

BSF
146
n++ GaAs contact layer
104
GaInP etch stop layer
103
GaAs buffer layer
102
GaAs Substrate
101

FIG.3

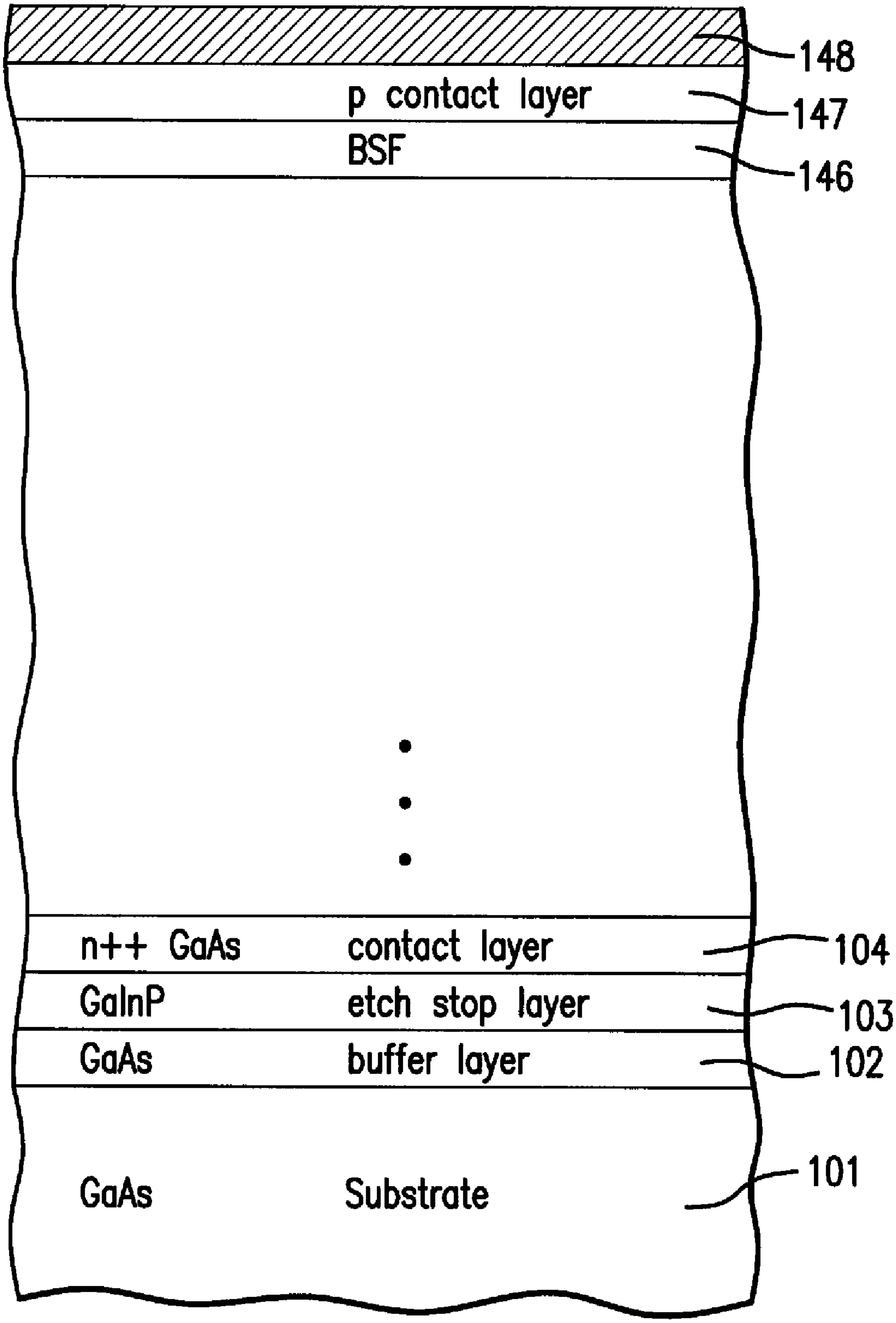

148
p contact layer
147
BSF
146
n++ GaAs
contact layer
104
GaInP
etch stop layer
103
GaAs
buffer layer
102
GaAs
Substrate
101

FIG.4

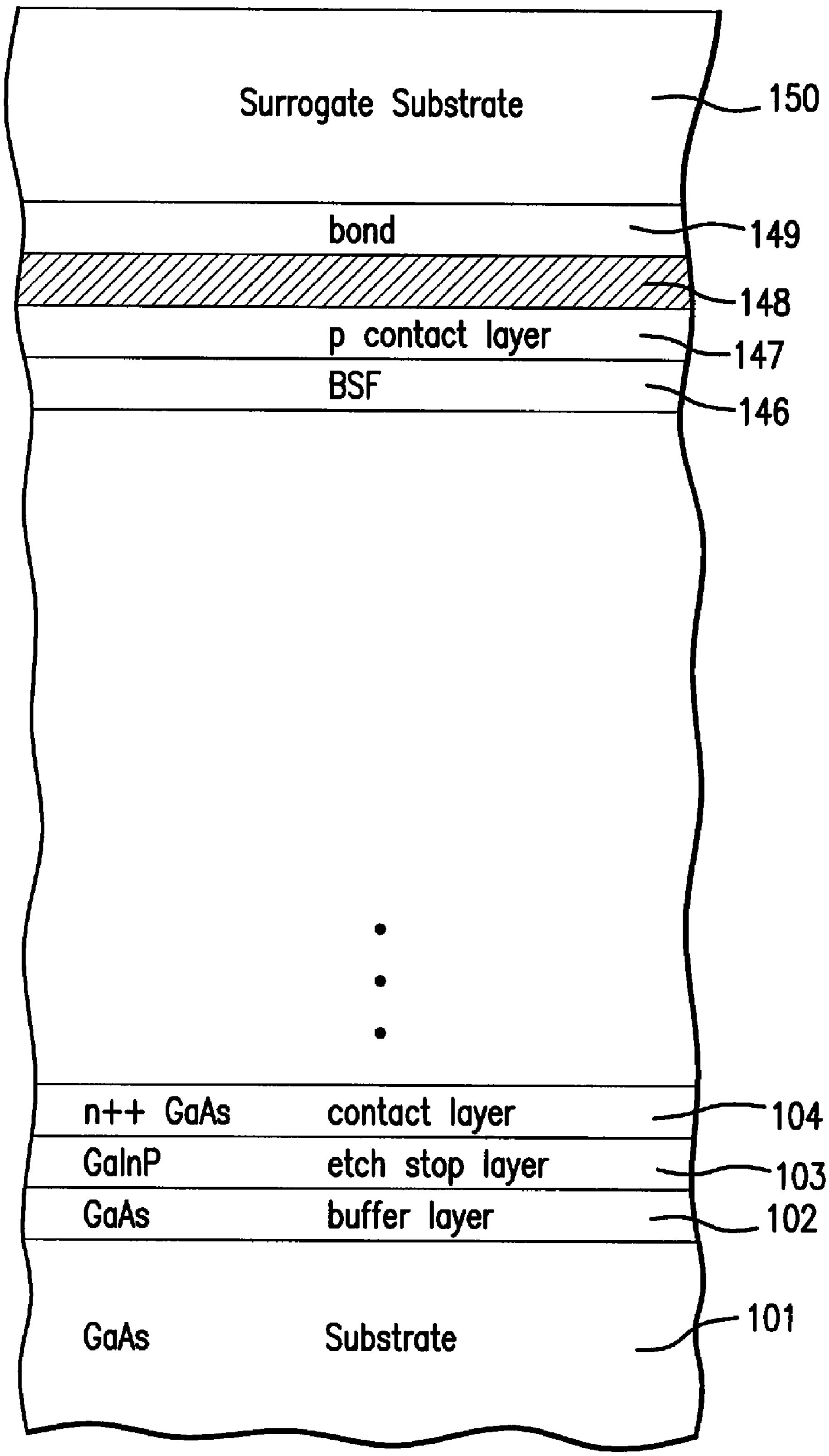

Surrogate Substrate
150
bond
149
148
p contact layer
147
BSF
146
n++ GaAs contact layer
104
GaInP etch stop layer
103
GaAs buffer layer
102
GaAs Substrate
101

FIG.5

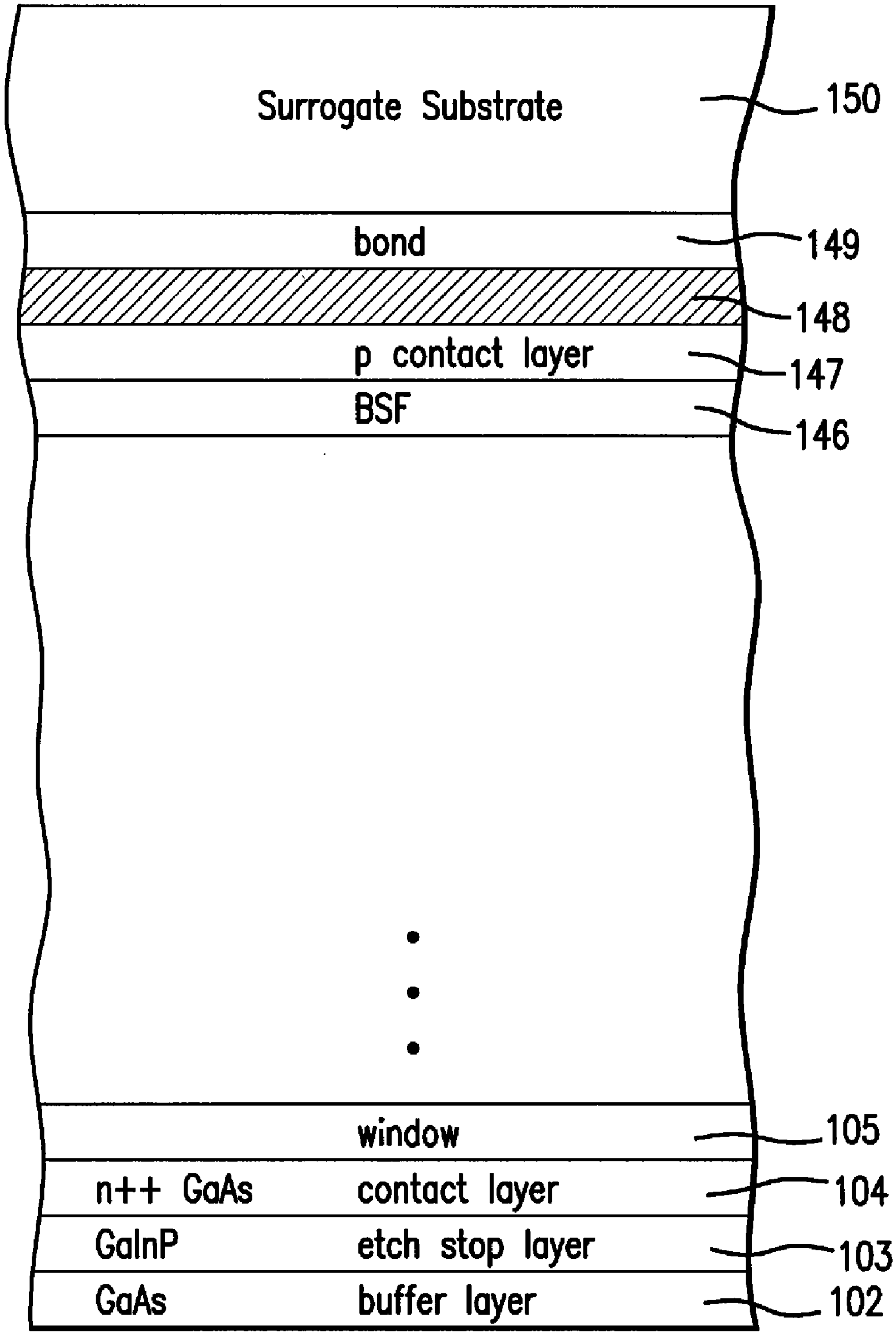

Surrogate Substrate
150
bond
149
148
p contact layer
147
BSF
146
window
105
n++ GaAs
contact layer
104
GaInP
etch stop layer
103
GaAs
buffer layer
102

FIG.6A

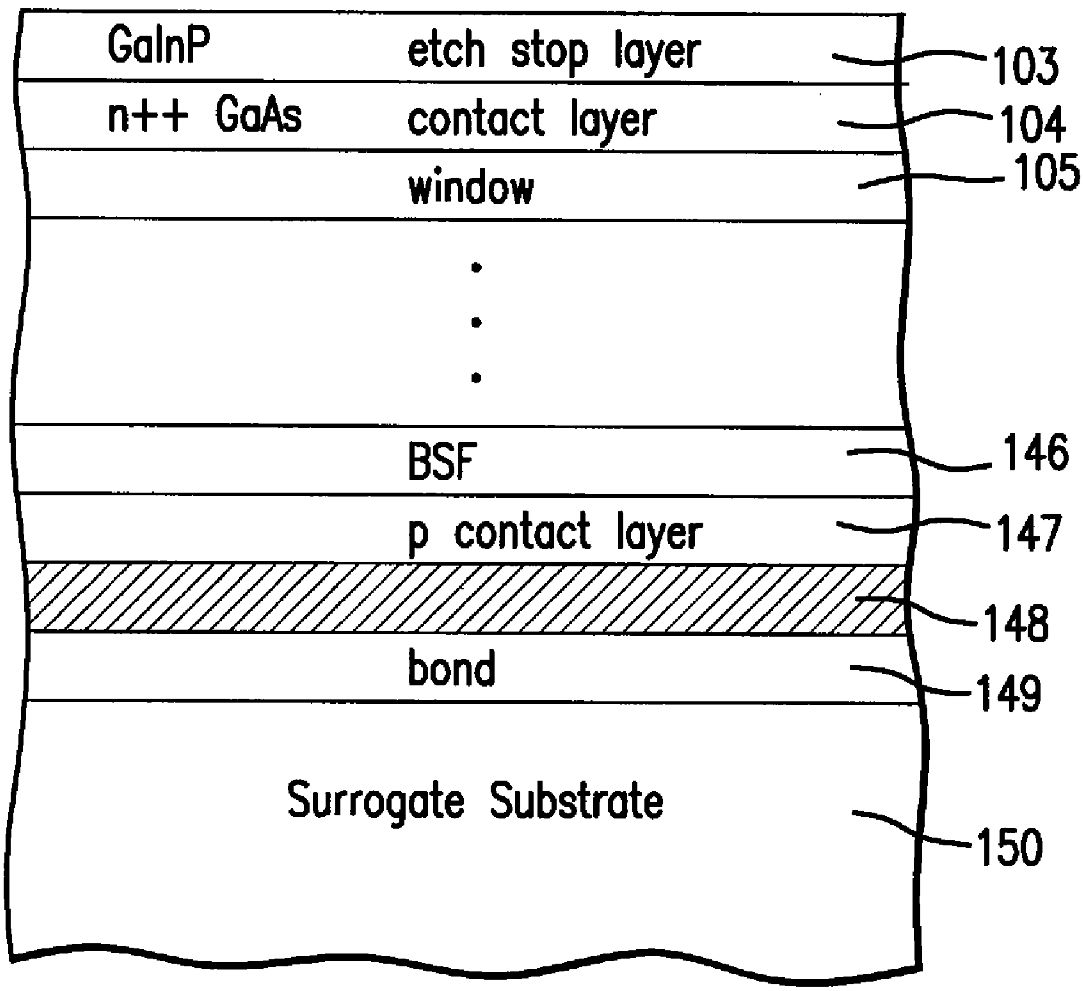

GaInP
etch stop layer
103
n++ GaAs
contact layer
104
window
105
BSF
146
p contact layer
147
148
bond
149
Surrogate Substrate
150

FIG.6B

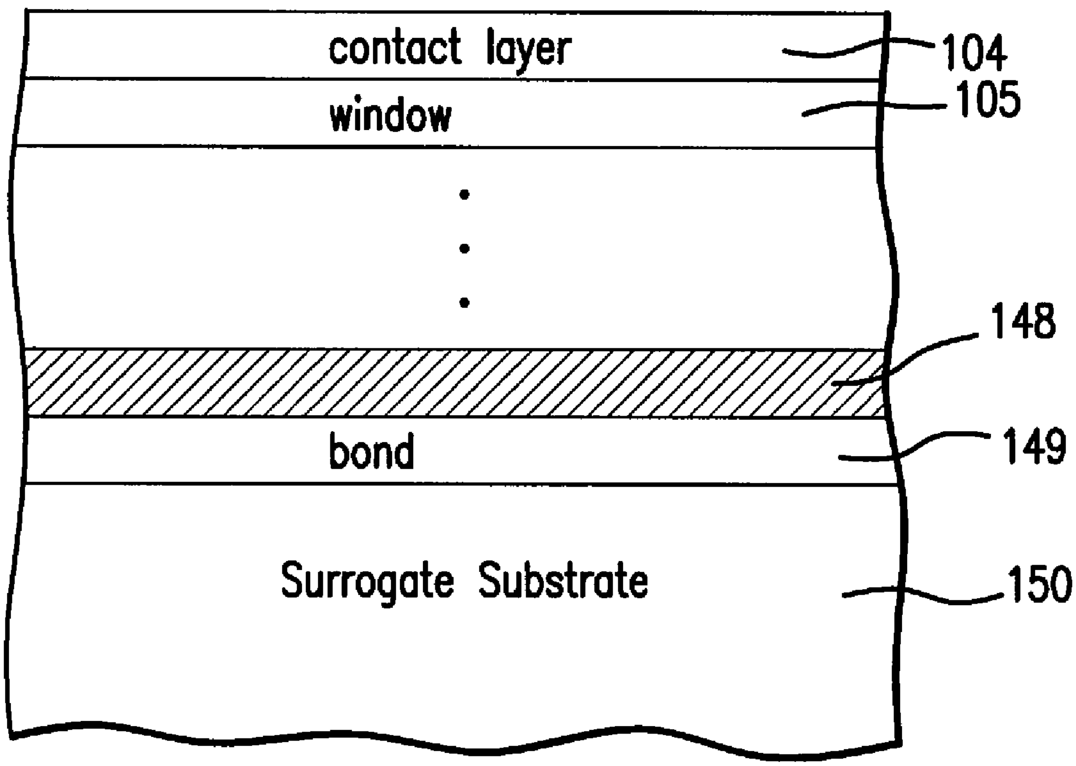

contact layer
104
window
105
148
bond
149
Surrogate Substrate
150

FIG.7

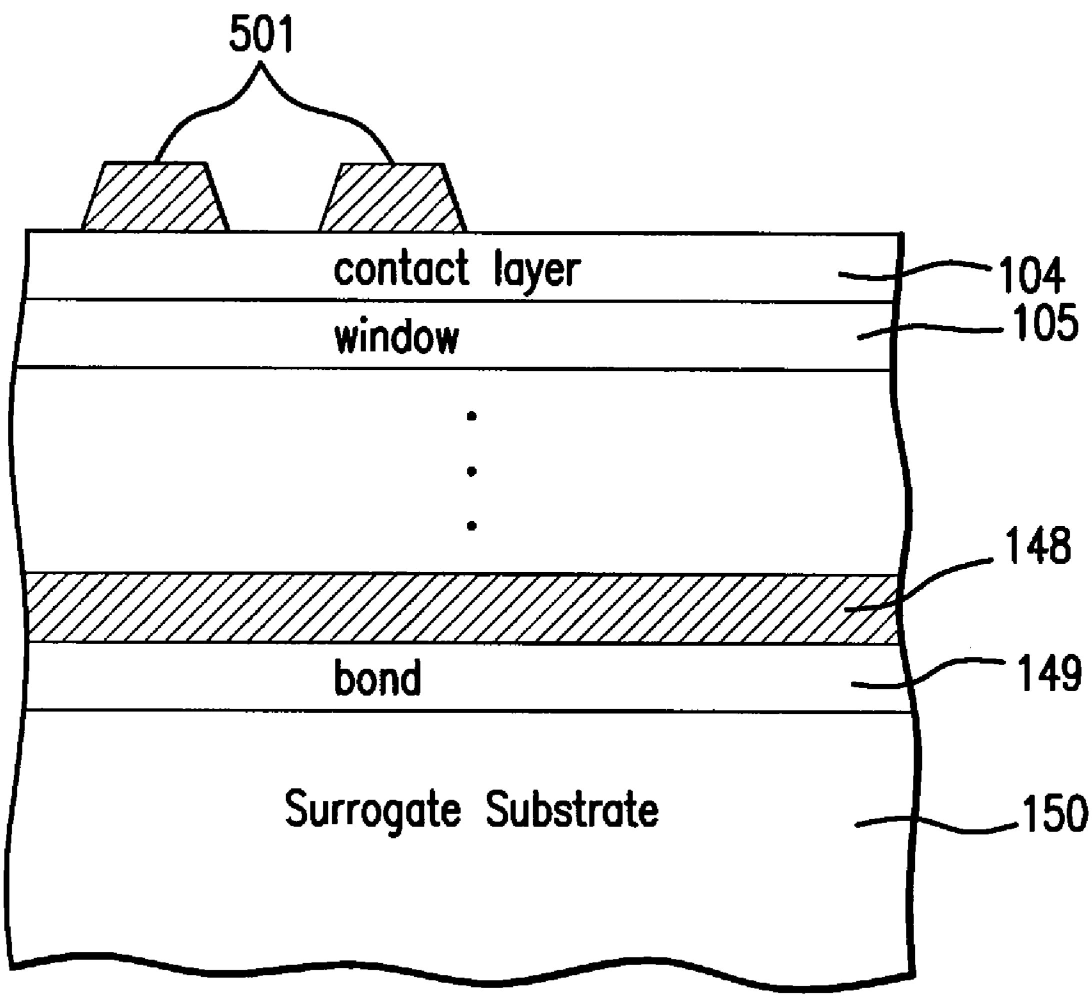

501
contact layer
104
window
105
148
bond
149
Surrogate Substrate
150

FIG.8

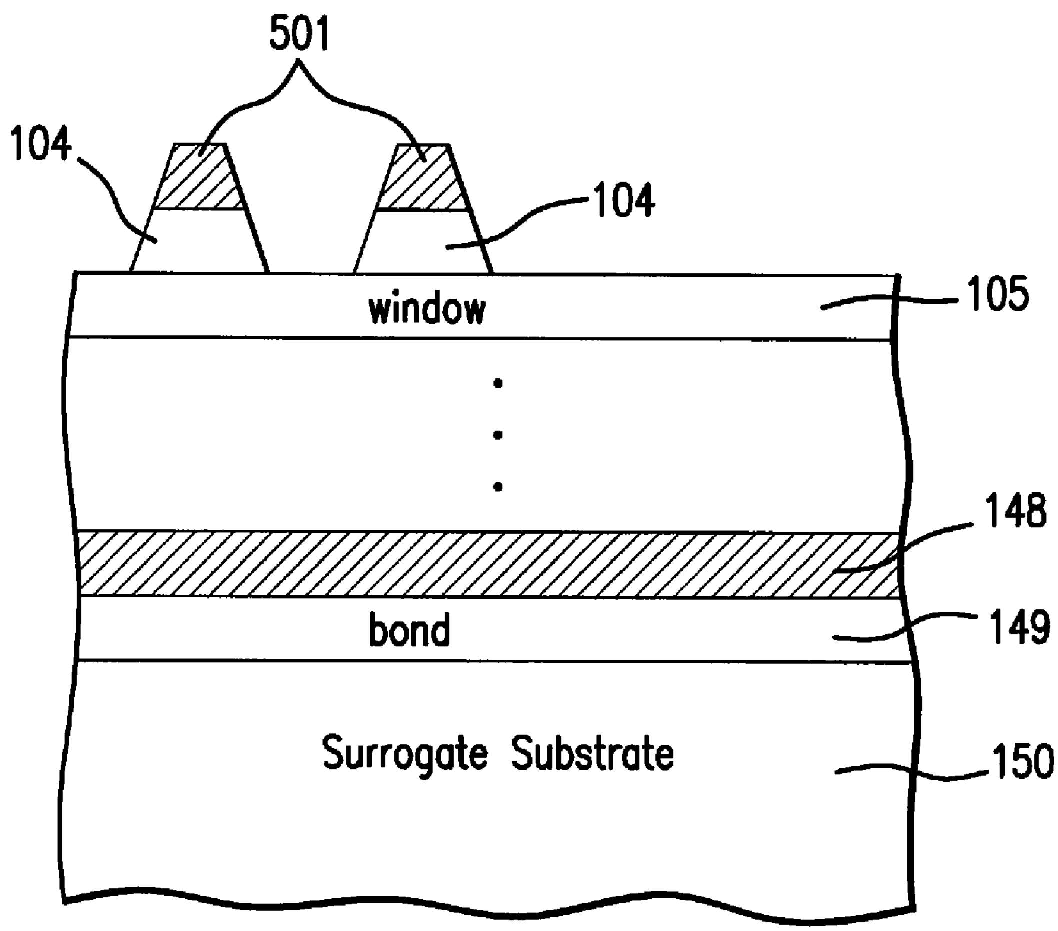


FIG.9

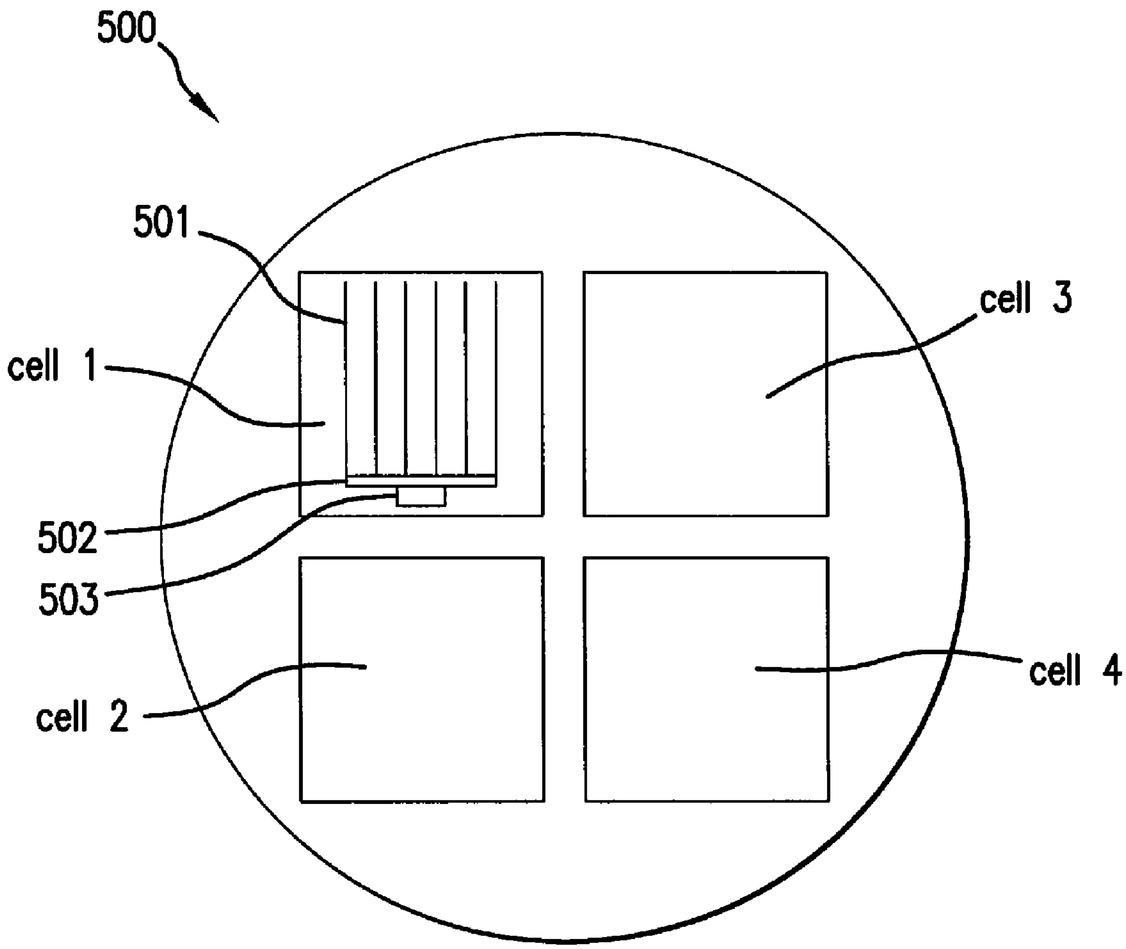


FIG.10A

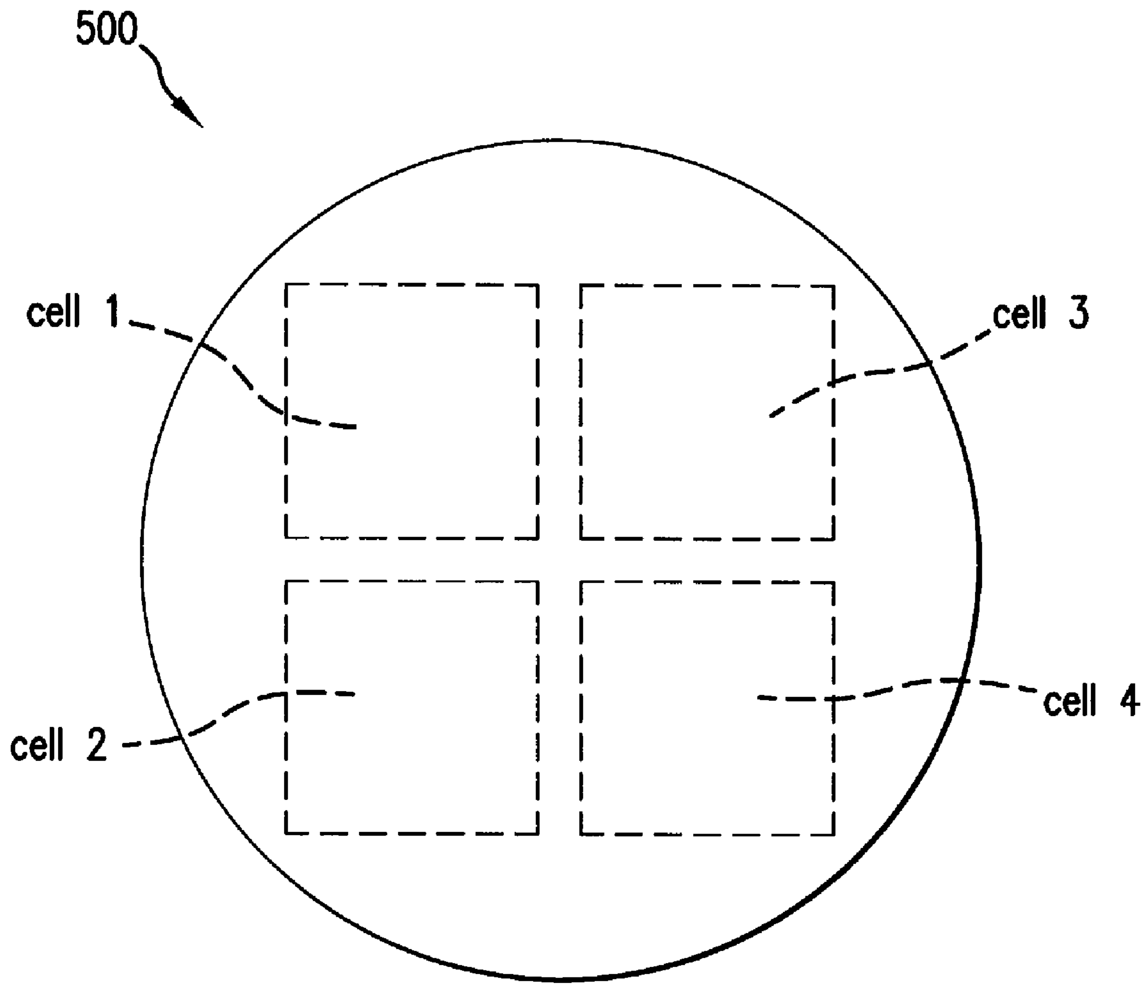


FIG.10B

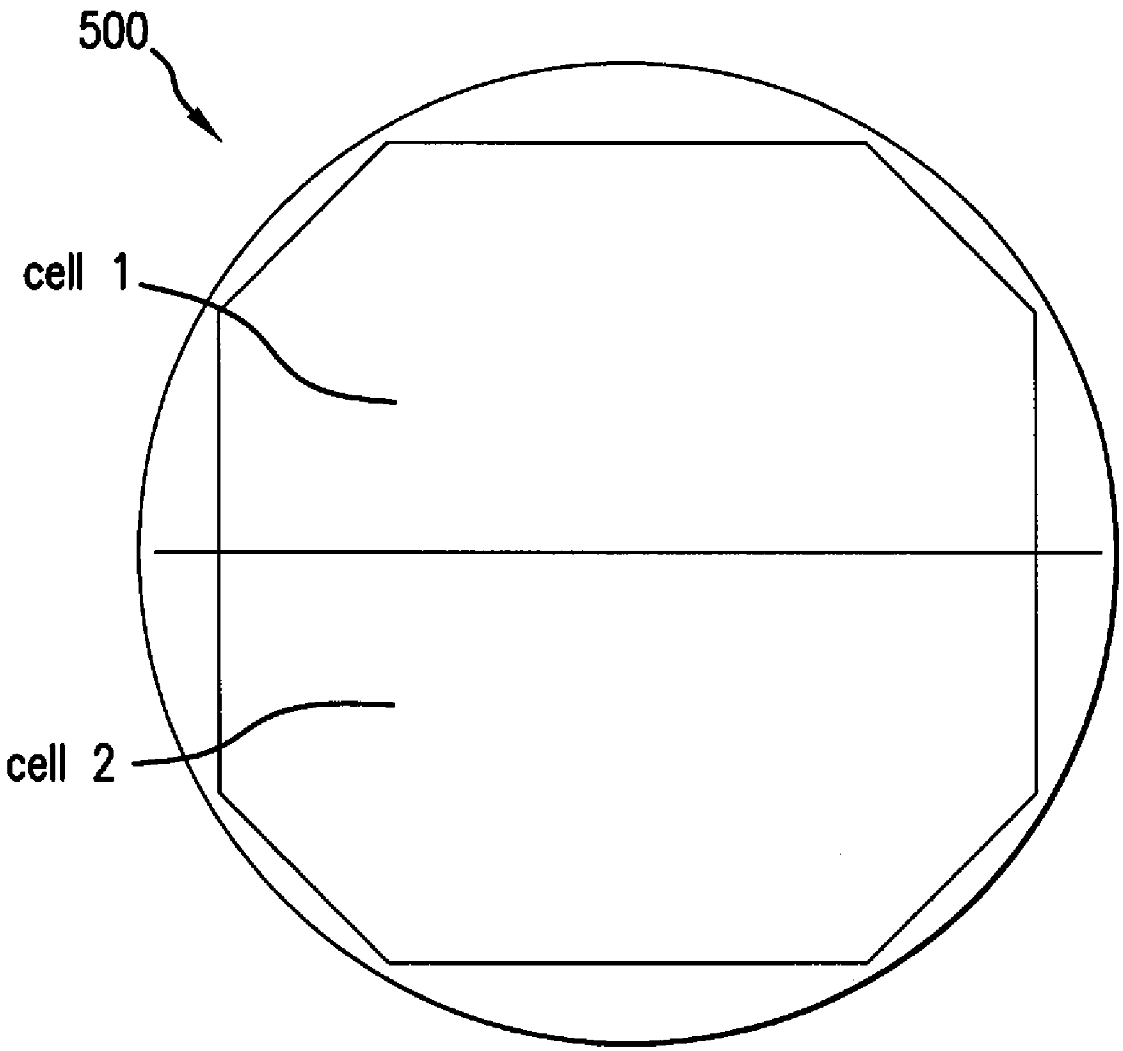


FIG. 10C

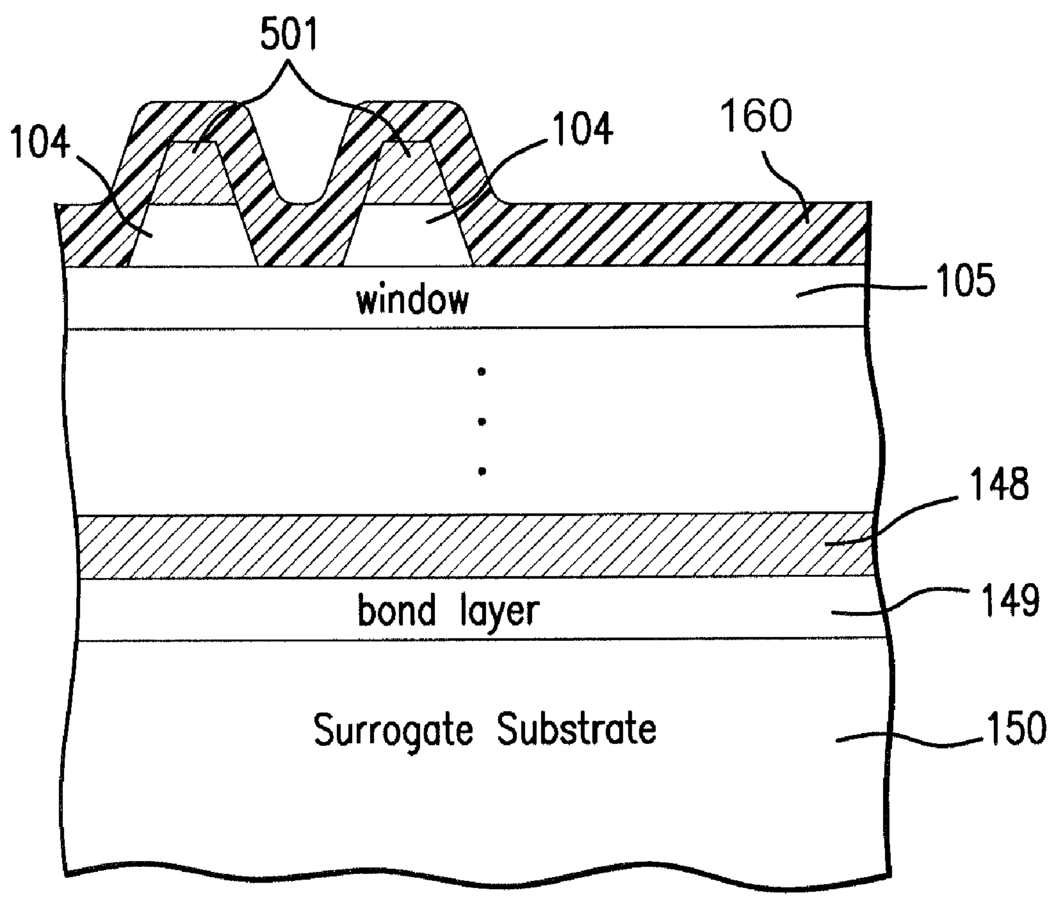

501
104
104
160
window
105
148
bond layer
149
Surrogate Substrate
150

FIG.11

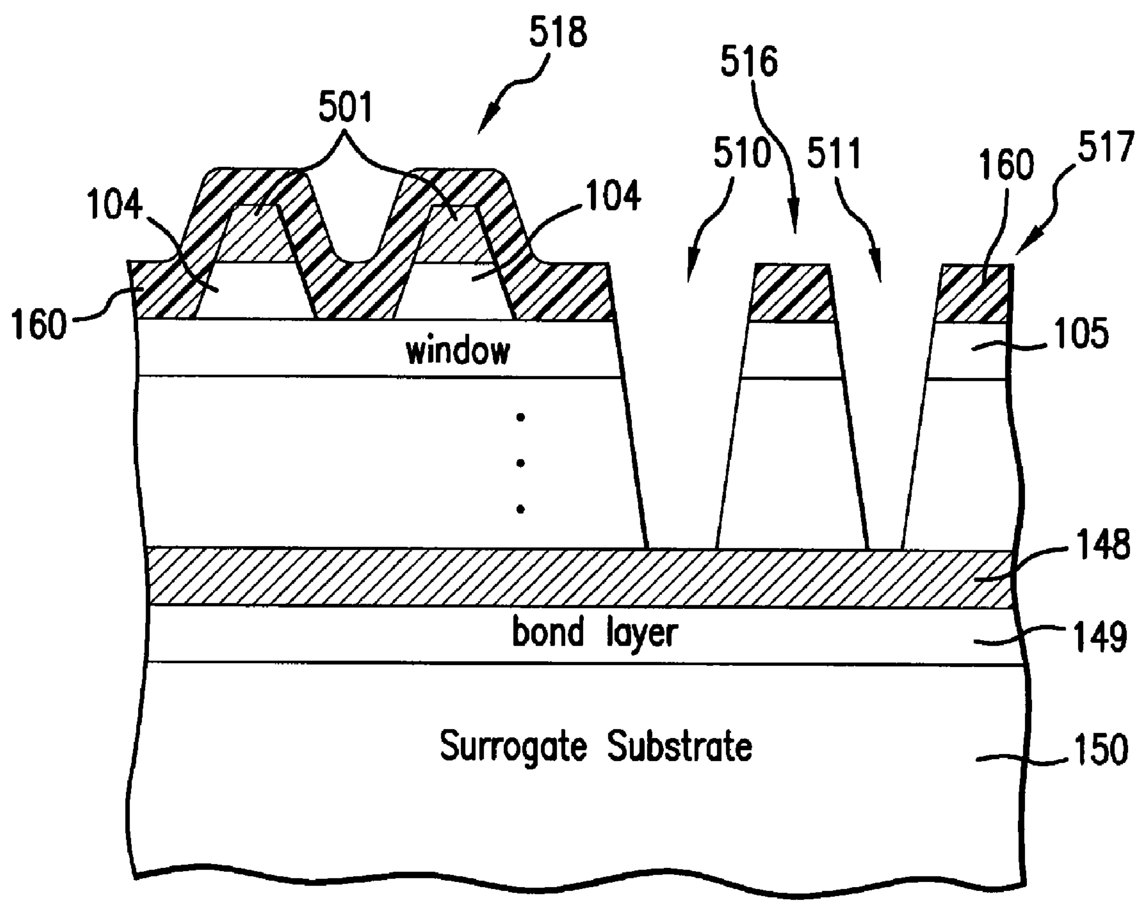

518
501
516
510
511
160
517
104
104
160
window
105
148
bond layer
149
Surrogate Substrate
150

FIG.12A

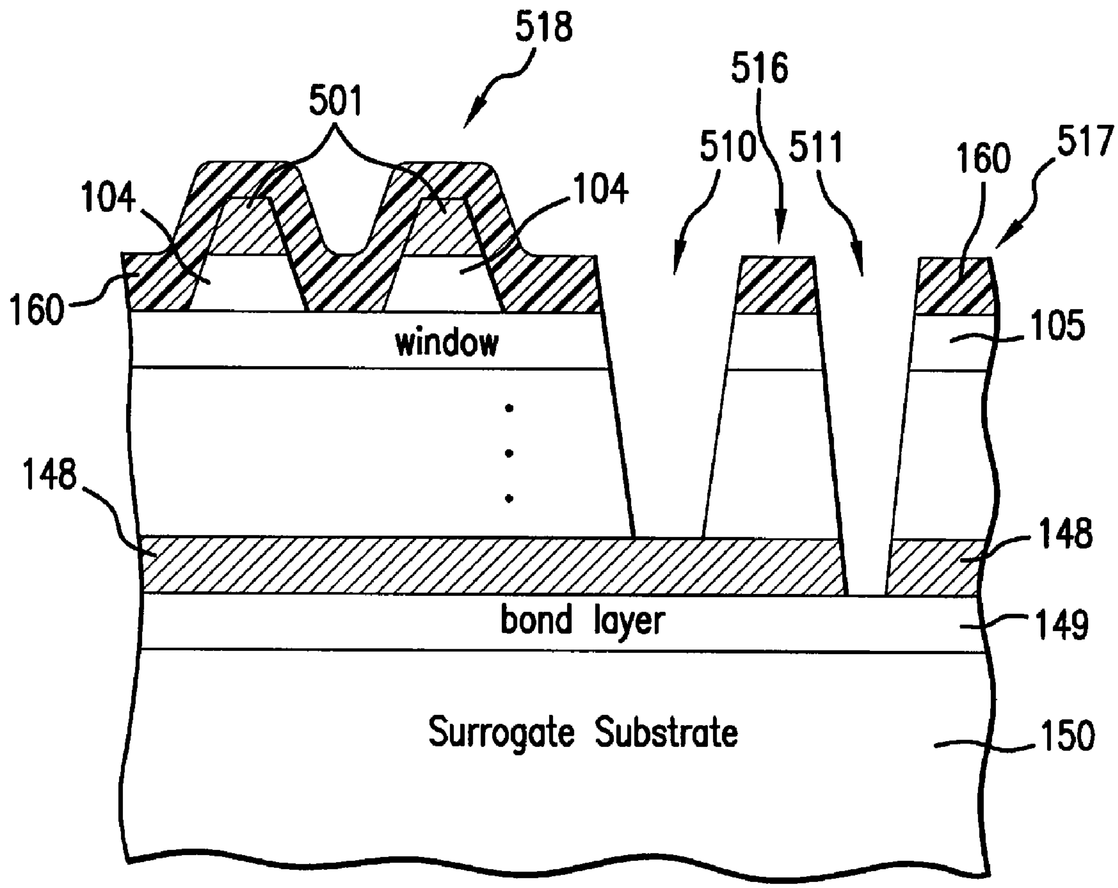

518
501
516
510
511
517
104
104
160
160
window
105
148
148
bond layer
149
Surrogate Substrate
150

FIG.12B

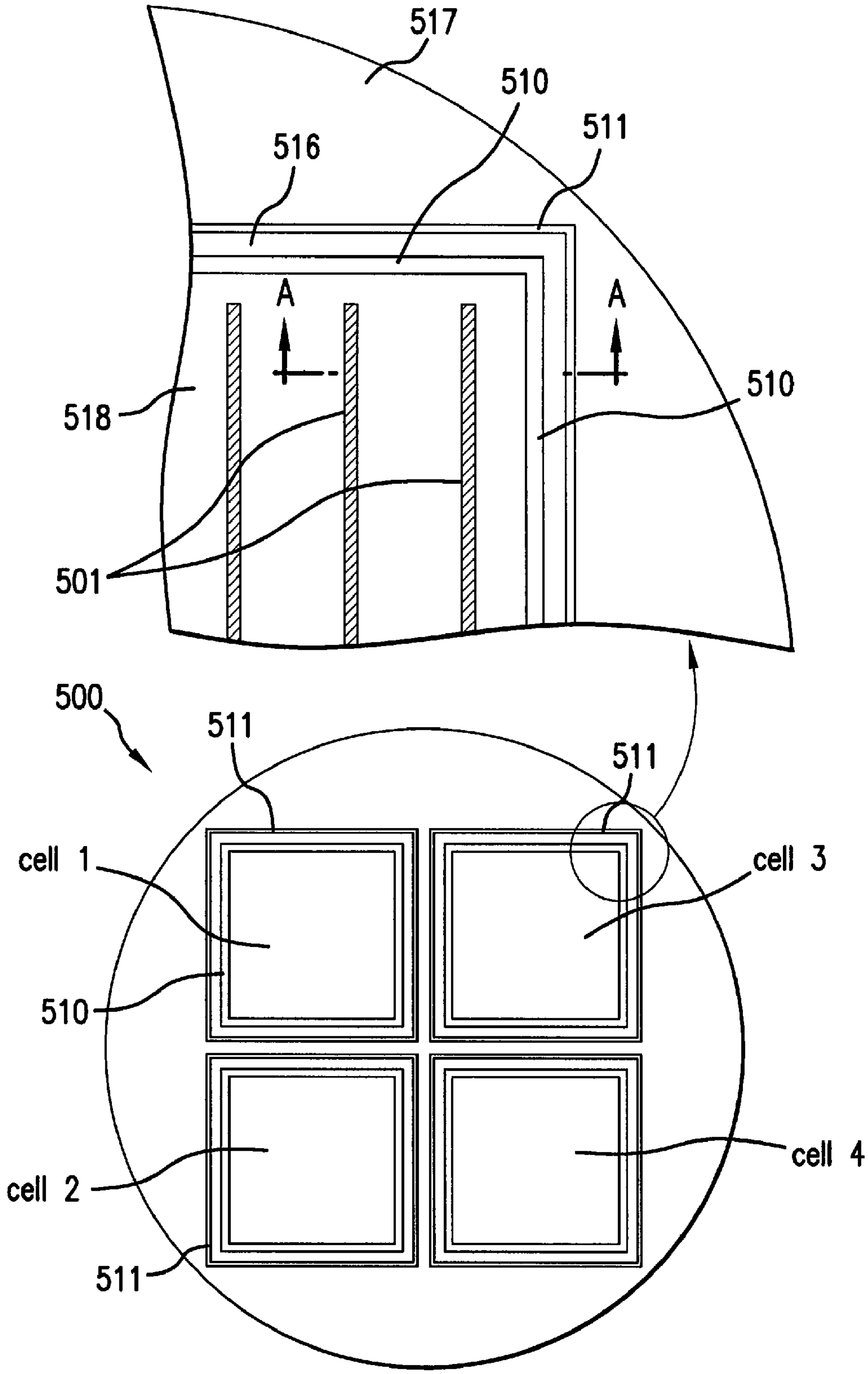

517
510
511
516
A
A
518
510
501
500
511
511
cell 1
cell 3
510
cell 2
cell 4
511

FIG.13A

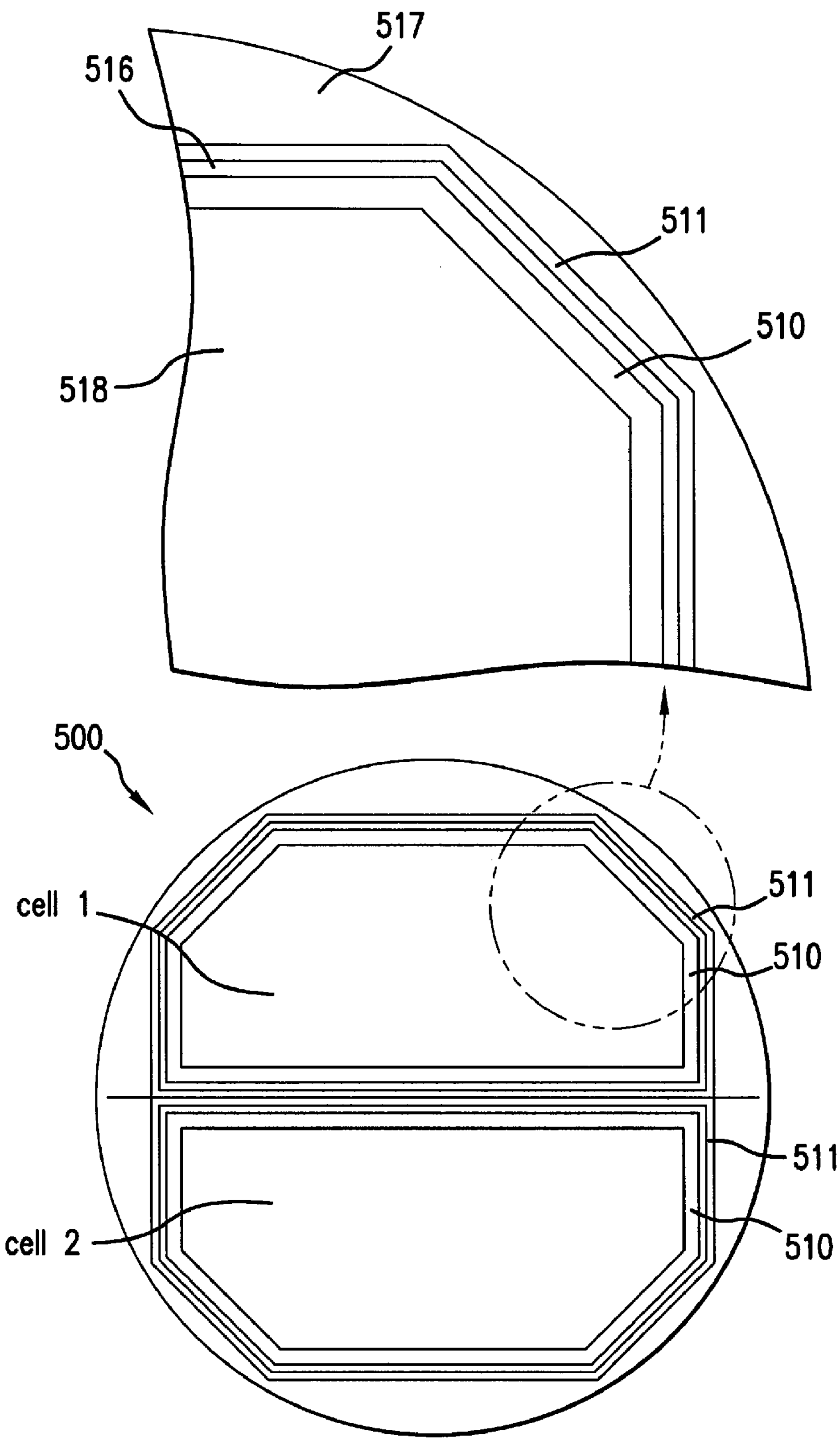


FIG. 13B

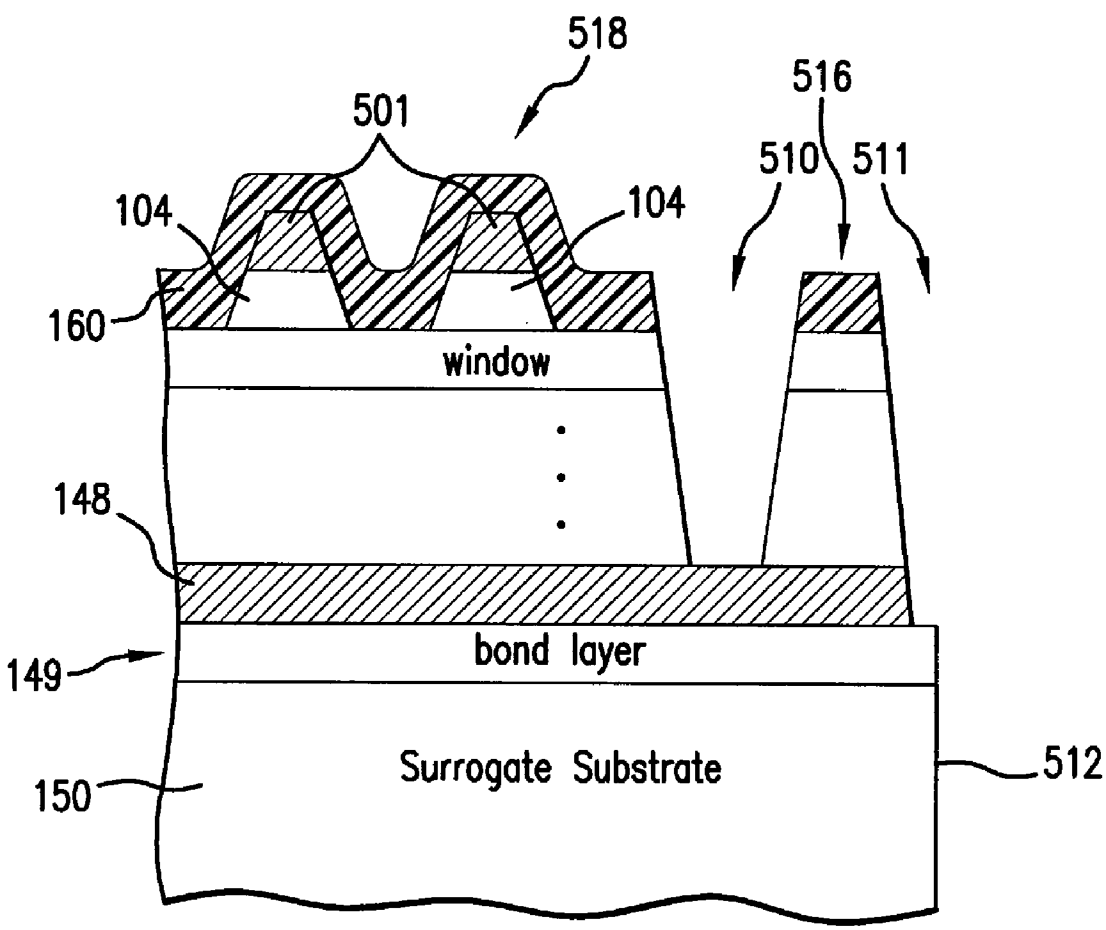

518
501
516
510
511
104
104
160
window
148
149
bond layer
Surrogate Substrate
150
512

FIG.14A

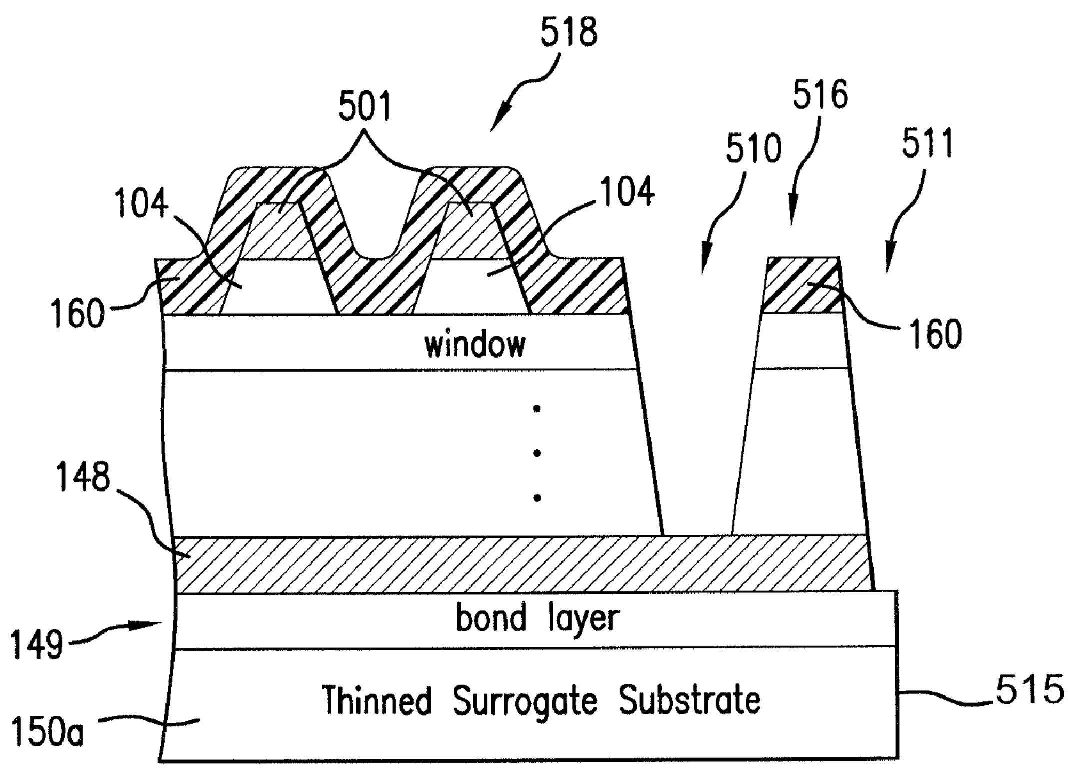

518
501
516
510
511
104
104
160
160
window
148
bond layer
149
Thinned Surrogate Substrate
515
150a

FIG.14B

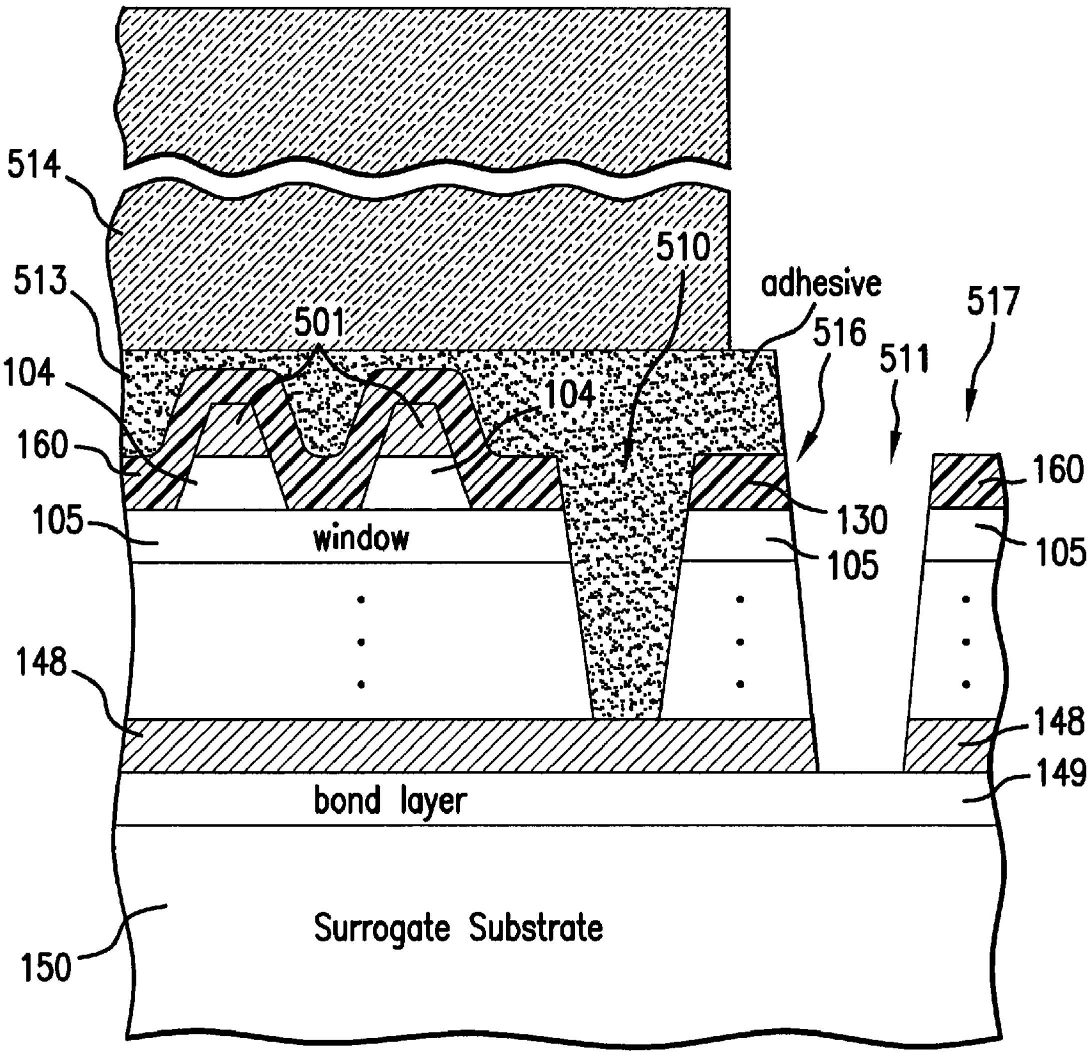

514
513
501
104
104
160
510
adhesive
516
511
517
160
130
105
window
105
105
148
148
149
bond layer
Surrogate Substrate
150

FIG.14C

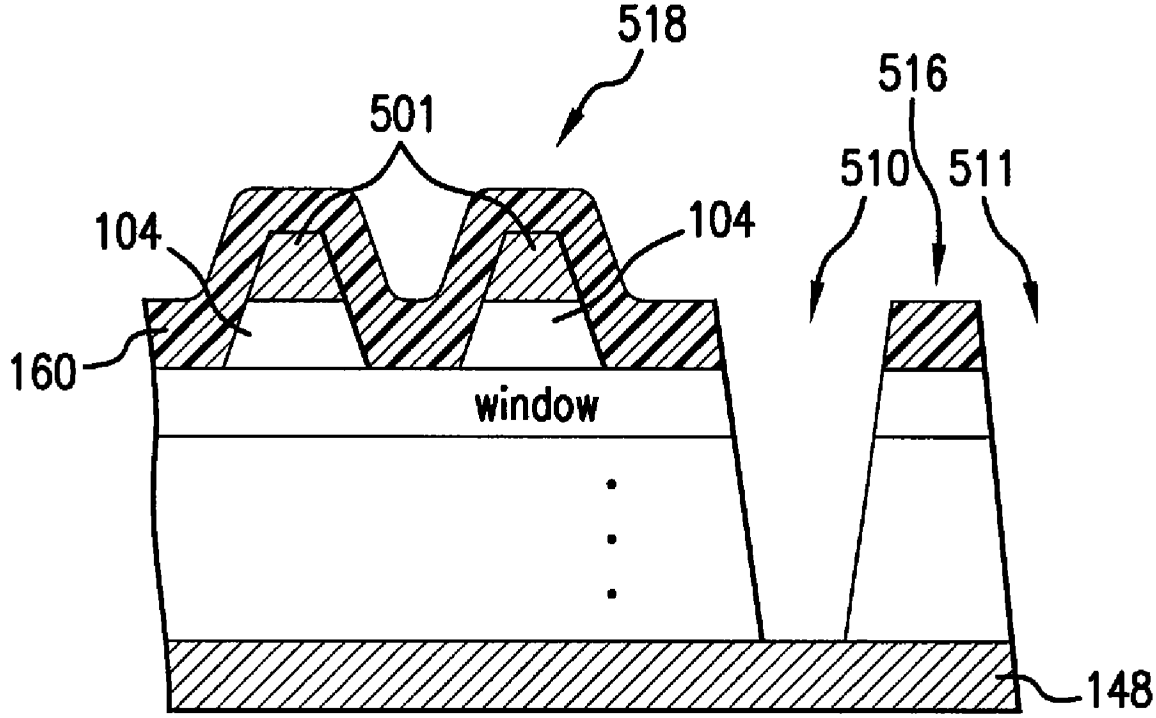


FIG.14D

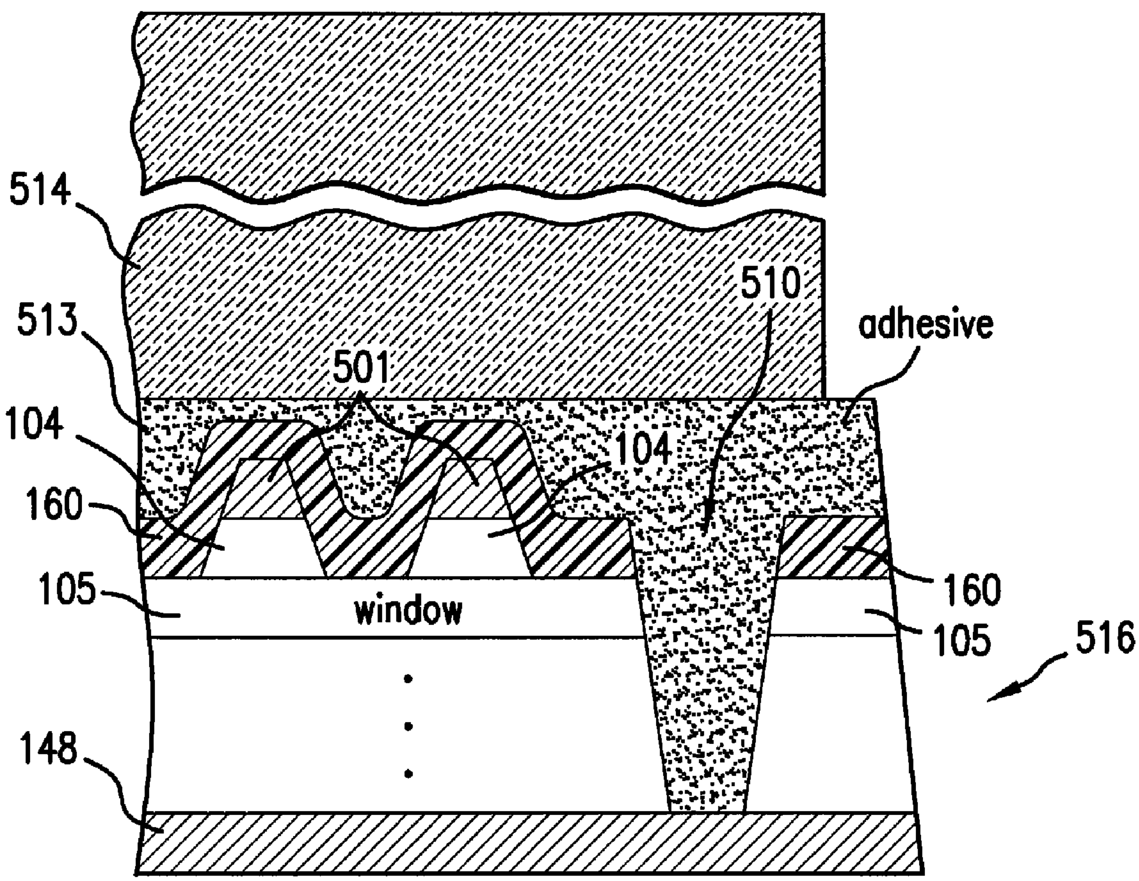

514
513
501
510
adhesive
104
104
160
160
105
window
105
516
148

FIG.15

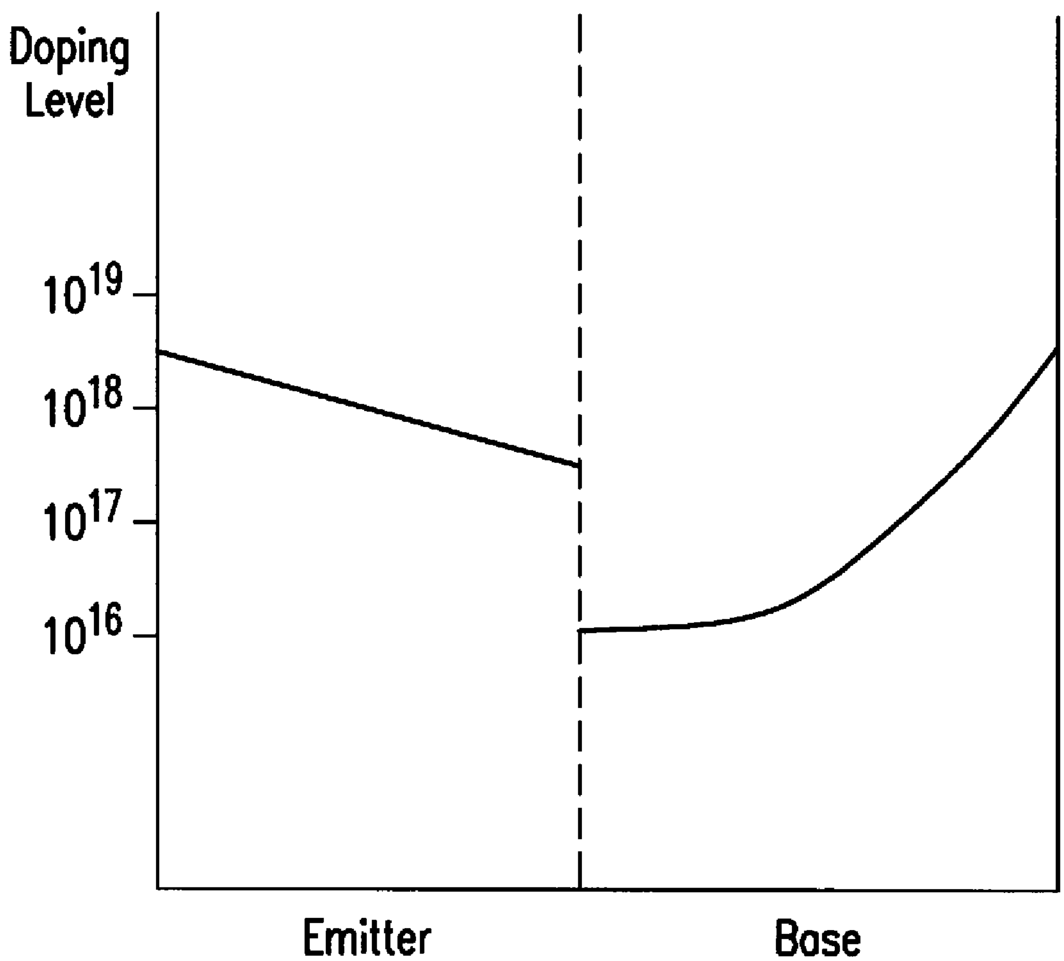


FIG.16

INVERTED MULTIJUNCTION SOLAR CELLS WITH GROUP IV/III-V HYBRID ALLOYS

REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to co-pending U.S. patent application Ser. No. 12/463,216 and Ser. No. 12/463,226, filed May 8, 2009.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to the field of semiconductor devices, and to fabrication processes and devices such as multijunction solar cells based on Group IV/III-V hybrid semiconductor compounds.

[0004] 2. Description of the Related Art

[0005] Solar power from photovoltaic cells, also called solar cells, has been predominantly provided by silicon semiconductor technology. In the past several years, however, high-volume manufacturing of III-V compound semiconductor multijunction solar cells for space applications has accelerated the development of such technology not only for use in space but also for terrestrial solar power applications. Compared to silicon, III-V compound semiconductor multijunction devices have greater energy conversion efficiencies and generally more radiation resistance, although they tend to be more complex to manufacture. Typical commercial III-V compound semiconductor multijunction solar cells have energy efficiencies that exceed 27% under one sun, air mass 0 (AM0), illumination, whereas even the most efficient silicon technologies generally reach only about 18% efficiency under comparable conditions. Under high solar concentration (e.g., 500×), commercially available III-V compound semiconductor multijunction solar cells in terrestrial applications (at AM1.5D) have energy efficiencies that exceed 37%. The higher conversion efficiency of III-V compound semiconductor solar cells compared to silicon solar cells is in part based on the ability to achieve spectral splitting of the incident radiation through the use of a plurality of photovoltaic regions with different band gap energies, and accumulating the current from each of the regions.

[0006] In satellite and other space related applications, the size, mass and cost of a satellite power system are dependent on the power and energy conversion efficiency of the solar cells used. Putting it another way, the size of the payload and the availability of on-board services are proportional to the amount of power provided. Thus, as payloads become more sophisticated, the power-to-weight ratio of a solar cell becomes increasingly more important, and there is increasing interest in lighter weight, "thin film" type solar cells having both high efficiency and low mass.

[0007] Typical III-V compound semiconductor solar cells are fabricated on a semiconductor wafer in vertical, multijunction structures. The individual solar cells or wafers are then disposed in horizontal arrays, with the individual solar cells connected together in an electrical series circuit. The shape and structure of an array, as well as the number of cells it contains, are determined in part by the desired output voltage and current.

[0008] Inverted growth processes, such as exemplified in the fabrication of inverted metamorphic multijunction solar cell structures based on III-V compound semiconductor layers, such as described in M. W. Wanlass et al., Lattice Mismatched Approaches for High Performance, III-V Photovoltaic Energy Converters (Conference Proceedings of the 31st IEEE Photovoltaic Specialists Conference, Jan. 3-7, 2005, IEEE Press, 2005), present an important conceptual starting point for the development of future commercial high efficiency solar cells.

SUMMARY OF THE INVENTION

[0009] Briefly, and in general terms, the present invention provides a method of manufacturing a solar cell comprising providing a growth substrate; depositing on said growth substrate a sequence of layers of semiconductor material including group IV/III-V hybrid alloys forming a solar cell; and removing the semiconductor substrate.

[0010] In another aspect the present invention provides a method of manufacturing a solar cell comprising providing a semiconductor growth substrate; depositing on said semiconductor growth substrate a sequence of layers of semiconductor material forming a solar cell, including at least one layer composed of GeSiSn and one layer grown over the GeSiSn layer composed of Ge; applying a metal contact layer over said sequence of layers; and applying a supporting member directly over said metal contact layer.

[0011] In another aspect the present invention provides a multijunction solar cell including a first solar subcell composed of InGaP or InGaAlP and having a first band gap; a second solar subcell composed of GaAs, InGaAsP, or InGaP and disposed over the first solar subcell having a second band gap smaller than the first band gap and lattice matched to said first solar subcell; and a third solar subcell composed of GeSiSn and disposed over the second solar subcell and having a third band gap smaller than the second band gap and lattice matched with respect to the second subcell.

[0012] Some implementations of the present invention may incorporate or implement fewer of the aspects and features noted in the foregoing summaries.

[0013] Additional aspects, advantages, and novel features of the present invention will become apparent to those skilled in the art from this disclosure, including the following detailed description as well as by practice of the invention. While the invention is described below with reference to preferred embodiments, it should be understood that the invention is not limited thereto. Those of ordinary skill in the art having access to the teachings herein will recognize additional applications, modifications and embodiments in other fields, which are within the scope of the invention as disclosed and claimed herein and with respect to which the invention could be of utility.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The invention will be better and more fully appreciated by reference to the following detailed description when considered in conjunction with the accompanying drawings, wherein:

[0015] FIG. **1** is a graph representing the bandgap of certain binary materials and their lattice constants;

[0016] FIG. **2**A is a cross-sectional view of the solar cell of the invention after the deposition of semiconductor layers on the growth substrate; according to a first embodiment of the present invention;

[0017] FIG. **2**B is a cross-sectional view of the solar cell of the invention after the deposition of semiconductor layers on the growth substrate; according to a second embodiment of the present invention;

[0018] FIG. 2C is a cross-sectional view of the solar cell of the invention after the deposition of semiconductor layers on the growth substrate; according to a third embodiment of the present invention;

[0019] FIG. 2D is a cross-sectional view of the solar cell of the invention after the deposition of semiconductor layers on the growth substrate; according to a fourth embodiment of the present invention;

[0020] FIG. 2E is a cross-sectional view of the solar cell of the invention after the deposition of semiconductor layers on the growth substrate; according to a fifth embodiment of the present invention;

[0021] FIG. 3 is a highly simplified cross-sectional view of the solar cell of FIG. 2 after the next process step of depositing a BSF layer over the "bottom" solar subcell;

[0022] FIG. 4 is a cross-sectional view of the solar cell of FIG. 3 after the next process step;

[0023] FIG. 5 is a cross-sectional view of the solar cell of FIG. 4 after the next process step in which a surrogate substrate is attached;

[0024] FIG. 6A is a cross-sectional view of the solar cell of FIG. 5 after the next process step in which the original substrate is removed;

[0025] FIG. 6B is another cross-sectional view of the solar cell of FIG. 6A with the surrogate substrate on the bottom of the Figure;

[0026] FIG. 7 is a cross-sectional view of the solar cell of FIG. 6B after the next process step;

[0027] FIG. 8 is a cross-sectional view of the solar cell of FIG. 7 after the next process step;

[0028] FIG. 9 is a cross-sectional view of the solar cell of FIG. 8 after the next process step;

[0029] FIG. 10A is a top plan view of a wafer in which four solar cells are fabricated;

[0030] FIG. 10B is a bottom plan view of the wafer of FIG. 10A;

[0031] FIG. 10C is a top plan view of a wafer in which two solar cells are fabricated;

[0032] FIG. 11 is a cross-sectional view of the solar cell of FIG. 9 after the next process step;

[0033] FIG. 12A is a cross-sectional view of the solar cell of FIG. 11 after the next process step;

[0034] FIG. 12B is a cross-sectional view of the solar cell of FIG. 12A after the next process step;

[0035] FIG. 13A is a top plan view of the wafer of FIG. 10A depicting the surface view of the trench etched around the cell, after the process step depicted in FIG. 12B;

[0036] FIG. 13B is a top plan view of the wafer of FIG. 10C depicting the surface view of the trench etched around the cell, after the process step depicted in FIG. 12B;

[0037] FIG. 14A is a cross-sectional view of the solar cell of FIG. 12B after the next process step in a first embodiment of the present invention;

[0038] FIG. 14B is a cross-sectional view of the solar cell of FIG. 12B after the next process step in a second embodiment of the present invention;

[0039] FIG. 14C is a cross-sectional view of the solar cell of FIG. 14A after the next process step of removal of the surrogate substrate;

[0040] FIG. 14D is a cross-sectional view of the solar cell of FIG. 14A in some embodiments;

[0041] FIG. 15 is a cross-sectional view of the solar cell of FIG. 14B after the next process step in a third embodiment of the present invention; and

[0042] FIG. 16 is a graph of the doping profile in the base and emitter layers of a subcell in the solar cell according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0043] Details of the present invention will now be described including exemplary aspects and embodiments thereof. Referring to the drawings and the following description, like reference numbers are used to identify like or functionally similar elements, and are intended to illustrate major features of exemplary embodiments in a highly simplified diagrammatic manner. Moreover, the drawings are not intended to depict every feature of the actual embodiment nor the relative dimensions of the depicted elements, and are not drawn to scale.

[0044] The basic concept of fabricating an inverted multijunction solar cell is to grow the subcells of the solar cell on a substrate in a "reverse" sequence. That is, the high band gap subcells (i.e. subcells with band gaps in the range of 1.8 to 2.1 eV), which would normally be the "top" subcells facing the solar radiation, are initially grown epitaxially directly on a semiconductor growth substrate, such as for example GaAs or Ge, and such subcells are consequently lattice matched to such substrate. One or more lower band gap middle subcells (i.e. with band gaps in the range of 1.2 to 1.8 eV) can then be grown on the high band gap subcells.

[0045] At least one lower subcell is formed over the middle subcell such that the at least one lower subcell is substantially lattice matched with respect to the growth substrate and such that the at least one lower subcell has a third lower band gap (i.e., a band gap in the range of 0.7 to 1.2 eV). A surrogate substrate or support structure is then attached or provided over the "bottom" or lower subcell, and the growth semiconductor substrate is subsequently removed. (The growth substrate may then subsequently be re-used for the growth of a second and subsequent solar cells).

[0046] A variety of different features and aspects of a type of inverted multijunction solar cell known as inverted metamorphic multijunction solar cells are disclosed in U.S. patent application Ser. No. 12/401,189 and the related applications noted in that application. Some or all of such features may be included in the structures and processes associated with the solar cells of the present invention.

[0047] The lattice constants and electrical properties of the layers in the semiconductor structure are preferably controlled by specification of appropriate reactor growth temperatures and times, and by use of appropriate chemical composition and dopants. The use of a vapor deposition method, such as Organo Metallic Vapor Phase Epitaxy (OMVPE), Metal Organic Chemical Vapor Deposition (MOCVD), Molecular Beam Epitaxy (MBE), or other vapor deposition methods for the reverse growth may enable the layers in the monolithic semiconductor structure forming the cell to be grown with the required thickness, elemental composition, dopant concentration and grading and conductivity type.

[0048] FIG. 2A depicts the multijunction solar cell according to a first embodiment of the present invention after the sequential formation of the three subcells A, B, and C on a GaAs growth substrate. More particularly, there is shown a substrate 101, which is preferably gallium arsenide (GaAs), but may also be germanium (Ge) or other suitable material. For GaAs, the substrate is preferably a 15° off-cut substrate, that is to say, its surface is orientated 15° off the (100) plane towards the (111)A plane, as more fully described in U.S. patent application Ser. No. 12/047,944, filed Mar. 13, 2008. Other alternative growth substrates, such as described in U.S. patent application Ser. No. 12/337,014 filed Dec. 17, 2008, may be used as well

[0049] In the case of a Ge substrate, a nucleation layer (not shown) is deposited directly on the substrate **101**. On the substrate, or over the nucleation layer (in the case of a Ge substrate), a buffer layer **102** and an etch stop layer **103** are further deposited. In the case of GaAs substrate, the buffer layer **102** is preferably GaAs. In the case of Ge substrate, the buffer layer **102** is preferably InGaAs. A contact layer **104** of GaAs is then deposited on layer **103**, and a window layer **105** of n+ type AlInP is deposited on the contact layer. The subcell A, consisting of an n+ emitter layer **106** and a p-type base layer **107**, is then epitaxially deposited on the window layer **105**. The subcell A is generally latticed matched to the growth substrate **101**.

[0050] It should be noted that the multijunction solar cell structure could be formed by any suitable combination of group III to V elements listed in the periodic table subject to lattice constant and bandgap requirements, wherein the group III includes boron (B), aluminum (Al), gallium (Ga), indium (In), and thallium (T). The group IV includes carbon (C), silicon (Si), germanium (Ge), and tin (Sn). The group V includes nitrogen (N), phosphorus (P), arsenic (As), antimony (Sb), and bismuth (Bi).

[0051] In one preferred embodiment, the emitter layer **106** is composed of InGa(Al)P and the base layer **107** is composed of InGa(Al)P. The aluminum or Al term in parenthesis in the preceding formula means that Al is an optional constituent, and in this instance in various embodiments of the invention may be used in an amount ranging from 0% to 30%. The doping profile of the emitter and base layers **106** and **107** according to one embodiment of the present invention will be discussed in conjunction with FIG. **16**.

[0052] Subcell A will ultimately become the "top" subcell of the inverted multijunction structure after completion of the process steps according to the present invention to be described hereinafter.

[0053] On top of the base layer **107** a back surface field ("BSF") layer **108** preferably p+ AlGaInP is deposited and used to reduce recombination loss.

[0054] The BSF layer **108** drives minority carriers from the region near the base/BSF interface surface to minimize the effect of recombination loss. In other words, a BSF layer **108** reduces recombination loss at the backside of the solar subcell A and thereby reduces the recombination in the base.

[0055] On top of the BSF layer **108** is deposited a sequence of heavily doped p-type and n-type layers **109***a* and **109***b* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell A to subcell B. Layer **109***a* is preferably composed of p++ AlGaAs, and layer **109***b* is preferably composed of n++ InGaP.

[0056] On top of the tunnel diode layers **109** a window layer **110** is deposited, preferably n+ InGaP, although other materials may be used as well. More generally, the window layer **110** used in the subcell B operates to reduce the interface recombination loss. It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention.

[0057] On top of the window layer **110** the layers of subcell B are deposited: the n+ type emitter layer **111** and the p type base layer **112**. These layers are preferably composed of InGaP and GaAs respectively (for a GaAs substrate), although any other suitable materials consistent with lattice constant and bandgap requirements may be used as well. Thus, in other embodiments subcell B may be composed of a GaAs, GaInP, GaInAs, GaAsSb, or GaInAsN emitter region and a GaAs, GaInAs, GaAsSb, or GaInAsN base region, respectively. The doping profile of layers **111** and **112** in various embodiments according to the present invention will be discussed in conjunction with FIG. **16**.

[0058] In some embodiments of the present invention, similar to the structure disclosed in U.S. patent application Ser. No. 12/023,772, the middle subcell may be a heterostructure with an InGaP emitter and its window is converted from InAlP to InGaP. This modification may eliminate the refractive index discontinuity at the window/emitter interface of the middle subcell. Moreover, in some embodiments the window layer **110** may be preferably doped more than that of the emitter **111** to move the Fermi level up closer to the conduction band and therefore create band bending at the window/emitter interface which results in constraining the minority carriers to the emitter layer.

[0059] In one of the preferred embodiments of the present invention, the middle subcell emitter has a band gap equal to the top subcell emitter, and the bottom subcell emitter has a band gap greater than the band gap of the base of the middle subcell. Therefore, after fabrication of the solar cell, and implementation and operation, neither the emitters of middle subcell B nor the bottom subcell C will be exposed to absorbable radiation.

[0060] Substantially all of the photons representing absorbable radiation will be absorbed in the bases of cells B and C, which have narrower band gaps than the emitters. Therefore, the advantages of using heterojunction subcells are: (i) the short wavelength response for both subcells will improve, and (ii) the bulk of the radiation is more effectively absorbed and collected in the narrower band gap base. The effect will be to increase the short circuit current J_{sc}.

[0061] Over the base layer **112** a BSF layer **113**, preferably p+ type AlGaAs, is deposited. The BSF layer **113** performs the same function as the BSF layer **108**.

[0062] The p++/n++ tunnel diode layers **114***a* and **114***b* respectively are deposited over the BSF layer **113**, similar to the layers **109***a*/**109***b*, forming an ohmic circuit element to connect subcell B to subcell C. The layer **114***a* is preferably composed of p++ GeSiSn, and layer **114***b* is preferably composed of n++ GeSiSn.

[0063] A window layer **115** preferably composed of n+ type GeSiSn is then deposited over the tunnel diode layer **114***b*. This window layer operates to reduce the recombination loss in subcell C. It should be apparent to one skilled in the art that additional layers may be added or deleted in the cell structure without departing from the scope of the present invention.

[0064] On top of the window layer **115**, the layers of subcell C are deposited: the n+ emitter layer **116**, and the p type base layer **117**. These layers are preferably composed of n+ type GeSiSn and p type GeSiSn, respectively, or n+ type and p type for a heterojunction subcell, although other suitable materials consistent with lattice constant and bandgap requirements may be used as well. The formation of the junction in subcell C may be implemented by the diffusion of As and P into the GeSiSn layers. The doping profile of layers **116** and **117** will be discussed in connection with FIG. **16**.

[0065] The band gaps of the sequence of solar subcells in the first embodiment are preferably approximately 1.85 eV for the top subcell A, 1.42 eV for subcell B, and 1.03 eV for subcell C.

[0066] As will be discussed in connection with FIG. **3**, a BSF layer, preferably composed of p+ type GeSiSn, may be deposited on top of the base layer **117** of subcell C, the BSF layer performing the same function as the BSF layers **108** and **113**.

[0067] The description of subsequent processing steps in the fabrication of the solar cell in the embodiment of FIG. **2**A will be described beginning with the description of FIG. **3** and subsequent Figures. Meanwhile, we will describe other embodiments of the multijunction solar cell semiconductor structure.

[0068] FIG. **2**B depicts the multijunction solar cell according to a second embodiment of the present invention after the sequential formation of the four subcells A, B, C, and D on a GaAs growth substrate. More particularly, there is shown a substrate **101**, which is preferably gallium arsenide (GaAs), but may also be germanium (Ge) or other suitable material. For GaAs, the substrate is preferably a 15° off-cut substrate, that is to say, its surface is orientated 15° off the (100) plane towards the (111)A plane, as more fully described in U.S. patent application Ser. No. 12/047,944, filed Mar. 13, 2008. Other alternative growth substrates, such as described in U.S. patent application Ser. No. 12/337,014 filed Dec. 17, 2008, may be used as well.

[0069] The composition of layers **101** through **117** in the embodiment of FIG. **2**B are similar to those described in the embodiment of FIG. **2**A, but may have different elemental compositions or dopant concentrations, and will not be repeated here.

[0070] In the embodiment of FIG. **2**B, a BSF layer **118**, preferably composed of p+ type GeSiSn, is deposited on top of the base layer **117** of subcell C, the BSF layer performing the same function as the BSF layers **108** and **113**.

[0071] The p++/n++ tunnel diode layers **119***a* and **119***b* respectively are deposited over the BSF layer **118**, similar to the layers **109***a*/**109***b* and **114***a*/**114***b*, forming an ohmic circuit element to connect subcell C to subcell D. The layer **119***a* is preferably composed of p++ GeSiSn, and layer **119***b* is preferably composed of n++ GeSiSn.

[0072] A window layer **120** preferably composed of n+ type GeSiSn is then deposited over the tunnel diode layer **119***b*. This window layer operates to reduce the recombination loss in subcell D. It should be apparent to one skilled in the art that additional layers may be added or deleted in the cell structure without departing from the scope of the present invention.

[0073] On top of the window layer **120**, the layers of subcell D are deposited: the n+ emitter layer **121**, and the p type base layer **122**. These layers are preferably composed of n+ type Ge and p type Ge, respectively, although other suitable materials consistent with lattice constant and bandgap requirements may be used as well. The formation of the junction in subcell C may be implemented by the diffusion of As and P into the GeSiSn layers. The doping profile of layers **121** and **122** in one embodiment will be discussed in connection with FIG. **16**.

[0074] As will be discussed in connection with FIG. **3**, a BSF layer **123**, preferably composed of p+ type GeSiSn, is then deposited on top of the subcell D, the BSF layer performing the same function as the BSF layers **108**, **113**, and **118**.

[0075] The band gaps of the sequence of solar subcells in the second embodiment are preferably approximately 1.85 eV for the top subcell A, 1.42 eV for subcell B, 1.03 eV for subcell C, and 0.73 eV for the top subcell D.

[0076] The description of subsequent processing steps in the fabrication of the solar cell in the embodiment of FIG. **2**B will be described beginning with the description of FIG. **3** and subsequent Figures. Meanwhile, we will describe other embodiments of the multijunction solar cell semiconductor structure.

[0077] FIG. **2**C depicts the multijunction solar cell according to another embodiment of the present invention after the sequential formation of the five subcells A, B C, D, and E on a GaAs growth substrate. More particularly, there is shown a substrate **101**, which is preferably gallium arsenide (GaAs), but may also be germanium (Ge) or other suitable material.

[0078] The composition and description of the substrate **101** through layer **105**, and the layers **114***a* through **123** are substantially similar to that described in connection with the embodiment of FIG. **2**B, but with different elemental compositions or dopant concentrations to result in different band gaps, and need not be repeated here. In particular, in the embodiment of FIG. **2**C, the band gap of subcell A may be approximately 2.05 eV, and the band gap of subcell B may be approximately 1.6 eV.

[0079] Turning to the embodiment depicted in FIG. **2**C, on top of the window layer **105**, the layers of subcell A are deposited: the n+ emitter layer **106***a*, and the p type base layer **107***a*. These layers are preferably composed of n+ type InGaAlP and p type InGaAlP, respectively, although other suitable materials consistent with lattice constant and bandgap requirements may be used as well. Subcell A preferably has a band gap of approximately 2.05 eV.

[0080] On top of the base layer **107***a* a back surface field ("BSF") layer **108** preferably p+ AlGaInP is deposited and used to reduce recombination loss.

[0081] The BSF layer **108** drives minority carriers from the region near the base/BSF interface surface to minimize the effect of recombination loss. In other words, a BSF layer **108** reduces recombination loss at the backside of the solar subcell A and thereby reduces the recombination in the base.

[0082] On top of the BSF layer **108** is deposited a sequence of heavily doped p-type and n-type layers **109***c* and **109***d* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell A to subcell B. Layer **109***c* is preferably composed of p++ AlGaAs, and layer **109***d* is preferably composed of n++ (Al)InGaP.

[0083] On top of the tunnel diode layers **109***c*/**109***d* a window layer **110** is deposited, preferably n+ InGaP, although other materials may be used as well. More generally, the window layer **110** used in the subcell B operates to reduce the interface recombination loss. It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention.

[0084] On top of the window layer **110** the layers of subcell B are deposited: the n+ type emitter layer **111***a* and the p type base layer **112***a*. These layers are preferably composed of InGaAsP and InGaAsP respectively, although any other suitable materials consistent with lattice constant and bandgap requirements may be used as well. Subcell B preferably has a band gap of approximately 1.6 eV. The doping profile of the emitter and base layers in one embodiment will be discussed in connection with FIG. **16**.

[0085] On top of the base layer **112***a* a back surface field ("BSF") layer **113***a* preferably p+ InGaAs is deposited and used to reduce recombination loss.

[0086] On top of the BSF layer **113***a* is deposited a sequence of heavily doped p-type and n-type layers **114***a* and **114***b* that form a tunnel diode The layers **114***a* through **123** are substantially similar to that described in connection with the embodiment of FIG. **2**B, but with different elemental compositions or dopant concentrations to result in different band gaps. The band gaps of the sequence of solar subcells C and D in this embodiment are preferably approximately 1.24 eV for the subcell C, and 0.95 eV for subcell D.

[0087] On top of the base layer **122** of subcell D a back surface field ("BSF") layer **123** preferably p+ GeSiSn is deposited and used to reduce recombination loss.

[0088] On top of the BSF layer **123** is deposited a sequence of heavily doped p-type and n-type layers **124***a* and **124***b* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell D to subcell E. Layer **124***a* is preferably composed of p++ GeSiSn, and layer **124***b* is preferably composed of n++ GeSiSn.

[0089] On top of the tunnel diode layers **124***a*/**124***b* a window layer **125** is deposited, preferably n+ GeSiSn, although other materials may be used as well. More generally, the window layer **125** used in the subcell E operates to reduce the interface recombination loss. It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention.

[0090] On top of the window layer **125** the layers of subcell E are deposited: the n+ type emitter layer **126** and the p type base layer **127**. These layers are preferably composed of Ge, although any other suitable materials consistent with lattice constant and bandgap requirements may be used as well. The formation of the junction in subcell E may be implemented by the diffusion of As and P into the Ge layer. The doping profile of layers **126** and **127** in one embodiment will be discussed in connection with FIG. **16**. Subcell E preferably has a band gap of approximately 0.73 eV.

[0091] As will be discussed in connection with FIG. **3**, a BSF layer **128**, preferably composed of p+ type GeSiSn, is then deposited on top of the subcell E, the BSF layer performing the same function as the BSF layers **108**, **113***a*, **118**, and **123**.

[0092] The band gaps of the sequence of solar subcells in this embodiment are preferably approximately 2.05 eV for the top subcell A, 1.6 eV for subcell B, and 1.24 eV for subcell C, 0.95 eV for subcell D, and 0.73 eV for subcell E.

[0093] The description of subsequent processing steps in the fabrication of the solar cell in the embodiment of FIG. **2**C will be described beginning with the description of FIG. **3** and subsequent Figures. Meanwhile, we will describe other embodiments of the multijunction solar cell semiconductor structure.

[0094] FIG. **2**D depicts the multijunction solar cell according to another embodiment of the present invention after the sequential formation of the six subcells A, B, C, D, E and F on a GaAs growth substrate. More particularly, there is shown a substrate **101**, which is preferably gallium arsenide (GaAs), but may also be germanium (Ge) or other suitable material.

[0095] The composition and description of the substrate **101** and the layers **102** through **110**, and layers **120** through **128** are substantially similar to that described in connection with the embodiment of FIG. **2**C, but with different elemental compositions or dopant concentrations to result in different band gaps, and need not be repeated here.

[0096] Turning to the embodiment depicted in FIG. **2**D, on top of the window layer **110** the layers of subcell B are deposited: the n+ type emitter layer **111***b* and the p type base layer **112***b*. These layers are preferably composed of n+ type InGaP and p type InGaP respectively, although any other suitable materials consistent with lattice constant and bandgap requirements may be used as well. Subcell B preferably has a band gap of approximately 1.74 eV.

[0097] On top of the base layer **112***b* a back surface field ("BSF") layer **113***b* preferably p+ AlGaAs is deposited and used to reduce recombination loss.

[0098] On top of the BSF layer **113***b* is deposited a sequence of heavily doped p-type and n-type layers **114***c* and **114***d* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell B to subcell C. Layer **114***c* is preferably composed of p++ AlGaAs and layer **114***d* is preferably composed of n++ AlGaInP.

[0099] On top of the tunnel diode layers **114***c*/**114***d* a window layer **115***a* is deposited, preferably n+ InAlP, although other materials may be used as well. More generally, the window layer **115***a* used in the subcell C operates to reduce the interface recombination loss. It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention.

[0100] On top of the window layer **115***a* the layers of subcell C are deposited: the n+ type emitter layer **116***a* and the p type base layer **117***a*. These layers are preferably composed of n+ type InGaAsP and p type InGaAsP respectively, although any other suitable materials consistent with lattice constant and bandgap requirements may be used as well. Subcell C preferably has a band gap of approximately 1.42 eV.

[0101] On top of the base layer **117***a* a back surface field ("BSF") layer **118***a* preferably p+ AlGaAs is deposited and used to reduce recombination loss.

[0102] On top of the BSF layer **118***a* is deposited a sequence of heavily doped p-type and n-type layers **119***c* and **119***d* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell C to subcell D. Layer **119***c* is preferably composed of p++ AlGaAs or GeSiSn and layer **119***d* is preferably composed of n++ GaAs or GeSiSn.

[0103] On top of the tunnel diode layers **119***c*/**119***d* a window layer **120** is deposited, preferably n+ GeSiSn, although other materials may be used as well. More generally, the window layer **120** used in the subcell D operates to reduce the interface recombination loss. It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention. As noted above, layers **120** through **128** are substantially similar to that described in connection with the embodiment of FIG. **2**C, but with different elemental compositions or dopant concentrations to result in different band gaps, and need not be repeated here. Thus, in this embodiment, subcell D preferably has a band gap of approximately 1.13 eV, and subcell E preferably has a band gap of approximately 0.91 eV.

[0104] On top of the BSF layer **128** composed of p type GeSiSn is deposited a sequence of heavily doped p-type and n-type layers **129***a* and **129***b* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell E to subcell F. Layer **129***a* is preferably composed of p++ GeSiSn and layer **129***b* is preferably composed of n++ GeSiSn.

[0105] On top of the tunnel diode layers **129***a*/**129***b* a window layer **130** is deposited, preferably n+ GeSiSn, although other materials may be used as well. More generally, the window layer **130** used in the subcell F operates to reduce the interface recombination loss. It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention.

[0106] On top of the window layer **130** the layers of subcell F are deposited: the n+ type emitter layer **131** and the p type base layer **132**. These layers are preferably composed of n+ type Ge and p type Ge respectively, although any other suitable materials consistent with lattice constant and bandgap requirements may be used as well. Subcell F preferably has a band gap of approximately 0.7 eV. The doping profile of the emitter and base layers in one embodiment will be discussed in connection with FIG. **16**.

[0107] As will be discussed in connection with FIG. **3**, a BSF layer **133**, preferably composed of p+ type GeSiSn, is then deposited on top of the subcell F, the BSF layer performing the same function as the BSF layers **108**, **113***a*, **118**, **123**, and **128**.

[0108] The band gaps of the sequence of solar subcells in this embodiment are preferably approximately 2.15 eV for the top subcell A, 1.74 eV for subcell B, and 1.42 eV for subcell C, 1.13 eV for subcell D, 0.91 eV for subcell E, and 0.7 for subcell F.

[0109] The description of subsequent processing steps in the fabrication of the solar cell in the embodiment of FIG. **2**D will be described beginning with the description of FIG. **3** and subsequent Figures. Meanwhile, we will describe one more embodiment of the multijunction solar cell semiconductor structure.

[0110] FIG. **2**E depicts the multijunction solar cell according to another embodiment of the present invention after the sequential formation of the seven subcells A, B, C, D, E, F and G on a GaAs growth substrate. More particularly, there is shown a substrate **101**, which is preferably gallium arsenide (GaAs), but may also be germanium (Ge) or other suitable material.

[0111] The composition and description of the substrate **101** and the layers **102** through **118***a*, and layers **125** through **133** are substantially similar to that described in connection with the embodiment of FIG. **2**D, but with different elemental compositions or dopant concentrations to result in different band gaps, and need not be repeated here. In particular, in the embodiment of FIG. **2**E, the band gap of subcell C may be approximately 1.6 eV, and in the sequence of layers **125** through **133**, the band gap of subcell E may be approximately 1.13 eV, and the band gap of subcell F may be approximately 0.91 eV.

[0112] Turning to the embodiment depicted in FIG. **2**E, on top of the BSF layer **118***a* composed of AlGaAs is deposited a sequence of heavily doped p-type and n-type layers **119***e* and **119***f* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell C to subcell D. Layer **119***e* is preferably composed of p++ AlGaAs and layer **119***f* is preferably composed of n++ InGaP.

[0113] On top of the tunnel diode layers **119***e*/**119***f* a window layer **120***a* is deposited, preferably n+ InAlP, although other materials may be used as well. More generally, the window layer **120***a* used in the subcell D operates to reduce the interface recombination loss. It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention.

[0114] On top of the window layer **120***a* the layers of subcell D are deposited: the n+ type emitter layer **121***a* and the p type base layer **122***a*. These layers are preferably composed of n+ type GaAs and p type GaAs respectively, although any other suitable materials consistent with lattice constant and bandgap requirements may be used as well. Subcell D preferably has a band gap of approximately 1.42 eV.

[0115] On top of the base layer **122***a* a back surface field ("BSF") layer **123***a* preferably p+ AlGaAs is deposited and used to reduce recombination loss.

[0116] On top of the BSF layer **123***a* is deposited a sequence of heavily doped p-type and n-type layers **124***c* and **124***d* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell D to subcell E. Layer **124***c* is preferably composed of p++ GeSiSn or AlGaAs, and layer **124***d* is preferably composed of n++ GeSiSn or GaAs.

[0117] On top of the tunnel diode layers **129***d*/**129***e* a window layer **130** is deposited, composed of n+ type GeSiSn. As noted above, layers **125** through **133** are substantially similar to that described in connection with the embodiment of FIG. **2**D, but with different elemental compositions or dopant concentrations to result in different band gaps, and need not be repeated here. Thus, in this embodiment, subcell E preferably has a band gap of approximately 1.13 eV, and subcell F preferably has a band gap of approximately 0.91 eV.

[0118] Turning again to the embodiment depicted in FIG. **2**E, on top of the BSF layer **133** composed of GeSiSn is deposited a sequence of heavily doped p-type and n-type layers **134***a* and **134***b* that form a tunnel diode, i.e. an ohmic circuit element that connects subcell F to subcell G. Layer **134***a* is preferably composed of p++ GeSiSn and layer **134***b* is preferably composed of n++ GeSiSn.

[0119] On top of the tunnel diode layers **134***a*/**134***b* a window layer **135** is deposited, preferably n+ GeSiSn, although other materials may be used as well. More generally, the window layer **135** used in the subcell G operates to reduce the interface recombination loss. It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention.

[0120] On top of the window layer **135** the layers of subcell G are deposited: the n+ type emitter layer **136** and the p type base layer **137**. These layers are preferably composed of n+ type GeSiSn and p type GeSiSn respectively, although any other suitable materials consistent with lattice constant and bandgap requirements may be used as well. Subcell G preferably has a band gap of approximately 0.73 eV. The doping profile of the emitter and base layers in one embodiment will be discussed in connection with FIG. **16**.

[0121] FIG. **3** is a highly simplified cross-sectional view of the solar cell structure of any of the embodiments of FIG. **2**A, **2**B, **2**C, **2**D or **2**E, depicting the top BSF layer of the solar cell structure, relabeled in this FIG. **3** and subsequent Figures, as BSF layer **146** deposited over the base layer of the last deposited subcell. The BSF layer **146** therefore represents the BSF layer **118**, **123**, **128**, **133**, or **138** depicted and described in connection with FIG. **2**A, **2**B, **2**C, **2**D, or **2**E respectively.

[0122] FIG. **4** is a cross-sectional view of the solar cell of FIG. **3** after the next process step in which a high band gap contact layer **147**, preferably composed of a suitable p++ type material, is deposited on the BSF layer **146**. This contact layer **147** deposited on the bottom (non-illuminated) side of the lowest band gap photovoltaic subcell, in a multijunction photovoltaic cell, can be suitably formulated to reduce absorption of the light that passes through the cell, so that (i) a subsequently deposited ohmic metal contact layer below (i.e. towards the non-illuminated side) the contact layer will also act as a mirror layer, and (ii) the contact layer doesn't have to be selectively etched off, to prevent absorption in the layer.

[0123] It should be apparent to one skilled in the art, that additional layer(s) may be added or deleted in the cell structure without departing from the scope of the present invention.

[0124] FIG. **4** further depicts the next process step in which a metal contact layer **148** is deposited over the p++ semiconductor contact layer **147**. The metal is preferably the sequence of metal layers Ti/Au/Ag/Au or Ti/Pd/Ag, although other suitable sequences and materials may be used as well.

[0125] The metal contact scheme chosen is one that has a planar interface with the semiconductor, after heat treatment to activate the ohmic contact. This is done so that (i) a dielectric layer separating the metal from the semiconductor doesn't have to be deposited and selectively etched in the metal contact areas; and (ii) the contact layer is specularly reflective over the wavelength range of interest.

[0126] FIG. **5** is a cross-sectional view of the solar cell of FIG. **4** after the next process step in which a bonding layer **149** is deposited over the metal contact layer **148**. In one embodiment of the present invention, the bonding layer **149** is an adhesive, preferably Wafer Bond (manufactured by Brewer Science, Inc. of Rolla, Mo.), although other suitable bonding materials may be used.

[0127] In the next process step, a surrogate substrate **150**, preferably sapphire, is attached over the bonding layer. Alternatively, the surrogate substrate may be GaAs, Ge or Si, or other suitable material. The surrogate substrate **150** is preferably about 40 mils in thickness, and in the case of embodiments in which the surrogate substrate is to be removed, it is perforated with holes about 1 mm in diameter, spaced 4 mm apart, to aid in subsequent removal of the adhesive and the substrate.

[0128] FIG. **6**A is a cross-sectional view of the solar cell of FIG. **5** after the next process step in which the original substrate **101** is removed by a sequence of lapping, grinding and/or etching steps. The choice of a particular etchant is growth substrate dependent. In some embodiments, the substrate **101** may be removed by an epitaxial lift-off process, such as described in U.S. patent application Ser. No. 12/367,991, filed Feb. 9, 2009, and hereby incorporated by reference.

[0129] FIG. **6**B is a cross-sectional view of the solar cell of FIG. **6**A after the buffer layer **102** is removed with the orientation with the surrogate substrate **150** being at the bottom of the Figure. Subsequent Figures in this application will assume such orientation.

[0130] FIG. **7** is a cross-sectional view of the solar cell of FIG. **6**B after the next process step in which the etch stop layer **103** is removed by a HCl/H_2O solution.

[0131] FIG. **8** is a cross-sectional view of the solar cell of FIG. **7** after the next sequence of process steps in which a photoresist layer (not shown) is placed over the semiconductor contact layer **104**. The photoresist layer is lithographically patterned with a mask to form the locations of the grid lines **501**, portions of the photoresist layer where the grid lines are to be formed are removed, and a metal contact layer is then deposited by evaporation or similar processes over both the photoresist layer and into the openings in the photoresist layer where the grid lines are to be formed. The photoresist layer portion covering the contact layer **104** is then lifted off to leave the finished metal grid lines **501**, as depicted in the Figure. As more fully described in U.S. patent application Ser. No. 12/218,582 filed Jul. 18, 2008, hereby incorporated by reference the grid lines **501** are preferably composed of the sequence of layers Pd/Ge/Ti/Pd/Au, although other suitable sequences and materials may be used as well.

[0132] FIG. **9** is a cross-sectional view of the solar cell of FIG. **8** after the next process step in which the grid lines **501** are used as a mask to etch down the surface to the window layer **105** using a citric acid/peroxide etching mixture.

[0133] FIG. **10**A is a top plan view of a 100 mm (or 4 inch) wafer in which four solar cells are implemented. The depiction of four cells is for illustration for purposes only, and the present invention is not limited to any specific number of cells per wafer.

[0134] In each cell there are grid lines **501** (more particularly shown in cross-section in FIG. **9**), an interconnecting bus line **502**, and a contact pad **503**. The geometry and number of grid and bus lines and contact pads are illustrative, and the present invention is not limited to the illustrated embodiment.

[0135] FIG. **10**B is a bottom plan view of the wafer of FIG. **10**A.

[0136] FIG. **10**C is a top plan view of a 100 mm (or 4 inch) wafer in which two solar cells are implemented. In some embodiments, each solar cell has an area of approximately 26.3 cm^2.

[0137] FIG. **11** is a cross-sectional view of the solar cell of FIG. **9** after the next process step in which an antireflective (ARC) dielectric coating layer **160** is applied over the entire surface of the "top" side of the wafer with the grid lines **501**.

[0138] FIG. **12**A is a cross-sectional view of the solar cell of FIG. **11** after the next process step according to the present invention in which first and second annular channels **510** and **511**, or portions of the semiconductor structure, are etched down to the metal layer **148** using phosphide and arsenide etchants. These channels, as more particularly described in U.S. patent application Ser. No. 12/190,449 filed Aug. 12, 2008, define a peripheral boundary between the cell, a surrounding mesa **516**, and a periphery mesa **517** at the edge of the wafer, and leave a mesa structure **518** which constitutes the solar cell. The cross-section depicted in FIG. **12**A is that as seen from the A-A plane shown in FIG. **13**A.

[0139] FIG. **12**B is a cross-sectional view of the solar cell of FIG. **12**A after the next process step in which channel **511** is exposed to a metal etchant, layer **123** in the channel **511** is removed, and channel **511** is extended in depth approximately to the top surface of the bond layer **149**.

[0140] FIG. **13**A is a top plan view of the wafer of FIG. **10**A depicting the channels **510** and **511** etched around the periphery of each cell.

[0141] FIG. **13**B is a top plan view of the wafer of FIG. **10**C depicting the channels **510** and **511** etched around the periphery of each cell.

[0142] FIG. 14A is a cross-sectional view of the solar cell of FIG. 12B after the individual solar cells (cell 1, cell 2, etc. shown in FIG. 13) are cut or scribed from the wafer through the channel 511, leaving a vertical edge 512 extending through the surrogate substrate 150. In this first embodiment of the present invention, the surrogate substrate 150 forms the support for the solar cell in applications where a cover glass (such as provided in the third embodiment to be described below) is not required. In an embodiment, electrical contact to the metal contact layer 148 may be made through the channel 510.

[0143] FIG. 14B is a cross-sectional view of the solar cell of FIG. 12B after the next process step in a second embodiment of the present invention in which the surrogate substrate 150 is appropriately thinned to a relatively thin layer 150*a*, by grinding, lapping, or etching. The individual solar cells (cell 1, cell 2, etc. shown in FIG. 13A) are cut or scribed from the wafer through the channel 511, leaving a vertical edge 515 extending through the surrogate substrate 150*a*. In this embodiment, the thin layer 150*a* forms the support for the solar cell in applications where a cover glass, such as provided in the third embodiment to be described below, is not required. In an embodiment, electrical contact to the metal contact layer 148 may be made through the channel 510.

[0144] FIG. 14C is a cross-sectional view of the solar cell of FIG. 12B after the next process step in a third embodiment of the present invention in which a cover glass 514 is secured to the top of the cell by an adhesive 513. The cover glass 514 is typically about 4 mils thick and preferably covers the entire channel 510, extends over a portion of the mesa 516, but does not extend to channel 511. Although the use of a cover glass is desirable for many environmental conditions and applications, it is not necessary for all implementations, and additional layers or structures may also be utilized for providing additional support or environmental protection to the solar cell.

[0145] FIG. 14D is a cross-sectional view of the solar cell of FIG. 14A after the next process step in some embodiments of the present invention in which the bond layer, the surrogate substrate 150 and the peripheral portion 517 of the wafer are entirely removed, leaving only the solar cell with the ARC layer 160 (or other layers or structures) on the top, and the metal contact layer 148 on the bottom, wherein the metal contact layer 148 forms the backside contact of the solar cell. The surrogate substrate is preferably removed by the use of a 'Wafer Bond' solvent. As noted above, the surrogate substrate includes perforations over its surface that allow the flow of solvent through the perforations in the surrogate substrate 150 to permit its lift off. After lift off, the surrogate substrate may be reused in subsequent wafer processing operations.

[0146] FIG. 15 is a cross-sectional view of the solar cell of FIG. 14C after the next process step in some embodiments of the present invention in which the bond layer 124, the surrogate substrate 150 and the peripheral portion 517 of the wafer is entirely removed, leaving only the solar cell with the cover glass 514 (or other layers or structures) on the top, and the layer on the bottom. The surrogate substrate is preferably removed by the use of a 'Wafer Bond' solvent. As noted above, the surrogate substrate includes perforations over its surface that allow the flow of solvent through the surrogate substrate 150 to permit its lift off. After lift off, the surrogate substrate may be reused in subsequent wafer processing operations.

[0147] FIG. 16 is a graph of a doping profile in the emitter and base layers in one or more subcells of the inverted metamorphic multijunction solar cell of the present invention. The various doping profiles within the scope of the present invention, and the advantages of such doping profiles are more particularly described in copending U.S. patent application Ser. No. 11/956,069 filed Dec. 13, 2007, herein incorporated by reference. The doping profiles depicted herein are merely illustrative, and other more complex profiles may be utilized as would be apparent to those skilled in the art without departing from the scope of the present invention.

[0148] It will be understood that each of the elements described above, or two or more together, also may find a useful application in other types of constructions differing from the types of constructions described above.

[0149] In addition, although the present embodiment is configured with top and bottom electrical contacts, the subcells may alternatively be contacted by means of metal contacts to laterally conductive semiconductor layers between the subcells. Such arrangements may be used to form 3-terminal, 4-terminal, and in general, n-terminal devices. The subcells can be interconnected in circuits using these additional terminals such that most of the available photogenerated current density in each subcell can be used effectively, leading to high efficiency for the multijunction cell, notwithstanding that the photogenerated current densities are typically different in the various subcells.

[0150] As noted above, the present invention may utilize an arrangement of one or more, or all, homojunction cells or subcells, i.e., a cell or subcell in which the p-n junction is formed between a p-type semiconductor and an n-type semiconductor both of which have the same chemical composition and the same band gap, differing only in the dopant species and types, and one or more heterojunction cells or subcells. Subcell A, with p-type and n-type InGaP is one example of a homojunction subcell. Alternatively, as more particularly described in U.S. patent application Ser. No. 12/023,772 filed Jan. 31, 2008, the present invention may utilize one or more, or all, heterojunction cells or subcells, i.e., a cell or subcell in which the p-n junction is formed between a p-type semiconductor and an n-type semiconductor having different chemical compositions of the semiconductor material in the n-type regions, and/or different band gap energies in the p-type regions, in addition to utilizing different dopant species and type in the p-type and n-type regions that form the p-n junction.

[0151] In some cells, a thin so-called "intrinsic layer" may be placed between the emitter layer and base layer, with the same or different composition from either the emitter or the base layer. The intrinsic layer may function to suppress minority-carrier recombination in the space-charge region. Similarly, either the base layer or the emitter layer may also be intrinsic or not-intentionally-doped ("NID") over part or all of its thickness. Some such configurations are more particularly described in copending U.S. patent application Ser. No. 12/253,051, filed Oct. 16, 2008.

[0152] The composition of the window or BSF layers may utilize other semiconductor compounds, subject to lattice constant and band gap requirements, and may include AlInP, AlAs, AlP, AlGaInP, AlGaAsP, AlGaInAs, AlGaInPAs, GaInP, GaInAs, GaInPAs, AlGaAs, AlInAs, AlInPAs, GaAsSb, AlAsSb, GaAlAsSb, AlInSb, GaInSb, AlGaInSb, AlN, GaN, InN, GaInN, AlGaInN, GaInNAs, AlGaInNAs, ZnSSe, CdSSe, and similar materials, and still fall within the spirit of the present invention.

[0153] While the invention has been illustrated and described as embodied in an inverted multijunction solar cell, it is not intended to be limited to the details shown, since various modifications and structural changes may be made without departing in any way from the spirit of the present invention.

[0154] Thus, while the description of this invention has focused primarily on solar cells or photovoltaic devices, persons skilled in the art know that other optoelectronic devices, such as thermophotovoltaic (TPV) cells, photodetectors and light-emitting diodes (LEDS) are very similar in structure, physics, and materials to photovoltaic devices with some minor variations in doping and the minority carrier lifetime. For example, photodetectors can be the same materials and structures as the photovoltaic devices described above, but perhaps more lightly-doped for sensitivity rather than power production. On the other hand LEDs can also be made with similar structures and materials, but perhaps more heavily-doped to shorten recombination time, thus radiative lifetime to produce light instead of power. Therefore, this invention also applies to photodetectors and LEDs with structures, compositions of matter, articles of manufacture, and improvements as described above for photovoltaic cells.

[0155] The foregoing described embodiments depict different components contained within, or connected with, different other components. It is to be understood that such depicted arrangements or architectures are merely exemplary, and that in fact many other arrangements or architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of specific structures, architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected" or "operably coupled" to each other to achieve the desired functionality.

[0156] While particular embodiments of the present invention have been shown and described, it will be understood by those skilled in the art that, based upon the teachings herein, changes and modifications may be made without departing from this invention and its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as are within the true spirit and scope of this invention. Furthermore, it is to be understood that the invention is solely defined by the appended claims. It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (e.g., in the bodies of the appended claims) are generally intended as "open" terms (e.g., the term "including" should be interpreted as "including but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes but is not limited to," "comprise" and variations thereof, such as, "comprises" and "comprising" are to be construed in an open, inclusive sense, that is as "including, but not limited to," etc.). It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to inventions containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an" (e.g., "a" and/or "an" should typically be interpreted to mean "at least one" or "one or more"); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should typically be interpreted to mean at least the recited number (e.g., the bare recitation of "two recitations," without other modifiers, typically means at least two recitations, or two or more recitations).

[0157] Without further analysis, the foregoing will so fully reveal the gist of the present invention that others can, by applying current knowledge, readily adapt it for various applications without omitting features that, from the standpoint of prior art, fairly constitute essential characteristics of the generic or specific aspects of this invention and, therefore, such adaptations should and are intended to be comprehended within the meaning and range of equivalence of the following claims.

1. A method of manufacturing a solar cell comprising:
providing a semiconductor growth substrate;
depositing on said semiconductor growth substrate a sequence of layers of semiconductor material forming a solar cell, including a subcell composed of a group IV/III-V hybrid alloy; and
removing the semiconductor growth substrate.

2. A method as defined in claim **1**, wherein the group IV/III-V hybrid alloy is GeSiSn.

3. A method as defined in claim **2**, wherein the GeSiSn subcell has a band gap in the range of 0.73 eV to 1.2 eV.

4. A method as defined in claim **3**, further comprising a subcell composed of germanium deposited over said GeSiSn subcell.

5. A method as defined in claim **1**, wherein the sequence of layers includes a first GeSiSn subcell having a band gap in the range of 0.91 eV to 0.95 eV, and a second GeSiSn subcell having a band gap in the range of 1.13 eV to 1.24 eV.

6. A method as defined in claim **1**, wherein said step of depositing a sequence of layers of semiconductor material includes forming a first solar subcell on said substrate having a first band gap; forming a second solar subcell over said first subcell having a second band gap smaller than said first band gap; and forming a third solar subcell over said second solar subcell having a third band gap smaller than said second band gap.

7. A method as defined in claim **6**, further comprising forming a fourth solar subcell having a fourth band gap smaller than said third band gap that is lattice matched to said third solar subcell.

8. A method as defined in claim **7**, further comprising forming a fifth solar subcell over said fourth solar subcell having a fifth band gap smaller than said fourth band gap.

9. A method as defined in claim **8**, further comprising forming a sixth solar subcell over said fifth solar subcell having a sixth band gap smaller than said fifth band gap.

10. A method as defined in claim **9**, further comprising forming a seventh solar subcell over said sixth solar subcell having a seventh band gap smaller than said sixth band gap.

11. A method as defined in claim **1**, further comprising applying a bonding layer over the sequence of layers of semiconductor material and attaching a surrogate substrate to the bonding layer.

12. A method as defined in claim **11**, wherein the semiconductor substrate is removed after the surrogate substrate has been attached by grinding, etching, or epitaxial lift-off.

13. A method as defined in claim **1**, wherein said first substrate is selected from the group consisting of GaAs and Ge.

14. A method as defined in claim **6**, wherein said first solar subcell is composed of an InGa(Al)P emitter region and an InGa(Al)P base region; said second solar subcell is composed of GaAs, InGaAsP, or InGaP; and said third solar subcell is composed of GeSiSn, InGaP, or GaAs.

15. A method as defined in claim **7**, wherein said fourth solar subcell is composed of Ge, GeSiSn, or GaAs.

16. A method as defined in claim **8**, wherein said fifth solar subcell is composed of Ge or GeSiSn.

17. A method as defined in claim **1**, wherein a junction is formed in the group IV/III-V hybrid alloy to form a photovoltaic subcell by the diffusion of As and/or P into the hybrid alloy layer.

18. A method as defined in claim **1**, further comprising forming window and BSF layers composed of the group IV/III-V hybrid alloy adjacent to the subcell composed of the group IV/III-V hybrid alloy.

19. A method of manufacturing a solar cell comprising:

providing a semiconductor growth substrate;

depositing on said semiconductor growth substrate a sequence of layers of semiconductor material forming a solar cell, including at least one layer composed of GeSiSn and one layer grown over the GeSiSn layer composed of Ge;

applying a metal contact layer over said sequence of layers; and

applying a supporting member directly over said metal contact layer.

20. A multijunction solar cell comprising:

a first solar subcell composed of InGaP or InGaAlP and having a first band gap;

a second solar subcell composed of GaAs, InGaAsP, or InGaP and disposed over the first solar subcell having a second band gap smaller than the first band gap and lattice matched to said first solar subcell; and

a third solar subcell composed of GeSiSn and disposed over the second solar subcell having a third band gap smaller than the second band gap and lattice matched with respect to the second subcell.

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