(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 February 2004 (05.02.2004)

PCT

(10) International Publication Number
WO 2004/012343 A2

(51) International Patent Classification[7]: H04B

(21) International Application Number: PCT/US2003/023007

(22) International Filing Date: 22 July 2003 (22.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/206,706 26 July 2002 (26.07.2002) US

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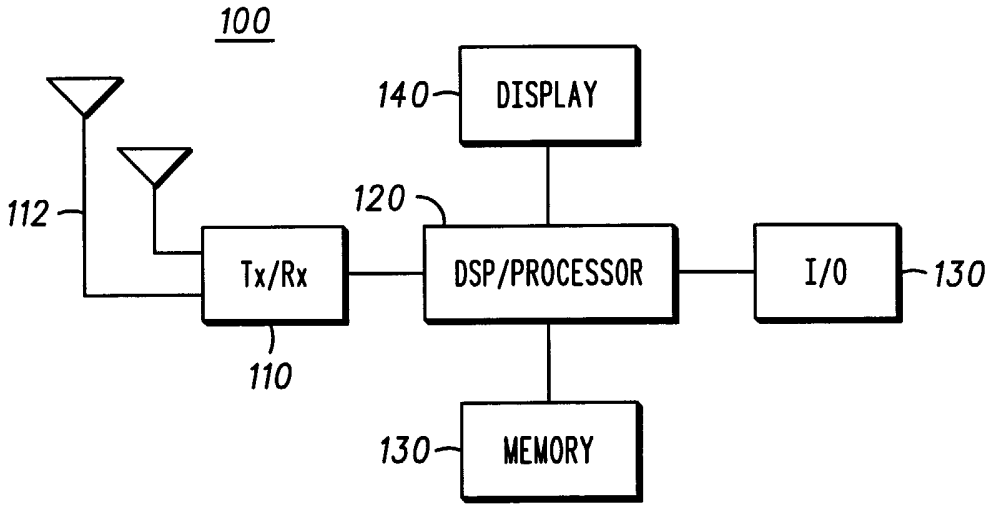
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: RADIO TRANSCEIVER ARCHITECTURES AND METHODS



(57) Abstract: A radio communications device 100 including a processor 120 having a digital signal processor (DSP) coupled to a transceiver 110. The transceiver includes a digital-to-phase synthesizer having one or more independently variable frequency or phase signal outputs coupled to a transmitter and/or to a receiver. The variable frequency and phase outputs of the digital-to phase synthesizer are mixed with corresponding received signals and are capable of frequency or phase modulating information signals for transmission. Amplitude modulated signals may be provided through polar modulation by combining synthesizer outputs at a summer.

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RADIO TRANSCEIVER ARCHITECTURES AND METHODS

FIELD OF THE INVENTIONS

The present inventions relate generally to radio communications, and more particularly to adaptive and multi-mode radio transceiver architectures, for example in wireless communications devices, and methods therefor.

BACKGROUND OF THE INVENTIONS

The various aspects, features and advantages of the present invention will become more fully apparent to those having ordinary skill in the art upon careful consideration of the following Detailed Description of the Invention with the accompanying drawings described below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is 1 is an exemplary communications device electrical schematic block diagram.

FIG. 2 is an electrical schematic block diagram of an exemplary digital-to-phase synthesizer.

FIG. 3 is an electrical schematic block diagram of an exemplary digital-to-phase synthesizer with multiple outputs.

FIG. 4 is an electrical schematic illustration of an exemplary radio receiver.

FIG. 5 is an exemplary receiver process flow diagram.

FIG. 6 is an exemplary frequency/phase modulation transmitter.

FIG. 7 is an exemplary amplitude modulation transmitter.

DETAILED DESCRIPTION OF THE INVENTIONS

FIG. 1 is an exemplary communications device 100 comprising a transceiver 110, for example a mobile wireless cellular communications transceiver or a base station transceiver. In other embodiments, the communications device is a receiver only or a transmitter only, examples of which are discussed below.

The exemplary communications device 100 also comprises generally a processor 120 having a digital signal processor (DSP) coupled to the transceiver 110. The exemplary DSP is integrated with the processor, although in other embodiments the DSP is a discrete component, and in some embodiments the DSP may not be required.

The processor 120 is coupled to memory 130, including for example RAM and ROM and in some embodiments some type of flash memory. The exemplary device includes a display 140, for example a low power LCD display device. The exemplary communications device also includes generally input and output devices 130, for example, an alphanumeric keypad, scrolling and/or pointing devices, a microphone, an audio output, input and output signal ports, etc., depending on the nature of the device.

The communications devices of the present invention include preferably a digital-to-phase synthesizer having one or more fixed or variable frequency and phase outputs coupled to a transmitter and/or to a receiver, or to a transceiver of the type illustrated schematically in FIG. 1.

FIG. 2 illustrates a digital-to-phase synthesizer 200 comprising

generally an integrated phase-locked loop (PLL) voltage controlled oscillator (VCO) 210 having a reference frequency input F_{REF} 212 and an integrated PLL VCO signal output F_{CLK} 214, which is coupled to an input of a delay line 220 that generates controlled delayed versions of the reference frequency signal input, which is the PLL VCO signal output F_{CLK} 214 in FIG. 2.

In the exemplary embodiment of FIG. 2, the delay line 220 comprises a plurality of inverter buffers 222 connected in series, only some of which are identified by reference numerals. The input and output of the delay line 220 is locked to a desired delay time with a phase detector and low pass filter 230 having an input 232 coupled to an output of the delay line. The phase detector and low pass filter 230 also includes an output 234 coupled to an input of the delay line.

In one embodiment, the delay line is tuned to a single wavelength of the VCO signal output, F_{CLK} 214, input to the delay line 220. In the exemplary embodiment, a serial arrangement of 32 buffers, each having a 31.25 p-second delay, is driven with a 1.0 GHz input clock, F_{CLK} 214, and locked to a total delay of 1000.0 p-seconds.

Digital-to-phase synthesizers and the delay locked loop circuits are disclosed more fully in co-pending U.S. Application No. 09/633,705 filed on 7 August 2000 entitled "Digital-To-Phase Converter", in co-pending U.S. Application No. 09/780,077 filed on 9 February 2001 entitled "Direct Digital Synthesizer Based On Delay Line With Sorted Taps", in co-pending U.S. Application No. 10/000,914 filed on 2 November 2001 entitled "Cascaded Delay Locked Loop Circuit", and in co-pending U.S. Application No. 10/365,558 filed on 21 December 2001 entitled Digital-To-Phase Converter With Extended Frequency Range", the subject matter of which is incorporated herein by reference.

In the exemplary embodiment of FIG. 2, the delay line 220 includes a plurality of output taps between each of the 32 buffers. Each output tap provides a 1.0 GHz output signal having a 360/32=11.25 degree offset relative to the

preceding output tap. In FIG. 2, a multiplexor 240 comprises a plurality of inputs coupled to the output signal taps along the delay line 220. A digital phase processor 250 comprises outputs that control the multiplexor 240 in a manner that selects combinations of phase shifted signals along output taps of the delay line to produce a new output signal F_{OUT} 242 having phase and frequency parameters independent of the original input clock signal F_{CLK} 214. The output signal of the digital-to-phase synthesizer may be frequency or phase modulated, which having utility in transmitter applications discussed further below.

Digital-to-phase synthesizers are disclosed more fully in co-pending U.S. Application No. 09/633,705 filed on 7 August 2000 entitled "Digital-To-Phase Converter", in co-pending U.S. Application No. 09/780,077 filed on 9 February 2001 entitled "Direct Digital Synthesizer Based On Delay Line With Sorted Taps", and in co-pending U.S. Application No. 10/365,558 filed on 21 December 2001 entitled Digital-To-Phase Converter With Extended Frequency Range", the subject matter of which is incorporated herein by reference.

Digital processing and tap selection windowing of digital-to phase synthesizers of the type utilized in the present invention comprises generally determining when to select a tap or taps and which ones to select. More particularly, the input clock cycle during which to process a tap signal output is determined by a frequency accumulator, and a phase accumulator determines which tap to route to the output path. Routing of selected delayed reference clock signal pulses to a subsequent delay line or output port is controlled by a window trigger signal.

The digital processing and tap selection windowing of digital-to-phase synthesizers is disclosed more fully in co-pending U.S. Application No. 10/050,233 filed on 16 January 2002 entitled "Delayed Locked Loop Synthesizer With Multiple Outputs And Digital Modulation" and in co-pending U.S. Application No. 10/365,558 filed on 21 December 2001 entitled "Digital-To-Phase

Converter With Extended Frequency Range", among the other applications referenced herein, the subject matter of which is incorporated herein by reference.

FIG. 3 illustrates a digital-to-phase synthesizer architecture 300 comprising a single delay line 320, the output taps of which are independently selectable by a plurality of parallel multiplexors 346, 344, 342 and 340 having corresponding independent output signals F_{OUTD}, F_{OUTC}, F_{OUTB} and F_{OUTA}, all of which have independently controllable frequencies and/or phases.

FIG. 4 is an exemplary radio receiver 400 comprising a digital-to-phase synthesizer 410 having a reference frequency input F_{REF} and one or more outputs having independently controlled frequencies and/or phases, as discussed generally above. The exemplary digital-to-phase synthesizer includes multiple signal outputs F_{OUT1}, F_{OUT2} and F_{OUT3}. The receiver 400 may be a stand-alone receiver or part of a transceiver.

In one embodiment, digital-to-phase synthesizer outputs are coupled to corresponding mixers having corresponding inputs coupled to one or more receiver antennas. In FIG. 4, the digital-to-phase synthesizer outputs F_{OUT1}, F_{OUT2} and F_{OUT3} are coupled to corresponding mixers 420, 422 and 424, respectively. The mixers 420, 422 and 424 are coupled to corresponding antennas 430, 432 and 434, but in other embodiments two or more of the mixers may be coupled to the same antenna. In some embodiments, there may be included amplification and frequency selection of the received signal prior to mixing. Also, the one or more received signals may be mixed with quadrature components of the digital-to-phase synthesizer output signals.

The output of the one or more mixers is coupled generally to a demodulator. In FIG. 4, the output of the mixers is filtered by filters 440, 442 and 444 and digitized at A/D converters 450, 452 and 454 before processing by baseband processors 460, 462 and 464. In the exemplary digital receiver architecture of FIG. 4, the baseband processing is performed by a digital signal

processor (DSP), as illustrated generally in FIG. 1. In embodiments with multiple mixers, the basesband processing may be performed by one or more processors, which may be integrated or discrete components.

In some embodiments, illustrated in the receiver process flow chart of FIG. 5, one or more signals are received at block 510. The received signal is down-converted by mixing 520 with a first digital-to-phase synthesizer output signal, and the down-converted signal is demodulated at block 530. As noted, the received signal or signals may be amplified and subject to frequency selection before mixing. In some embodiments where multiple signals are received, the second signal is down-converted by mixing with a second digital-to-phase synthesizer output signal while down-converting the first received signal.

In diversity receiver applications, the received signal is down-converted by mixing it with first and second digital-to-phase synthesizer output signals having the same frequency and the same phase. In one embodiment, the signal is received at first and second antennas having a diversity relationship, for example spacial diversity. Other diversity receiver embodiments are characterized by polarizing diversity, or some form of propagation mode diversity, or time diversity, et cetera as known generally by those having ordinary skill in the art.

In multiple input multiple output (MIMO) receiver applications, a signal received at different antennas of the receiver is mixed with at least two digital-to-phase synthesizer output signals having the same frequency.

In adaptive array receiver applications, a signal received by multiple antennas is mixed with a corresponding multiple of digital-to-phase synthesizer output signals having the same frequency. An adaptive array is realized by changing the phases of at least one of the multiple digital-to-phase synthesizer output signals mixed with the received signal.

In multi-mode receiver applications, the receiver receives multiple signals having different frequencies, for example Global Positioning System (GPS)

enabled wireless communications devices, and multi-system cellular devices, combination wide area network (WAN) and cellular communications devices, etc.Multi-mode receivers thus generally include one or more baseband processors capable of processing the variety of signals received. In some applications, the receiver includes different antennas for receiving the various signals, for example a GPS antenna and a multi-band cellular antenna. The received signals are mixed with corresponding digital-to-phase synthesizer output signals having different frequencies and/or phases prior to baseband processing, or demodulation.

In cellular network neighbor list scanning applications, at least two signals having different frequencies are received and mixed with corresponding digital-to-phase synthesizer output signals having different frequencies. Neighbor lists may thus be scanned while receiving another signal on a broadcast or a dedicated channel.

FIG. 6 is an exemplary radio transmitter 600 comprising a digital-to-phase synthesizer 610 having one or more frequency or phase modulated signal outputs coupled to corresponding antennas 620, 622 and 624 for transmission. The transmitter may be a stand-alone device or part of a transceiver. The modulated signal outputs of the digital-to-phase synthesizer are typically amplified before transmission, for example by amplifiers 630, 632 and 634 in FIG. 6. In some embodiments having more than one modulated output signal from the digital-to-phase synthesizer, the modulated outputs are transmitted from a common antenna, depending upon the requirements of the particular application.

In FIG. 6, the digital-to-phase synthesizer 610 frequency or phase modulates one or more information signals for transmission by selectively tapping the phase shifted outputs signals along the delay line of the digital-to-phase synthesizer, as discussed above and disclosed more fully in one or more of the co-pending patent applications referenced hereinabove. In FIG. 6, an adaptive array transmitter may be realized by changing the phase of at least one of multiple

frequency modulated signals transmitted by the transmitter.

FIG. 7 is another exemplary radio transmitter 700 comprising a digital-to-phase synthesizer 710 having two frequency modulated outputs that are added at a summer 720, the output of which may be amplified before transmission.

While the present inventions and what is considered presently to be the best modes thereof have been described in a manner that establishes possession thereof by the inventors and that enables those of ordinary skill in the art to make and use the inventions, it will be understood and appreciated that there are many equivalents to the exemplary embodiments disclosed herein and that myriad modifications and variations may be made thereto without departing from the scope and spirit of the inventions, which are to be limited not by the exemplary embodiments but by the appended claims.

What is claimed is:

CLAIMS

1. A method in a radio transmitter, comprising:

receiving a first signal;

down-converting the first signal received by mixing it with a first digital-to-phase synthesizer output signal;

receiving a second signal while receiving the first signal;

down-converting the second signal received by mixing it with a second digital-to-phase synthesizer output signal while down-converting the first signal received.

2. The method of Claim 1,

generating the first digital-to-phase synthesizer output signal by multiplexing a first plurality of signals tapped along a delay line,

generating the second digital-to-phase synthesizer output signal by multiplexing a second plurality of signals tapped along a delay line.

3. The method of Claim 1,

receiving the first signal at a first antenna, receiving the second signal at a second antenna ,

the first and second digital-to-phase synthesizer output signals having the same frequency and the same phase.

4. The method of Claim 1,

receiving the first signal at a first antenna, receiving the second signal at a second antenna;

the first and second digital-to-phase synthesizer output signals having the same frequency,

realizing an adaptive array by changing the phases of at least one of the first and second digital-to-phase synthesizer output signals.

5. The method of Claim 1,

the first and second signals having different frequencies

the first and second digital-to-phase synthesizer output signals having different frequencies.

6. The method of Claim 1,

the first signal is the same as the second signal;

receiving the first signal at a first antenna, receiving the second signal at a second antenna,

the first and second digital-to-phase synthesizer output signals having the same frequency.

7. The method of Claim 1,

the first signal has a different frequency than the second signal,

scanning a neighbor list by receiving the second signal while receiving the first signal,

the first and second digital-to-phase synthesizer output signals

having different frequencies.

8. The method Claim 1, mixing the first signal with quadrature components of the first digital-to-phase synthesizer output signal.

9. The method of Claim 1,down-converting the first and second signals received by mixing the first and second signals with corresponding first and second fixed frequency digital-to-phase synthesizer output signals.

10. A radio transceiver, comprising:

a digital-to-phase synthesizer having a reference frequency input and a plurality of digital-to-phase synthesizer signal outputs,

an antenna;

a first mixer having a first input coupled to the antenna, a first one of the plurality of digital-to-phase synthesizer signal outputs coupled to the first mixer;

a second mixer having a second input coupled to the antenna, a second one of the plurality of digital-to-phase synthesizer signal outputs coupled to the second mixer;

a demodulator, an output of the first mixer coupled to a first input of the demodulator, an output of the second mixer coupled to a second input of the demodulator.

11. The radio transceiver of Claim 10, the digital-to-phase synthesizer

comprising:

an integrated phase-locked loop (PLL) voltage controlled oscillator (VCO) having the reference frequency input and an integrated PLL VCO signal output,

a delay line having a delay line input coupled to the integrated PLL VCO signal output;

a phase detector having an input coupled to an output of the delay line, an output of the phase detector coupled to an input of the delay line;

a first multiplexor having a plurality of inputs coupled to signal taps along the delay line, the first multiplexor having the first one of the plurality of digital-to-phase synthesizer signal outputs coupled to the input of the first mixer;

a second multiplexor having a plurality of inputs coupled to signal taps along the delay line, the second multiplexor having the second one of the plurality of digital-to-phase synthesizer signal outputs coupled to the input of the second mixer.

12. The radio transceiver of Claim 11, the digital-to-phase synthesizer comprising a digital-to-phase processor and a tap selector for controlling inputs of the first and second multiplexors.

13. The radio transceiver of Claim 10, the first and second of the plurality of digital-to-phase synthesizer signal outputs having the same frequency.

14. The radio transceiver of Claim 10, the first and second of the plurality of digital-to-phase synthesizer signal outputs having the same phase.

15. The radio transceiver of Claim 10, the first and second of the plurality of digital-to-phase synthesizer signal outputs having a different phase.

16. The radio transceiver of Claim 10, one of the first and second of the plurality of digital-to-phase synthesizer signal outputs include quadrature components.

17. The radio transceiver of Claim 10, the demodulator includes a global positioning system (GPS) baseband processing portion, the demodulator includes a cellular communications baseband processing portion.

18. The radio transceiver of Claim 10, the demodulator includes a wireless wide area network (WAN) baseband processing portion, the demodulator includes a cellular communications baseband processing portion.

19. A method in a radio transmitter, comprising:

providing a first modulated signal by modulating a first signal with a digital-to-phase synthesizer;

transmitting the first modulated signal.

20. The method of Claim 19, frequency modulating the first signal with a digital-to-phase synthesizer by selectively tapping signals along a delay line

of the digital-to-phase synthesizer.

21. The method of Claim 19, phase modulating the first signal with a digital-to-phase synthesizer by selectively tapping signals along a delay line of the digital-to-phase synthesizer.

22. The method of Claim 19,

providing a second modulated signal by frequency modulating a second signal with a digital-to-phase synthesizer;

transmitting the second modulated signal.

23. The method of Claim 22,

providing an amplitude modulated signal by summing the first and second phase modulated signals;

transmitting the amplitude modulated signal.

24. The method of Claim 22,

realizing an adaptive array transmitter by changing the phase of at least one of the first and second frequency modulated signals.

25. The method of Claim 22, transmitting the first and second modulated signals from a two terminal differential antenna.

26. A radio transceiver comprising

a digital-to-phase synthesizer having a reference frequency input, the digital-to-phase synthesizer having a first frequency modulated signal output;

an antenna,

the first modulated signal output of the digital-to-phase synthesizer coupled to the antenna.

27. The radio transceiver of Claim 26, the digital-to-phase synthesizer comprising:

an integrated phase-locked loop (PLL) voltage controlled oscillator (VCO) having the reference frequency input and an integrated PLL VCO signal output,

a delay line comprising having a delay line input coupled to the integrated PLL VCO signal output;

a phase detector having an input coupled to an output of the delay line, an output of the phase detector coupled to an input of the delay line;

a first multiplexor having a plurality of inputs coupled to the delay line, the first multiplexor having the first one of the plurality of digital-to-phase synthesizer signal outputs coupled to the input of the first mixer;

a second multiplexor having a plurality of inputs coupled to the delay line, the second multiplexor having the second one of the plurality of digital-to-phase synthesizer signal outputs coupled to the input of the second mixer.

28. The radio transceiver of Claim 26, the digital-to-phase synthesizer having a second modulated signal output coupled to the antenna,

frequency modulating the first and second modulated outputs if the digital-to-phase synthseizer.

29. The radio transceiver of Claim 28, the antenna is a two terminal differential antenna

30. The radio transceiver of Claim 26,

the digital-to-phase synthesizer having a second frequency modulated signal output;

a summer having inputs, the summer having an output coupled to the antenna,

the first frequency modulated signal output of the digital-to-phase converter coupled to a first input of the summer, the second frequency modulated signal output of the digital-to-phase converter coupled to a second input of the summer.

31. A method in a radio transceiver, comprising:

receiving a signal;

down-converting the signal received by mixing it with a digital-to-phase synthesizer output signal;

demodulating the down-converted signal.

32. The method of Claim 31, down-converting the signal received by mixing it with a first and second digital-to-phase synthesizer output signals

having the same frequency and phase.

33. The method of Claim 31,

receiving the signal at first and second separate antennas;

mixing the signal with the first and second digital-to-phase synthesizer output signals having the same frequency,

realizing an adaptive array by changing the phases of at least one of the first and second digital-to-phase synthesizer output signals.

34. The method of Claim 31, generating the output signal of the digital-to-phase synthesizer by selecting taps along a delay line of the digital–to-phase synthesizer.

35. The method of Claim 31, receiving the signal by receiving first and second signals at a two terminal differential antenna, down-converting the first and second signals received by mixing the first and second signals with corresponding first and second digital-to-phase synthesizer output signals, demodulating the down-converted signals.

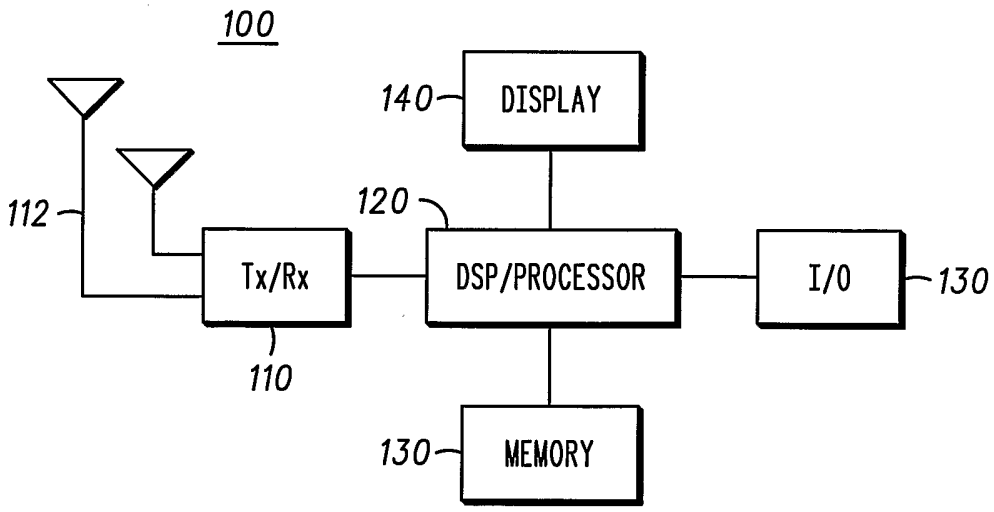

100
140
DISPLAY
112
120
Tx/Rx
DSP/PROCESSOR
I/O
130
110
130
MEMORY

FIG. 1

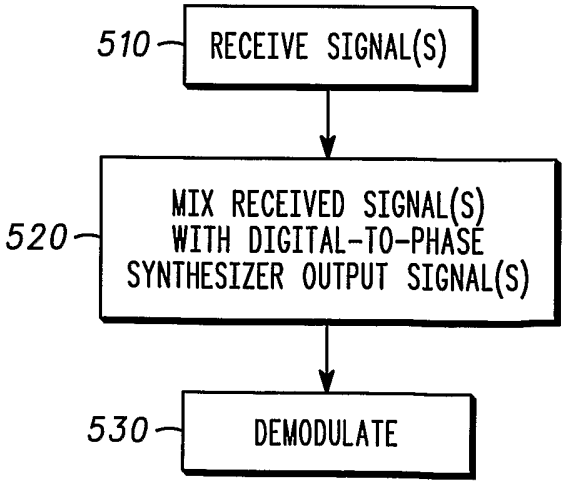

510
RECEIVE SIGNAL(S)
520
MIX RECEIVED SIGNAL(S) WITH DIGITAL-TO-PHASE SYNTHESIZER OUTPUT SIGNAL(S)
530
DEMODULATE

FIG. 5

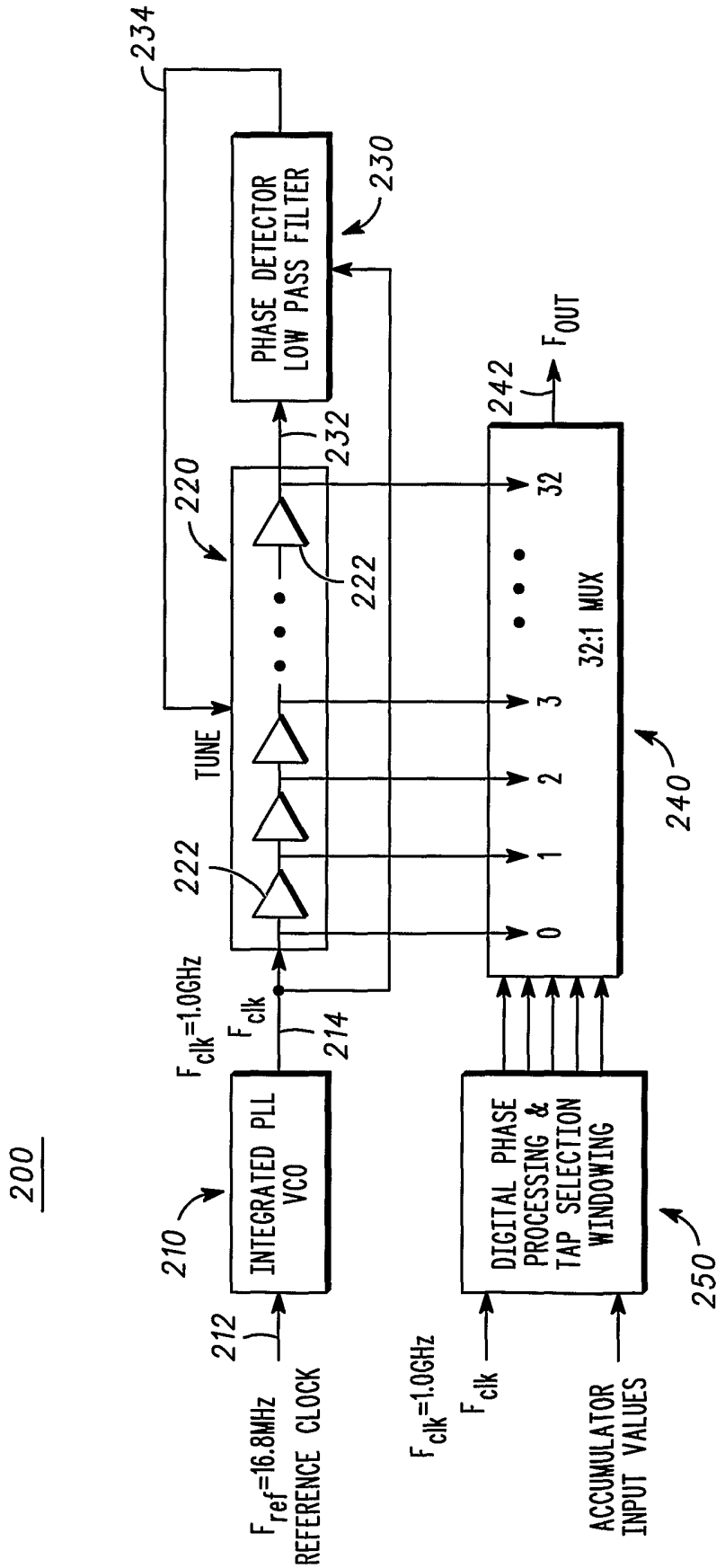

200
210
INTEGRATED PLL VCO
212
F_{ref}=16.8MHz
REFERENCE CLOCK
F_{clk}=1.0GHz
F_{clk}
214
220
222
TUNE
230
PHASE DETECTOR LOW PASS FILTER
232
234
240
32:1 MUX
0
1
2
3
32
242
F_{OUT}
250
DIGITAL PHASE PROCESSING & TAP SELECTION WINDOWING
F_{clk}=1.0GHz
F_{clk}
ACCUMULATOR INPUT VALUES

FIG. 2

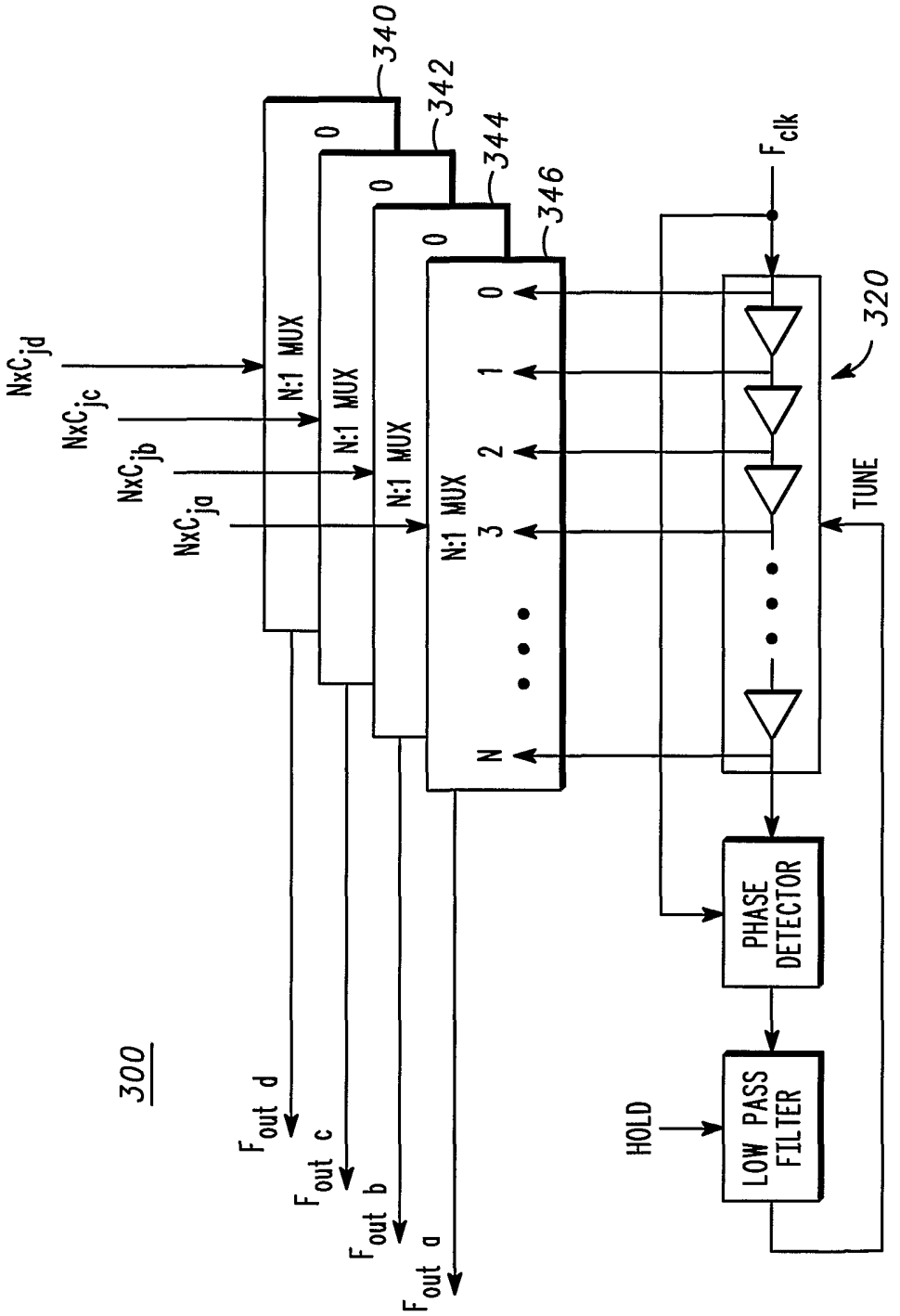

300
340
342
344
346
320
NxC$_{jd}$
NxC$_{jc}$
NxC$_{jb}$
NxC$_{ja}$
N:1 MUX
N:1 MUX
N:1 MUX
N:1 MUX
0
0
0
0
0
1
2
3
N
F$_{clk}$
TUNE
PHASE DETECTOR
LOW PASS FILTER
HOLD
F$_{out}$ d
F$_{out}$ c
F$_{out}$ b
F$_{out}$ a

FIG. 3

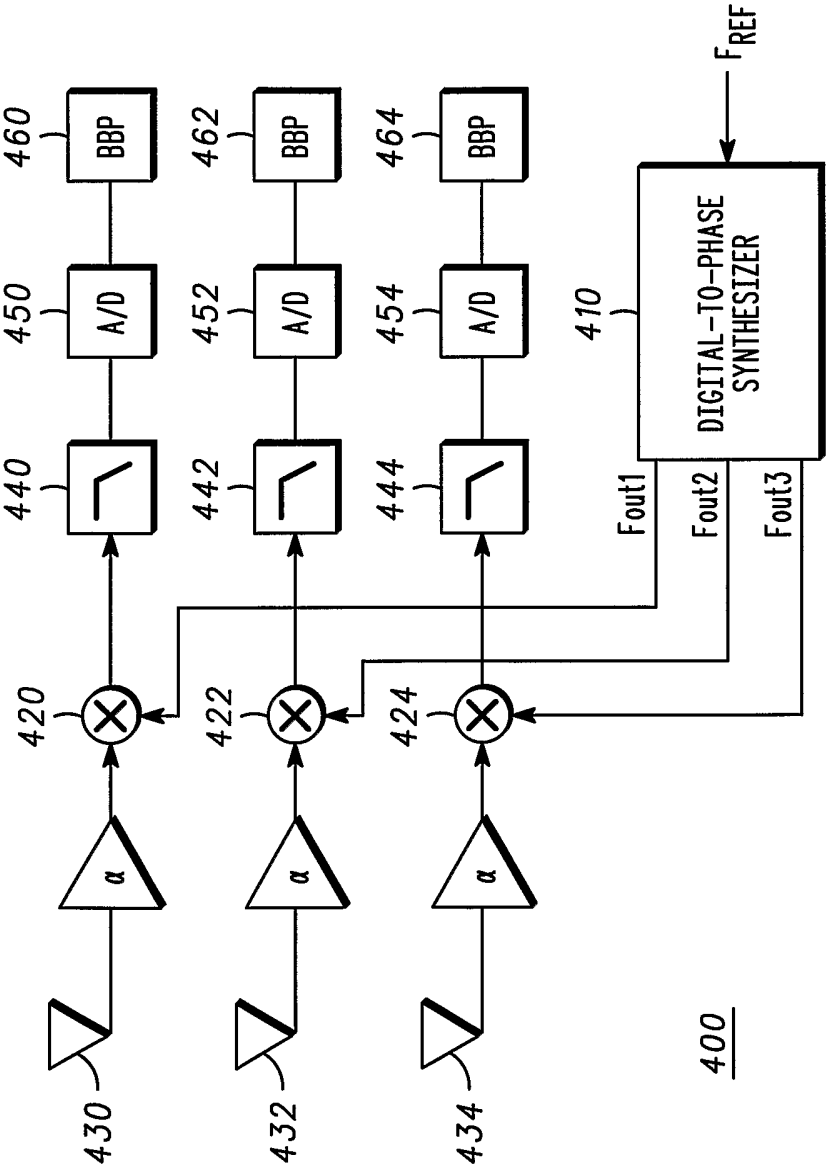

460
462
464
BBP
BBP
BBP
450
452
454
A/D
A/D
A/D
440
442
444
410
DIGITAL-TO-PHASE SYNTHESIZER
F_{REF}
Fout1
Fout2
Fout3
420
422
424
α
α
α
430
432
434
400

FIG. 4

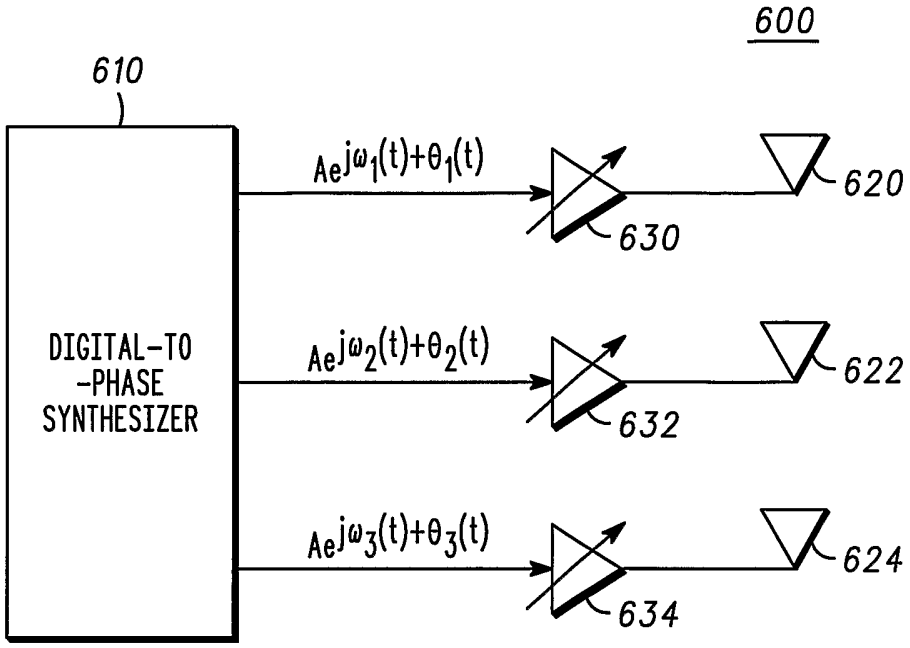

600
610
DIGITAL-TO
-PHASE
SYNTHESIZER
$Ae^{j\omega_1(t)+\theta_1(t)}$
$Ae^{j\omega_2(t)+\theta_2(t)}$
$Ae^{j\omega_3(t)+\theta_3(t)}$
620
622
624
630
632
634

FIG. 6

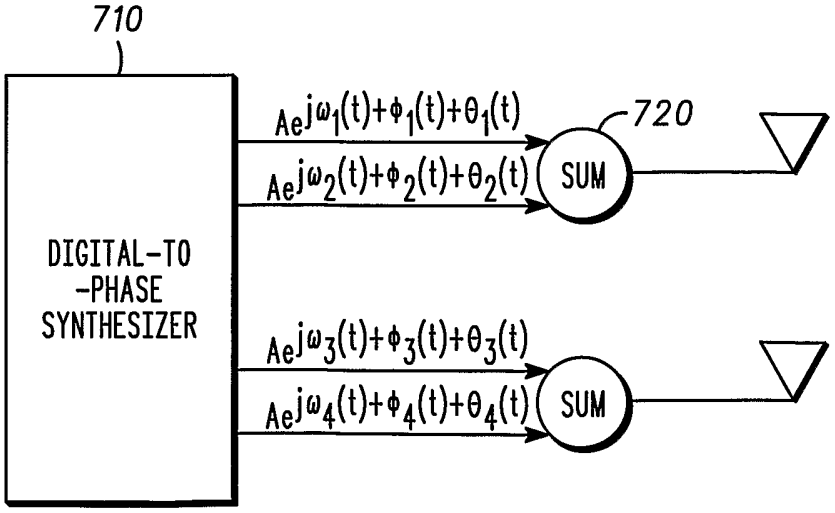

710
DIGITAL-TO
-PHASE
SYNTHESIZER
$Ae^{j\omega_1(t)+\phi_1(t)+\theta_1(t)}$
$Ae^{j\omega_2(t)+\phi_2(t)+\theta_2(t)}$
$Ae^{j\omega_3(t)+\phi_3(t)+\theta_3(t)}$
$Ae^{j\omega_4(t)+\phi_4(t)+\theta_4(t)}$
SUM
SUM
720

FIG. 7