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(54) NANO WIRES AND METHOD OF MANUFACTURING THE SAME

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(57) **ABSTRACT**

The present invention provides a method of manufacturing nano wires and nano wires having a p-n junction structure. The method includes: stacking a mask layer on a substrate; patterning the mask layer into stripes; and performing an oxygen ion injection process on the substrate and the mask layer to form oxygen ion injection regions in the substrate, thereby forming nano wire regions embedded in the substrate and separated from the substrate by the oxygen ion injection regions.

FIG. 1A

FIG. 1B

FIG. 1C

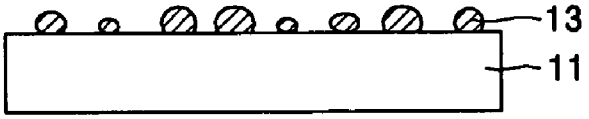


FIG. 1D

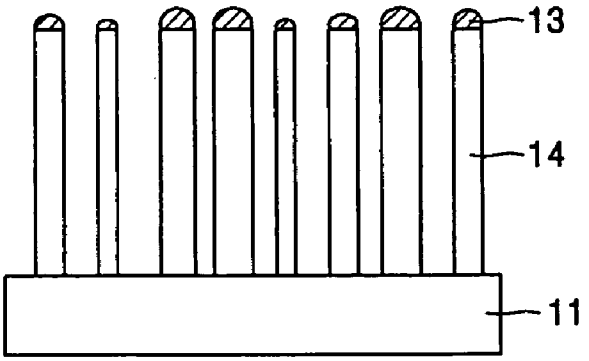


FIG. 2A

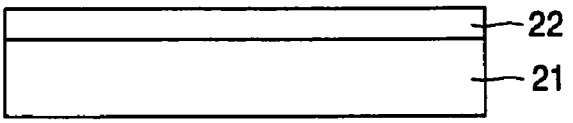


FIG. 2B

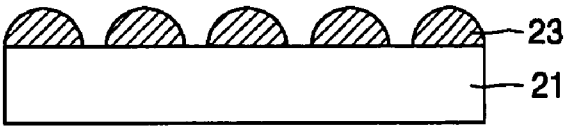


FIG. 2C

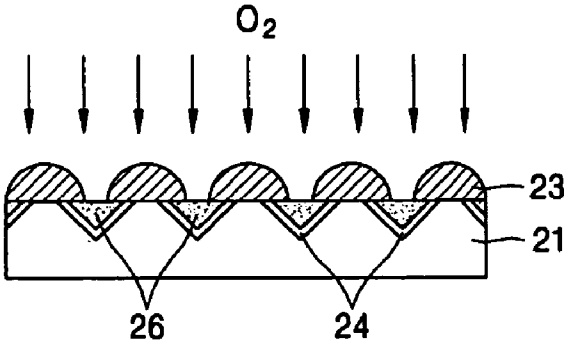


FIG. 2D

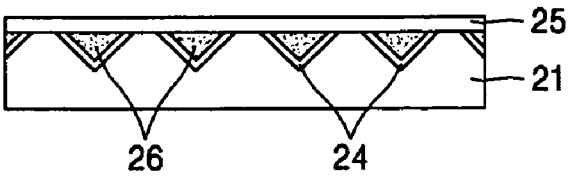


FIG. 2E

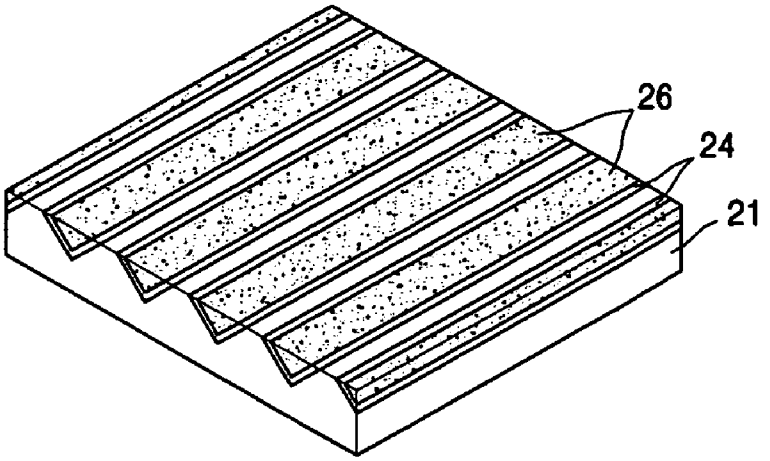


FIG. 3A

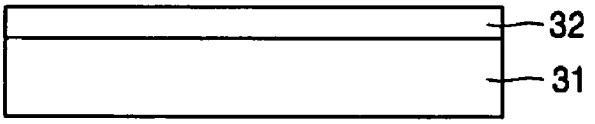


FIG. 3B

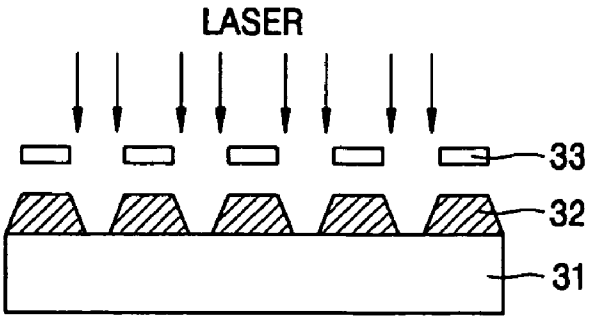


FIG. 3C

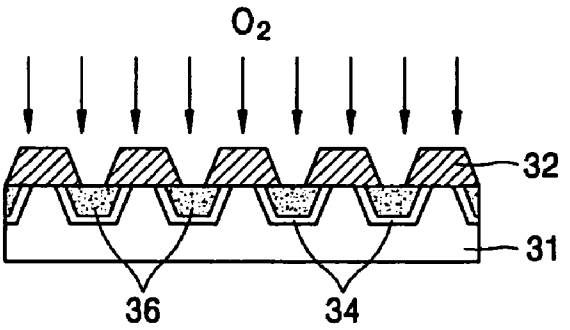


FIG. 3D

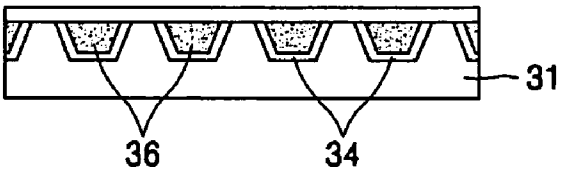


FIG. 3E

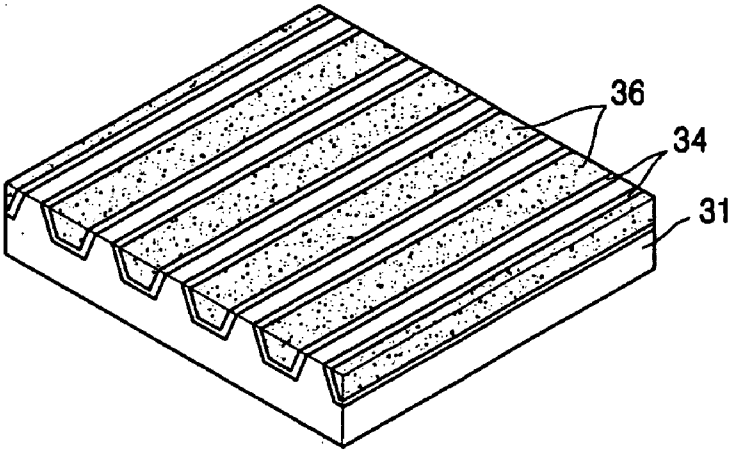


FIG. 4A

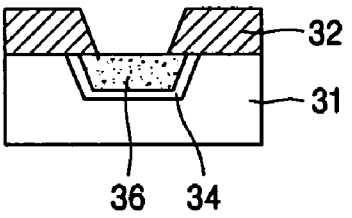


FIG. 4B

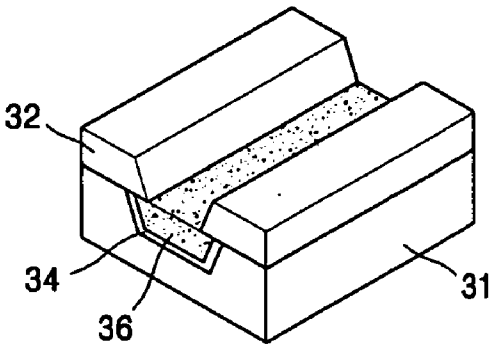


FIG. 4C

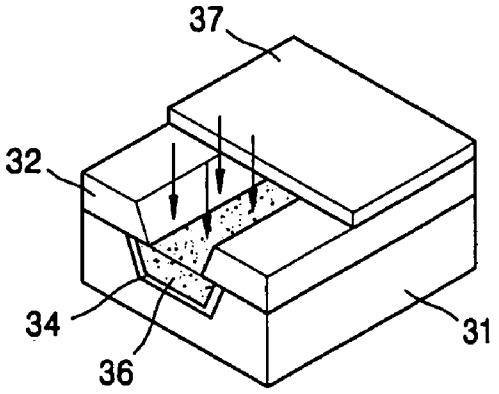


FIG. 4D

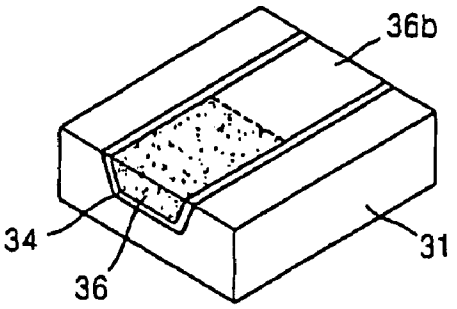


FIG. 4E

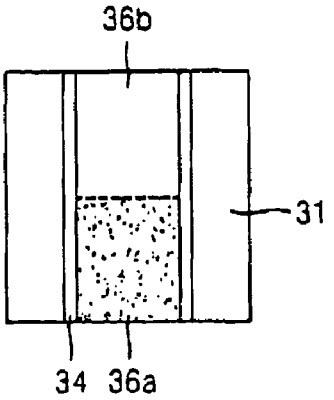
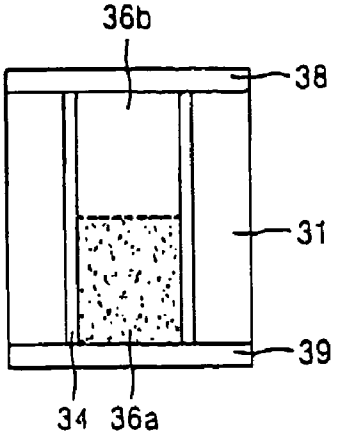


FIG. 4F



NANO WIRES AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

[0001] This application claims the priority of Korean Patent Application No. 10-2005-0016185, filed on Feb. 28, 2005 in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

[0002] 1. Field of the Invention

[0003] The present invention relates to nano wires and a method of manufacturing the same, and more particularly, to nano wires made by accurately controlling regions of a silicon substrate on which the nano wires are formed and sizes of the nano wires, and a method of manufacturing the same.

[0004] 2. Description of the Related Art

[0005] Nano wires are currently being widely researched, and are a next-generation technology used in various devices such as optical devices, transistors, and memory devices. Materials used in conventional nano wires include silicon, tin oxide, and gallium nitride, which is a light emitting semiconductor. The conventional nano wire manufacturing technique is sufficiently developed to be used for altering of the length and width of nano wires.

[0006] Nano light emitting devices using quantum dots are used in conventional nano light emitting devices. Organic EL devices using quantum dots have high radiative recombination efficiency but low carrier injection efficiency. GaN LEDs, which use quantum wells, have relatively high radiative recombination efficiency and carrier injection efficiency. However, it is very difficult to mass produce GaN LED due to a defect caused by the difference in the crystallization structures of the GaN LED and a commonly used sapphire substrate, and thus the manufacturing costs of GaN LEDs are relatively high. A nano light emitting device using nano wires has very high radiative recombination efficiency and relatively high carrier injection efficiency. In addition, the manufacturing process of a nano light emitting device is simple and a nano light emitting device can be formed to have a crystallization structure that is practically identical to that of a substrate, and thus it is easy to mass produce the nano light emitting device.

[0007] **FIGS. 1A through 1D** are cross-sectional views illustrating a vapor-liquid-solid (VLS) method, which is a conventional method of manufacturing nano wires.

[0008] Referring to **FIG. 1A**, first, a substrate **11** is provided. The substrate **11** is a commonly used silicon substrate.

[0009] Thereafter, referring to **FIG. 1B**, a metal layer **12** is formed on top of the substrate **11** by spreading a metal such as Au.

[0010] Then, referring to **FIG. 1C**, the resultant structure is thermally processed at approximately 500° C. As a result, materials in the metal layer **12** are agglomerated, thereby forming catalysts **13**. As illustrated in **FIG. 1C**, the sizes of the catalysts **13** are irregular, that is, they have random sizes.

[0011] Next, referring to **FIG. 1D**, nano wires **14** are formed with the catalysts **13** as nucleation regions. To grow the nano wires **14**, silane (SiH_4), which is a compound of silicon and hydrogen, is supplied to the catalysts **13** to grow the nano wires **14** by inducing nucleation of Si of silane at lower portions of the catalysts **13** at the eutectic temperature. The growth of the nano wires **14** formed at the lower portion of the catalysts **13** and having a desired length can be controlled by controlling the amount of supplied silane, as illustrated in **FIG. 1D**.

[0012] As the method of forming nano wires illustrated in **FIGS. 1A through 1** described above, nano wires with desired lengths can be easily formed by appropriately controlling the amount of supplied material gas such as silane. However, the growth of nano wires can be limited by the diameters and distribution of the catalysts, and thus it is difficult to accurately control the thicknesses, locations, and distribution of nano wires. In addition, the nano wires can be formed only perpendicular to a substrate using the method described above, and thus a technique to form nano wires parallel to the substrate is required.

SUMMARY OF THE INVENTION

[0013] The present invention provides a method of manufacturing nano wires which are grown by controlling the diameters and distribution of nucleation regions for forming the nano wires, and nano wires accurately grown using the method.

[0014] The present invention also provides nano wires that have a p-n junction structure and that are formed to an accurate size, and a method of manufacturing the same.

[0015] According to an aspect of the present invention, there is provided a method of manufacturing nano wires. The method includes: stacking a mask layer on a substrate, and patterning the mask layer into stripes; and performing an oxygen ion injection process on the substrate and the mask layer to form oxygen ion injection regions in the substrate, thereby forming nano wire regions embedded in the substrate and separated from the substrate by the oxygen ion injection regions.

[0016] The stacking of the mask layer may include: forming a photoresist layer by coating a photoresist on top of the substrate, and the patterning the mask layer into stripes may include: patterning the photoresist layer.

[0017] The stacking of the mask layer may include: forming a photoresist layer by coating a photoresist on top of the substrate; and the patterning the mask layer into stripes may include: patterning the photoresist layer by placing a striped grating over the photoresist layer and emitting a laser thereon; and performing a thermal process on the patterned photoresist layer to form the mask layer.

[0018] The method further includes: controlling the sizes of the nano wires by performing an oxidizing process on a surface of the substrate and the nano wire regions to form an oxidation layer on the surface of the substrate and the nano wire regions.

[0019] The substrate may be a silicon substrate.

[0020] According to another aspect of the present invention, there is provided a method of manufacturing nano wires having a p-n junction structure. The method includes: stacking a mask layer on top of a substrate doped with a first impurity, and patterning the mask layer into stripes; performing an oxygen ion injection process on the substrate and

the mask layer to form oxygen ion injection regions in the substrate, thereby forming nano wire regions embedded in the substrate and separated from the substrate by the oxygen ion injection regions; and forming a second impurity region contacting a first impurity region in each of the nano wires by disposing a third mask layer over some regions of the substrate and the mask layer and doping with a second impurity.

[0021] The method may further include: forming a first electrode contacting the first impurity region and a second electrode contacting the second impurity region by spreading a conductive material on the substrate after removing the mask layer.

[0022] According to another aspect of the present invention, there is provided a nano wire structure including: a substrate; nano wires formed in stripes in the substrate; and oxygen ion injection regions formed at a border between the substrate and the nano wires to separate the substrate and the nano wires.

[0023] According to another aspect of the present invention, there is provided a nano wires having a p-n junction structure. The nano wires include: a substrate doped with a first impurity; nano wires formed in stripes in the substrate with first and second impurity regions; oxygen ion injection regions formed at a border between the substrate and the nano wires to separate the substrate and the nano wires; and a first electrode that contacts the first impurity region and is formed on the substrate, and a second electrode that contacts the second impurity region and is formed on the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

[0025] **FIGS. 1A through 1D** are cross-sectional views illustrating a conventional method of manufacturing nano wires;

[0026] **FIGS. 2A through 2E** are cross-sectional views illustrating a method of manufacturing nano wires according to an embodiment of the present invention;

[0027] **FIGS. 3A through 3E** are cross-sectional views illustrating a method of manufacturing nano wires according to another embodiment of the present invention; and

[0028] **FIGS. 4A through 4F** are views illustrating a method of forming a p-n structure with the nano wires manufactured using the method illustrated in **FIGS. 1A through 2E** or **FIGS. 3A through 3E** according to the first and second embodiments according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0029] Nano wires and a method of manufacturing the same according to the present invention will now be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. In the drawings, the lengths and sizes of layers are exaggerated for clarity.

[0030] **FIGS. 2A through 2E** are cross-sectional views illustrating a method of manufacturing nano wires according to an embodiment of the present invention.

[0031] Referring to **FIG. 2A**, first, a photoresist material is coated to a thickness of several to tens of nm on a substrate **21** to form a photoresist layer **22**. The substrate **21** is a commonly used silicon substrate.

[0032] Referring to **FIG. 2B**, the photoresist layer **22** is patterned into stripes on the substrate **21** on which the photoresist layer **22** is formed, and the resultant structure is heated to near the melting point of the material of the photoresist layer **11**. Then, each of the stripes of the photoresist layer **22** can be formed to have a semicircular cross section. Consequently, a mask layer **23** composed of stripes having semi circular cross sections can be formed.

[0033] Next, referring to **FIG. 2C**, an implantation process in which oxygen is ion injected into the substrate **21** is performed. When the oxygen ion injection is performed using a plasma doping process, the ion injection energy can be selectively controlled in the range from 1 to 100 keV. In this process, an oxygen concentration of 5×10^{17} to 3×10^{18}/cm^2 may be used, as in separation by implantation of oxygen (SIMOX). A deeper ion injection region can be formed in portions of the substrate **21** where the ions are injected directly into the substrate **21** than in portions of the substrate **21** where the ions are injected via the mask layer **23**. That is, oxygen ion injection regions **24** are affected by the shape of the cross section of the mask layer **23**, as illustrated in **FIG. 2C**. Since the cross section of the mask layer **23** is a semicircle, the oxygen ions injected via relatively thick regions of the mask layer **23** cannot enter the substrate **21**, but remain in the mask layer **23**, while the depth of the oxygen ions via relatively thin regions of the mask layer **23** are injected deeper into the substrate **21** at. Therefore, the shape of the oxygen ion injection regions **24** can be controlled according to the shape and thickness of the mask layer **23** or by adjusting ion injection time.

[0034] Referring to **FIG. 2D**, the mask layer **23** is removed and an oxidizing process is performed on a top surface of the substrate **21** under an oxygen atmosphere. The oxidation process is optional, and can be performed to control the sizes of the oxygen ion injection regions **24**. It was described that the shape of the mask layer **23** and ion injection process condition can be controlled to control the size and shape of the oxygen ion injection regions **24** with reference to **FIG. 2C**. In addition, to control the depth of the oxygen ion injection regions **24** from the surface of the substrate **21**, an oxidizing process can be further performed to the substrate **21**. As illustrated in **FIG. 2D**, when the oxidizing process is performed to the substrate **21**, an oxidation layer **25** is formed on the substrate **21** and the depth of the oxygen ion injection regions **24** decreases.

[0035] Referring to **FIG. 2E**, when the oxidation layer **25** is removed, nano wire **26** regions embedded in the substrate **21** can be obtained. The nano wires **26** can be separated by the substrate **21** and the oxygen ion injection regions **24**. The shapes and widths of the nano wires **26** are controlled by controlling the shape of the mask layer **23**, the oxygen ion injection process, and the range of the thickness of the oxidation layer **25**, as described with reference to **FIGS. 2C and 2D**.

[0036] **FIGS. 3A through 3E** are cross-sectional views illustrating a method of manufacturing nano wires according to another embodiment of the present invention.

[0037] Referring to **FIG. 3A**, a photoresist material is coated to a thickness of tens of nm on a substrate **31** to form a photoresist layer **32**. The substrate **31** is a commonly used silicon substrate.

[0038] Referring to **FIG. 3B**, a striped grating **33** is disposed above the substrate **31** on which the photoresist layer **32** is formed and the photoresist layer **32** is patterned using a laser. For example, the patterning process may be similar to that used to make a grating of a DFB-laser. Here, a solid laser or a gas laser is used. Regions of the photoresist layer **32** on which the laser is emitted during the patterning process are removed. Thus, the stripes of the photoresist layer **32** have trapezoidal cross-sections. A separate heating process as illustrated in **FIG. 2B** is not performed in the present embodiment.

[0039] Referring to **FIG. 3C**, an implantation process in which oxygen is ion injected into the substrate **31** is performed. If the ion injection energy of the oxygen that is ion injected is uniformly controlled, oxygen ion injection regions **34** are formed deeper where the oxygen is injected directed into the substrate **31** than when the oxygen is injected into the substrate **31** via the photoresist layer **32**. Consequently, the oxygen ion injection regions **34** are affected by the cross-sections of the photoresist layer **32** and are trapezoidals, as illustrated in **FIG. 3C**. Of course, the depths of the oxygen ion injection regions **34** can be increased if the ion injection energy, which can be controlled, is increased.

[0040] Referring to **FIG. 3D**, the photoresist layer **32** is removed, and an oxidizing process is performed on the top surface of the substrate **31** under an oxygen atmosphere. The objective of the oxidizing process is the same as described with reference to **FIG. 2D**, to control the depth of the oxygen ion injection regions **34**, and the depth of a formed oxidation layer can be controlled.

[0041] Referring to **FIG. 3E**, when the oxidation layer is removed, nano wires **36** embedded in the substrate **31** can be obtained. The nano wires **36** are separated by the oxygen ion injection regions **34**, and are composed of the same material as the substrate **31**. The nano wires **36** are formed during the oxygen ion injection process like the nano wires **26** and **36** illustrated in **FIGS. 2C and 3C**. That is, the oxygen ion injection regions **24** and **34** are respectively formed in the substrates **21** and **31** during the oxygen ion injection process, and regions separated from the substrates **21** and **31** are formed. The forming of the mask layer **23** or the removing of the photoresist layer **32** and the oxidizing process that are performed after the oxygen ion injection regions **24** and **34** are formed are optional processes. Particularly, it should be kept in mind that the oxidizing process is an optional process for controlling the sizes of the nano wires **26** and **36**.

[0042] Nano wires having a p-n structure according to an embodiment of the present invention will now be described with reference to **FIGS. 4A through 4F** below.

[0043] **FIG. 4A** is a cross-section of a portion of a sample in which the oxygen ion injection region **34** formed during the oxygen ion injection process illustrated in **FIG. 3C** and the nano wire **36** are formed. The same process can be applied to a sample illustrated in **FIG. 2C**. **FIG. 4B** is a perspective view of the sample illustrated in **FIG. 4A**.

[0044] Referring to **FIGS. 4A and 4B**, the oxygen ion injection region **34** is formed in the substrate **31** made of, for example, silicon, which is commonly used in a semiconductor process, and a nano wire **36** separated from the substrate **31** by the oxygen ion injection region **34** is formed. When the substrate **31** is made of silicon, silicon nano wires are formed in the substrate **31** parallel to the substrate **31**. The photoresist layers **32** patterned to have trapezoidal cross-sections are formed on top of the substrate **31**. When using a semiconductor substrate **31** that is initially doped with a p- or n-type impurity, the nano wire **36** is also doped with a p- or n-type impurity. Therefore, the substrate **31** and the nano wire **36** can be doped with a first impurity.

[0045] Referring to **FIG. 4C**, a mask **37** is disposed above the substrate **31**, and a second impurity is doped into the structure. The second impurity used here can be any material used in a general semiconductor process.

[0046] Consequently, referring to **FIG. 4D**, the nano wire **36** is divided into two regions by the doping process. **FIG. 4E** is a plane view of the sample illustrated in **FIG. 4D**. Referring to **FIGS. 4D and 4E**, a single nano wire **36** has a p-n structure in which a first impurity region **36***a* and a second impurity region **36***b* are formed. When the photoresist layers **32** and the mask **37** are removed, a nano wire region is formed in the substrate **31**, and the substrate **31** and the nano wire **36** are structurally separated from each other by the oxygen ion injection region **34**. The nano wire is divided into the first impurity region **36***a* and the second impurity region **36***b*.

[0047] Referring to **FIG. 4F**, a first electrode **39** is formed by coating a conductive material on the substrate **31** so that the first electrode **37** contacts the first impurity region **36***a*, and a second electrode **38** is formed by coating a conductive material on the substrate **31** so that the second electrode **38** contacts the second impurity region **36***b*. In this way, a p-n junction semiconductor device can be obtained.

[0048] The present invention has the following advantages.

[0049] First, the application range of the nano wires of the present invention is very wide since the nano wires are embedded in a substrate, unlike conventional nano wires, which are formed perpendicular to a substrate.

[0050] Second, since the locations, sizes, and distribution of the nano wires can be controlled, it is possible to mass produce the nano wires in an array structure.

[0051] Third, a process of forming nano wires having a p-n junction structure to apply the nano wires in the devices can be easily performed. The process itself is simplified since a MOS-FET is not used, and a conventional semiconductor processing technique can be used.

[0052] Fourth, conventionally, it is difficult to manufacture a semiconductor device having a transistor structure with a precision of 45 nm or less. However, a in the present invention, a highly integrated device having a precision of less than 45 nm can be obtained with a simple p-n junction structure.

[0053] While the present invention has been particularly shown and described with reference to exemplary embodi-

ments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims. For example, it is possible to form nano wires with a p-n junction by doping impurities using a structure illustrated in **FIG. 2E** or **3**E. Therefore, the scope of the invention is defined not by the detailed description of the invention but by the appended claims, and all differences within the scope will be construed as being included in the present invention.

What is claimed is:

1. A method of manufacturing nano wires, the method comprising:

stacking a mask layer on a substrate, and patterning the mask layer into stripes; and

performing an oxygen ion injection process on the substrate and the mask layer to form oxygen ion injection regions in the substrate, thereby forming nano wire regions embedded in the substrate and separated from the substrate by the oxygen ion injection regions.

2. The method of claim 1, wherein the stacking of the mask layer comprises:

forming a photoresist layer by coating a photoresist on top of the substrate,

and the patterning the mask layer into stripes comprises:

patterning the photoresist layer; and

performing a thermal process on the patterned photoresist later to form the mask layer.

3. The method of claim 1, wherein the stacking of the mask layer comprises:

forming a photoresist layer by coating a photoresist on top of the substrate;

and the patterning the mask layer into stripes comprises: and

patterning the photoresist layer by placing a striped grating over the photoresist layer and emitting a laser thereon.

4. The method of claim 1, further comprising: controlling the sizes of the nano wires by performing an oxidizing process on a surface of the substrate and the nano wire regions to form an oxidation layer on the surface of the substrate and the nano wire regions.

5. The method of claim 1, wherein the substrate is a silicon substrate.

6. A method of manufacturing nano wires having a p-n junction structure, the method comprising:

stacking a mask layer on top of a substrate doped with a first impurity, and patterning the mask layer into stripes;

performing an oxygen ion injection process on the substrate and the mask layer to form oxygen ion injection regions in the substrate, thereby forming nano wire regions embedded in the substrate and separated from the substrate by the oxygen ion injection regions; and

forming a second impurity region contacting a first impurity region in each of the nano wires by disposing a third mask layer over some regions of the substrate and the mask layer and doping with a second impurity.

7. The method of claim 1, wherein the stacking of the mask layer comprises:

forming a photoresist layer by coating a photoresist on top of the substrate,

and the patterning the mask layer into stripes comprises:

patterning the photoresist layer; and

performing a thermal process on the patterned photoresist later to form the mask layer.

8. The method of claim 1, wherein the stacking of the mask layer comprises:

forming a photoresist layer by coating a photoresist on top of the substrate;

and the patterning the mask layer into stripes comprises:

patterning the photoresist layer by placing a striped grating over the photoresist layer and emitting a laser thereon; and

performing a thermal process on the patterned photoresist layer to form the mask layer.

9. The method of claim 6, further comprising forming a first electrode contacting the first impurity region and a second electrode contacting the second impurity region by spreading a conductive material on the substrate after removing the mask layer.

10. A nano wire structure comprising:

a substrate;

nano wires formed in stripes in the substrate; and

oxygen ion injection regions formed at a border between the substrate and the nano wires to separate the substrate and the nano wires.

11. The nano wires of claim 10, wherein the substrate and the nano wires are made of silicon.

12. Nano wires having a p-n junction structure, the nano wires comprising:

a substrate doped with a first impurity;

nano wires formed in stripes in the substrate with first and second impurity regions;

oxygen ion injection regions formed at a border between the substrate and the nano wires to separate the substrate and the nano wires; and

a first electrode that contacts the first impurity region and is formed on the substrate, and a second electrode that contacts the second impurity region and is formed on the substrate.

13. The nano wires of claim 12, wherein the substrate and the nano wires are made of silicon.

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