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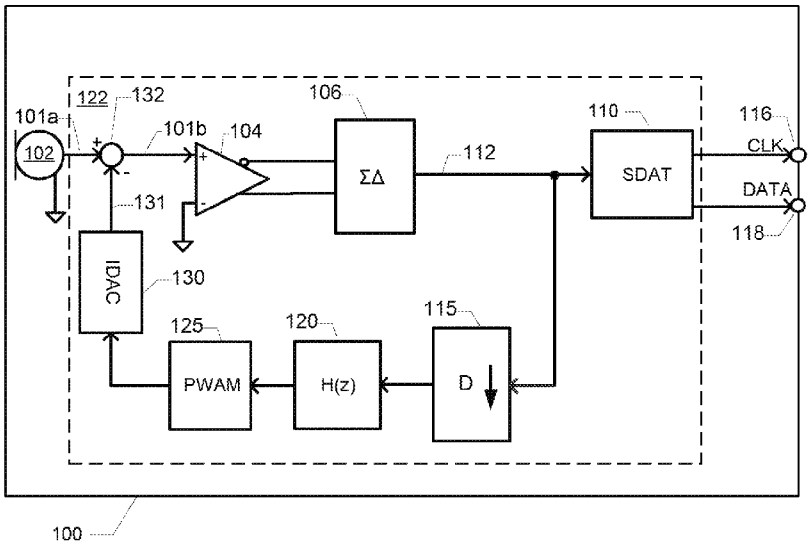


FIG. 2

(57) Abstract: A microphone assembly includes a transducer element and a processing circuit. The processing circuit includes an analog-to-digital converter (ADC) configured to receive, sample and quantize a microphone signal generated by the transducer element to generate a corresponding digital microphone signal. The processing circuit includes a feedback path including a digital loop filter configured to receive and filter the digital microphone signal to provide a first digital feedback signal and a digital-to-analog converter (DAC) configured to convert the first digital feedback signal into a corresponding analog feedback signal. The processing circuit additionally includes a summing node at the transducer output configured to combine the microphone signal and the analog feedback signal.

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MICROPHONE ASSEMBLY WITH DIGITAL FEEDBACK LOOP

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of and priority to U.S. Patent Application No. 15/202,404, filed July 5, 2016, the entire contents of which are incorporated herein by reference.

BACKGROUND

[0002] Portable communication and computing devices such as smartphones, mobile phones, tablets etc. are compact devices which are powered from rechargeable battery sources. The compact dimensions and battery source put severe constraints on the maximum acceptable dimensions and power consumption of microphones and microphone amplification circuit utilized in such portable communication devices.

[0003] US 2011/0051954 A1 discloses a signal conditioner for a capacitive transducer. The signal conditioner includes a differential preamplifier which includes a non-inverting input connected to a microphone transducer output and a separate inverting input connected to the output of a feedback path. The feedback path includes a digital-to-analogue converter and extends from an output of an analogue-to-digital converter to the inverting input of the preamplifier.

[0004] However, there exists a continued need to improve the sound quality and robustness of microphone assemblies for example by accurately controlling the frequency response and reducing or eliminating overload distortion of signal processing circuits like microphone preamplifiers at high sound pressure levels. The overload and distortion problems are often caused by saturation and non-linearity of active amplification elements like transistors of the signal processing circuits.

SUMMARY

[0005] A first aspect relates to a microphone assembly including a transducer element configured to convert sound into a microphone signal at a transducer output and a processing circuit. The processing circuit includes a preamplifier including an input node connected to the transducer output for receipt of the microphone signal, the preamplifier being configured

to generate at least one of an amplified microphone signal and a buffered microphone signal, and an analog-to-digital converter (ADC) configured to receive, sample and quantize the amplified or buffered microphone signal to generate a corresponding digital microphone signal. The processing circuit additionally includes a feedback path including a digital loop filter which includes an adjustable or fixed transfer function, the digital loop filter being configured to receive and filter the digital microphone signal to provide a first digital feedback signal and a digital-to-analog converter (DAC) configured to convert the first digital feedback signal into a corresponding analog feedback signal. The processing circuit additionally includes a summing node at the transducer output configured to combine the microphone signal and the analog feedback signal.

[0006] A second aspect relates to a method of controlling a frequency response of a signal amplification path of a microphone. The method includes a) converting incoming sound into a corresponding microphone signal at a microphone transducer output; b) sampling and quantizing the microphone signal by an analog-to-digital converter (ADC) to generate a corresponding digital microphone signal; c) lowpass filtering the digital microphone signal to provide a first digital feedback signal; d) converting the first digital feedback signal into a corresponding analog feedback signal by digital-to-analog converter (DAC); and e) combining the microphone signal and the analog feedback signal at the microphone transducer output to close a digital feedback loop.

[0007] The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the following drawings and the detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. These drawings depict only several embodiments in accordance with the disclosure and are, therefore, not to be considered limiting of its scope. Various embodiments are described in more detail below in connection with the appended drawings.

[0009] FIG. 1 is a schematic illustration of an exemplary miniature microphone assembly according to various embodiments.

[0010] FIG. 2 is a simplified electrical block diagram of a processing circuit of a miniature microphone assembly according to various embodiments.

[0011] FIG. 3 is a block diagram of a digital loop filter of a feedback loop or path according to various embodiments.

[0012] FIG. 4 is a simplified block diagram of a hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM) of a feedback loop or path of a processing circuit according to various embodiments.

[0013] FIG. 5 is a simplified block diagram of an exemplary embodiment of a noise-shaping up-sampler and quantizer.

[0014] FIG. 6 is a schematic block diagram of the operation of a modulator portion of a hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM) according to various embodiments.

[0015] FIG. 7 is a simplified schematic block diagram of an exemplary embodiment of a current output converter forming part of a current mode DAC of the processing circuit.

[0016] FIG. 8 is a simplified schematic block diagram of a controllable current generator and the exemplary current output converter operating in an idle state according to various embodiments.

[0017] FIG. 9A and 9B are simplified schematic block diagrams of a controllable current generator operating in first and second states, respectively, according to various embodiments.

[0018] FIG. 10 is a simplified schematic block diagram of an exemplary microphone preamplifier of a processing circuit.

[0019] In the following detailed description, various embodiments are described with reference to the appended drawings. The skilled person will understand that the accompanying drawings are schematic and simplified for clarity and therefore merely show details which are essential to the understanding of the present disclosure, while other details have been left out. Like reference numerals refer to like elements or components throughout. Like elements or components will therefore not necessarily be described in detail with respect

to each figure. It will further be appreciated that certain actions and/or steps may be described or depicted in a particular order of occurrence while those skilled in the art will understand that such specificity with respect to sequence is not actually required.

DETAILED DESCRIPTION

[0020] One aspect of the present disclosure relates to a microphone assembly including a transducer element and a processing circuit. The processing circuit includes an analog-to-digital converter (ADC) configured to receive, sample and quantize a microphone signal generated by the transducer element to generate a corresponding digital microphone signal. The processing circuit includes a feedback path including a digital loop filter configured to receiving and filtering the digital microphone signal to provide a first digital feedback signal and a digital-to-analog converter (DAC) configured for converting the first digital feedback signal into a corresponding analog feedback signal. The processing circuit additionally includes a summing node at the transducer output configured to combining the microphone signal and the analog feedback signal.

[0021] Another aspect relates to a microphone assembly including a transducer element configured to convert sound into a microphone signal at a transducer output and a processing circuit. The processing circuit includes a preamplifier including an input node connected to the transducer output for receipt of the microphone signal, the preamplifier being configured to generate at least one of an amplified microphone signal and a buffered microphone signal, and an analog-to-digital converter (ADC) configured to receive, sample and quantize the amplified or buffered microphone signal to generate a corresponding digital microphone signal. The processing circuit additionally includes a feedback path including a digital loop filter which includes an adjustable or fixed transfer function, the digital loop filter being configured to receive and filter the digital microphone signal to provide a first digital feedback signal and a digital-to-analog converter (DAC) configured to convert the first digital feedback signal into a corresponding analog feedback signal. The processing circuit additionally includes a summing node at the transducer output configured to combine the microphone signal and the analog feedback signal.

[0022] The transducer element may include a capacitive transducer element (e.g., a microelectromechanical system (MEMS) transducer) configured to convert incoming sound

into a corresponding microphone signal. The capacitive transducer element may for example exhibit a transducer capacitance between 0.5 pF and 10 pF. Some embodiments of the capacitive transducer element may include first and second mutually charged transducer plates, e.g. a diaphragm and back plate, respectively, supplying the microphone signal. The charge may be injected onto one of the diaphragm and back plate by an appropriate high-impedance DC bias voltage supply. The processing circuit may include a semiconductor die, for example a mixed-signal CMOS semiconductor device integrating the preamplifier, analog-to-digital converter, digital loop filter, digital-to-analog converter and optionally various other analog and digital circuits as discussed below.

[0023] The microphone assembly may be shaped and sized to fit into portable audio and communication devices such as smartphones, tablets and mobile phones, etc. The transducer element may be responsive to audible sound.

[0024] The analog-to-digital converter may be adapted to producing a multibit or single-bit digital microphone signal representative of the microphone signal depending on the particular converter type. Some embodiments of the analog-to-digital converter may include an oversampled converter type such as a single-bit or multibit sigma-delta converter ($\Sigma\Delta$) configured to generate a single-bit (PDM) or multibit digital microphone signal at a first sampling frequency. The multibit sigma-delta converter ($\Sigma\Delta$) may be configured to generate the multibit digital microphone signal with samples of two, three or four bits. The first sampling frequency may lie between 1 MHz and 20 MHz, such as between 2.048 MHz and 4.196 MHZ, for example 3.092 MHz. The feedback path may include a decimator arranged in-front of an input of the digital loop filter. The decimator is configured to convert the single-bit (PDM) or multibit digital microphone signal into a decimated multibit (PCM) microphone signal at a second sampling frequency. The second sampling frequency is lower than the previously discussed first sampling frequency. The second sampling frequency may be between 8 and 64 times lower than the first sampling frequency, e.g., accomplished by configuring the decimator with decimation factors between 8 and 64, such as 16 or 32. The samples of the decimated multibit (PCM) microphone signal may possess a higher number of bits, e.g., between 12 and 32 bits, or for example, 24 bits, than the samples of the single-bit or multibit digital microphone signal to retain high signal resolution through the feedback path despite the reduced sampling frequency. The skilled person will understand that the

preamplifier or buffer may be integrated within the analog-to-digital converter in some embodiments.

[0025] The digital-to-analog converter is configured to convert the first digital feedback signal into a corresponding analog feedback signal which is combined with the microphone signal at the transducer output such that a feedback loop is closed in-front of and around the microphone preamplifier. In some embodiments, the analog feedback signal and microphone signal may be summed by electrically connecting the transducer output and an output of the digital-to-analog converter. The application of the analog feedback signal to the transducer output of the transducer element leads to numerous advantages compared with prior art approaches. The coupling scheme effectively prevents low-frequency overload of the preamplifier or buffer which must receive and process the full dynamic range of the microphone signal generated by the transducer element without unacceptable distortion. This is accomplished by an anti-phase low-frequency component supplied by the analog feedback signal which cancels or suppresses low-frequency components of the microphone signal at the input node, or nodes, of the preamplifier or buffer. Hence, attenuating or supressing high level low-frequency components of the microphone signal at the input of the preamplifier or buffer. The high level low-frequency components of the microphone signal are caused by the exposure to intense subsonic or low-frequency sounds generated by wind noise, large machinery, etc. This suppression of high level low-frequency components of the microphone signal at the input of the preamplifier or buffer markedly reduces the maximum signal level of the microphone signal which the preamplifier or buffer must be able to handle in an undistorted manner. Hence, eliminating the vulnerability of the preamplifier or buffer to low-frequency induced overload and distortion.

[0026] The preamplifier may be a DC-coupled design or an AC-coupled design. The DC-coupled preamplifier or buffer possesses several advantageous properties over the AC-coupled design due to the elimination of resistors and capacitor of a traditional analog highpass filter used to set a highpass cut-off frequency of a forward microphone amplification path. The forward microphone amplification path may be extending from the transducer output to at least the analog-to-digital converter output. The elimination of the resistors and capacitors of the analog highpass filter at the preamplifier or buffer leads to a smaller semiconductor die area, reduced thermal noise and much improved flexibility in the choice of the highpass cut-off frequency of the forward microphone amplification path.

Instead, the highpass cut-off frequency of the forward microphone amplification path may be controlled or dominated by a lowpass cut-off frequency of the digital loop filter as discussed below. The frequency response of the digital loop filter, including its lowpass cut-off frequency, is inherently significantly more accurate than the frequency response of the traditional analog highpass filter, because resistors and capacitors of the analog highpass filter exhibit substantial manufacturing spread and drift over time and temperature making accurate frequency response control difficult, expensive or both.

[0027] The accurate frequency response setting of the forward microphone amplification path afforded by the properties of the digital loop filter also improves frequency response matching, inclusive phase matching, between individual microphone assemblies of a beamforming microphone array. This improved response matching leads to improved, predictable and stable directional response of the beamforming microphone array.

[0028] The digital-to-analog converter may exhibit a very large output impedance to supply the current of the analog feedback signal into a load including a high-impedance capacitive transducer element without causing undesirable attenuation and/or distortion of the microphone signal at the transducer output. In certain embodiments, the output impedance of the digital-to-analog converter 10 kHz may be larger than 1 MΩ, such as larger than 10 MΩ, or 100 MΩ.

[0029] The skilled person will understand that the analog feedback signal may be directly connected to the transducer output, e.g., at least one transducer plate of a capacitive transducer element. In that context, directly means through an electrically conductive path without any intervening active devices like transistors, but possibly through passive components like resistors, capacitors, electrical traces, wires, etc. This feature effectively prevents the above-mentioned overload and distortion problems of the preamplifier and buffer at high levels of the microphone signal caused by saturation and non-linearity of active amplification elements like transistors of the preamplifier or buffer circuitry. This low-frequency cut-off frequency may in practice be accurately controlled by a setting of the lowpass cut-off frequency of the digital loop filter as discussed above. The digital signal processing of the digital loop filter allows a very accurate and stable setting of the frequency response of the forward microphone amplification path, in particular in combination with the DC-coupled preamplifier or buffer as discussed above.

[0030] The digital loop filter may include a lowpass filter possessing a cut-off frequency placed at or above 10 Hz, for example at or above 50 Hz, 100 Hz or 1000 Hz. The lowpass filter may include a first, second or third order response characteristic. The skilled person will understand that the lowpass cut-off frequency of the digital loop filter may be selected such that a desired highpass cut-off frequency of the forward microphone amplification path is obtained. The latter highpass cut-off frequency may be situated between 10 Hz and 4000 Hz, such as between 100 Hz and 1 kHz, for various embodiments of the microphone assembly depending on requirements of a specific application. The digital loop filter may include an adjustable or programmable transfer function in certain embodiments of the processing circuit. The transfer function may be controlled by filter configuration data which may determine the previously discussed cut-off frequency of the lowpass filter. The filter configuration data may include respective values of one or more filter coefficients of the digital loop filter. The filter configuration data may be received by the processing circuit via an integrated command and control interface. The integrated command and control interface allows the microphone assembly to connect to a compatible data interface of the host processor and thereby receive the filter configuration data from the host processor. The programmable transfer function of the digital loop filter allows the microphone assembly to be tailored to requirements of a particular application in connection with, or after, manufacturing in a flexible manner and therefore serves to reduce the number of variants needed of the microphone assembly.

[0031] The processing circuit may include a digital processor implementing the functionality of the digital loop filter and/or other control functions of the processing circuit such as state switching of the digital-to-analog converter, controlling the operation of a command and control interface connectable to host processor of a portable communication device, e.g. a smartphone, etc. The digital processor may comprise a digital state machine and/or a software programmable microprocessor such as a digital signal processor (DSP).

[0032] According to some embodiments, the digital-to-analog converter (DAC) includes a hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM) configured to generate the analog feedback signal by converting the first digital feedback signal into a corresponding pulse-width and pulse-amplitude modulated signal at a higher sampling frequency than a sampling frequency of the first digital feedback signal. The pulse-width and pulse-amplitude modulated signal may include a sequence of variable width and amplitude current pulses

generated by a current output converter representative of the samples of the first digital feedback signal. Hence, one embodiment of the hybrid Pulse-Width and Pulse-Amplitude Modulator includes a current output converter configured for converting the pulse-width and pulse-amplitude modulated signal into a corresponding sequence of variable width and amplitude current pulses. The current output converter includes a plurality of individually controllable current generators connected in parallel to the DAC output. The current output converter may include between 8 and 32 individually controllable current generators connected in parallel to the DAC output. The skilled person will understand that the capacitance of the capacitive transducer element at the transducer output effectively lowpass filters or smooths the variable width and amplitude current pulses that may be supplied by the output of the hybrid Pulse-Width and Pulse-Amplitude Modulator to suppress or eliminate undesired high frequency components in the analog feedback signal. In the above-mentioned current output converter each of the plurality of individually controllable current generators may include a first current source connected between a positive DC supply rail of the current output converter and the DAC output for sourcing a first current level to the DAC output; and a second current source connected between the DAC output and a negative DC supply rail of the current output converter for sinking a second current level from the DAC output. The individually controllable current generator may furthermore include a DC error suppression circuit configured for matching the first and second current levels. The matching or equalization of the first and second current levels by the operation of the DC error suppression circuit has several noticeable advantages, for example, leading to a linear I/O characteristic of the current output converter. The DC error suppression circuit also prevents the build-up of DC voltage components on the load which is a noticeable advantage in connection with driving capacitive transducer elements where DC off-sets or DC imbalances of the output signal at the DAC output will tend to drive a DC operating point of the capacitive transducer element away from a target DC operating point as discussed in further detail below with reference to the appended drawings.

[0033] Some embodiments of the hybrid Pulse-Width-Modulator and Pulse-Amplitude-Modulator may include a noise-shaping quantizer configured to receive samples, having a first bit-width, of the first digital feedback signal outputted by the digital loop filter; and quantize the samples of the first digital feedback signal to generate samples of a second digital feedback signal with a reduced bit-width. The noise-shaping quantizer may quantize samples of an incoming digital signal to fewer bits, e.g., samples with reduced bit-width. The

noise-shaping quantizer may for example quantize samples of the first digital feedback signal from e.g., 32 bits or 24 bits down to less than 16 bits, or less than 12 bits, such as 11 bits. The noise-shaping quantizer is configured to shape a spectrum of the quantization noise generated by the quantization process to reduce its audibility. Hence, the quantization noise may be pushed upwards in frequency above the audible range, for example above 20 kHz. The first digital feedback signal may have a sampling frequency at or above 48 kHz, for example above 96 kHz, such as 192 kHz or 384 kHz. The second digital feedback signal may subsequently be converted into the pulse-width and pulse-amplitude modulated signal as discussed in further detail below with reference to the appended drawings.

[0034] The hybrid Pulse-Width and Pulse-Amplitude Modulator is capable of generating the analog feedback signal with a high resolution at a relatively low conversion frequency as discussed in further detail below with reference to the appended drawings. The skilled person will understand that alternative embodiments of the hybrid Pulse-Width and Pulse-Amplitude Modulator may lack the current output converter and instead exhibit a relatively small output impedance supplying the pulse-width and pulse-amplitude modulated signal as a sequence of variable width and amplitude voltage pulses. The hybrid Pulse-Width and Pulse-Amplitude Modulator disclosed herein may be exploited for conversion of digital signals into corresponding analog signals in a variety of other applications than the microphone assembly described herein.

[0035] The skilled person will also understand that the current output converter described herein can be utilized for DC error-free conversion of a digital signal to an analog signal in numerous other applications than the hybrid Pulse-Width and Pulse-Amplitude Modulator described herein.

[0036] Further aspects of the present disclosure relate to a method of controlling a frequency response of a signal amplification path of a microphone. The method includes a) converting incoming sound into a corresponding microphone signal at a microphone transducer output; b) sampling and quantizing the microphone signal by an analog-to-digital converter (ADC) to generate a corresponding digital microphone signal; c) lowpass filtering the digital microphone signal to provide a first digital feedback signal; d) converting the first digital feedback signal into a corresponding analog feedback signal by digital-to-analog converter (DAC); and e) combining the microphone signal and the analog feedback signal at the microphone transducer output to close a digital feedback loop.

[0037] The methodology may further include f) applying the analog feedback signal to a capacitive transducer element for example applying the analog feedback signal to at least one transducer plate of a capacitive microelectromechanical (MEMS) transducer element supplying the microphone signal. The application of the analog feedback signal of the capacitive transducer element allows accurate control of the frequency response of the forward microphone amplification path for the reasons discussed in considerable detail above.

[0038] The method of controlling the frequency response of the signal amplification path may further include g) quantizing and noise shaping the first digital feedback signal to generate a second digital feedback signal with a smaller bit-width than a bit-width of the first digital feedback signal.

[0039] The bit-width of the first digital feedback signal may be larger than 20 bits, such as 24 bits, while the bit-width of the second digital feedback signal may be less than 16 bits, such as 11 bits, e.g., 10 bits magnitude representation and one sign bit, as discussed in further detail below with reference to the appended drawings.

[0040] The method of controlling the frequency response of the signal amplification path may further include increasing a sampling frequency of the second digital feedback signal with a predetermined upsampling factor, N, to generate a third digital feedback signal; and converting the third digital feedback signal into a pulse-width and pulse-amplitude modulated signal.

[0041] The skilled person will understand that the above conversion of the third digital feedback signal may include h) dividing a first sample of the third digital feedback signal with the predetermined upsampling factor, N, to compute a modulus value and remainder value of the first sample; i) converting the modulus value of the first sample into a first pulse segment having a combined pulse width and pulse amplitude representative of the modulus value; j) converting each remainder value of the first sample into a second pulse segment with a pulse width representing the remainder value; k) combining the first and second pulse segments of the first sample to form a first variable width and amplitude pulse; and l) repeating steps h) – k) for subsequent samples of the third digital feedback signal to generate the pulse-width and pulse-amplitude modulated signal by a sequence of variable width and amplitude pulses. Hence, the sequence of variable width and amplitude pulses are

representative of the samples of the third digital feedback signal as discussed in further detail below with reference to the appended drawings.

[0042] Further aspects of the present disclosure relate to a semiconductor die including a processing circuit according to any of the above-described embodiments thereof. The processing circuit may include a CMOS semiconductor die. The processing circuit may be shaped and sized for integration into a miniature microphone housing or package. The microphone assembly may therefore include a microphone housing enclosing and supporting the transducer element and the processing circuit. A bottom portion of the microphone housing may include a carrier board, such as a printed circuit board, onto which the processing circuit and the transducer element are attached or fixed by a suitable bonding mechanism. The microphone housing may include a sound port or inlet allowing sound passage to the transducer element as discussed in further detail below with reference to the appended drawings.

[0043] Further aspects of the present disclosure relate to a portable communication device including a microphone assembly according to any of the above-described embodiments thereof. The portable communication device may include an application processor, e.g., a microprocessor such as a Digital Signal Processor. The application processor may include a data communication interface compliant with, and connected to, an externally accessible data communication interface of the microphone assembly. The data communication interface may include a proprietary interface or a standardized data interface, such as one of I^2C, USB, UART, SoundWire or SPI compliant data communication interfaces. Various types of configuration data of the processing circuit, for example for programming or adapting characteristics of the digital loop filter, may be transmitted from the application processor to the microphone assembly, as discussed in further detail below with reference to the appended drawings.

[0044] In some embodiments, the present microphone assembly may form part of a portable communication device such as a smartphone where one, two, three or more microphone assemblies may be integrated for picking-up and processing various types of acoustic signals such as speech and music. Some exemplary embodiments of the present approaches, microphone assemblies and methodologies may be tuned or adapted to different types of applications through configurable parameters as discussed in further detail below. These parameters may be loaded into suitable memory cells of the microphone assembly on

request via the configuration data discussed above, for example, using the previously mentioned command and control interface. The latter may include a standardized data communication interface such as SoundWire, I2C, UART and SPI.

[0045] FIG. 1 shows an exemplary embodiment of a microphone assembly or system 100. The microphone assembly 100 includes a capacitive transducer element 102, e.g. a microelectromechanical system (MEMS) transducer, configured to convert incoming sound into a corresponding microphone signal. The transducer element 102 may, for example, exhibit a transducer capacitance between 0.5 pF and 10 pF. The capacitive transducer element may include first and second mutually charged transducer plates, e.g. a diaphragm and back plate, respectively, supplying the microphone signal. The charge may be injected onto one of the diaphragm and back plates by an appropriate high-impedance DC bias voltage supply (not shown). The microphone assembly 100 additionally includes a processing circuit 122, which may include a semiconductor die, for example a mixed-signal CMOS semiconductor device integrating the various analog and digital circuits discussed below. The processing circuit 122 is shaped and sized for mounting on a substrate or carrier element 111 of the assembly 100, where the carrier element likewise supports the capacitive transducer element 102. The microphone assembly 100 includes a housing lid 103 mounted onto a peripheral edge of the substrate or carrier element 111 such that the housing lid 103 and carrier element 111 jointly form a microphone housing enclosing and protecting the transducer element 102 and the processing circuit 105 of the assembly 100. The microphone housing may include a sound inlet or sound port 109 projecting through the carrier element 111, or through the housing lid 103 in other embodiments, for conveying sound waves to the transducer element 102.

[0046] The transducer element 102 generates a microphone signal at a transducer output (item 101a of FIG. 2) in response to impinging sound. The transducer output may for example include a pad or terminal of the element 102 that is electrically coupled to the processing circuit 122 via one or more bonding wires 107 electrically interconnecting respective signal pads of the transducer element 102 and processing circuit 122.

[0047] FIG. 2 shows a simplified electrical block diagram of an exemplary embodiment of the processing circuit 122 of the miniature microphone assembly 100. The processing circuit 122 includes a preamplifier or buffer 104 having an input node or terminal 101b connected to the transducer output 101a of the transducer element 102 for receipt of the microphone signal

produced by the transducer element 102. The output of the preamplifier 104 supplies an amplified and/or buffered microphone signal to an analog-to-digital converter 106, which is configured for receipt, sampling and quantization of the amplified or buffered microphone signal to generate a corresponding digital microphone signal. The analog-to-digital converter 106 may be adapted to produce a multibit or single-bit digital microphone signal representative of the microphone signal depending on the particular converter type. Some embodiments of the analog-to-digital converter 106 includes a sigma-delta converter ($\Sigma\Delta$) configured to generate a single-bit (PDM) digital microphone signal at a first sampling frequency. The first sampling frequency may lie between 2 MHz and 20 MHz such as 3.092 MHz. The skilled person will understand that the preamplifier 104 may be integrated with the analog-to-digital converter 106 in other embodiments.

[0048] The digital microphone signal is transmitted to an input of a command and control interface 110 configured to receive various types of data commands and filter configuration data for a programmable digital loop filter 120 from a host processor (now shown) of a portable communication device (e.g. a smartphone). The command/control interface 110 may include a separate clock line 116 (CLK) that clocks data on a data line 118 (DATA) of the interface 110. The command and control interface 110 may include a standardized data communication interface according to various serial data communication protocols, e.g., I^2C, USB, UART, SoundWire or SPI. The command and control interface 110 is configured to structure and encode the digital microphone signal in accordance with the relevant protocol of the interface 110 and transmits the digital microphone signal to the host processor. The microphone assembly 100 may be configured to receive and utilize various types of configuration data transmitted by the host processor. The configuration data may include data concerning a configuration of the processing circuit 122 such as filter coefficients of the digital loop filter 120.

[0049] The processing circuit 122 includes a feedback path extending at least from the digital microphone signal at the output 112 of the analog-to-digital converter 106 and back to the transducer output 101a, or microphone preamplifier input node 101b, since these nodes are electrically connected. The feedback path supplies an analog feedback signal to the summing node 132 at the transducer output 101a such that the path may be operative to set a highpass cut-off frequency of the frequency response of the forward microphone amplification path from the transducer output to the output 112 of the analog-to-digital

converter 106. This highpass cut-off frequency may in practice be accurately controlled by a setting of a lowpass cut-off frequency of the digital loop filter 120 discussed above. The digital loop filter may via its digital processing nature exhibit a very accurate and stable frequency response setting in contrast to frequency response settings of conventional analog filters which rely on values of components like capacitors and resistors to determine the frequency response. Components like capacitors and resistors exhibit substantial manufacturing spread of component values and drift over time and temperature such that the frequency response setting of conventional analog filters are less accurate and stable than desired.

[0050] If the analog-to-digital converter 106 produces a digital microphone signal in the form of a single-bit (PDM) digital microphone signal or a multibit digital microphone signal with 2-4 bits, the digital feedback loop of the processing circuit 122 may include a decimator 115 arranged in-front of, e.g., at the input of, the digital loop filter 120. This decimator 115 is configured to convert the single-bit (PDM) or multibit digital microphone signal into a decimated multibit (PCM) feedback signal at a second sampling frequency. The second sampling frequency is lower than the first sampling frequency, which may lie between 2 MHz and 20 MHz, of the single-bit (PDM) digital microphone signal as discussed above. The second sampling frequency may be between 8 and 64 times lower than the first sampling frequency, e.g. accomplished by configuring the decimator 115 with decimation factors between 8 and 64, such as 16 or 32. The samples of the decimated multibit feedback signal may include between 16 and 32 bits to maintain a high signal resolution in the digital feedback path. This decimation and associated lowpass filtering of the single-bit (PDM) digital microphone signal may be helpful to suppress high-frequency noise components of the single-bit (PDM) digital microphone signal. The decimated multibit feedback signal is applied to an input of the digital loop filter 120 which filters the signal in accordance with an adjustable or fixed transfer function, such as the previously discussed lowpass frequency response, of the filter 120 to in response generate a first digital feedback signal at a filter output. Exemplary topologies and transfer functions of the digital loop filter 120 are discussed in detail below.

[0051] The first digital feedback signal supplied by the digital loop filter 120 is applied to a digital-to-analog converter (DAC) of the digital feedback loop. The DAC includes a hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM) 125 connected in series with a

current output converter (IDAC) 130. The DAC is configured to convert the first digital feedback signal into a corresponding analog feedback signal, which is applied to the microphone preamplifier input node 101b. The latter node 101b is connected to the transducer output 101a as discussed herein, thereby closing the digital feedback loop. The skilled person will understand that the transducer output may be an extremely high impedance circuit node, e.g. an impedance corresponding to a capacitance of 0.5 pF to 10 pF, of a miniature capacitive transducer element. This property of the transducer output, and the design and electrical properties, in particular output impedance, of the current output converter 130 are discussed in further detail below with reference to the schematic diagram of the converter 130. The application of the analog feedback signal to the transducer output of the miniature capacitive transducer element 102 leads to numerous advantages compared with prior art approaches. The direct coupling of the analog feedback signal to the transducer output effectively prevents low-frequency overload of the preamplifier or buffer 104 and/or the converter 106. This is accomplished by the lowpass filtering of the analog feedback signal carried out by the digital loop filter 120, which lowpass filtering cancels or suppresses low-frequency components of the microphone signal at the input node 101b, or input nodes, of the preamplifier or buffer 104. Furthermore, the noise floor of the microphone assembly 100 may be lowered by tailoring a frequency response of the miniature capacitive transducer element 102 to the accurate frequency response of the forward microphone amplification path. Furthermore, the accurate control over the frequency response of the forward microphone amplification path improves frequency response matching, including phase matching, between individual microphone assemblies of a beamforming microphone array which may include 2, 3 or more microphone assemblies. This improved response matching leads to improved, predictable and stable directional response of the beamforming microphone array.

[0052] The upper portion of FIG. 3 shows a block diagram of an exemplary embodiment of the previously discussed digital loop filter 120 of the digital feedback loop or path of the processing circuit 122. The digital loop filter 120 has second order lowpass filter characteristics using a classical IIR filter bi-quad topology. The skilled person will understand that other digital filter types and topologies, such as FIR filters or other types of IIR filter topologies, may be utilized in alternative embodiments of the digital loop filter 120. Likewise, other filter orders may be used. The transfer function of the illustrated digital loop filter 120 is determined by values of the filter coefficients which include: a1, a2, b0, b1 and b2. The frequency response graph 300 of the lower portion of FIG. 3 shows an exemplary

magnitude response 310 of the digital loop filter 120 where the lowpass cut-off frequency has been tuned to about 200 Hz. The corresponding magnitude response 305 of the forward microphone amplification path for this particular setting of the response 310 of the digital loop filter is also plotted. The skilled person will notice the expected 2nd order highpass magnitude response of the forward microphone amplification path. The highpass cut-off frequency is set to approximately 30 Hz. The skilled person will understand that the lowpass cut-off frequency of the digital loop filter 120 may be adjusted over a broad frequency range to obtain a desired highpass cut-off frequency of the forward microphone amplification path. The latter highpass cut-off frequency may be situated in the frequency range between 10 Hz and 200 Hz for various embodiments of the microphone assembly depending on requirements of a specific application.

[0053] The skilled person will understand that certain embodiments of the processing circuit 122 may include an adjustable or programmable transfer function of the digital loop filter 120 where the transfer function is controlled by filter configuration data. The filter configuration data may include respective values of one or more of the previously discussed filter coefficients a1, a2, b0, b1 and b2. The filter configuration data may be received by the processing circuit 122 via the previously discussed command and control interface 110 from a host processor. The programmable transfer function of the digital loop filter 120 allows the microphone assembly to be tailored to requirements of a particular application after manufacturing in a flexible manner and therefore reduces the number of variants needed of the microphone assembly.

[0054] Other types of configuration data for various circuits and functions of the processing circuit 122 may likewise be programmed through the command and control interface 110. The configuration data, including filter configuration data, may be stored in rewriteable memory cells (not shown) of the processing circuit, such as flash memory, EEPROM, RAM, register files or flip-flops. These rewriteable memory cells may hold or store certain default values of the filter configuration data.

[0055] FIG. 4 shows a simplified block diagram of an exemplary embodiment of the previously discussed hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM) 125 of the feedback path of the processing circuit. The output of the digital loop filter 120 is connected to the input of the PWAM 125 such that the previously discussed first digital feedback signal is applied to the input of the PWAM 125. The first digital feedback signal

may be a multibit signal with a relatively high resolution - for example between 16 and 32 bits per sample, such as 24 bits per sample, to maintain a high signal resolution through the feedback path. The sampling frequency of the first digital feedback signal may lie between 32 kHz and 384 kHz, for example between 96 kHz and 192 kHz. The PWAM 125 includes a noise-shaping up-sampler and quantizer 410 at the input receiving the first digital feedback signal. The noise-shaping up-sampler and quantizer 410 raises the sampling frequency of the first digital feedback signal with a pre-set or programmable ratio - for example an integer ratio between 2 and 16 to generate a second digital feedback signal 415 at a second sampling frequency. The noise-shaping up-sampler and quantizer 410 is furthermore configured to quantize samples of the second digital feedback signal to a smaller number of bits than the samples of the first digital feedback signal. According to one exemplary embodiment of the quantizer 410 the samples of the first digital feedback signal has 24 bits per sample while the samples of the second digital feedback signal have been decimated to 11 bits. These samples may be generated according to a signed sample format where a sign bit takes one bit and a magnitude portion is represented by the residual 10 bits of the sample.

[0056] FIG. 5 shows a simplified block diagram of the noise-shaping up-sampler and quantizer 410 of the PWAM 125. The first digital feedback signal is represented by X(z) and the second digital feedback signal by X(z) + E(z), where E(z) represents a quantization noise component caused by the quantization operation carried out by the quantizer 504. The noise-shaping up-sampler and quantizer 410 includes a noise-shaping feedback loop extending through loop filter Hn(z) 506 to a second adder 510 on the input side, which adder shapes the spectrum of the generated quantization noise to higher frequencies and therefore maintains a relatively high resolution of the second digital feedback signal throughout the audio frequency range despite the quantization. The noise-shaping up-sampler and quantizer 410 may include a feedforward loop as illustrated extending to an output side summer 512. The noise-shaping up-sampler and quantizer 410 may also include the illustrated Dither generator 502, which adds a pseudo-random noise signal of appropriate level to the first digital feedback signal at the input of the noise-shaping up-sampler and quantizer 410 using a first input side adder 508. This pseudo-random noise signal may reduce audible artefacts associated with the quantization operation in a well-known manner.

[0057] Referring further to FIG. 4, the PWAM 125 additionally includes a modulator 420 connected to the output of the noise-shaping up-sampler and quantizer 410 for receipt of the

second digital feedback signal X(z)+E(z). The operation and functionality of an exemplary embodiment of the modulator 420 is schematically illustrated in FIG. 6. The modulator 420 takes the second feedback digital signal in the multibit (PCM) format and converts the second feedback digital signal into a pulse-width and pulse-amplitude modulated signal. The sampling frequency of this pulse-width and pulse-amplitude modulated signal may be markedly higher than the sampling frequency of the second digital feedback signal as discussed below. The sampling frequency of the pulse-width and pulse-amplitude modulated signal 425 may be at least 16 times higher than the sampling frequency of the second digital feedback signal, such as 32 or 64 times higher. One embodiment of the modulator 420 accepts a 192 kHz sampling frequency of the second digital feedback signal and generates a corresponding pulse-width and pulse-amplitude modulated signal at a sampling frequency of 12.288 MHz, and hence raises the sampling frequency of the latter by an upsampling factor of 64. The pulse-width and pulse-amplitude modulated signal 425 may be applied to a current converter control circuit or block 430 – (see, e.g., FIG. 4). The current converter control circuit 430 is configured to convert or transform the pulse-width and pulse-amplitude modulated signal into a corresponding sequence of variable width and amplitude current pulses at the output of the previously discussed current output converter (IDAC) 130 by controlling how individually controllable current generators (illustrated in FIGS. 7 and 8) are activated. The current converter control circuit 430 may include an appropriately configured digital state machine. One embodiment of the current converter control circuit 430 may include a dynamic element matching circuit 432 as schematically illustrated where the selection of individually controllable current generators of the current output converter is carried out in a randomized manner to average out offsets between nominally identical current generators.

[0058] Referring to FIG. 6, the second digital feedback signal X(z)+E(z) is applied to the input of the modulator 420 and the sampling frequency raised with a predetermined ratio, N, such as 64. In the present embodiment, the resolution of the second digital feedback signal is 11 bits as discussed previously. A dividing block or circuit 603 divides each 11 bits sample of the second digital feedback signal with N to compute respective modulus values and remainder values of the samples. The drawing shows four exemplary values, 138, 40, 522 and 276 using decimal notation, of the 11 bit samples of the second digital feedback signal expressed in decimal format initially. The decimal sample value 138 is divided by 64 producing a modulus value of 2 and a remainder value of 10 as illustrated. The corresponding

computation is also illustrated for the three remaining samples 40, 522 and 276. The decimal sample value 138 is converted into binary format showing how the modulus value 2 corresponds to 00010b and the remainder value of 10 corresponds to 001010b. A first variable width and amplitude pulse 610 of the pulse-width and pulse-amplitude modulated signal is generated by conversion of the decimal sample value 138. The first variable width and amplitude pulse 610 is essentially constructed from two segments. A first pulse segment (2*64) has an amplitude of "2" (y-axis scale) spanning over a full pulse width, i.e. 100 % modulation and pulse amplitude of 2 – hence representing the modulus value "2." The first variable width and amplitude pulse 610 additionally includes a second pulse segment (1*10) spanning over merely 10 sample time clocks of the 12.288 MHz sampling frequency of the pulse-width and pulse-amplitude modulated signal. Stated in another way, the decimal sample value 138 is converted into an "analog" variable width and amplitude pulse with a corresponding pulse area.

[0059] The conversion of the decimal sample value 40 into the second variable width and amplitude pulse 620 is also illustrated. The decimal sample value 40 leads to a modulus value of 0 and a remainder value of 40 as illustrated. The corresponding, second, variable width and amplitude pulse 620 reflects this outcome by merely including a second pulse segment (1*40) with a "one" amplitude and spanning over merely 40 sample time clocks of the 12.288 MHz sampling frequency of the pulse-width and pulse-amplitude modulated signal. The conversion of the decimal sample value 522 into a third variable width and amplitude pulse 630 is finally illustrated using the same principles outlined above. The skilled person will understand that the modulator 420 is configured to convert incoming sample values into corresponding sequences of variable width and amplitude pulses where the pulse area of each of the variable width and amplitude pulses 610, 620, 630 represents the sample value in question. Hence, each of the variable width and amplitude pulses 610, 620, 630 can be viewed as an analog representation of the sample value in question.

[0060] The skilled person will understand that the modulator 420 may be configured to generate the variable width and amplitude pulses following different modulation schemes. In the present embodiment, each of the variable width and amplitude pulses is preferably centred at a midpoint of the pulse period, e.g., centered at the sample clock time 32 in this embodiment using an upsampling factor of 64. This centering is often referred to as a double-

edge pulse-width modulation. However, other embodiments of the modulator 420 may be adapted to build the variable width and amplitude pulses by applying single-edge modulation.

[0061] FIG. 7 shows a simplified schematic block diagram of an exemplary embodiment of the current output converter 130 forming part of the current mode DAC of the processing circuit. The current output converter 130 includes a predetermined number, N, of individually controllable current generators IDAC1, IDAC2, IDAC3, IDACN, for example between 4 and 32 current generators, such as 16 current generators. The respective outputs of the N individually controllable current generators are connected in parallel to a common DAC output node 131. A capacitive transducer element 702 is connected to the common DAC output node 131. The skilled person will understand that the capacitive transducer element 702 may include the previously discussed capacitive transducer element 102 of a miniature microphone assembly for sound reproduction. However, other types of capacitive transducer elements for sensing of various types of physical variables may in the alternative be driven by the present current mode DAC 702. The N individually controllable current generators IDAC1, IDAC2, IDAC3, IDACN may be nominally identical, but the skilled person will understand that component variations associated with semiconductor manufacturing may cause minor variations of characteristics between the controllable current generators, in particular current sinking and sourcing capabilities. Each of the N individually controllable current generators IDAC1, IDAC2, IDAC3, IDACN is configured to selectively source current into the capacitive transducer element 702 or sink current from the capacitive transducer element 702 in accordance with the switching control carried out by the current converter control circuit 430, and thereby charge or discharge voltage across the element 702. Each of the N individually controllable current generators IDAC1, IDAC2, IDAC3, IDACN can be considered a one-bit or 1.5 bit binary values +1 or -1. The sourcing and sinking of the predetermined current amount or level may be carried out by selecting between a first state and second state of the controllable current generator. Finally, each of the individually controllable current generators may include a third state or an idle/zero output state where the current generator neither sources nor sinks current to/from its output. In this idle state, the current generator may be placed in a high-impedance mode effectively disconnecting the current generator from the common DAC output 131 as discussed in further detail below. The skilled person will appreciate that the maximum positive output value of the current converter may correspond to setting all N individually controllable current generators IDAC1, IDAC2, IDAC3, IDACN to source current while the maximum negative output value corresponds to

setting all N individually controllable current generators IDAC1, IDAC2, IDAC3, IDACN to sink current.

[0062] FIG. 8 is a simplified schematic block diagram of the controllable current generator IDACN of the current output converter 130 when placed in the idle state or off-state discussed above. The controllable current generator IDACN includes a first current source 802 and a second current source 804 connected in series between the positive DC supply rail VDD and a negative DC supply rail which is ground (GND) in the present embodiment. A first switch pair, including switches SW2 and SW5, is coupled in-between the first and second current sources 802, 804 and is operating in a synchronized manner where both switches are simultaneously closed/conducting or open/non-conducting. The switches of the first switch pair SW2 and SW5 are closed in the idle state while the residual SW1, SW3, SW4 and SW6 are placed in open/non-conducting states as illustrated. This means that the current flowing through the first current source 802 and second current source 804 runs directly from VDD to GND as illustrated by the current path 810. Consequently, each of the first and second current sources 802, 804 is electrically disconnected from the output node 831 and the controllable current generator IDACN does therefore not source or sink any noticeable current to the capacitive transducer element 702 when placed in the idle state.

[0063] The controllable current generator IDACN additionally includes a DC voltage reference 806 connected to an inverting input of a differential loop amplifier 808, e.g. an operational amplifier or other differential amplifier, of a feedback regulation loop of the IDACN. The voltage of the DC voltage reference 806 may be equal to one-half VDD. The differential loop amplifier 808 has a non-inverting input (+) connected to a midpoint node 812 arranged in-between the first switch pair SW2, SW5. An output of the differential loop amplifier 808 is connected to a control input 805 of the second current source 804 where the control input 805 is configured to adjust the current level of the second current source 804. The operation of the differential loop amplifier 808 therefore seeks to dynamically or adaptively adjust the voltage at the midpoint node 812 to approximately one-half VDD, which is the voltage set at the negative input of the differential loop amplifier 808, by adjusting the current flowing through second current source 804 via the control input 805. This adaptive adjustment of the voltage at the midpoint node 812 is carried out by a feedback regulation loop. Hence, the differential loop amplifier 808, the second current source 804 and the DC voltage reference 806 therefore jointly form a DC error suppression circuit which is

configured to match or align the first and second current levels supplied by the first and second current sources 802, 804 during the idle state of the controllable current generator IDACN. In certain embodiments, the differential loop amplifier 808 may possess a relatively small bandwidth, or large time constant, compared to the sampling frequency of the incoming pulse-width and pulse-amplitude modulated signal. The upper cut-off frequency of the differential loop amplifier 808 may, for example, be smaller than 100 kHz, or smaller than 40 kHz, which effectively performs a slow averaging of the current source balancing to secure a long-term zero DC offset at the output of each of the controllable current generators.

[0064] This property has several noticeable advantages, for example leading to a linear I/O characteristic of the current output converter 130. The DC error suppression circuit also prevents build-up of DC voltage components on the load, which is a noticeable advantage in connection with driving capacitive transducer elements where DC off-sets or DC imbalances of the analog feedback signal will tend to drive the DC operating point of the capacitive transducer element away from a target DC operating point. This potential build-up of DC off-set is caused by the charge integration carried out by the capacitance of the capacitive transducer element. The controllable current generator IDACN is operating in the previously discussed idle state where the output node 831 is in a high-impedance state supplying substantially zero current output. Each of the switches SW1, SW2, SW3, SW4, SW5 and SW6 may include a controllable semiconductor switch for example a MOSFET. Each of the switches SW1, SW2, SW3, SW4, SW5 and SW6 may include a control terminal, for example a gate terminal of a MOSFET, which switches the controllable semiconductor switch between its conducting and non-conducting states. These control terminals are connected to the previously discussed current converter control circuit 430. The current level supplied by the first and second current sources 802, 804 may vary depending on requirements of a particular application such as a load impedance, e.g. the capacitance of the capacitive transducer element 702 in the present embodiment, the sampling frequency of the pulse-width and pulse-amplitude modulated signal, the number of parallel connected controllable current generators of the current output converter 130, etc. In one exemplary embodiment of the current output converter 130 comprising 16 controllable current generators, the respective currents of the first and second current sources 802, 804 are set to about 100 pA, e.g. between 50 pA and 200 pA, when configured for driving a 1-4 pF capacitive transducer element. The current settings of the controllable current generators generally depend on a dv/dt at the peak amplitude of the analog feedback signal at the highest frequency of interest of the feedback

loop. The currents of the controllable current generators should preferably be capable of charging the capacitance of the capacitive transducer element 102 without slew-induced distortion under these conditions. The highest frequency of interest of the analog feedback signal may lie between 300 Hz and 3 kHz, for example about 1 kHz, in exemplary embodiments of the microphone assembly 100.

[0065] An output impedance at10 kHz of each of the individually controllable current generators IDAC1, IDAC2, IDAC3, IDACN is in some embodiments preferably larger than 1 MΩ, such as larger than 10 MΩ or 100 MΩ, when operating in either the first state or the second state.

[0066] FIG. 9A is a simplified schematic block diagram of the controllable current generator IDACN of the current output converter 130 when placed in the first state, or + 1 state, discussed above where the output 831 is sourcing the predetermined current level to the capacitive transducer element 702 or other load circuit. In the first state, the switches of the first switch pair SW2 and SW5 are open or non-conducting and the switches SW1 and SW6 are both open or non-conducting as illustrated. The residual switches SW4 and SW3 are in contrast placed in conducting or closed states as illustrated. This combination of switch states means that the current flowing through the first current source 802 is sourced into the capacitive transducer element 702 via current path 810a while the current generated by the second current source 804 runs from the DC voltage reference 806, which may be equal to one-half VDD, directly to GND via the current path 810b. Consequently, the controllable current generator IDACN sources the predetermined current level to the capacitive transducer element 702 when placed in the first state. The skilled person will understand that the DC balancing of the current levels of the first current source 802 and the second current source 804 is still maintained by the operation of the previously discussed DC error suppression circuit.

[0067] FIG. 9B is a simplified schematic block diagram of the controllable current generator IDACN of the current output converter 130 when placed in the second state, or - 1 state, discussed above where the output 831 is sinking the predetermined current level from the capacitive transducer element 702 or other load circuit to discharge the load circuit. In the second state, the switches of the first switch pair SW2 and SW5 are open or non-conducting and the switches SW4 and SW3 are both open or non-conducting as illustrated. The residual switches SW1 and SW6 are in contrast placed in conducting or closed states as illustrated.

This combination of switch states means that the current flowing through the first current source 802 is sourced into the DC voltage reference 806 and thereafter to GND via the current path 880a. In contrast, the predetermined current generated by the second current source 804 is drawn out of the capacitive transducer element 702 via current path 880b to discharge the capacitive transducer element 702. Consequently, the controllable current generator IDACN sinks the predetermined current level from the capacitive transducer element 702 when placed in the second state. The skilled person will understand that the DC balancing of the current levels of the first current source 802 and the second current source 804 is still maintained by the operation of the previously discussed DC error suppression circuit.

[0068] The skilled person will understand that above outlined switch arrangement and associated switching scheme of the switches SW1, SW2, SW3, SW4, SW5 and SW6 through the first, second and third states of each of the controllable current generators allow the first and second current sources to operate in an unswitched manner even during time periods where they do not source or sink current to the load circuit. Instead, the superfluous current of a particular current generator is directed through the DC voltage reference 806 by selecting an appropriate setting of the switches. This feature eliminates switching noise for example caused by charge injection from repetitious switching of the first and second current sources when cycling through the first, second and third states.

[0069] FIG. 10 is a simplified schematic block diagram of an exemplary AC-coupled microphone preamplifier 104 suitable for use in the processing circuit to interface to the transducer element at the input side and to a differential input of the previously discussed analog-to-digital converter 106 at the output side. The skilled person will understand that other embodiments of the processing circuit may include a DC-coupled preamplifier to achieve the previously discussed advantages.

[0070] The microphone preamplifier 104 includes a unity gain buffer stage 1001 coupled in series with an AC-coupled gain stage 1003. The input voltage Vin to the unity gain buffer stage 1001 includes the microphone signal supplied via the previously discussed (See, e.g., FIG. 2) input node 101b connected to the transducer output 101a of the transducer element 102. The unity gain buffer stage 1001 is single-ended in the present embodiment and delivers a buffered microphone signal or voltage to the input 1005 of the AC-coupled gain stage 1003. The small signal gain of the AC-coupled gain stage 1003 to a positive output at Vop is

determined by a capacitance ratio between capacitors C1 and C2 and may lie between 12 and 30 dB. The small signal gain of the AC-coupled gain stage 1003 to a negative output at Von is determined by a capacitance ratio between capacitors C4 and C3. The latter small signal is preferably set equal to the small signal gain to the positive output at Vop of the AC-coupled gain stage 1003. Consequently, the microphone preamplifier 104 generates an amplified microphone signal in differential or balanced format across the positive and negative outputs Vop, Von based on the single-ended microphone signal at the input 101b. The unity gain buffer stage 1001 may exhibit an extremely high input impedance to avoid loading the transducer output in view of the potentially very high output impedance of the transducer element as discussed above. If the transducer element includes the previously discussed capacitive transducer element 102 the input impedance of the unity gain buffer stage 1001 may be larger than 100 MΩ, such as larger than 1 GΩ. The differential or balanced microphone voltage at the positive and negative outputs Vop, Von is applied to a differential input of the analog-to-digital converter for conversion into the single-bit or multibit digital microphone signal as discussed above.

[0071] The herein described subject matter sometimes illustrates different components contained within, or connected with, different other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected," or "operably coupled," to each other to achieve the desired functionality, and any two components capable of being so associated can also be viewed as being "operably couplable," to each other to achieve the desired functionality. Specific examples of operably couplable include but are not limited to physically mateable and/or physically interacting components and/or wirelessly interactable and/or wirelessly interacting components and/or logically interacting and/or logically interactable components.

[0072] With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to

the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

[0073] It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as "open" terms (e.g., the term "including" should be interpreted as "including but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes but is not limited to," etc.).

[0074] It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to inventions containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an" (e.g., "a" and/or "an" should typically be interpreted to mean "at least one" or "one or more"); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should typically be interpreted to mean at least the recited number (e.g., the bare recitation of "two recitations," without other modifiers, typically means at least two recitations, or two or more recitations).

[0075] Furthermore, in those instances where a convention analogous to "at least one of A, B, and C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., "a system having at least one of A, B, and C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). In those instances where a convention analogous to "at least one of A, B, or C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., "a system having at least one of A, B, or C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B

and C together, and/or A, B, and C together, etc.). It will be further understood by those within the art that virtually any disjunctive word and/or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase "A or B" will be understood to include the possibilities of "A" or "B" or "A and B." Further, unless otherwise noted, the use of the words “approximate,” “about,” “around,” “substantially,” etc., mean plus or minus ten percent.

[0076] The foregoing description of illustrative embodiments has been presented for purposes of illustration and of description. It is not intended to be exhaustive or limiting with respect to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the disclosed embodiments. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

WHAT IS CLAIMED IS:

1. A microphone assembly comprising:

a transducer element configured to convert sound into a microphone signal at a transducer output; and

a processing circuit comprising:

a preamplifier comprising an input node connected to the transducer output for receipt of the microphone signal, the preamplifier being configured to generate at least one of an amplified microphone signal and a buffered microphone signal;

an analog-to-digital converter (ADC) configured to receive, sample and quantize the amplified or buffered microphone signal to generate a corresponding digital microphone signal; and

a feedback path comprising:

a digital loop filter being configured to receive and filter the digital microphone signal to provide a first digital feedback signal;

a digital-to-analog converter (DAC) configured to convert the first digital feedback signal into a corresponding analog feedback signal; and

a summing node at the transducer output configured to combine the microphone signal and the analog feedback signal.

2. The microphone assembly of claim 1, wherein the transducer element comprises a capacitive transducer supplying the microphone signal across first and second mutually charged transducer plates.

3. The microphone assembly of claim 2, wherein the transducer element exhibits a transducer capacitance between 0.5 pF and 10 pF.

4. The microphone assembly of claim 2, wherein the analog feedback signal is directly connected to the transducer output without any intervening active amplification or buffer circuits.

5. The microphone assembly of claim 4, wherein the analog feedback signal is directly connected to at least one of the first and second mutually charged transducer plates.

6. The microphone assembly of claim 1, wherein the analog-to-digital converter comprises a sigma-delta modulator generating a single-bit (PDM) or a multibit digital microphone signal at a first sampling frequency;

wherein the feedback path comprises a decimator in-front of the digital loop filter which is configured for converting the single-bit or multibit digital microphone signal into a first multibit (PCM) digital signal at a second sampling frequency, wherein the second sampling frequency is lower than the first sampling frequency; and

wherein the first multibit (PCM) digital signal is coupled to an input of the digital loop filter.

7. The microphone assembly of claim 1, wherein the digital loop filter comprises a lowpass filter possessing a cut-off frequency placed at or above 10 Hz.

8. The microphone assembly of claim 7, wherein the lowpass filter possesses a cut-off frequency placed at or above 50 Hz.

9. The microphone assembly of claim 7, wherein the lowpass filter possesses a cut-off frequency placed at or above 100 Hz.

10. The microphone assembly of claim 1, wherein the processing circuit further comprises:

a command and control interface for receipt of filter configuration data from a host processor.

11. The microphone assembly of claim 10, wherein the command and control interface includes at least one of an I^2C, USB, UART or SPI command and control interface.

12. The microphone assembly of claim 10, wherein the digital loop filter comprises an adjustable or programmable transfer function controlled by the filter configuration data.

13. The microphone assembly of claim 1, wherein the digital-to-analog converter (DAC) comprises:

a hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM) configured to generate the analog feedback signal by:

converting the first digital feedback signal into a corresponding pulse-width and pulse-amplitude modulated signal at a higher sampling frequency than a sampling frequency of the first digital feedback signal.

14. The microphone assembly of claim 13, wherein the hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM) comprises:

a current output converter configured to convert the pulse-width and pulse-amplitude modulated signal into a corresponding sequence of variable width and amplitude current pulses; and

wherein the current output converter comprises a plurality of individually controllable current generators connected in parallel to the DAC output.

15. The microphone assembly of claim 14, wherein each of the plurality of individually controllable current generators comprises:

a first current source connected between a positive DC supply rail of the current output converter and the DAC output for sourcing a first current level to the DAC output; and

a second current source connected between the DAC output and a negative DC supply rail of the current output converter for sinking a second current level from the DAC output; and

a DC error suppression circuit configured for matching the first and second current levels.

16. The microphone assembly of claim 15, wherein each of the plurality of individually controllable current generators comprises:

a first current source connected between a positive DC supply rail of the current output converter and the DAC output for sourcing a first current level to the DAC output; and

a second current source connected between the DAC output and a negative DC supply rail of the current output converter for sinking a second current level to the DAC output; and

a DC error suppression circuit configured to match the first and second current levels.

17. The microphone assembly of claim 16, wherein an output impedance at 10 kHz of each of the individually controllable current generators is larger than 1 MΩ.

18. The microphone assembly of claim 16, wherein an output impedance at 10 kHz of each of the individually controllable current generators is larger than 10 MΩ.

19. The microphone assembly of claim 16, wherein an output impedance at 10 kHz of each of the individually controllable current generators is larger than 100 MΩ.

20. The microphone assembly of claim 16, wherein each of the plurality of individually controllable current generators comprises:

a feedback regulation loop connected to at least one of the first and second current sources for dynamically adjusting at least one of the first current levels and the second current level.

21. The microphone assembly of claim 16, wherein the feedback regulation loop comprises a differential loop amplifier;

the differential loop amplifier comprising a first input connected to a midpoint node in-between the first and second current sources and a second input connected to a DC reference voltage; and an output connected to the at least one of the first and second current sources.

22. The microphone assembly of claim 17, wherein each of the plurality of individually controllable current generators comprises a controllable switch arrangement configured to:

in a first state of the controllable current generator, connect the first current source to the DAC output and the second current source to a DC voltage reference or ground node;

in a second state of the controllable current generator, connect the second current source to the DAC output and the first current source to a DC voltage reference or ground node.

23. The microphone assembly of claim 22, wherein the controllable switch arrangement comprises a third state or off-state configured to:

connect the first current source and the second current source in series between the positive DC supply rail and the negative DC supply rail; and

disconnect each of the first and second current sources from the DAC output.

24. The microphone assembly of claim 22, wherein the controllable switch arrangement comprises:

a first controllable semiconductor switch inserted between the first current source and the DAC output and a second controllable semiconductor switch inserted between the DAC output and the second current source; and

a third controllable semiconductor switch inserted between the first current source and the DC voltage reference and a fourth controllable semiconductor switch inserted between the DC voltage reference and the second current source; and

a fifth controllable semiconductor switch inserted between the first current source and the midpoint node and a sixth controllable semiconductor switch inserted between the midpoint node and the second current source.

25. The microphone assembly of claim 13, wherein the hybrid Pulse-Width-Modulator and Pulse-Amplitude-Modulator comprises:

a noise-shaping quantizer configured to:

receive samples, having a first bit-width, of the first digital feedback signal outputted by the digital loop filter; and

quantize the samples of the first digital feedback signal to generate samples of a second digital feedback signal with a reduced bit-width.

26. The microphone assembly of claim 25, wherein the hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM) is configured to:

increase a sampling frequency of the second digital feedback signal with a predetermined upsampling factor, N, to generate a third digital feedback signal; and

convert the third digital feedback signal into the pulse-width and pulse-amplitude modulated signal.

27. The microphone assembly of claim 26, wherein generation of the pulse-width and pulse-amplitude modulated signal comprises:

dividing samples of the third digital feedback signal with the predetermined upsampling factor, N, to compute respective modulus values and remainder values of the samples;

converting the modulus value of a sample into a first pulse segment having a combined pulse width and pulse amplitude representative of the modulus value;

converting the remainder value of a sample into a second pulse segment with a pulse width representing the remainder value; and

combining the first and second pulse segments to form a variable width and amplitude pulse of the pulse-width and pulse-amplitude modulated signal.

28. The microphone assembly of claim 26, wherein the second feedback digital signal has a sampling frequency between 48 kHz and 356 kHz; and

wherein the third digital feedback signal has a sampling frequency at least 16 times higher than the second sampling frequency.

29. The microphone assembly of claim 1, wherein the preamplifier is DC-coupled from the input node to the output.

30. The microphone assembly of claim 1, further comprising:

a microphone housing enclosing and supporting the transducer element and the processing circuit.

31. A portable communication device comprising the microphone assembly of claim 1.

32. A semiconductor die comprising:

a processing circuit, the processing circuit comprising:

a preamplifier comprising an input node connected to a transducer output for receipt of a microphone signal, the preamplifier being configured to generate at least one of an amplified microphone signal and a buffered microphone signal;

an analog-to-digital converter (ADC) configured to receive, sample and quantize the amplified or buffered microphone signal to generate a corresponding digital microphone signal; and

a feedback path comprising:

a digital loop filter being configured to receive and filter the digital microphone signal to provide a first digital feedback signal;

a digital-to-analog converter (DAC) configured to convert the first digital feedback signal into a corresponding analog feedback signal; and

a summing node at the transducer output configured to combine the microphone signal and the analog feedback signal.

33. A method of controlling a frequency response of a signal amplification path of a microphone, the method comprising:

a) converting incoming sound into a corresponding microphone signal at a microphone transducer output;

b) sampling and quantizing the microphone signal by an analog-to-digital converter (ADC) to generate a corresponding digital microphone signal;

c) lowpass filtering the digital microphone signal to provide a first digital feedback signal;

d) converting the first digital feedback signal into a corresponding analog feedback signal by digital-to-analog converter (DAC); and

e) combining the microphone signal and the analog feedback signal at the microphone transducer output to close a digital feedback loop.

34. The method of controlling a frequency response of a signal amplification path of claim 33, further comprising:

f) applying the analog feedback signal to at least one transducer plate of a capacitive microelectromechanical (MEMS) transducer element supplying the microphone signal.

35. The method of controlling a frequency response of a signal amplification path of claim 33, wherein step d) further comprises:

quantizing and noise shaping the first digital feedback signal to generate a second digital feedback signal with a smaller bit-width than a bit-width of the first digital feedback signal.

36. The method of controlling a frequency response of a signal amplification path of claim 35, further comprising:

g) increasing a sampling frequency of the second digital feedback signal with a predetermined upsampling factor, N, to generate a third digital feedback signal; and

converting the third digital feedback signal into a pulse-width and pulse-amplitude modulated signal.

37. The method of controlling a frequency response of a signal amplification path of claim 36, wherein converting the third digital feedback signal comprises:

h) dividing a first sample of the third digital feedback signal with the predetermined upsampling factor, N, to compute a modulus value and remainder value of the first sample;

i) converting the modulus value of the first sample into a first pulse segment having a combined pulse width and pulse amplitude representative of the modulus value;

j) converting each remainder value of the first sample into a second pulse segment with a pulse width representing the remainder value;

k) combining the first and second pulse segments of the first sample to form a first variable width and amplitude pulse; and

l) repeating steps h) – k) for subsequent samples of the third digital feedback signal to generate the pulse-width and pulse-amplitude modulated signal by a sequence of variable width and amplitude pulses.

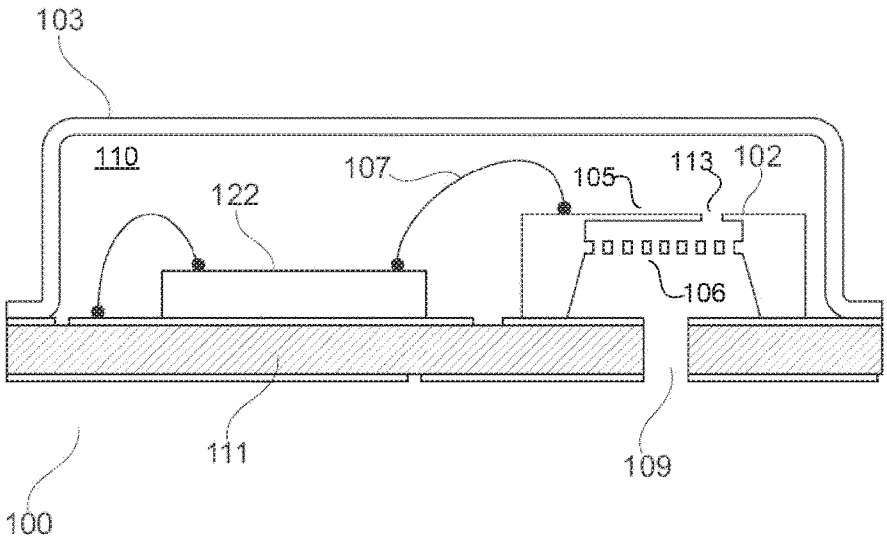


FIG. 1

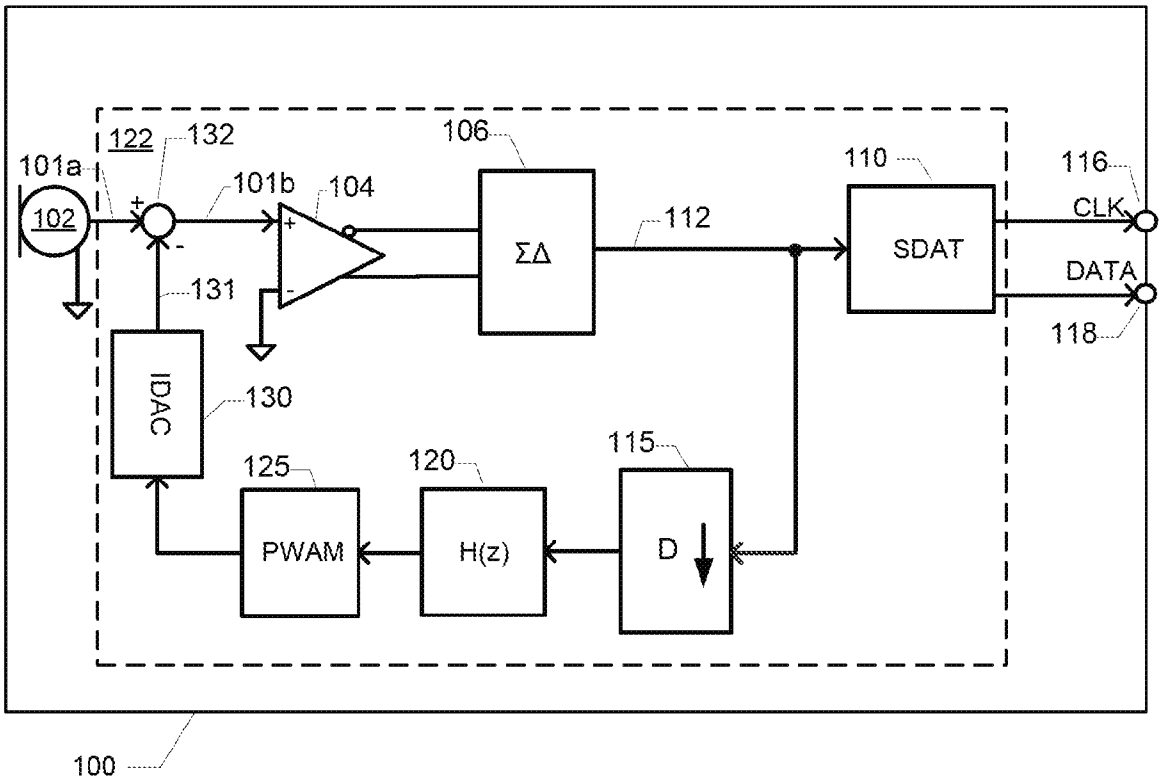
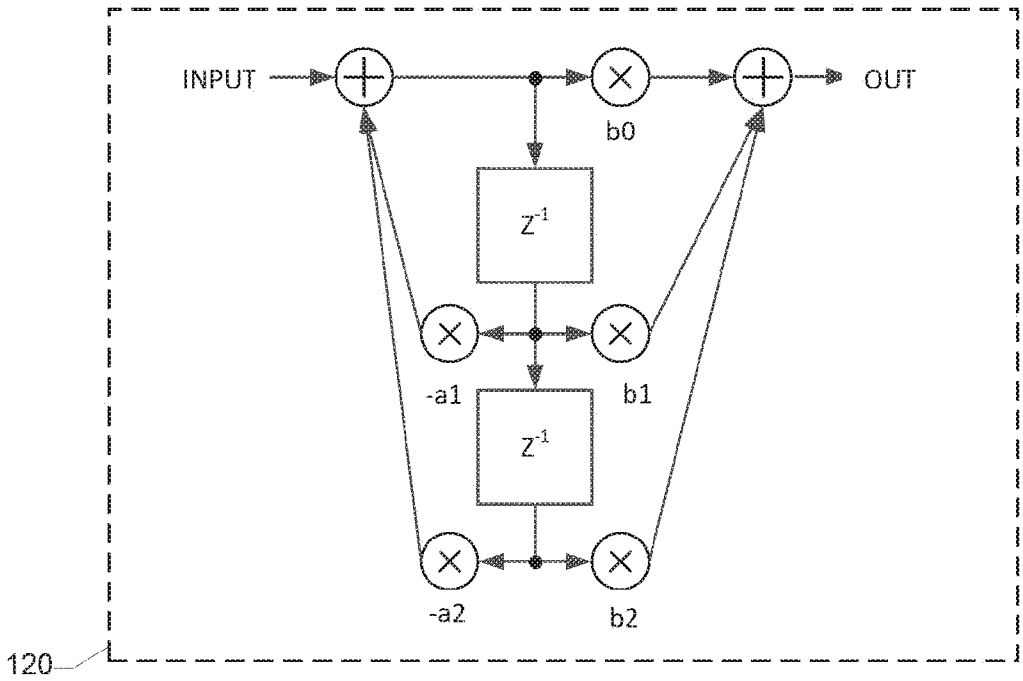

100
101a
102
122
132
101b
104
106
ΣΔ
112
110
SDAT
116
CLK
DATA
118
131
IDAC
130
125
PWAM
120
H(z)
115
D

FIG. 2


INPUT
OUT
b0
Z^{-1}
-a1
b1
Z^{-1}
-a2
b2
120

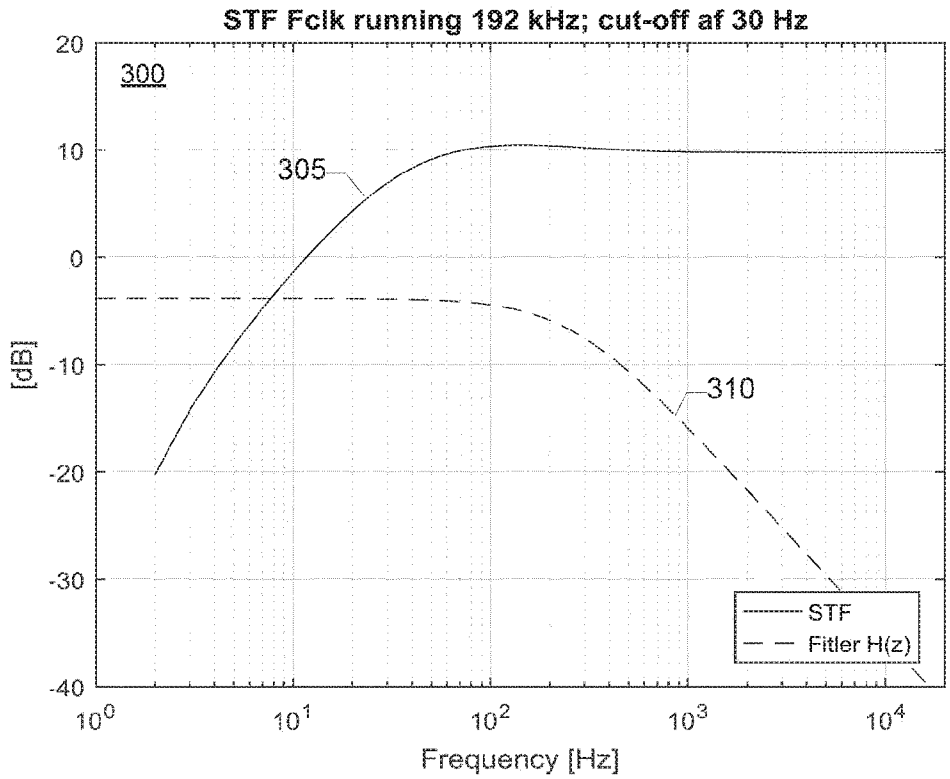
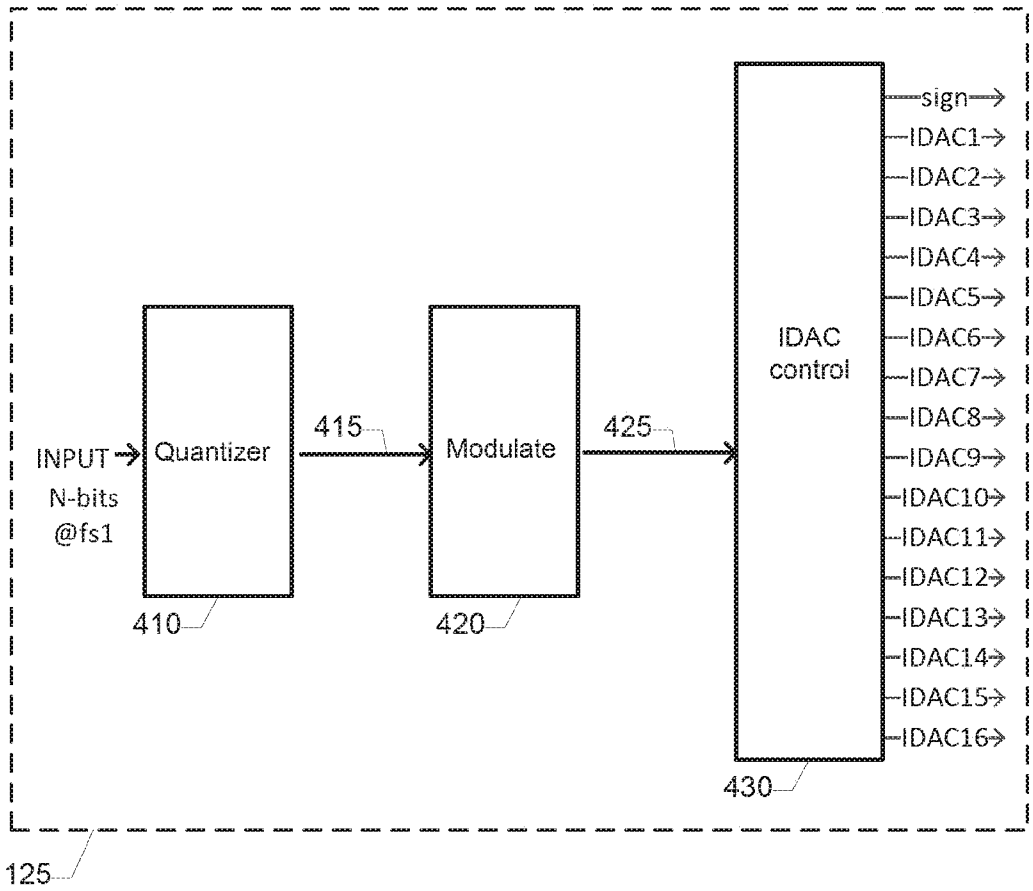

STF Fclk running 192 kHz; cut-off af 30 Hz
300
305
310
[dB]
Frequency [Hz]
STF
Fitler H(z)

FIG. 3


INPUT
N-bits
@fs1
Quantizer
410
415
Modulate
420
425
IDAC
control
430
sign
IDAC1
IDAC2
IDAC3
IDAC4
IDAC5
IDAC6
IDAC7
IDAC8
IDAC9
IDAC10
IDAC11
IDAC12
IDAC13
IDAC14
IDAC15
IDAC16
125

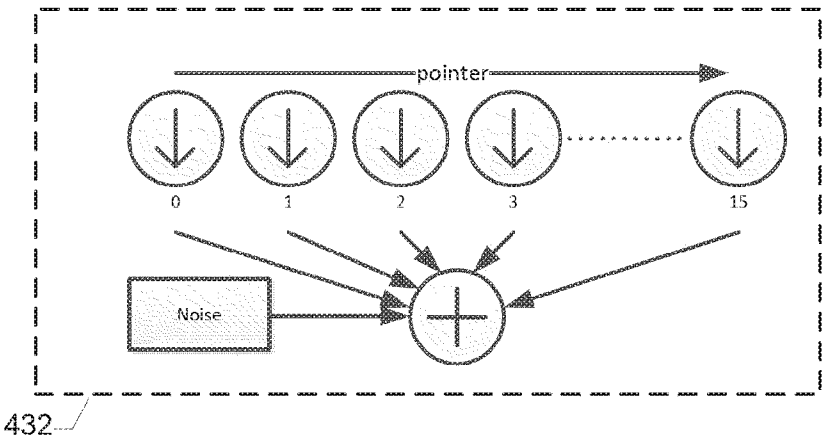

pointer
0
1
2
3
15
Noise
432

FIG. 4

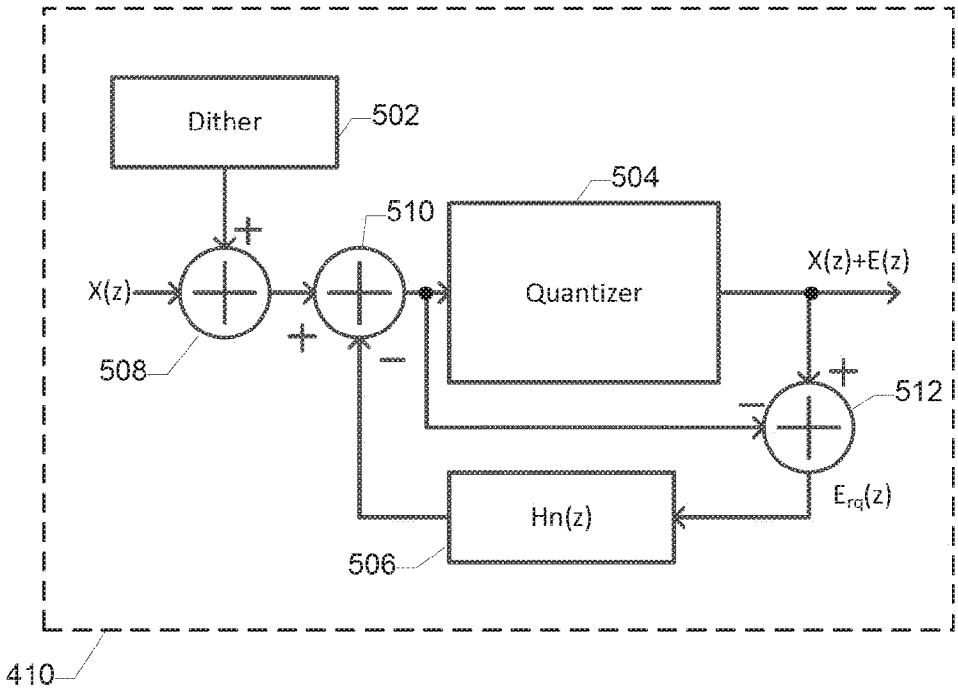


FIG. 5

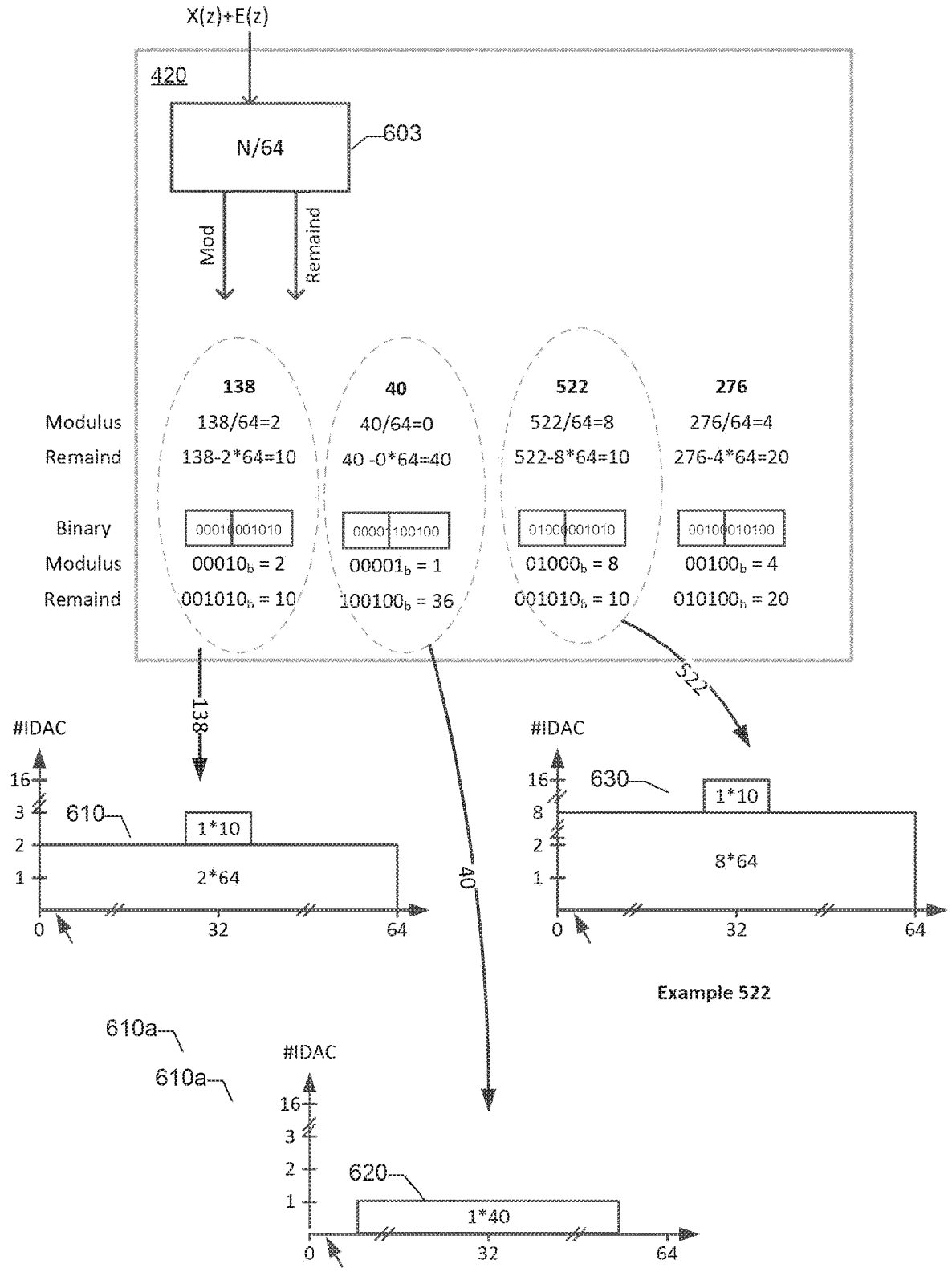

X(z)+E(z)
420
N/64
603
Mod
Remaind
138
40
522
276
Modulus
138/64=2
40/64=0
522/64=8
276/64=4
Remaind
138-2*64=10
40 -0*64=40
522-8*64=10
276-4*64=20
Binary
00010001010
00001100100
01000001010
00100010100
Modulus
00010b = 2
00001b = 1
01000b = 8
00100b = 4
Remaind
001010b = 10
100100b = 36
001010b = 10
010100b = 20
138
40
522
#IDAC
16
3
2
1
610
1*10
2*64
0
32
64
#IDAC
16
8
2
1
630
1*10
8*64
0
32
64
Example 522
610a
610a
#IDAC
16
3
2
1
620
1*40
0
32
64

FIG. 6

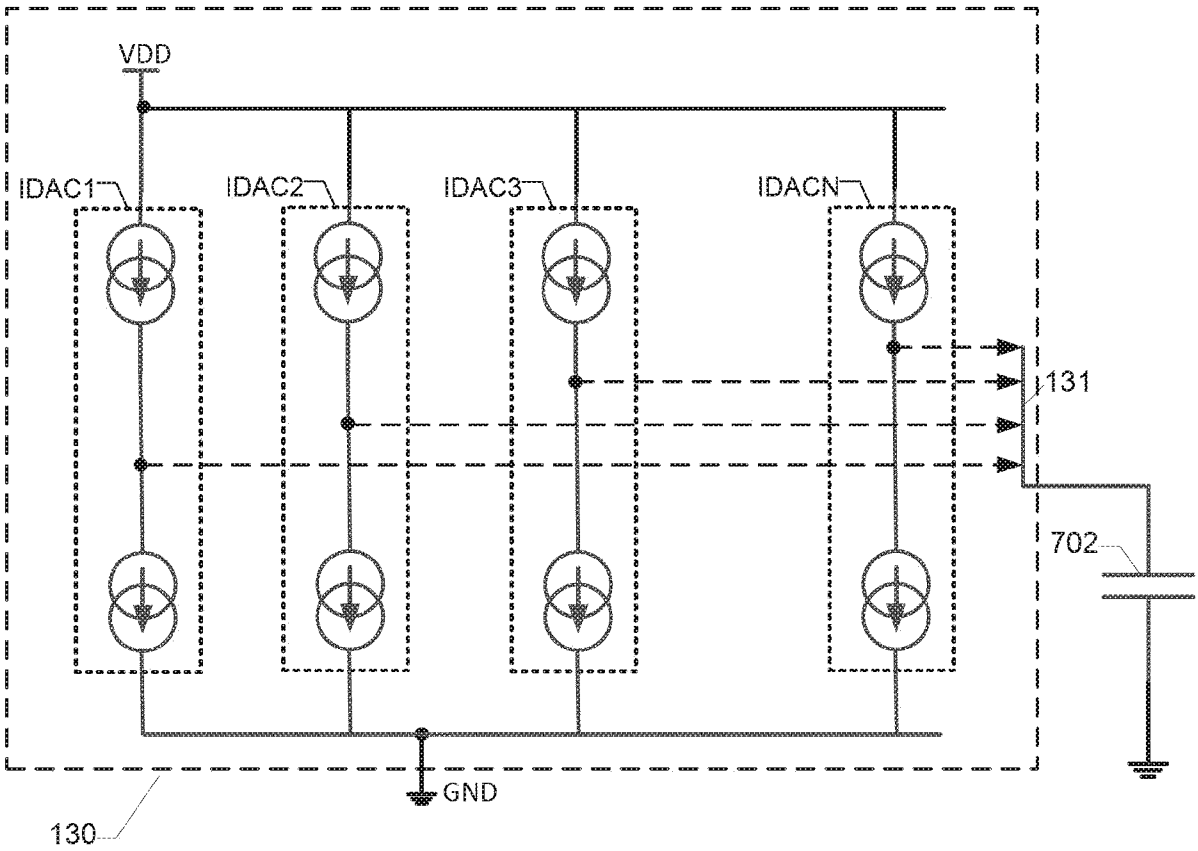


FIG. 7

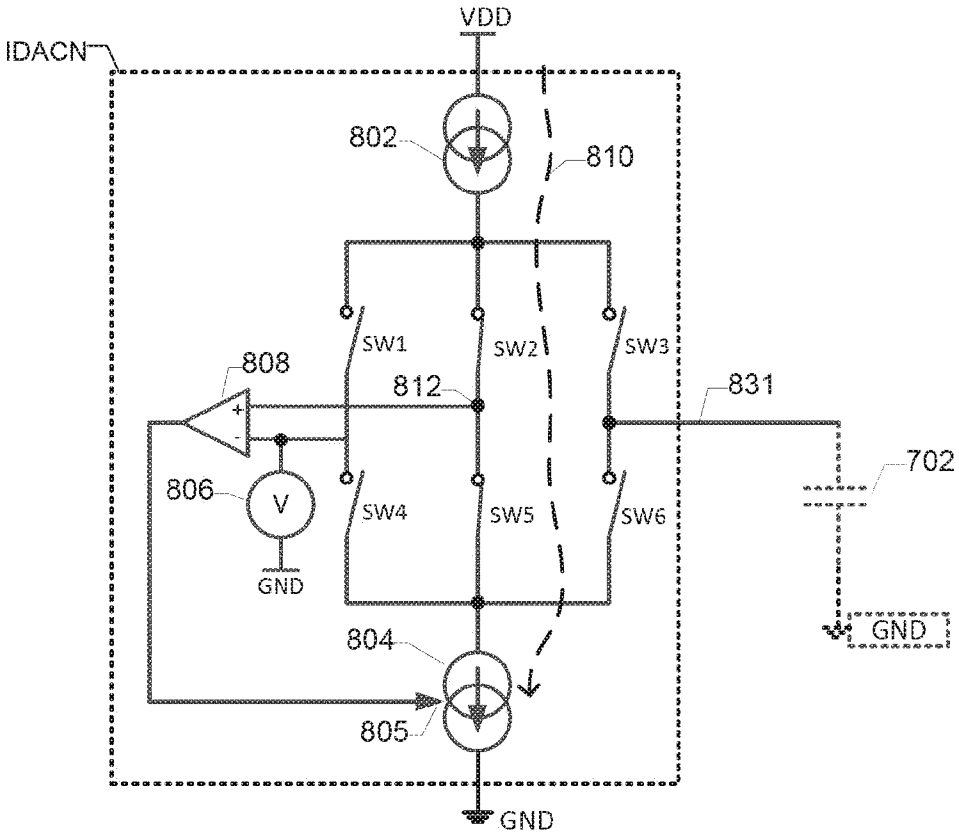

VDD
IDACN
802
810
SW1
SW2
SW3
808
812
831
806
V
SW4
SW5
SW6
702
GND
GND
804
805
GND

FIG. 8

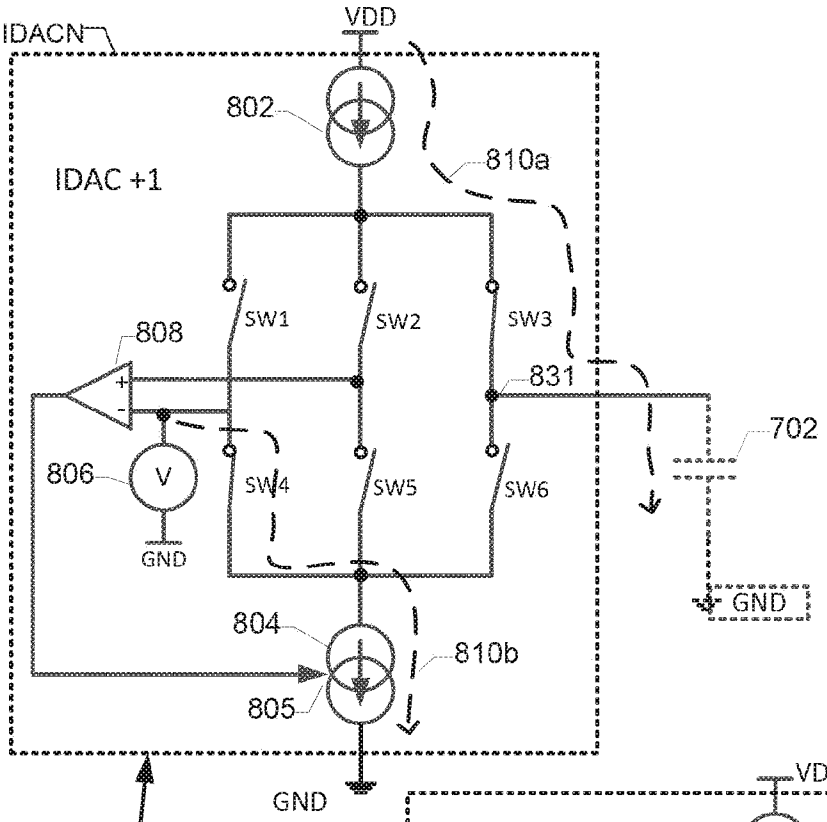

IDACN
VDD
802
IDAC +1
810a
SW1
SW2
SW3
808
831
702
806
V
SW4
SW5
SW6
GND
GND
804
810b
805
GND

FIG. 9A

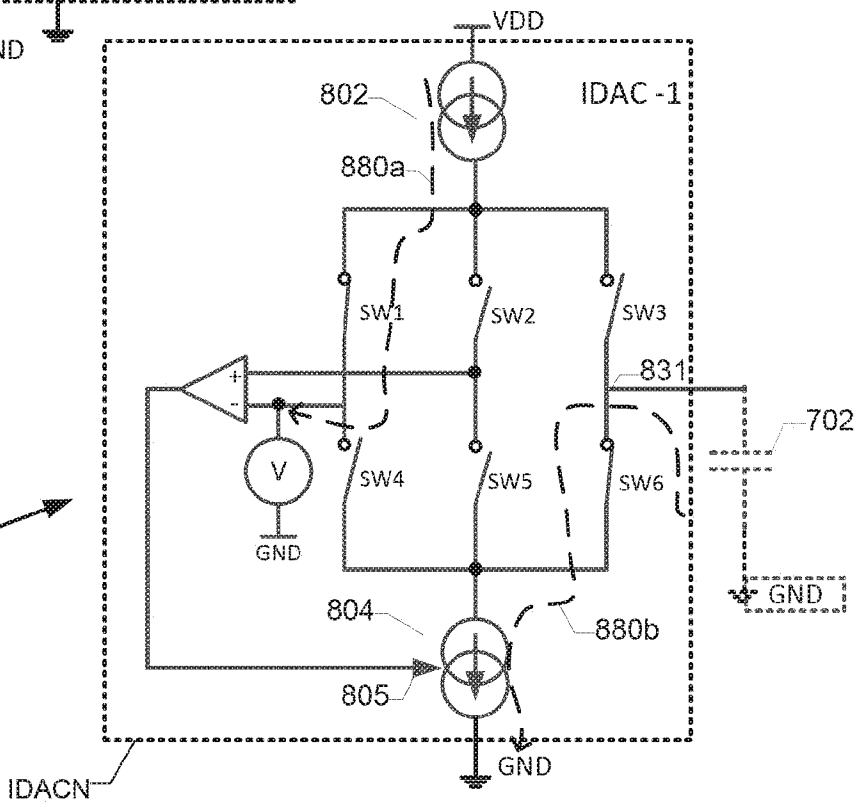

VDD
802
IDAC -1
880a
SW1
SW2
SW3
831
702
V
SW4
SW5
SW6
GND
GND
804
880b
805
GND
IDACN

FIG. 9B

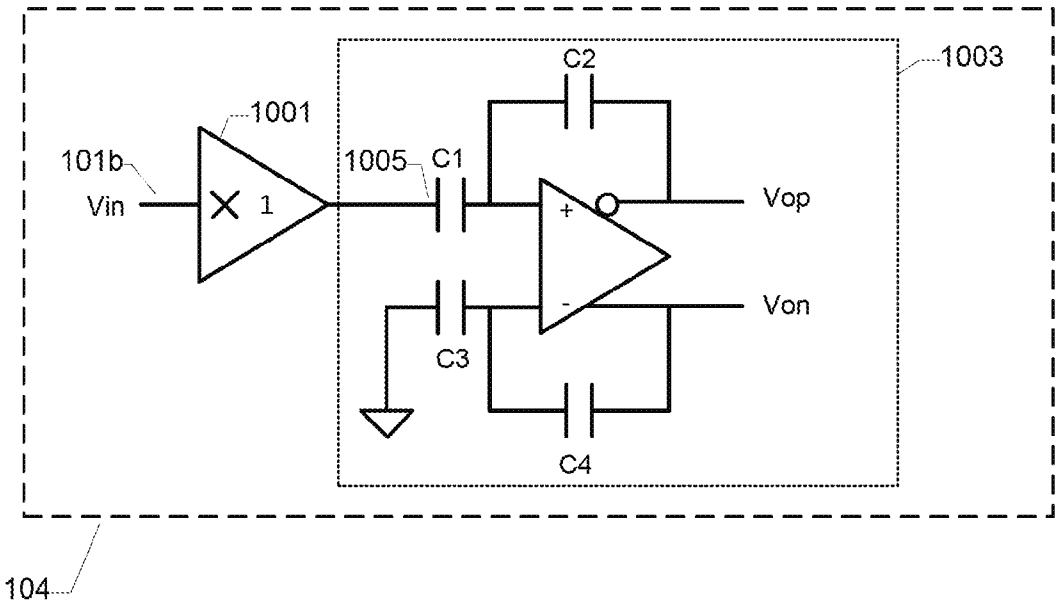


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/036855

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04R3/04
ADD. H03M1/12 H03G5/16 H03F3/181 H03M3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04R H03M H03G H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2012/043974 A1 (VAN DEN BOOM JEROEN [NL] ET AL) 23 February 2012 (2012-02-23) the whole document -----	1-5,7-9, 30-34 6
Y A	US 2008/129569 A1 (MUHAMMAD KHURRAM [US] ET AL) 5 June 2008 (2008-06-05) paragraphs [0017], [0033]; figures 1, 3, 4, 7 -----	6 1,32,33
X	US 2016/112795 A1 (BACH ELMAR [AT] ET AL) 21 April 2016 (2016-04-21) paragraphs [0002], [0027], [0030], [0032], [0048]; figures 1 - 3, 5, 6, 8 -----	1,2,4,5, 30-34
X A	US 2008/272946 A1 (MELANSON JOHN L [US]) 6 November 2008 (2008-11-06) paragraphs [0031], [0033], [0041], [0048], [0060], [0062], [0063]; figures 3, 5, 9, 11, 12 -----	1,32,33 2-9,30, 31,34

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 August 2017	02/10/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lörch, Dominik

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/036855

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-9, 30-34

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-9, 30-34

   digital feedback loop comprises decimator upstream of digital loop filter

1.1. claims: 8, 9

   specific ranges for cut-off frequency of lowpass filter in feedback path

1.2. claim: 30

   housing

---

2. claims: 10-12

   command and control interface; adjustable/programmable transfer function of digital loop filter

---

3. claims: 13-28

   digital-to-analog converter in feedback path comprises hybrid Pulse-Width and Pulse-Amplitude Modulator (PWAM)

---

4. claim: 29

   DC-coupled pre-amplifier

---

5. claims: 35-37

   quantizing and noise shaping in the feedback path to generate smaller bit-width digital feedback signal

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2017/036855

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		WO 2008137662 A1	13-11-2008