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PULSE GENERATOR

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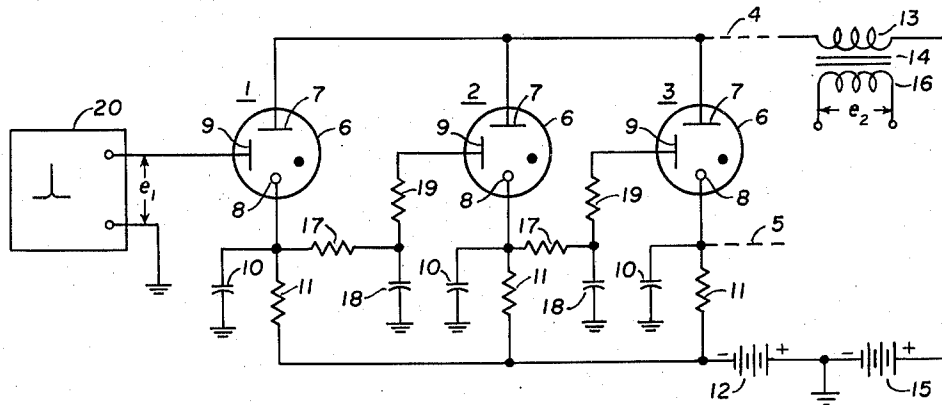


FIG. 1

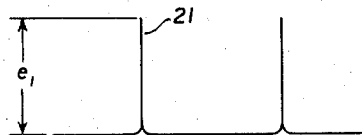


FIG. 2

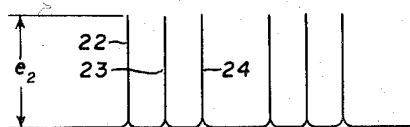


FIG. 3

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PULSE GENERATOR

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2 Claims. (Cl. 250—27)

My invention relates to pulse generators, and more particularly to pulse generators of the pulse multiplier type, that is, pulse generators which furnish a plurality, or a train, of pulses in response to a single initiating pulse.

It is an object of my invention to provide a pulse generator of the pulse multiplier type which is of novel configuration, yet which is simple and employs a minimum of parts.

In general, I accomplish this and other objects of my invention by providing a plurality of stages connected in cascade. Each stage has two load circuits, one individual thereto. The individual load is used to transfer conduction to the following stage, and the common load develops the desired output.

Further objects and advantages of my invention will become apparent as the following description proceeds and the features of novelty which characterize my invention will be pointed out with particularity in the claims annexed to and forming a part of this specification.

For a better understanding of my invention, reference may be had to the accompanying drawing in which

Fig. 1 is a schematic circuit diagram of one embodiment of my invention; and

Figs. 2 and 3 are waveform diagrams useful in explaining the embodiment of Fig. 1.

Referring now to Fig. 1, there is provided a pulse generator having a plurality of stages connected in cascade. The embodiment of Fig. 1 shows stages 1, 2 and 3, with dashed lines 4 and 5 indicating how additional stages may be added. My invention may be used with a minimum of two stages and with an unlimited maximum number of stages.

Each of the stages includes an electron discharge device 6 having at least an anode 7, a cathode 8 and a governing electrode 9. I prefer that each of these electron discharge devices be of the cold cathode gaseous discharge type, and I have accordingly so indicated in Fig. 1.

Each of the electron discharge devices has an input circuit extending from the governing electrode 9, which in the case of a gaseous discharge device is generally termed a starting electrode, and the cathode. The cathode connection is preferably completed via a bypass capacitor 10.

Each stage has a load circuit individual thereto. This individual load is preferably a resistor 11 which may be connected between cathode 8 and a source of bias potential 12. The anodes 7 may be connected in parallel to one end of a common load circuit, preferably the primary 13 of transformer 14. Primary 13 is connected to a source of operating potential, such as battery 15, for electron discharge devices 6. Transformer 14 is provided with a secondary 16.

There may be provided time delay means individual to each stage. Thus, in the case of stage 1, resistor 17 and capacitor 18 form such time delay means. Resistor 17 may be connected in series between cathode 8 of stage

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1 and the governing electrode, or starting electrode, of stage 2 via a series resistor 19. Resistor 19 acts as a current limiting resistor. Capacitor 18 is effectively connected in shunt across the input circuit of stage 2.

Stage 1 differs from the remaining stages of the cascade connection in that its input circuit has connected thereto a source 20 of control pulses.

The operation of the circuit of Fig. 1 may best be understood with the aid of Figs. 2 and 3. The input to stage 1 from pulse source 20 may be represented by pulse 21, as shown in Fig. 2, having a magnitude e_1 . Upon receipt of control pulse 21 from source 20, stage 1 conducts because the positive potential existing between its anode 7 and cathode 8 (due to potential sources 15 and 12 in series) is sufficient for the purpose only if start electrode 9 is positive. The current drawn by stage 1 flows through the primary of transformer 14, and the change of current consequently induces a voltage in secondary 16 which is proportional to the time rate of change thereof. Thus a pulse 22 appears in the output waveform, e_2 of Fig. 3.

The current drawn by stage 1 creates a drop across the individual load circuit resistor 11, and so constitutes a signal generated at this point. The leading edge of this signal, or voltage drop, is delayed by time delay means 17, 18 and is then applied to the input circuit of stage 2. When the start anode 9 of stage 2 receives this signal from the preceding stage and so reaches an increased potential, conduction is initiated in stage 2. This change of current in the primary 13 of transformer 14 causes a second pulse 23 to appear in secondary 16, as shown in Fig. 3. However, conduction in stage 2 causes an additional voltage drop across the common load, primary 13, thereby lowering the potential available at all anodes 7 of the cascade connection. The value of the common load, primary 13, is proportioned relative to that of potential source 15 such that conduction can no longer be maintained in stage 1 due to the lowered potential available through primary 13. Discharge device 6 of stage 1 is therefore extinguished.

The conduction current of stage 2 causes a voltage drop in the individual cathode load resistor of stage 2 in the same fashion as in stage 1. The delayed leading edge of the signal resulting from this voltage drop is delayed in fashion similar to that of stage 1, and is applied to the input of stage 3. The same action thereupon takes place in the latter stage as just described in connection with stage 2. Identical action may occur in succeeding stages if provided; in the present instance wherein three stages are shown, pulses 22, 23 and 24, respectively, obtained from the conduction of stages 1, 2 and 3 in turn, are obtained in waveform e_2 for each input pulse 22 in waveform e_1 (Fig. 2).

While I have shown and described my invention as applied to a specific embodiment thereof, other modifications will readily occur to those skilled in the art. For example, tubes other than cold cathode gaseous discharge may be employed, or other forms of time delay means may be used. Similarly, other forms of common load may be employed. I do not, therefore, desire my invention to be limited to the specific arrangement shown and described, and I intend in the appended claims to cover all modifications within the spirit and scope of my invention.

What I claim is:

1. In a pulse generator, the combination of a plurality of stages connected in cascade; each said stage including a gaseous discharge device having at least an anode, a cathode, and a governing electrode; and an input circuit for each said gaseous discharge device between said governing electrode and said cathode; a load circuit individual to each said gaseous discharge device in said cathode

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circuit; a source of operating potential for said gaseous discharge device; said anodes being connected in parallel; a load circuit common to said stages connected between said source of operating potential and said anodes; time delay means individual to each stage; said input circuit for each stage except the first said stage being connected to said individual load circuit of the preceding said stage through said time delay means individual thereto; a source of control pulses connected to said input of said first stage, each of said control pulses being operative to cause conduction within said first stage; the magnitude of said source of operating potential and of said load circuits being proportioned such that an individual one of said gaseous discharge devices, other than said first gaseous discharge device, begins conduction only upon receipt of a signal from said individual load circuit of the preceding one of said stages and maintains conduction only until another one of said stages conducts; and means for obtaining a voltage proportional to the time rate of change of current in said common load circuit, whereby each said gaseous discharge device conducts in turn along said cascade connection upon receipt by said

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first discharge device of a pulse from said pulse source and said last-named means furnishes a voltage pulse as each said gaseous discharge devices begins to conduct.

2. The combination of claim 1 in which said individual time delay means comprises resistive means connected in series between said cathode of one said stage and said governing electrode of the next said stage and capacitive means connected in shunt across said input circuit.

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