

[54] TIMING OR COUNTING SYSTEM

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[58] Field of Search 235/92 T, 92 PE, 92 DM, 235/92 CA; 58/23 R, 23 A; 324/181, 186; 307/226; 328/48

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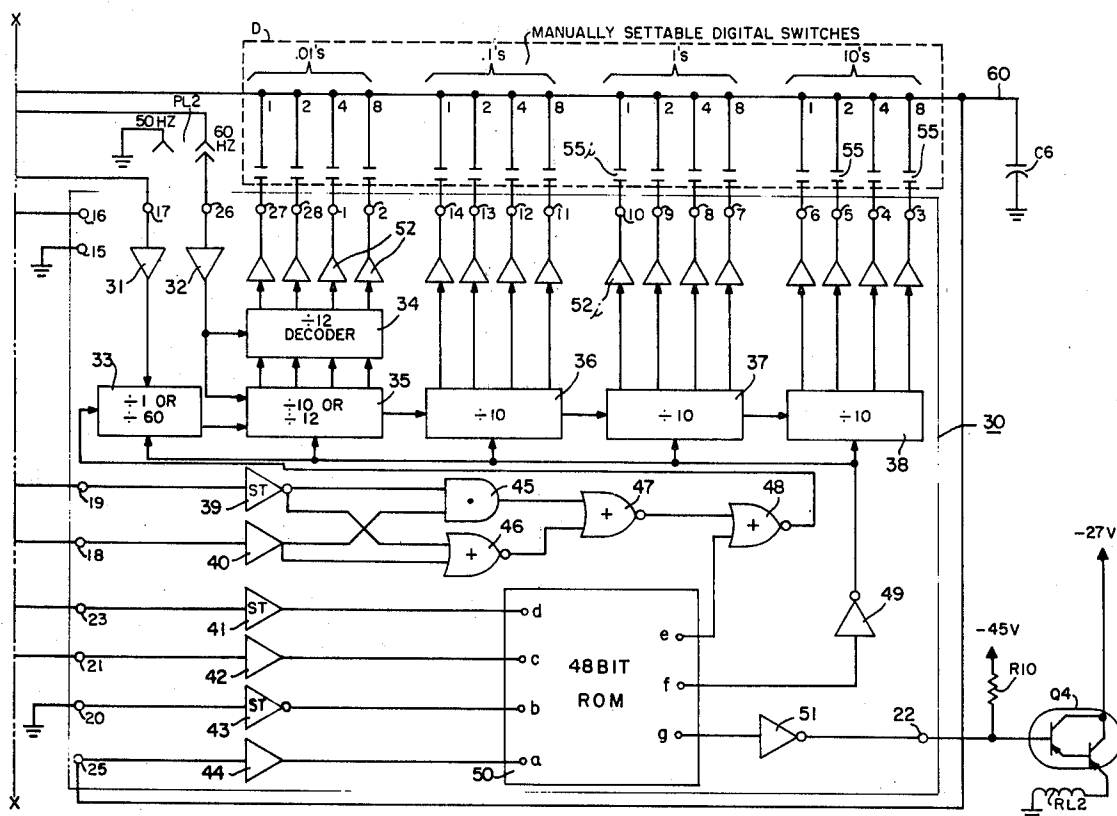
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[57] ABSTRACT

A timing or counting system of the purely electronic type which may be used with 50 or 60 Hz-voltages. As a timer, it is regulated by the cycles of the line. It can also time from 10 milliseconds to 1½ hours. Manually settable digital switches are associated with the present circuit to enable selection of a predetermined decimal count or timing interval. The input line frequency (60 cycles) is doubled, then divided by a number of frequency dividing circuits. A clock pulse generator feeds clock pulses via Schmidt triggers and logic circuits to a read-only memory which controls the operation of the dividers. A special decoding circuit operates to convert to a decimal form the output of one of the dividers associated with the decimal switch for the least significant place.

4 Claims, 2 Drawing Figures



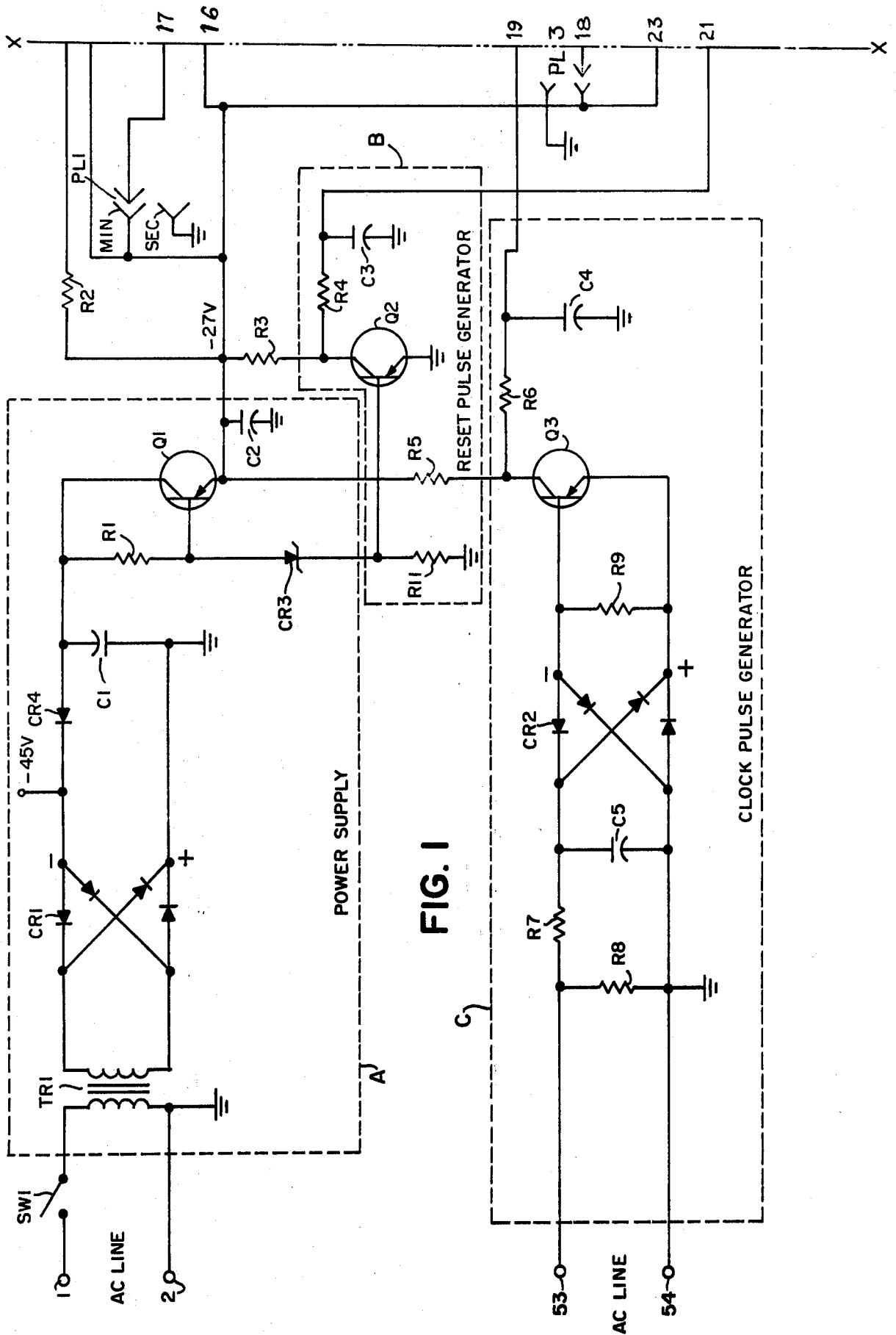
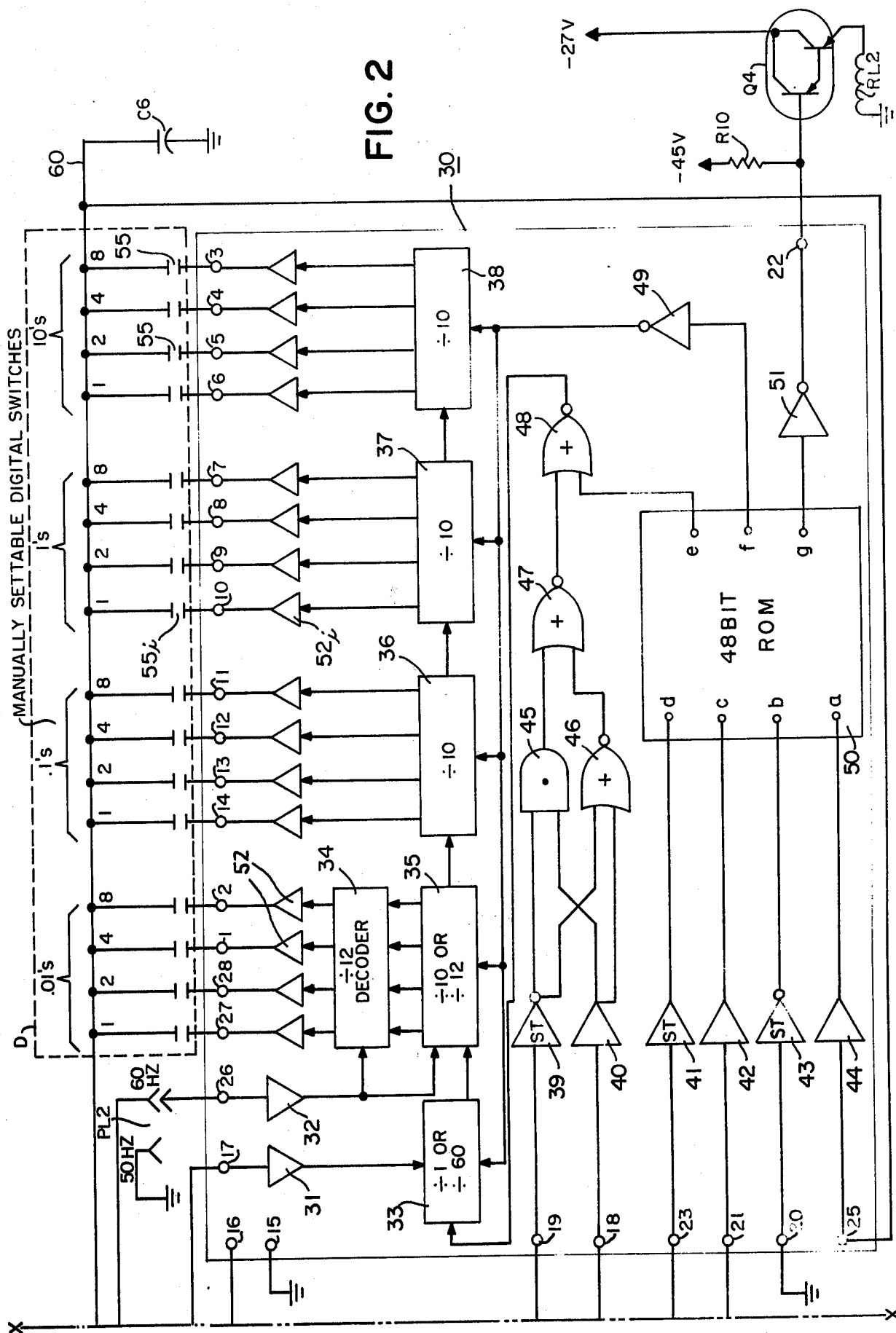


FIG. 2



TIMING OR COUNTING SYSTEM

This is a continuation application of Ser. No. 248,632, filed Apr. 28, 1972 now abandoned.

BACKGROUND OF THE INVENTION**1. Field of the Invention**

The invention relates to counters or timers of the purely electronic type. As a timer, it relates to those monitored by the cycles of the supply line alternating current.

2. Prior Art

Electro mechanical timers and counters have limited ranges and/or resolution. This is also true of electronic timers which incorporate a resistance-capacitance circuit as the primary timing circuit. Therefore, to cover a wide range these former systems required the use of many different timers and dials, which is not only inconvenient for the user but entails more expensive production investment on the part of the manufacturer. Furthermore, as a result of the inter-relation of the various mechanical parts the life expectancy of electro mechanical timers left something to be desired. It was also necessary with electro mechanical timers to change the driving motors if the timers were to be operated on 50 Hz as opposed to 60 Hz.

While there did exist in the prior art timers having digital setting capability, the timing resolution of these timers was somewhat limited.

The objects of the present invention therefore include the provision of a purely electronic timer or counter whose life expectancy is determined primarily by the life of the output relay with which it is customarily used. Also, a simple plug-in change converts its operation from 50 Hz to 60 Hz, and vice versa. Its resolution is considerably better than electro mechanical types because essentially every cycle of the line voltage is counted in the timing mode. The present invention also does not require expensive, fast-operating circuits to drive the counters in it, as is the case with other timers or counters employing MOS. The present invention also provides a much greater range capability than previously was available.

BRIEF SUMMARY OF THE INVENTION

A timing (or counting) circuit which is manually settable to a predetermined digital timing (or counting) setting. Means are provided for dividing the frequency of the line to produce counting pulses supplied to the various decades feeding the decimal digital setting switches. This means includes means for dividing a multiple of the line frequency and decoding the quotient so as to provide signals corresponding to the ten possible settings of the digital switch associated with the least significant place.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1 and 2 are schematic and partially block diagrams of the timing or counting systems according to the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS**Overall Summary of Components**

Referring to FIG. 1 and its continuation of FIG. 2, an overall schematic and logic diagram is shown which includes a power supply contained within a broken-line rectangle A which is connected via switch SW1 to the AC line terminals 1 and 2. There is also a reset pulse

generator (which does not include resistor R5) shown within another such rectangle B and a clock pulse generator shown in rectangle C. A plurality of manually-settable digital switches 55 is shown in still another broken-line rectangle D, which are connected to an MOS integrated circuit 30. The power supply A furnishes filtered DC to all of the other components. The reset pulse generator B readies the circuits on the MOS 30 for the beginning of a cycle of operation. The clock pulse generator C supplies clock pulses to the circuits on the integrated circuit 30 at a rate determined by the frequency of the AC line. The manually-settable decimal digital switches 55 are set by the operator of the timing (or counting) circuit according to a predetermined time lapse, interval or count. When set, they determine the time-lapse cycle interval or counting operation of the integrated circuit 30 to which they are connected. I/C 30 divides the clock pulses and counts them until the setting of the digital switches is matched, whereupon the cycle is completed. Plug-socket assembly PL 1 enables the operator to choose timing either by minutes or by seconds. Plug-socket assembly PL 2 permits the operator to set the timer for operation from the standard 60-cycle line or a 50-cycle line.

Operation — Reset and Enabling Counting

When switch SW1 is closed, line voltage is supplied to input terminals 1 and 2 at 50 cycles or 60 cycles as the case may be. If it is 60 cycles, the assembly PL2 is set as shown; if 50 cycles, the plug is moved to the 50 cycle socket. When power is supplied by throwing the switch SW1, the power supply A is turned on but requires a finite time to reach its steady-state condition. As the voltage builds up across C1, transistor Q1 is rendered conductive and voltage is applied to terminal 21 through resistors R3 and R4. The Zener diode CR3 prior to achievement of the steady state condition is not conductive, there is no voltage across R11, and consequently transistor Q2 is off. The voltage applied via R3 and R4 to terminal 21 of I/C 30 is a logic "1" and is transmitted via buffer amplifier 42 to ROM terminal c. The ROM is structured so that the pulse which emerges from terminal f is a logic "0" and is applied through inverting amplifier 49 as a logic "1" to set all of the counters on I/C 30 to zero.

When capacitor C1 charges to a predetermined voltage, the Zener diode CR3 in parallel with it conducts so that there is current through resistor R11 and out of the base of PNP transistor Q2, turning the latter on. When this happens, the voltage at the terminal 21 effectively goes to a logic "0" (zero or ground) which is transferred through buffer amplifier 42 to the terminal c of the ROM 50. As a result, due to the circuit characteristics of the ROM, terminal f of the ROM 50 goes to "1" which, when transmitted via the inverting amplifier 49 as a "0", conditions the counters 33, 35, 36, 37, and 38 to accept counts at their respective inputs.

Operation — Clock Pulse Generation System

The clock generator C is connected via input terminals 53 and 54 to the regular 60 Hertz AC line. It includes a full-wave rectifier bridge CR2 which supplies a 120 Hz wave to the base of transistor Q3 when the circuit is operated as a timer. This turns the transistor on and off at a 120 Hertz rate. The collector of Q3 is connected through R5 to the regulated -27V. at the emitter of Q1 and therefore the collector of Q3 swings

between -27V. (logic "1") and approximately zero volts at a 120 Hz. rate. This 120 Hz. clamped voltage wave is applied to the input terminal 19 of I/C 30 which is connected to an inverting Schmidt trigger circuit 39 that inverts the input signal.

Ordinarily, very fast circuits are required to drive counters, but such fast-acting circuits are susceptible to noise since noise spikes may be electrically indistinguishable from the output pulses since they both have fast rise and fall times. By using Schmidt trigger circuits on the I/C 30, the use of fast driving circuits off the I/C 30 are obviated. When the slow-rise 120 Hz. pulses are applied to the input of the Schmidt trigger 39, the latter produces inverted rectangular 120 Hz. pulses having very sharp leading and trailing edges. These pulses are eventually applied to the counters 33, 35, etc., when the circuit is used for a timing operation, via gates 45 - 48. When the circuit is used for counting, these gates determine the polarity of the signal applied to the counters. In the timing operation, the 120 Hz rectangular pulses are applied to one input of NOR circuit 46 as well as to one input of AND circuit 45. At the same time, there is applied to the other inputs of NOR circuit 46 and AND circuit 45 a constant -27 volt ("1") signal from the emitter of Q1 (which has been rendered conductive) via terminal 18 and buffer amplifier 40. When the input to one terminal of AND circuit 45 is a "1", the output will be a replica of the input to its other terminal.

The NOR circuit 46 will have a logic "0" output that is applied to one input of NOR gate 47. To the other input of the same gate there will be applied the output signal from AND gate 45 so that the output of NOR gate 47 will be an inversion of the output of gate 45. The output wave of gate 47 is applied to one input of NOR gate 48 together with a signal from the *e* terminal of the ROM 50. If this signal is a "0", the 120 cycle clock pulse train is passed by gate 48 onto the input of frequency divider 33. If the signal at the output terminal *e* is a "1", there is no output from NOR gate 48 and counting is thereby disabled.

When the circuit is used to count, assembly PL3 may be alternatively connected so that the plug is grounded, i.e., a "0", rather than plugged into -27 volts ("1"). In this hook-up, 0's will be applied via terminal 18 to gates 45 and 46 so that the pulses to be counted will have their polarity reversed.

Operation — Frequency Dividing Circuits

The divider 33 is conditioned to divide by 60 only when there is a "1" at terminal 17 and a "1" at ROM terminal *f*. A "1" at terminal 17 is passed via buffer amplifier 31 to the divider 33 when the plug of plug-socket assembly PL-1 is in the "minutes" position shown. (If the plug were in the "seconds" position, it would be grounded thereby producing a "0" and the divider 33 would be conditioned to operate as a divider by 1.)

When the divider 33 is operating in the "divide by 60" mode there will be two pulses out per second for each 120 cycles per second applied thereto. Stated in another way, there will be 120 pulses out per minute. The output of the divider 33 is applied to one input of the dual-mode divider 35. This divider is capable of dividing, depending upon its input control signal, either by 10 or by 12. When PL2 is connected for 60-cycle operation as shown, the counter 35 will divide by 12

since there is applied to its other input a "1" via buffer amplifier 32 from the -27 volt line connected to the emitter of Q1. The same "1" is also applied to one input of the decoder 34.

The divider 35, since it has divided the 120 pulses per minute by 12, will produce and apply to divider 36 10 pulses per minute. Divider 36 will therefore produce and apply to divider 37 one pulse per minute. Divider 37 will therefore produce and apply to divider 38 one pulse per each 10 minutes. The divider 38 has no "carry" output.

It is seen that the dividers 36, 37 and 38 each produce four-bit binary outputs that are connected through buffer amplifiers 52 to contacts of the manually settable decimal digital switches. Divider 38 is connected to contacts which when manually set by manipulation of the digit wheels represent 10's. Dividers 37 and 36 are connected to switches 55 that are operated by digit wheels representing, respectively, one's and ten's.

It may thus be seen that the maximum range from the counter will be 99.99 minutes when the plug-socket PL-1 is connected as shown. If it were connected so that the plug was in the "seconds" socket, there would be a "0" at terminal 17 which would, when applied to the divider 33, disable the division by 60. Therefore, instead of two pulses out of the divider 33 per second there would be 120 pulses out per second. However, since the other dividers 35, 36, 37, and 38 would function the same, the maximum count would then be 99.99 seconds. The digital switches respectively close or open a set of four contacts for each decimal numeral visible to the operator.

The divider 35, however, is not directly connected to four switches representing binary digital places corresponding to hundredths. Rather, the divider 35 is connected through a decoder 34 and four buffer amplifiers to one set of contacts.

Operation — Decoder 34

Decoder 34 is employed since the divider 35, when operating in the "divide by twelve" mode, produces 12 different output configurations during each 12-count counting cycle. However, the digital switch 55 associated with divider 35 can only be set to any one of 10 digital positions. It may be demonstrated that in the absence of the decoder 34, there would be a maximum error of approximately 0.015 seconds for a setting of a "9" on the digital switch representing the hundredths. Using the decoder 34 constructed to operate according to the following "Truth Table" (Table 1) gives a maximum error less than 0.003.

TABLE 1

Count	÷ 12 mode Output B	Output F	Normal Output B	(÷ 10) mode Output F
0	0000	0000	0000	0000
1	0001	0001	0001	0001
2	0010	0010	0010	0010
3	0011	0010	0011	0011
4	0100	0011	0100	0100
5	0101	0100	0101	0101
6	0110	0101	0110	0110
7	0111	0110	0111	0111
8	1000	0111	1000	1000
9	1001	0111	1001	1001
10	1010	1000	0000*	0000
11	1011	1001	0001	0001
12	0000*	0000	0010	0010

*Carry propagate output to counter 36.

The Output B column of the above table is applicable only to operation when the divider 35 is operative in the "divide by twelve" mode corresponding to operation of the timer on 60 cycles and the setting of the plugsocket PL-2 as shown. The "Output F" column is applicable for 50 cycle operation or for use of the circuit in the counting mode. By reference to Table 1, it is seen that the inputs to the decoder 34 are the same as the outputs therefrom when the count is 0, 1 and 2. When the count at the input to the decoder is 3, the output count is 2. When the counts at the input are 4, 5, 6 and 7 respectively, the outputs lag behind, being 3, 4, 5 and 6 respectively. When the count at the input is 8 or 9, the count at the output is 7 in both instances. When the count at the input is 10 and 11, the output count is 8 and 9 respectively. When the count is 12, the outputs are the same (i.e., zero) and this is a recycle or carry count.

Thus, twice during the count two successive input digits result in the same output digit. This happens for input digits 2 and 3 which result in output digit 2, and input digits 8 and 9 which result in output digits 7. Consequently, even though 120 pulses per second are applied to divider 35, only 10 different digital output signals result corresponding to the 10 different possible settings of the associated digit wheels.

Each of the buffer amplifiers 52 has a low resistance to ground, which act as means for comparing the outputs of the counters (or decoder 34) with the settings of the switches 55, for a logic "0" and a high resistance for a logic "1." For example, if the timer is set to time out at one second operating at 60 cycles per second, all of the switches 55 will be open except switch 55 *i*. The plug of assembly PL-1 will be put into the "seconds" socket so that terminal 17 will be grounded and therefore a "0" will appear at it. If the plug in PL2 is in the 60 cycles position, terminal 26 will be at -27 volts (a logic "1") so that the buffer amplifier 32 applies a "1" to decoder 34 and divider 35. When timing is started by closure of the switch SW1, capacitor C1 begins to charge and power is applied to the reset pulse generator B. The reset pulse generator functions as previously explained to set all the counters to "0" and thereafter, after the Zener diode CR3 conduct all the counters and other circuits of the I/C 30 are enabled to begin counting. After reset has been accomplished, the inputs to the ROM 50 are as follows:

$d=1$ (always at -27v.)
 $c=0$ (Q2 is on)
 $b=1$ (grounded and inverted)
 $a=0$

The input terminal *a* is "0" since switch 55 *i* is closed and 52 *i* is at "0" having just been reset. The "1" place (or "1" bit) output line of divider 37 connected thereto is at "0" because it has not yet started to count. Reference is now made to the following Table 2 which is the "truth table" for the ROM 50.

TABLE 2

Inputs	Outputs	Inputs	Outputs
<i>abcd</i>	<i>efg</i>	<i>abcd</i>	<i>efg</i>
0000	011	0001	010
1000	110	1001	000
0100	010	0101	011
1100	111	1101	110
0010	001	0011	001

TABLE 2-Continued

Inputs	Outputs	Inputs	Outputs
1010	001	1011	001
0110	001	0111	001
1110	001	1111	001

With the starting condition as stated above for input terminals *a*, *b*, *c* and *d*, it is seen that the output terminals *e*, *f*, *g* are at 0, 1, and 1. Since the terminal *e* is at 0, the NOR circuit 48 permits the 120 Hertz signal to be applied to the divider 33 and counting may begin. The "1" appearing at the terminal *f* is inverted to "0" by the inverting buffer amplifier 49 so that when applied to the dividers 33, 35, 36, 37 and 38 they are not reset. The "1" at terminal *g* is inverted by buffer amplifier 51 so that a "0" is applied to transistor Q4 and renders it non-conductive so that output relay coil RL-2 is not energized. Since the terminal 17 is at "0", the divider 33 is enabled to begin counting by ones the 120 Hz wave at the output of NOR circuit 48. These same pulses are applied to divider 35 which is linked to divider 36 and counting at their respective inputs proceeds. The timing operation continues until the first "carry" pulse is issued by divider 36. This produces a signal in the output line of divider 37 corresponding to the least significant binary place. This output line is connected to the buffer amplifier 52 *i* that is connected to the digital switch 55 *i*. Until this happens, all of the bus 60 is at ground potential. As soon as amplifier 52 *i* receives the "1" signal, it becomes non-grounded and the bus 60 goes to -27 volts. This makes terminal *a* of ROM 50 go to a logic 1. Thus, the terminals of the ROM are then as follows:

$a=1$
 $b=1$
 $c=0$
 $d=1$

Therefore, the output terminals are as follows:

$e=1$
 $f=1$
 $g=0$

When this happens, relay coil RL2 is actuated and the timing cycle, is terminated. Simultaneously, the timing operation is disabled by the application of a "1" from terminal *e* to one input of NOR gate 48 which thereupon blocks passage of the 120 Hz signal through it. However, the reset is not activated because the "1" on terminal *f* is inverted by inverting amplifier 49 to a "0". Opening switch SW1 deenergizes the relay completing the cycle.

General Comments

When the circuit is used for counting, the clock pulse generator C is disconnected and, instead, the pulses to be counted are applied to terminal 19 of I/C 30. If the setting of plug-socket assembly PL 3 is as shown in FIG. 1, the signal applied to be counted at the input to divider 33 will be reversed in polarity as compared with its appearance at terminal 19. If the plug of that assembly is connected to ground, the signal at the input to divider 33 will have the same polarity as it did at terminal 19.

When the circuit is operated as a timer with a 50 Hz line voltage, the assembly PL 2 is set with the plug grounded. This causes a "0" to appear at terminal 26 and this disables the decoder 34. That "0" will also

cause divider 35 to operate in the "divide by ten" mode on the 100 Hz signal applied to terminal 19.

In order to use the circuit for interval timing rather than for delayed timing, the terminal 23 may be grounded instead of being connected to -27 volts. If this is done, the relay coil RL 2 will be energized during the desired interval, but not before and after.

The decimal binary switches 55 may be, for example, of the type shown in U.S. Pat. No. 3,497,138 of Fisher or could be modifications of the wheels shown in U.S. Pat. No. 3,100,299 issued to Congdon. Another suitable type of switch is shown in the co-pending application of Donald H. Ross, Ser. No. 251,922, filed May 10, 1972, which is assigned to the same assignee as this invention, and now abandoned.

I claim:

1. A timing or counting system comprising:

- a. a source of an AC signal having a predetermined frequency,
- b. a non-decimal modulus binary digital counting means to which said source frequency is applied,
- c. a series of binary digital counting means to which said non-decimal modulus counting means is coupled,
- d. a plurality of sets of switching means coupled to a voltage source and being settable to a plurality of conditions in which they produce a binary signal corresponding to selected decimal numbers,
- e. a plurality of variable conductive means respectively coupled to said sets of switching means,
- f. conversion means coupled to said non-decimal modulus counter and to the one of said sets of switching means associated with the counting of the least significant figure of a selected decimal number, said conversion means converting the output binary count of said non-decimal modulus counter to a binary number count having a decimal modulus, the others of said sets of switching means being coupled to the series of binary counting means which are associated with the more signifi-

cant figures of said selected decimal number.

2. The system according to claim 1 wherein said (b) means includes a means for dividing the frequency of the signal by 12 and wherein said (c) means includes a divider by 60 and a predetermined number of dividers by 10, all of said dividers being serially connected.

3. A timing or counting system operable from an AC voltage source comprising:

- a. means for multiplying the frequency of said AC voltage,
 - b. a non-decimal modulus binary digital counting means to which said frequency-multiplied AC voltage is applied,
 - c. a series of binary digital counting means to which said first-mentioned counting means is coupled,
 - d. a plurality of sets of switching means coupled to another voltage source and being settable to a plurality of conditions in which they produce binary signals corresponding to selected decimal numbers,
 - e. a plurality of variable conductive means coupled to said sets of switching means,
 - f. conversion means coupled to said non-decimal modulus counter and to the one of said sets of switching means associated with the counting of the least significant figure of a selected decimal number, said conversion means converting the output binary count of said non-decimal modulus counter to a binary number count having a decimal modulus,
- the others of said (d) means being coupled to the counters associated with the more significant figures of said selected number.

4. The system according to claim 3 wherein said conversion means is coupled to said one of said sets of switching means through the variable conductive means associated therewith and wherein the others of said switching means are coupled to their respective associated counters through corresponding associated ones of said variable conductive means.

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