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[Continued on next page]

- (54) Title: MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES

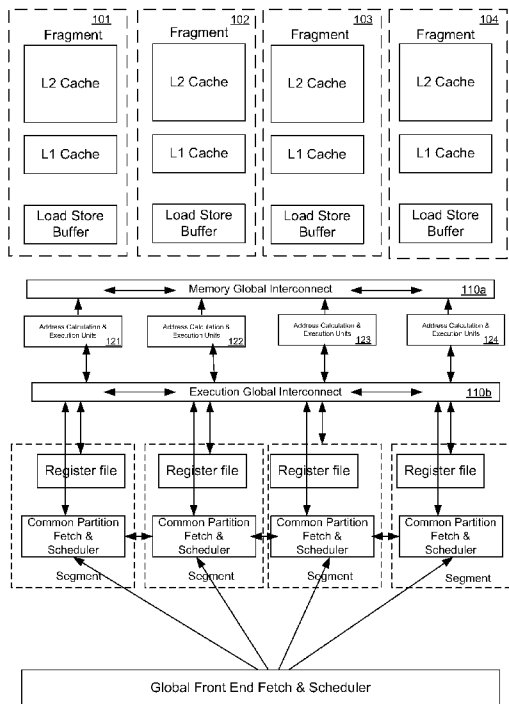


FIG. 1B

(57) Abstract: A system for executing instructions using a plurality of memory fragments for a processor. The system includes a global front end scheduler for receiving an incoming instruction sequence, wherein the global front end scheduler partitions the incoming instruction sequence into a plurality of code blocks of instructions and generates a plurality of inheritance vectors describing interdependencies between instructions of the code blocks. The system further includes a plurality of virtual cores of the processor coupled to receive code blocks allocated by the global front end scheduler, wherein each virtual core comprises a respective subset of resources of a plurality of partitionable engines, wherein the code blocks are executed by using the partitionable engines in accordance with a virtual core mode and in accordance with the respective inheritance vectors. A plurality memory fragments are coupled to the partitionable engines for providing data storage.

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## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2012/030409****A. CLASSIFICATION OF SUBJECT MATTER***G06F 9/06(2006.01)i, G06F 9/30(2006.01)i, G06F 12/08(2006.01)i, G06F 15/76(2006.01)i*

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

G06F 9/06; G06F 9/02; G06F 15/80; G06F 9/46; G06F 9/45; G06F 9/50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models  
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: instruction partition dependencies, memory fragment, inheritance vector;

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011-0067016 A1 (MIZRACHI SHAY et al.) 17 March 2011 See abstract, paragraph [0117], claim 1, and figure 5.	1-24
A	US 6948172 B1 (DAVID D'SOUZA) 20 September 2005 See abstract, column 4, lines 42-50, column 6, lines 45-60, claim 2, and figure 4.	1-24
A	US 2009-0113170 A1 (ABDALLAH MOHAMMAD A) 30 April 2009 See abstract, paragraphs [0038]-[0040].	1-24
A	WO 2009-101563 A1 (NXP B.V. et al.) 20 August 2009 See abstract, pages 1-2, and claim 1.	1-24

 Further documents are listed in the continuation of Box C. See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2012/030409**

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