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(71) Applicant *(for all designated States except US)*: **MOSAID TECHNOLOGIES INCORPORATED** [CA/CA]; 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **KIM, Jin-Ki** [CA/CA]; 46 Ironside Court, Kanata, Ontario K2K 3H6 (CA).

(74) Agents: **HAMMOND, Daniel** et al.; MOSAID Technologies Incorporated, 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

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(54) Title: SOLID STATE DRIVE OR OTHER STORAGE APPARATUS THAT INCLUDES A PLURALITY OF ENCAPSULATED SEMICONDUCTOR CHIPS

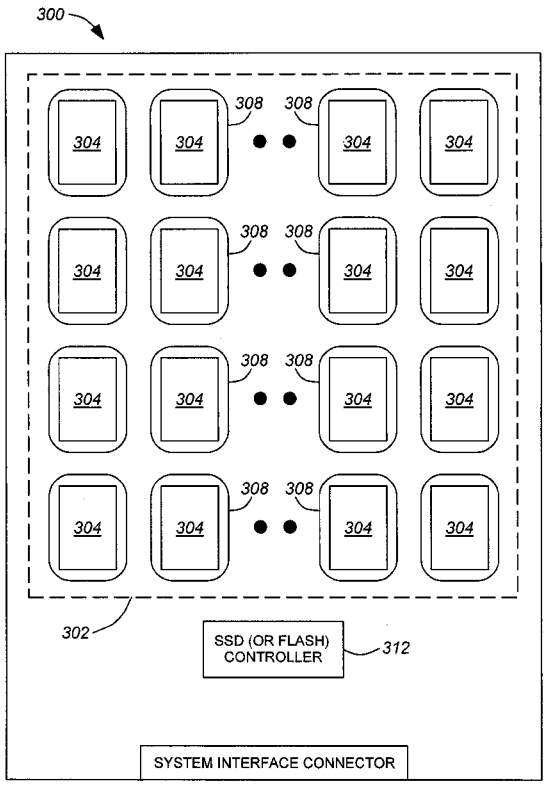

FIG. 5

(57) Abstract: A solid state drive is disclosed. The solid state drive includes a circuit board having opposing first and second surfaces. A plurality of semiconductor chips are attached to the first surface of the circuit board of the solid state drive, and the plurality of semiconductor chips of the solid state drive include at least one memory chip that is at least substantially encapsulated in a resin. An in-line memory module-type form factor circuit board is also disclosed. The in-line memory module-type form factor circuit board has opposing first and second surfaces. A plurality of semiconductor chips are attached to the first surface of the in-line memory module-type form factor circuit board, and these semiconductor chips include at least one memory chip that is at least substantially encapsulated in a resin.

WO 2010/054478 A1

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SOLID STATE DRIVE OR OTHER STORAGE APPARATUS THAT INCLUDES A PLURALITY OF ENCAPSULATED SEMICONDUCTOR CHIPS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority of U.S. Provisional Patent Application Serial No. 61/114,154 filed November 13th, 2008, and also U.S. Patent Application Serial No. 12/367,056 filed February 6th, 2009, and these patent applications are incorporated herein by reference in their entireties.

BACKGROUND OF THE DISCLOSURE

[0002] Chip-On-board (COB) technology involves mounting (integrating) an Application Specific Integrated Circuit (ASIC), processor, memory semiconductor die, or other die/chip directly on a substrate (typically the printed circuit board) without the need for a packaged component. In addition to the die bonding, the process of integrating the die/chip may include the wire bonding, and possibly testing before or after encapsulation.

[0003] As will be appreciated by those skilled in the art, COB technology can help achieve high integration density. For example, eliminating the Thin Small-Outline Package (TSOP) or Fine-Pitch Ball Grid Array (FBGA) component package reduces the required substrate area and assembly weight. The saving in area can be as much as 20% in some cases. Using conventional Printed Circuit Boards (PCBs) and standard wire bonding technology, COB technology can yield very substantial weight and volume reduction. COB technology also reduces the number of interconnects between an active die and the substrate (i.e., the package pins), which improves the overall circuit speed, leads to higher clock rates, better electrical performance and improved signal quality, and increases the overall reliability of the module. Also, unlike other types of packaging, COB packaging is a Chip Scalable Packaging (CSP), meaning the packaging

is not as limited by dimensioning and size standards as, for example, TSOP packaging. Additional benefits of COB packaging include better protection against reverse-engineering and, in some instances, elimination of soldering associated with conventional packaging.

[0004] Those skilled in the art will appreciate that, in connection with various COB processes, a coating of an epoxy encapsulent (or glob top) is applied for hermetically sealing and protecting the die and the wire bonded interconnections. The glob top also acts like a heat spreader between dies, improves heat emission, adds low Coefficients of Thermal Expansion (CTEs), and provides a hermetically sealed module assembly. The die may be glued directly to the PCB, and therefore increased heat dissipation from the die through the PCB is provided for.

[0005] Because COB technology is less pervasive in semiconductor manufacturing as compared to other conventional technologies, there exist gaps in research and development efforts with respect to systems that derive benefit from COB technology. Accordingly, there is a need for improved systems that are characterized by COB technology.

SUMMARY

[0006] It is an object of the invention to provide an improved system that includes at least one encapsulated memory chip.

[0007] According to one aspect of the invention, there is provided a solid state drive that includes a circuit board having opposing first and second surfaces. A plurality of semiconductor chips are attached to the first surface. The plurality of semiconductor chips include at least one memory chip that is at least substantially encapsulated in a resin. A controller is in communication with at least a number of the plurality of semiconductor chips. The number of semiconductor chips includes the at least one memory chip. The controller includes an interface that receives, from a computer system, signals for processing within the solid state drive.

[0008] According to another aspect of the invention, there is provided an apparatus that includes an in-line memory module-type form factor circuit board having

opposing first and second surfaces. A plurality of semiconductor chips are attached to the first surface. The plurality of semiconductor chips includes at least one memory chip that is at least substantially encapsulated in a resin. A controller is in communication with the at least one memory chip. The controller includes an interface that receives signals comprising commands and data that effect operations within the at least one memory chip.

[0009] According to yet another aspect of the invention, there is provided a computer system that includes a main enclosure and a solid state drive. The solid state drive includes a housing and a circuit board that is within the housing and has opposing first and second surfaces. A plurality of semiconductor chips are attached to the first surface. The plurality of semiconductor chips include at least one memory chip that is at least substantially encapsulated in a resin. A controller is within the housing and is in communication with at least a number of the plurality of semiconductor chips. The number of semiconductor chips include the at least one memory chip, and the controller includes an interface that receives signals for processing within the solid state drive. The computer system also includes means for providing the signals to the interface. The solid state drive and the providing means are both within the main enclosure.

[0010] Thus, an improved solid state drive and other storage apparatuses have been provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Reference will now be made, by way of example, to the accompanying drawings:

[0012] FIG. 1 is a diagram of an example computing device;

[0013] FIG. 2 is a diagram of an example PCB for a Solid State Drive (SSD);

[0014] FIG. 3 is a diagram of a top front portion of an example desktop computer;

[0015] FIG. 4 is a diagram providing further detail of the controller shown in FIG. 2;

[0016] FIG. 5 is a diagram of a PCB for an SSD in accordance with an example embodiment;

[0017] FIG. 6 is a diagram of a PCB for an SSD in accordance with another example embodiment;

[0018] FIG. 7 is a diagram of a PCB for an SSD in accordance with another example embodiment;

[0019] FIG. 8 is a diagram of a PCB for an SSD in accordance with another example embodiment;

[0020] FIG. 9 is a diagram of a PCB for an SSD in accordance with another example embodiment;

[0021] FIG. 10 is a diagram of a PCB in accordance with another example embodiment, the illustrated PCB having an in-line memory module-type form factor;

[0022] FIG. 11 is a diagram of a PCB in accordance with another example embodiment, the illustrated PCB having an in-line memory module-type form factor;

[0023] FIG. 12 is a diagram of a PCB in accordance with another example embodiment, the illustrated PCB having an in-line memory module-type form factor;

[0024] FIG. 13 is a diagram of a PCB area in accordance with an example embodiment, the illustrated area being, in some examples, a part of a larger area of a PCB for an SSD;

[0025] FIG. 14 is a diagram of a PCB area in accordance with another example embodiment, the illustrated area being, in some examples, a part of a larger area of a PCB for an SSD;

[0026] FIG. 15 is a diagram of a PCB area in accordance with another example embodiment, the illustrated area being, in some examples, a part of a larger area of a PCB for an SSD;

[0027] FIG. 16 is a diagram of a PCB area in accordance with another example embodiment, the illustrated area being, in some examples, a part of a larger area of a PCB for an SSD;

[0028] FIG. 17 is a diagram of a PCB area in accordance with another example embodiment, the illustrated area being, in some examples, a part of a larger area of a PCB for an SSD;

[0029] FIG. 18 is a diagram of a PCB area in accordance with another example embodiment, the illustrated area being, in some examples, a part of a larger area of a PCB for an SSD;

[0030] FIG. 19 is a diagram of a PCB area in accordance with another example embodiment, the illustrated area being, in some examples, a part of a larger area of a PCB for an SSD;

[0031] FIG. 20 is a diagram of a PCB area in accordance with another example embodiment, the illustrated area being, in some examples, a part of a larger area of a PCB for an SSD;

[0032] Similar or the same reference numerals may have been used in different figures to denote similar example features illustrated in the drawings.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0033] Mass data storage systems in accordance with embodiments of the present invention can be incorporated into numerous types of computing devices, including desktop computers, laptops, netbooks, tablet PCs, servers (including web servers and mainframes) and mobile electronic communication devices, to name a few non-limiting possibilities.

[0034] Reference is made to FIG. 1, which shows a computing device 100 such as, for example, a desktop computer, a laptop, a netbook, a tablet PC, a server (for instance, a web server or a mainframe), a mobile electronic communication device, etc. The device 100 includes a processor 112 that processes data signals. The processor 112 may be a Complex Instruction Set Computer (CISC) microprocessor, a Reduced Instruction Set Computing (RISC) microprocessor, a Very Long Instruction Word (VLIW) microprocessor, a processor implementing a combination of instruction sets, or other processor device. The processor 112 can be a single-core or multi-core processor. Also, not excluded is the possibility of there being multiple processors, similar to the processor 112, in the computing device 100.

[0035] The processor 112 is electrically connected to a Memory Controller Hub (MCH) 114, which interfaces to a main memory 116. The main memory 116 may be a

Dynamic Random Access Memory (DRAM) device, a Synchronous Dynamic Random Access Memory (SDRAM) device, or other high speed volatile memory device. The main memory 116 may store instructions and code that are executable by the processor 112.

[0036] The MCH 114 also interfaces to an I/O Controller Hub (ICH) 118, which is electrically connected to a bus 120 that transmits data signals between the I/O Controller Hub (ICH) 118 and other components electrically connected to the bus 120. The bus 120 may be a single bus or a combination of multiple buses. As an example, the bus 120 may comprise a Peripheral Component Interconnect (PCI) bus, a PCI-Express bus, a Serial ATA bus, a Personal Computer Memory Card International Association (PCMCIA) bus, other buses or combinations thereof.

[0037] The bus 120 provides communication links among components in the computing device 100. Specifically, a display device controller 122 is electrically connected to the bus 120. The display device controller 122 permits use of a display device 132 and acts as an interface between the display device 132 (or a frame buffer thereof) and a remainder of the computing device 100. The display device controller 122 may be a Monochrome Display Adapter (MDA) card, a Color Graphics Adapter (CGA) card, an Enhanced Graphics Adapter (EGA) card, an Extended Graphics Array (XGA) card or other display device controller. The display device 132 may be integrated to the computing device 100 but it may also be an external device such as, for example, a television set, a computer monitor, a flat-panel display or other suitable display device coupled to the computing device 100 via a port or cable. The display device 132 receives data signals from the processor 112 through the display device controller 122 and converts the data signals into a visual output presented to the user of the computing device 100.

[0038] In addition, a further interface controller 124 is electrically connected to the bus 120. The further interface controller 124 is electrically connected to one or more further peripheral device(s) 134 such as, for example, a keyboard, mouse, network device or audio device.

[0039] In addition, a data storage system 126 is electrically connected to the bus 120. The data storage system 126 comprises a controller 128 (for example, an SSD controller) and a solid state memory system 130 (example embodiments of which will be subsequently described). The data storage system 126 may store large quantities of data that may be accessed by the processor 112.

[0040] Referring now to FIG. 2, illustrated in diagrammatic form is a PCB 200 for a conventional example of the data storage system 126. Now in connection with Hard Disk Drives (HDDs), which are the predecessor of SSDs, these are known to be manufactured in accordance with any of a limited number of form factors (i.e. physical dimensions). The 1.8", 2.5" and 3.5" form factors are example standards. Also, height is not necessarily the same between two HDDs of the same form factor. For instance, a so-called "half-height" HDD in compliance with the 3.5" form factor standard would be expected to have dimensions of 4.0" width, 5.75" depth, and 1.63" height; however a so-called "low-profile" HDD in compliance with the 3.5" form factor standard would be expected to have dimensions of 4.0" width, 5.75" depth, and 1.0" height.

[0041] Interestingly, it is currently advantageous to continue to follow these existing form factor standards when manufacturing SSDs. A reason for this is that by complying with the existing form factor standards, drop-in SSD replacement of existing HDDs within computing devices is typically better facilitated. Shown in FIG. 3 is a desktop computer 232 which includes a bay 233. A rectangular shaped housing 235 is sized for insertion into the bay 233. Received within the rectangular shaped housing 235 would be a PCB such as, for example, the PCB 200 shown in FIG. 2. Also, although in the illustrated example a desktop computer is shown, those skilled in the art will appreciate that there exist other types of computing devices that include similar bays such as, for example, laptop computers.

[0042] As discussed above, it is currently advantageous to follow existing HDD form factor standards when manufacturing SSDs. It will be understood however that flash memory devices offer significant flexibility in terms of spatial arrangement, and therefore there may be a variety of different form factors that may possibly gain acceptance in flash storage systems in the not too distant future.

[0043] Still with reference to FIG. 2, the PCB 200 includes an area 202. It is at least primarily within the PCB area 202 that the solid state memory system 130 (FIG. 1) is found. The solid state memory system of the illustrated example takes the form of an implementation that includes a plurality of rows and columns of packaged chips 204. These packaged chips 204 include a plurality of pins that may be connected to electrical paths of the PCB 200 in a conventional manner such as, for example, by way of soldering. (For diagrammatic simplicity, above-referred to pins of the packaged chips 204 and electrical paths of the PCB 200 have not been illustrated.)

[0044] Attached at or proximate edge 228 of the PCB 200 is a system interface connector 230. Signals that are originating or destined to other parts of the computing device incorporating the data storage system, and that are transmitted to or from the PCB 200 travel through the system interface connector 230. The system interface connector 230 may be connected to, for example, one end of a ribbon cable, another end of which may in turn be connected to the bus 120 shown in FIG. 1.

[0045] Also shown on the PCB 200 is the SSD controller 128. Although the SSD controller 128 that is shown in FIG. 2 is a single monolithic chip, in alternative examples the SSD controller 128 may comprise multiple chips. The SSD controller 128 in accordance with some examples is shown in more detail in the diagram of FIG. 4.

[0046] As shown in FIG. 4, the SSD controller 128 is provided a base clock signal from a crystal (Xtal) 250. The crystal 250 is connected to a clock generator and control component 252. The clock generator and control component 252 provides various clock signals to a Central Process Unit (CPU) 254, a control module 256, and a physical layer transceiver 258 (Serial ATA PHY in the illustrated example). The CPU 254 communicates with other subsystems by a common bus 260. The control module 256 includes a physical flash interface 264, an Error Correcting Code (ECC) component 266, and a file and memory management component 268. Flash devices within the solid state memory system 130 are accessed through the physical flash interface 264. Accessed data from these flash devices are checked and corrected by the ECC component 266. The file and memory management component 268 provides logical-to physical address translation, wear-leveling algorithm, etc.

[0047] Also shown within the illustrated SSD controller 128 are Random Access Memory and Read Only Memory 270 (RAM & ROM 270). The RAM is used as buffer memory and the ROM stores executable codes (i.e. firmware). In some examples, the RAM & ROM 270 may be integral to the SSD controller 128. In alternative examples, the RAM & ROM 270 may be separate component(s). For instance, the SSD controller 128 might be implemented as a System-on-Chip (SoC) but with the RAM & ROM 270 as separate chip(s).

[0048] Finally, there is additionally shown a SATA controller 280. The SATA controller 280 controls operation of the SATA transceiver in a manner well known to those skilled in the art. Also, an interface 290 is provided for connectivity to other parts of the computing device incorporating the data storage system. Although the interface 290 may be a SATA interface, those skilled in the art will be aware of other suitable alternative interface such as, for example, PATA interface, eSATA interface, USB interface, SCSI interface, PCIe interface, Serial Attached SCSI (SAS) interface.

[0049] Referring now to FIG. 5, illustrated in diagrammatic form is a PCB 300 in accordance with an example embodiment. Within an area 302 of the PCB 300, there exists a plurality of rows and columns of memory chips 304. As contrasted with the PCB area 202 of the PCB 200 shown in FIG.2, each individual memory chip 304 within the PCB area 302 is not within a conventional package, but is rather within a corresponding (respective) encapsulation 308, and hence memory chips are provided on the PCB 300 in accordance with COB technology. In the illustrated example embodiment a controller 312 is outside of the area 302 and is not encapsulated; however alternatively the controller 312 may be encapsulated as well. In summary, a data storage system in accordance with the example embodiment of FIG. 5 is similar to a data storage system in accordance with the example of FIG. 2, with a primary difference being that the former inventively incorporates COB technology, whereas the latter does not.

[0050] Referring now to FIG. 6, illustrated in diagrammatic form is a PCB 500 in accordance with an example embodiment. Within an area 502 of the PCB 500, there exists a plurality of rows and columns of memory chips 504. Also, each row is within a

corresponding (respective) encapsulation 508. A controller 512 is outside of the area 502 and is not encapsulated. In summary, the example embodiment of FIG. 6 is similar to the example embodiment of FIG. 5, with a primary difference being that in the former each row is within the respective encapsulation 508 of the row, whereas in the later each of the memory chips 304 is within the respective encapsulation of the individual chip.

[0051] Referring now to FIG. 7, illustrated in diagrammatic form is a PCB 550 in accordance with another example embodiment. Within an area 552 of the PCB 550, there exists a plurality of rows and columns of memory chips 554. Also, each column is within a corresponding (respective) encapsulation 558. A controller 562 is outside of the area 552 and is not encapsulated. Thus, the example embodiment of FIG. 7 is similar to the example embodiment of FIG. 6, with a primary difference being that in the former each column is within the respective encapsulation 558 of the column, whereas in the later each row is within the respective encapsulation of the row.

[0052] Referring now to FIG. 8, illustrated in diagrammatic form is a PCB 600 in accordance with another example embodiment. Within an area 602 of the PCB 600, there exists a plurality of rows and columns of memory chips 604. Also, all rows and columns are within a single encapsulation 608. A controller 612 is outside of the area 602 and is not encapsulated. In summary, the example embodiment of FIG. 8 is similar to the example embodiment of FIG. 7, with a primary difference being that in the former all rows and columns are within the single encapsulation 608, whereas in the later each column is within the respective encapsulation of the column.

[0053] Referring now to FIG. 9, illustrated in diagrammatic form is a PCB 650 in accordance with another example embodiment. Within an area 652 of the PCB 650, there exists a plurality of rows and columns of memory chips 654. Also, all rows and columns are within a single encapsulation 658. A controller 662 is outside of the area 652 and is encapsulated within the encapsulation 658. Thus, the example embodiment of FIG. 9 is similar to the example embodiment of FIG. 8, with a primary difference being that in the former the controller is within the encapsulation, whereas in the latter

the controller is not encapsulated but may instead be within, for instance, conventional chip packaging.

[0054] Referring now to FIG. 10, illustrated is a PCB 750 in accordance with another example embodiment, and the PCB 750 having an in-line memory module-type form factor. Within an area 752 of the PCB 750, there exists a row of memory chips 754, with each individual memory chip encapsulated in a corresponding (respective) encapsulation 758. A controller 762 outside of the area 752 is not encapsulated.

[0055] Referring now to FIG. 11, illustrated is a PCB 800 in accordance with another example embodiment, and the PCB 800 having an in-line memory module-type form factor. Within an area 802 of the PCB 800, there exists a row of memory chips 804, with each individual memory chip encapsulated in a corresponding (respective) encapsulation 808. A controller 812 is outside of the area 802 and is encapsulated in a respective encapsulation 813.

[0056] Referring now to FIG. 12, illustrated is a PCB 850 in accordance with another example embodiment, and the PCB 850 having an in-line memory module-type form factor. Within an area 852 of the PCB 850, there exists a row of memory chips 854, with the entire row encapsulated within an encapsulation 858. A controller 862 outside of the area 852 is encapsulated within the encapsulation 858.

[0057] Referring now to FIG. 13, illustrated is a PCB area 900 in accordance with an example embodiment. It should be noted that, in some examples, the illustrated PCB area 900 can correspond to a flash chip area similar to any of those shown in dashed lines in any of FIGS. 5 through 9; however it will be understood that the presently described example embodiment is not limited to only PCBs that are employed in SSDs. Within the PCB area 900, there is a plurality of series-connected interface chips 904, such that the illustrated system may be characterized as having a ring-type architecture. In connection with data transmissions occurring within some examples of the illustrated system, data may be transmitted from one of the interface chips 904 to a neighboring interface chip in a manner as described in commonly owned US Patent Application Serial No. 12/033,577 entitled "SYSTEM HAVING ONE OR MORE MEMORY DEVICES", the entire contents of which are incorporated herein by

reference. In alternative examples of the illustrated system, data transmission between different ring stages may be realized in some other suitable manner.

[0058] Still with reference to FIG. 13, each of the interface chips 904 is electrically connected to a corresponding (respective) NAND flash chip 908. Also, it will be understood that at each stage (segment) of the illustrated ring there is a NAND flash chip-interface chip pair. Each NAND flash chip-interface chip pair is within a corresponding (respective) encapsulation 912. In connection with data transmissions occurring between chips of a chip pair, data may be transmitted from the NAND flash chip 908 to the interface chip 904 (or vice-versa) in the typical manner associated with asynchronous NAND. Alternatively, in other examples these data transmissions will occur in some other manner such as, for instance, synchronously as described in "Open NAND Flash Interface Specification", Revision 2.0, Feb. 27, 2008 (ONFi 2.0 spec.). Those skilled in the art will appreciate that the ONFi 2.0 spec. is compatible with a so-called "multi-drop bus" topology. In such a topology, it is typical for all signal paths, such as, for example, those for input, output and control signals, but with the exception of chip enable signals, to be provided by a common bus. The controller can access each memory device via the common bus, and (assuming only one channel) only a single memory device can be selected at one time by assertion of a chip enable signal on the device.

[0059] Referring now to FIG. 14, illustrated is a PCB area 950 in accordance with another example embodiment. It should be noted that, in some examples, the illustrated PCB area 950 can correspond to a flash chip area similar to any of those shown in dashed lines in any of FIGS. 5 through 9; however it will be understood that the presently described example embodiment is not limited to only PCBs that are employed in SSDs. Within the PCB area 950, there is a plurality of series-connected interface chips 954, such that the illustrated system may be characterized as having a ring-type architecture. In connection with data transmissions occurring within some examples of the illustrated system, data may be transmitted from one of the interface chips 954 to a neighboring interface chip in a manner as described in US Patent Application Serial No. 12/033,577 entitled "SYSTEM HAVING ONE OR MORE

MEMORY DEVICES". In alternative examples of the illustrated system, data transmission between different ring stages may be realized in some other suitable manner.

[0060] Still with reference to FIG. 14, each of the interface chips 954 communicates with a corresponding (respective) NAND flash chip 958 via electrical paths provided by the PCB. Also, it will be understood that at each stage (segment) of the illustrated ring there is a NAND flash chip-interface chip pair. Each NAND flash chip-interface chip pair is encapsulated within a corresponding (respective) encapsulation 962. In connection with data transmissions occurring between chips of a chip pair, data may be transmitted from the NAND flash chip 958 to the interface chip 954 (or vice-versa) in the typical manner associated with asynchronous NAND. Alternatively, in other examples these data transmissions will occur in some other manner such as, for instance, synchronously as described in the ONFi 2.0 spec.

[0061] Referring now to FIG. 15, illustrated is a PCB area 1000 in accordance with another example embodiment. It should be noted that, in some examples, the illustrated PCB area 1000 can correspond to a flash chip area similar to any of those shown in dashed lines in any of FIGS. 5 through 9; however it will be understood that the presently described example embodiment is not limited to only PCBs that are employed in SSDs. Within the PCB area 1000, there is a plurality of series-connected interface chips 1004, such that the illustrated system may be characterized as having a ring-type architecture in which there are a plurality of stages. In connection with data transmissions occurring within some examples of the illustrated system, data may be transmitted from one of the interface chips 1004 to a neighboring interface chip in a manner as described in US Patent Application Serial No. 12/033,577 entitled "SYSTEM HAVING ONE OR MORE MEMORY DEVICES". In alternative examples of the illustrated system, data transmission between different ring stages may be realized in some other suitable manner.

[0062] Still with reference to FIG. 15, each of the interface chips 1004 is electrically connected to a corresponding (respective) NAND flash chip 1008. A first group of NAND flash chips 1008 and interface chips 1004 (in the illustrated example

embodiment, four and four for a total of eight) are encapsulated within an encapsulation 1012. A second group of NAND flash chips 1008 and interface chips 1004 (in the illustrated example embodiment, four and four for a total of eight) are encapsulated within another encapsulation 1014. In the illustrated example embodiment therefore, half of the eight stages of the ring are within the encapsulation 1012, and the other half of the eight stages of the ring are within the encapsulation 1014. In connection with data transmissions occurring between chips belonging to the same ring stage, data may be transmitted from the NAND flash chip 1008 to the interface chip 1004 (or vice-versa) in the typical manner associated with asynchronous NAND. Alternatively, in other examples these data transmissions will occur in some other manner such as, for instance, synchronously as described in the ONFi 2.0 spec.

[0063] Referring now to FIG. 16, illustrated is a PCB area 1050 in accordance with another example embodiment. It should be noted that, in some examples, the illustrated PCB area 1050 can correspond to a flash chip area similar to any of those shown in dashed lines in any of FIGS. 5 through 9; however it will be understood that the presently described example embodiment is not limited to only PCBs that are employed in SSDs. Within the PCB area 1050, there is a plurality of series-connected interface chips 1054, such that the illustrated system may be characterized as having a ring-type architecture. In connection with data transmissions occurring within some examples of the illustrated system, data may be transmitted from one of the interface chips 1054 to a neighboring interface chip in a manner as described in US Patent Application Serial No. 12/033,577 entitled "SYSTEM HAVING ONE OR MORE MEMORY DEVICES". In alternative examples of the illustrated system, data transmission between different ring stages may be realized in some other suitable manner.

[0064] Still with reference to FIG. 16, each of the interface chips 1054 is electrically connected to a corresponding (respective) NAND flash chip 1058. Also, each of the interface chips 1054 is stacked on their corresponding NAND flash chip 1058. Also, it will be understood that at each stage (segment) of the illustrated ring there is a NAND flash chip-interface chip pair (stack of two chips). Each NAND flash

chip-interface chip pair is encapsulated within a corresponding (respective) encapsulation 1062. With respect to data transmissions occurring between chips belonging to the same ring stage (i.e. stack), data may be transmitted from the NAND flash chip 1058 to the interface chip 1054 (or vice-versa) in the typical manner associated with asynchronous NAND. Alternatively, in other examples these data transmissions will occur in some other manner such as, for instance, synchronously as described in the ONFi 2.0 spec.

[0065] Referring now to FIG. 17, illustrated is a PCB area 1100 in accordance with another example embodiment. It should be noted that, in some examples, the illustrated PCB area 1100 can correspond to a flash chip area similar to any of those shown in dashed lines in any of FIGS. 5 through 9; however it will be understood that the presently described example embodiment is not limited to only PCBs that are employed in SSDs. Within the PCB area 1100, there is a plurality of series-connected interface chips 1104, such that the illustrated system may be characterized as having a ring-type architecture in which there are a plurality of stages. In connection with data transmissions occurring within some examples of the illustrated system, data may be transmitted from one of the interface chips 1104 to a neighboring interface chip in a manner as described in US Patent Application Serial No. 12/033,577 entitled "SYSTEM HAVING ONE OR MORE MEMORY DEVICES". In alternative examples of the illustrated system, data transmission between different ring stages may be realized in some other suitable manner.

[0066] Still with reference to FIG. 17, each of the interface chips 1104 is electrically connected to a corresponding (respective) NAND flash chip 1108. Also, each of the interface chips 1104 is stacked on their corresponding NAND flash chip 1108. A first group of NAND flash chips 1108 and interface chips 1104 (in the illustrated example embodiment, four and four for a total of eight) are encapsulated within an encapsulation 1112. A second group of NAND flash chips 1108 and interface chips 1104 (in the illustrated example embodiment, four and four for a total of eight) are encapsulated within another encapsulation 1114. In the illustrated example embodiment therefore, half of the eight stages of the ring are within the encapsulation

1112, and the other half of the eight stages of the ring are within the encapsulation 1114. In connection with data transmissions occurring between chips belonging to the same ring stage (i.e. stack), data may be transmitted from the NAND flash chip 1108 to the interface chip 1104 (or vice-versa) in the typical manner associated with asynchronous NAND. Alternatively, in other examples these data transmissions will occur in some other manner such as, for instance, synchronously as described in the ONFi 2.0 spec.

[0067] Referring now to FIG. 18, illustrated is a PCB area 1150 in accordance with another example embodiment. It should be noted that, in some examples, the illustrated PCB area 1150 can correspond to a flash chip area similar to any of those shown in dashed lines in any of FIGS. 5 through 9; however it will be understood that the presently described example embodiment is not limited to only PCBs that are employed in SSDs. Within the PCB area 1150, there is a plurality of series-connected interface chips 1154, such that the illustrated system may be characterized as having a ring-type architecture. In connection with data transmissions occurring within some examples of the illustrated system, data may be transmitted from one of the interface chips 1154 to a neighboring interface chip in a manner as described in US Patent Application Serial No. 12/033,577 entitled "SYSTEM HAVING ONE OR MORE MEMORY DEVICES". In alternative examples of the illustrated system, data transmission between different ring stages may be realized in some other suitable manner.

[0068] Still with reference to FIG. 18, each of the interface chips 1154 is electrically connected to each of a plurality (four in the illustrated example embodiment) of NAND flash chips 1158 in a stage. Also, each of the plurality of NAND flash chips 1158 in a stage are stacked one on top of each other, with the interface chip 1154 at the top of the stack. Eight stages are present in the illustrated ring (one stack per stage, each stack five chips in height). Each of the eight stacks is encapsulated within its own encapsulation 1162. In connection with data transmissions occurring between chips belonging to the same ring stage (i.e. stack), data may be transmitted from any one of the NAND flash chips 1158 to the interface chip 1154 (or

vice-versa) in the typical manner associated with asynchronous NAND. Alternatively, in other examples these data transmissions will occur in some other manner such as, for instance, synchronously as described in the ONFi 2.0 spec.

[0069] Referring now to FIG. 19, illustrated is a PCB area 1200 in accordance with another example embodiment. Within the PCB area 1200, there is a plurality of series-connected interface chips 1204, such that the illustrated system may be characterized as having a ring-type architecture. It should be noted that, in some examples, the illustrated PCB area 1200 can correspond to a flash chip area similar to any of those shown in dashed lines in any of FIGS. 5 through 9; however it will be understood that the presently described example embodiment is not limited to only PCBs that are employed in SSDs. In connection with data transmissions occurring within some examples of the illustrated system, data may be transmitted from one of the interface chips 1204 to a neighboring interface chip in a manner as described in US Patent Application Serial No. 12/033,577 entitled "SYSTEM HAVING ONE OR MORE MEMORY DEVICES". In alternative examples of the illustrated system, data transmission between different ring stages may be realized in some other suitable manner.

[0070] Still with reference to FIG. 19, each of the interface chips 1204 is electrically connected to each of a plurality (four in the illustrated example embodiment) of NAND flash chips 1208 in a stage. Also, each of the plurality of NAND flash chips 1208 in a stage are stacked one on top of each other, with the interface chip 1204 at the top of the stack. Eight stages are present in the illustrated ring (one stack per stage, each stack five chips in height). Also with respect to the illustrated example embodiment, a first group of four of the eight stacks are encapsulated within an encapsulation 1212, and a second group of four of the eight stacks are encapsulated within another encapsulation 1214. In connection with data transmissions occurring between chips belonging to the same ring stage (i.e. stack), data may be transmitted from any one of the NAND flash chips 1208 to the interface chip 1204 (or vice-versa) in the typical manner associated with asynchronous NAND. Alternatively, in other

examples these data transmissions will occur in some other manner such as, for instance, synchronously as described in the ONFi 2.0 spec.

[0071] Referring now to FIG. 20, illustrated is a PCB area 1250 in accordance with another example embodiment. Within the PCB area 1250, there is a plurality of series-connected interface chips 1254, such that the illustrated system may be characterized as having a ring-type architecture. It should be noted that, in some examples, the illustrated PCB area 1250 can correspond to a flash chip area similar to any of those shown in dashed lines in any of FIGS. 5 through 9; however it will be understood that the presently described example embodiment is not limited to only PCBs that are employed in SSDs. In connection with data transmissions occurring within some examples of the illustrated system, data may be transmitted from one of the interface chips 1254 to a neighboring interface chip in a manner as described in US Patent Application Serial No. 12/033,577 entitled "SYSTEM HAVING ONE OR MORE MEMORY DEVICES". In alternative examples of the illustrated system, data transmission between different ring stages may be realized in some other suitable manner.

[0072] Still with reference to FIG. 20, each of the interface chips 1254 communicates with each of a plurality (four in the illustrated example embodiment) of NAND flash chips 1258 in a stage via electrical paths provided by the PCB. Also, each of the plurality of NAND flash chips 1258 in a stage are stacked one on top of each other, with the interface chip 1254 at the top of the stack. Eight stages are present in the illustrated ring (one stack/stage, each stack five chips in height). Each of the eight stacks is encapsulated within its own encapsulation 1262. In connection with data transmissions occurring between chips belonging to the same ring stage (i.e. stack), data may be transmitted from any one of the NAND flash chips 1258 to the interface chip 1254 (or vice-versa) in the typical manner associated with asynchronous NAND. Alternatively, in other examples these data transmissions will occur in some other manner such as, for instance, synchronously as described in the ONFi 2.0 spec.

[0073] Although the example embodiments of FIGS. 16 through 20 have been described in terms of the memory chips being of a uniform type, mixed types of a

memory chips within a memory system is contemplated. For example, in connection with the example embodiments of FIGS. 16 through 20, the memory chip(s) in a first stage might include a NAND flash chip, whereas the memory chip(s) in a subsequent stage might include a DRAM chip. In connection with the example embodiments of FIGS. 18 through 20, mixed types of a memory chips within an individual stage is contemplated.

[0074] Although in FIGS. 18 through 20 the illustrated stacks are five chips in height, it will be understood that in alternative example embodiments this number will vary, and in fact stacks formed of any suitable number of chip are contemplated. For conventional packaging, stacking beyond four chips may be difficult because heat and stress become big issues. By contrast, for example embodiments herein that are characterized by COB technology, stacking even in excess of ten chips is contemplated. Those skilled in the art will appreciate that such large chip number stacking is achievable by making the dies ultra thin. In this regard, typically during semiconductor manufacturing the backside of the wafer is grinded down to bring the thickness within the range of, for example, 300-100 μm. However in connection with the production of ultra thin dies, the backside of the wafer is grinded down even further such as, for example, down to the range of 100-50 μm. Thus in connection with ultra thin dies, large chip number stacking is possible, as compared to less thin dies and having regard to heat and stress issues.

[0075] Still with reference to FIGS. 18 through 20, it will be seen that there is a staggering of the NAND flash chips to leave chip edges exposed to facilitate wiring, and it will be understood that various example embodiments are characterized by this and other inventive features disclosed in commonly owned US Patent Application Serial No. 12/168,354 entitled "DATA STORAGE AND STACKABLE CONFIGURATIONS", the entire contents of which are herein incorporated by reference.

[0076] Also, it will be understood that various alternative COB example embodiments are characterized by stacked chips that are interconnected in accordance with Through-Silicon Via (TSV) as disclosed in the above-mentioned patent application

and also commonly owned US Patent Application Serial No. 12/236,874 entitled "METHOD FOR STACKING SERIALLY-CONNECTED INTEGRATED CIRCUITS AND MULTI-CHIP DEVICE MADE FROM SAME", the entire contents of which are herein incorporated by reference. As will be appreciated by those skilled in the art, the short interconnect of through hole vias can be expected to provide less inductance, capacitance, and resistance so that signal integrity of the encapsulated stack of chips may be better than if bonding wire had been used. In some instances, the capacitive effect of each lead on a package can easily be as big as three to four picofarads, so TSV implementations may be desirable because it removes any issues associated with these capacitive effects.

[0077] Continuing on, various illustrated COB example embodiments are characterized by stacking with edge wire bonding. Although not illustrated, alternative COB example embodiments are characterized by stacking with center wire bonding.

[0078] In some examples, the interface chips shown in connection with any of the example embodiments of FIGS. 13 through 20 may operate as described in commonly owned US Provisional Patent Application Serial No. 61/111,013 entitled "SYSTEM HAVING ONE OR MORE NONVOLATILE MEMORY DEVICES", the entire contents of which are herein incorporated by reference. For instance, as described in the above-referenced application, each memory chip that communicates with an interface chip via a lower performance interface may be effectively addressed by the interface chip as a bank, with a data channel for each bank so that the number of channels between the interface chip and the banks equals the number of banks. Also, to reduce potential latency (overhead) in delivery of read data from the conventional memory chips, one or more of the interface chips may include embedded memory such as, for example, Static Random Access Memory (SRAM) that is configured to store data. With respect to an implementation of a system including flash devices and an interface chip with SRAM, data may be transferred from the physical page buffer within the one of the convention flash devices to the interface chip before initiation of the burst data read on the higher performance (i.e. series-connection configuration) interface. Also, overhead in conjunction with flash operations can be further managed by having

data size transfers to the SRAM of sizes less than an entire page. In this manner data transfer time associated with a read operation within the system is not bottlenecked by the time for a full page transfer. In some examples, the data width of the lower performance interface may be greater than the data width of the higher performance interface. For instance, if the data width of the lower performance interface is, for example, x16, x32 or x64, then the data width of the higher performance interface may be, for example, x4 or x8.

[0079] While the PCBs shown in FIGS. 5 through 12 are illustrated with respect to one side of the PCB, example embodiments are not limited to PCB with chips on only one side of the PCB. Some example embodiments are characterized by additional chips on the other side of the PCB that may be similarly encapsulated as has been described. Also, although in each of FIGS. 5 through 12 the SSD controller is shown attached to the PCB, alternatively the SSD controller may be separate from the PCB.

[0080] A number of example embodiments can be applied to any suitable solid state memory systems such as, for example, those that include NAND Flash EEPROM device(s), NOR Flash EEPROM device(s), AND Flash EEPROM device(s), DiNOR Flash EEPROM device(s), Serial Flash EEPROM device(s), DRAM device(s), SRAM device(s), Ferro RAM device(s), Magneto RAM device(s), Phase Change RAM device(s), or any suitable combination of these devices.

[0081] Certain adaptations and modifications of the described embodiments can be made. Therefore, the above discussed embodiments are considered to be illustrative and not restrictive. Also, in some instances in which circuit schematics have been presented and described herein, certain details not sufficiently relevant to an understanding of example embodiments may have been omitted so as not to obscure inventive features disclosed herein.

CLAIMS

What is claimed is:

1. A solid state drive comprising:

a circuit board having opposing first and second surfaces;

a plurality of semiconductor chips attached to the first surface, the plurality of semiconductor chips including at least one memory chip that is at least substantially encapsulated in a resin; and

a controller in communication with at least a number of the plurality of semiconductor chips, the number of semiconductor chips including the at least one memory chip, and the controller including an interface that receives, from a computer system, signals for processing within the solid state drive.

2. A solid state drive as claimed in claim 1 wherein the plurality of semiconductor chips are geometrically arranged on the first surface to form a plurality of rows and columns.

3. A solid state drive as claimed in claim 2 wherein either each row or each column is encapsulated within a respective encapsulation.

4. A solid state drive as claimed in claim 2 wherein either more than one entire row or more than one entire column are encapsulated within a respective encapsulation.

5. A solid state drive as claimed in any one of claims 1 to 4 further comprising a rectangular shaped housing for receiving the circuit board therein, the housing sized for insertion into a bay of either a laptop computer, a netbook or a desktop computer.

6. A solid state drive as claimed in any one of claims 1 to 5 wherein the resin is epoxy-based.

7. A solid state drive as claimed in any one of claims 1 to 6 further comprising a second plurality of semiconductor chips attached to the second surface, the second plurality of semiconductor chips including at least one memory chip that is at least substantially encapsulated in a resin.

8. A solid state drive as claimed in any one of claims 1 to 7 wherein the controller is physically and rigidly joined to the circuit board.

9. A solid state drive as claimed in any one of claims 1 to 8 wherein the at least one memory chip is a NAND flash memory chip.

10. A solid state drive as claimed in any one of claims 1 to 9 wherein the plurality of semiconductor chips includes at least one stack of memory chips that is at least substantially encapsulated in a resin.

11. A solid state drive as claimed in any one of claims 1 to 10 wherein the interface is either a Serial Advanced Technology Attachment (SATA) interface, a Peripheral Component Interconnect express (PCIe) interface, an external Serial Advanced Technology Attachment (eSATA) interface, a Parallel Advanced Technology Attachment (PATA) interface, a Universal Serial Bus (USB) interface, or a Serial Attached SCSI (SAS) interface.

12. Apparatus comprising:

an in-line memory module-type form factor circuit board having opposing first and second surfaces;

a plurality of semiconductor chips attached to the first surface, the plurality of semiconductor chips including at least one memory chip that is at least substantially encapsulated in a resin; and

a controller in communication with the at least one memory chip, and the controller including an interface that receives signals comprising commands and data that effect operations within the at least one memory chip.

13. An apparatus as claimed in claim 12 wherein the at least one memory chip is a NAND flash memory chip.

14. An apparatus as claimed in claim 12 or 13 further comprising a second plurality of semiconductor chips attached to the second surface, the second plurality of semiconductor chips including at least one memory chip that is at least substantially encapsulated in a resin.

15. An apparatus as claimed in any one of claims 12 to 14 wherein the controller is physically and rigidly joined to the circuit board.

16. An apparatus as claimed in claim 15 wherein the controller and the plurality of semiconductor chips are encapsulated in a same encapsulation.

17. An apparatus as claimed in claim 15 wherein the controller is at least substantially encapsulated within its respective encapsulation.

18. A flash memory storage system comprising:

a circuit board having opposing first and second surfaces;

a plurality of semiconductor chips attached to the first surface, the plurality of semiconductor chips including at least one flash memory chip that is at least substantially encapsulated in a resin; and

a controller in communication with at least a number of the plurality of semiconductor chips, the number of semiconductor chips including the at least one flash memory chip, and the controller including an interface that receives, from a computer system, signals for processing within the flash memory storage system.

19. A flash memory storage system as claimed in claim 18 wherein the plurality of semiconductor chips are geometrically arranged on the first surface to form a plurality of rows and columns.

20. A flash memory storage system as claimed in claim 19 wherein either each row or each column is encapsulated within a respective encapsulation.

21. A flash memory storage system as claimed in claim 19 either more than one entire row or more than one entire column are encapsulated within a respective encapsulation.

22. A flash memory storage system as claimed in any one of claims 18 to 21 further comprising a second plurality of semiconductor chips attached to the second surface, the second plurality of semiconductor chips including at least one memory chip that is at least substantially encapsulated in a resin.

23. A flash memory storage system as claimed in any one of claims 18 to 22 wherein the at least one flash memory chip is a NAND flash memory chip.

24. A flash memory storage system as claimed in any one of claims 18 to 23 wherein the plurality of semiconductor chips includes at least one stack of memory chips that is at least substantially encapsulated in a resin.

25. A computer system comprising:

a main enclosure;

a solid state drive that includes:

a housing;

a circuit board within the housing and having opposing first and second surfaces;

a plurality of semiconductor chips attached to the first surface, the plurality of semiconductor chips including at least one memory chip that is at least substantially encapsulated in a resin; and

a controller within the housing and in communication with at least a number of the plurality of semiconductor chips, the number of semiconductor chips including the at least one memory chip, and the controller including an interface that receives signals for processing within the solid state drive; and

means for providing the signals to the interface, and the solid state drive and the providing means both within the main enclosure.

26. The computer system as claimed in claim 25 wherein the computer system is a desktop computer.

27. The computer system as claimed in claim 25 wherein the computer system is a laptop.

28. The computer system as claimed in claim 25 wherein the computer system is a netbook.

29. The computer system as claimed in claim 25 wherein the computer system is a tablet PC.

30. The computer system as claimed in claim 25 wherein the computer system is a mobile electronic communication device.

31. The computer system as claimed in any one of claims 25 to 30 wherein the providing means includes an I/O Controller Hub, a Memory Controller Hub and at least one bus.

32. The computer system as claimed in any one of claims 25 to 31 wherein the controller is physically and rigidly joined to the circuit board.

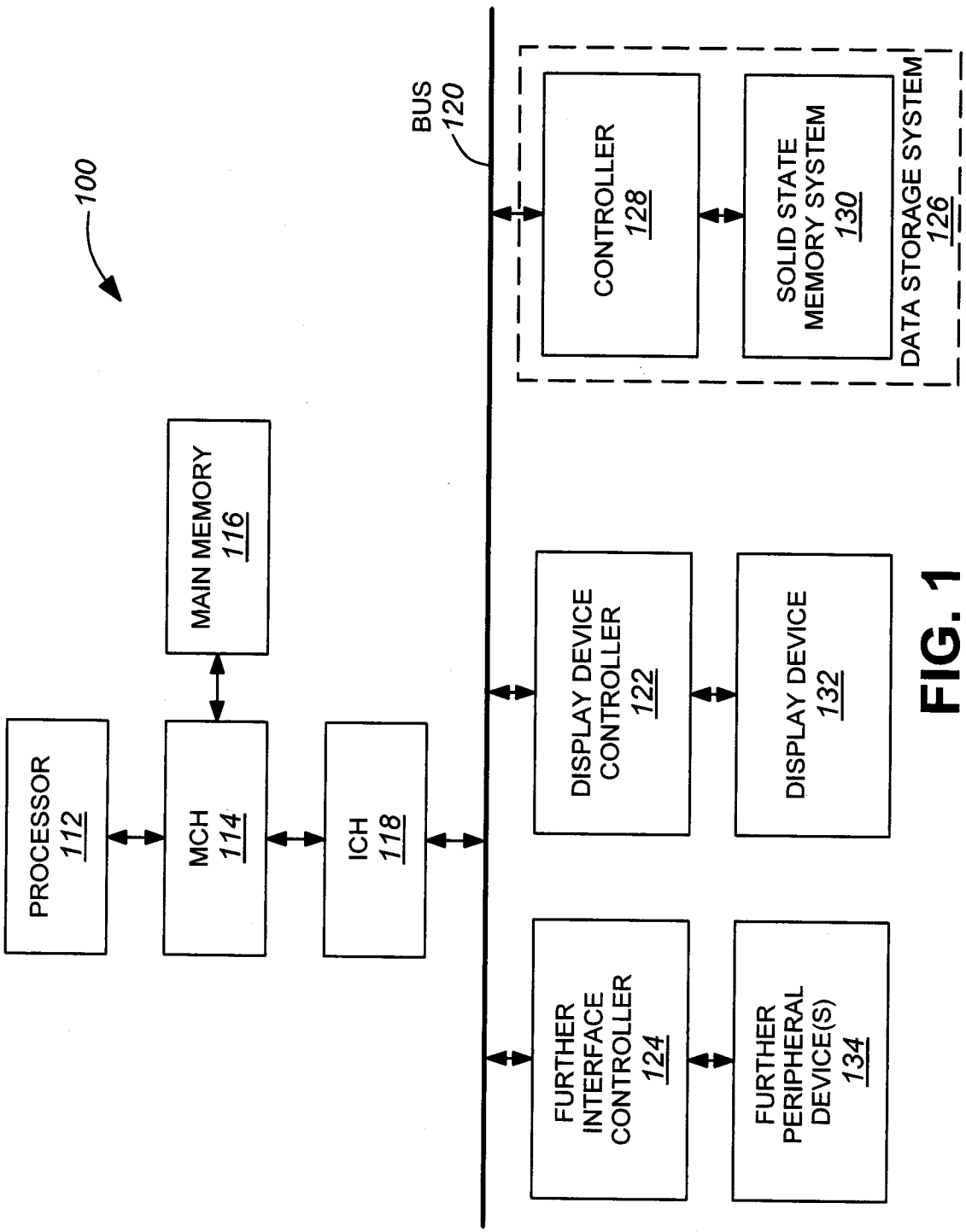

100
BUS
120
PROCESSOR
112
MCH
114
MAIN MEMORY
116
ICH
118
DISPLAY DEVICE CONTROLLER
122
DISPLAY DEVICE
132
FURTHER INTERFACE CONTROLLER
124
FURTHER PERIPHERAL DEVICE(S)
134
DATA STORAGE SYSTEM
126
CONTROLLER
128
SOLID STATE MEMORY SYSTEM
130

FIG. 1

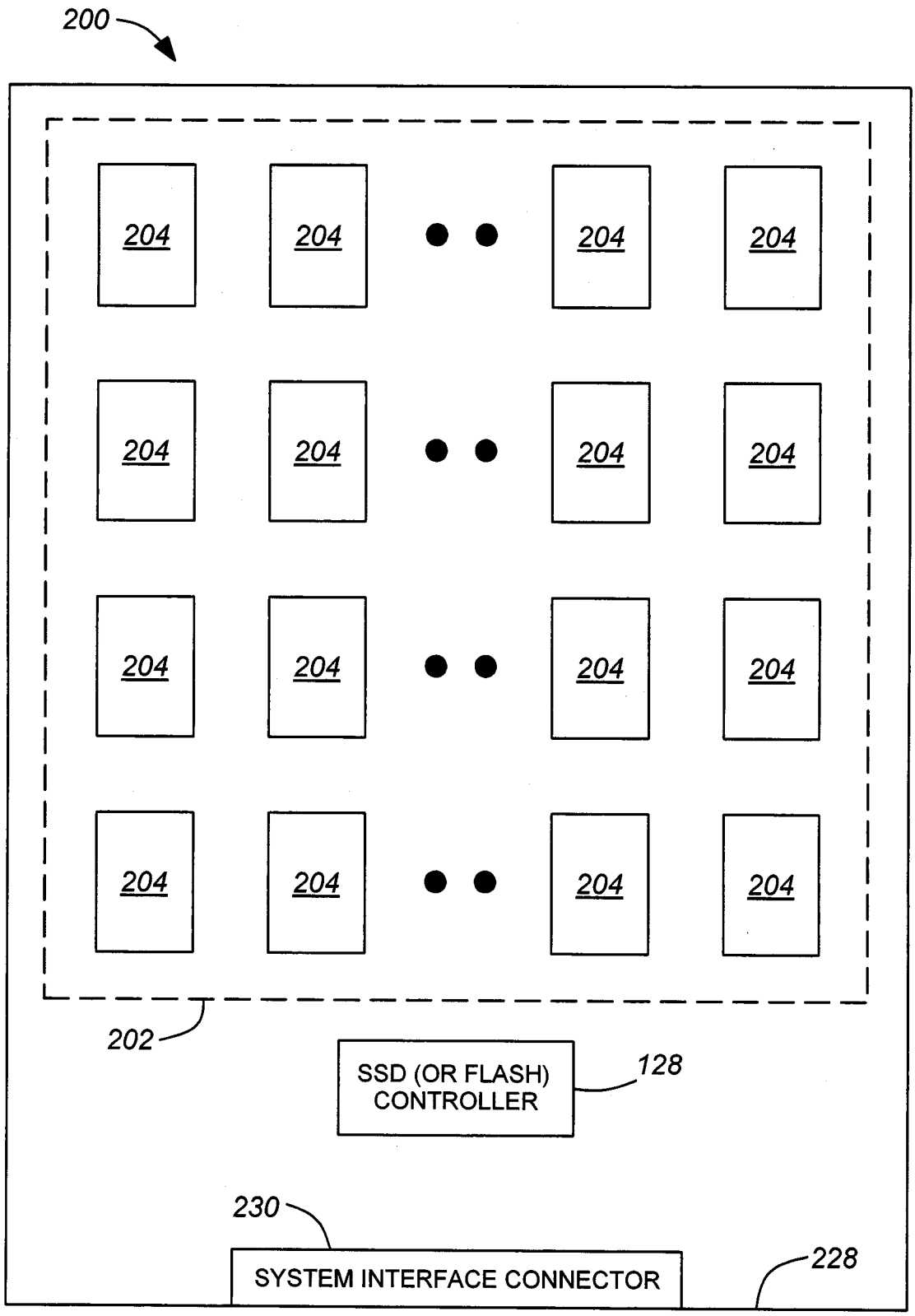

200
204
202
SSD (OR FLASH) CONTROLLER
128
230
SYSTEM INTERFACE CONNECTOR
228

FIG. 2

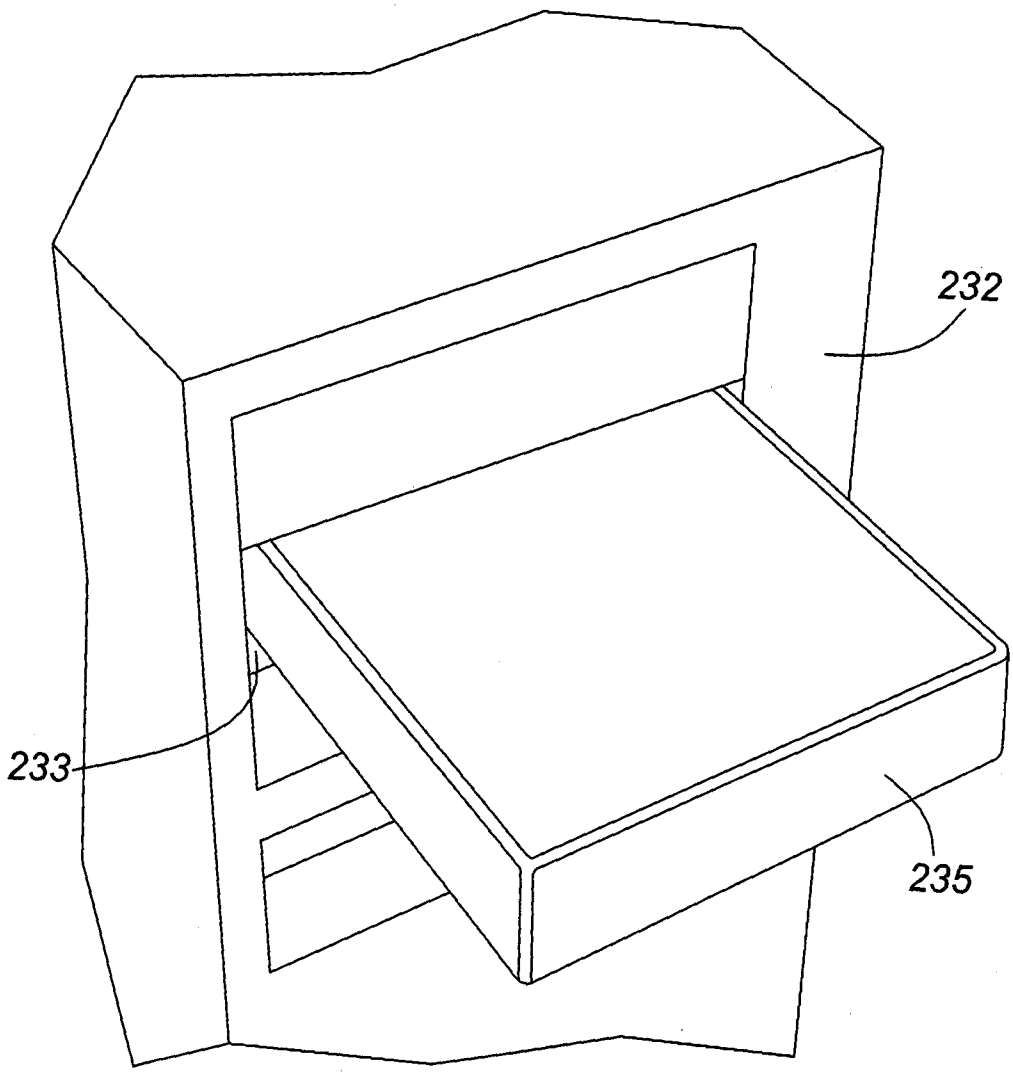


FIG. 3

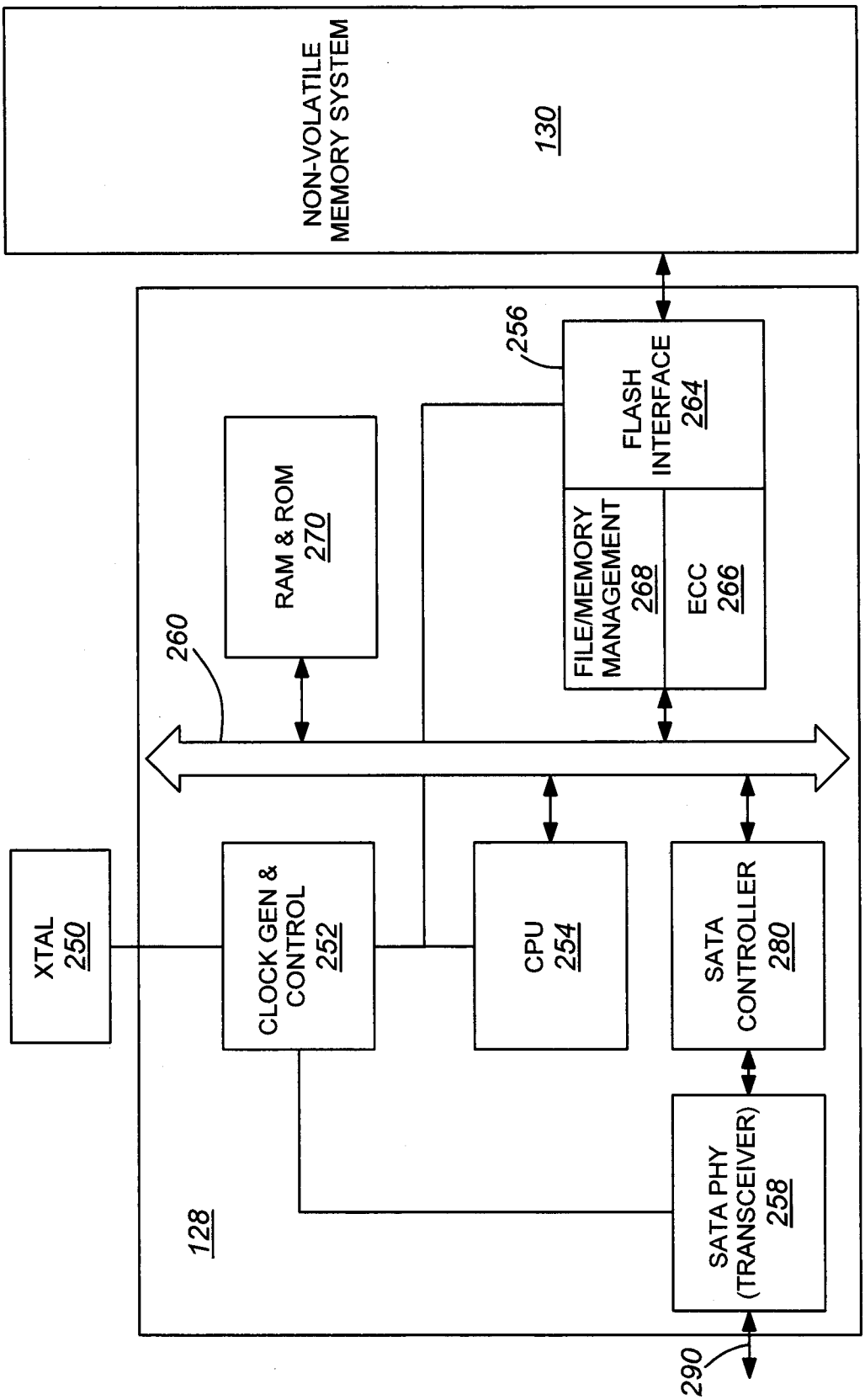
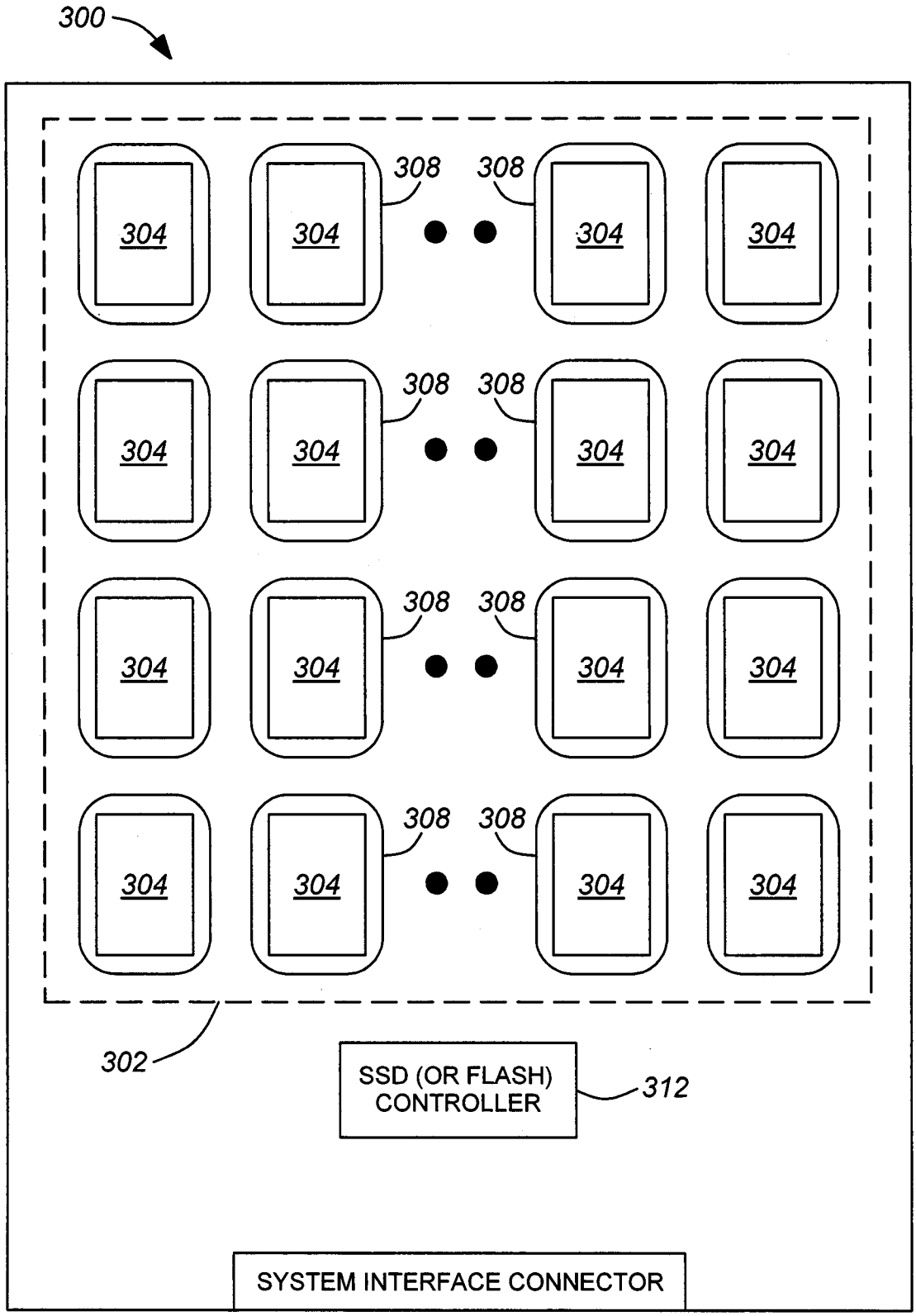

NON-VOLATILE MEMORY SYSTEM
130
256
FLASH INTERFACE 264
RAM & ROM 270
FILE/MEMORY MANAGEMENT 268
ECC 266
260
XTAL 250
CLOCK GEN & CONTROL 252
CPU 254
SATA CONTROLLER 280
SATA PHY (TRANSCEIVER) 258
128
290

FIG. 4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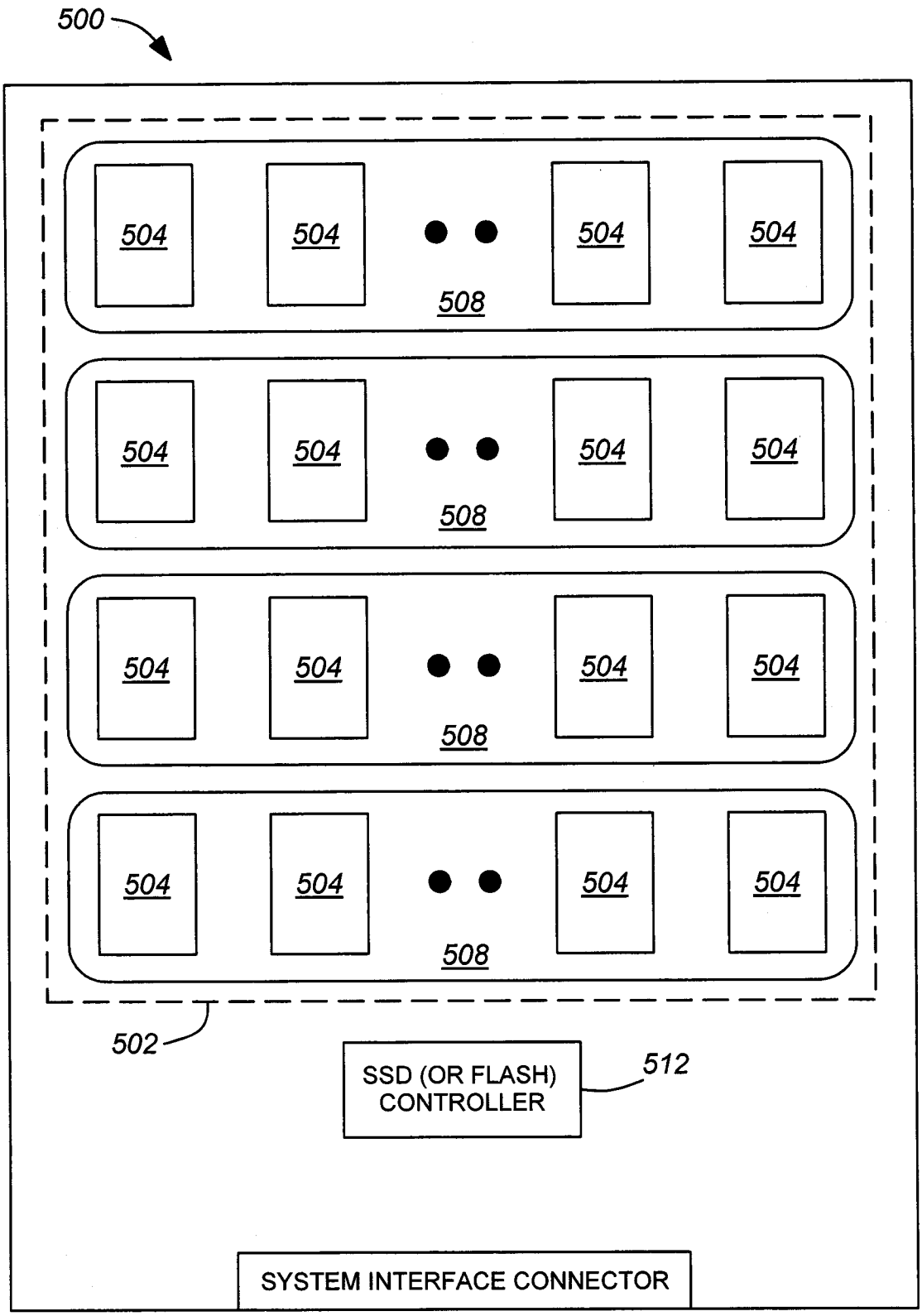
SSD (OR FLASH) CONTROLLER
312
SYSTEM INTERFACE CONNECTOR

FIG. 5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508
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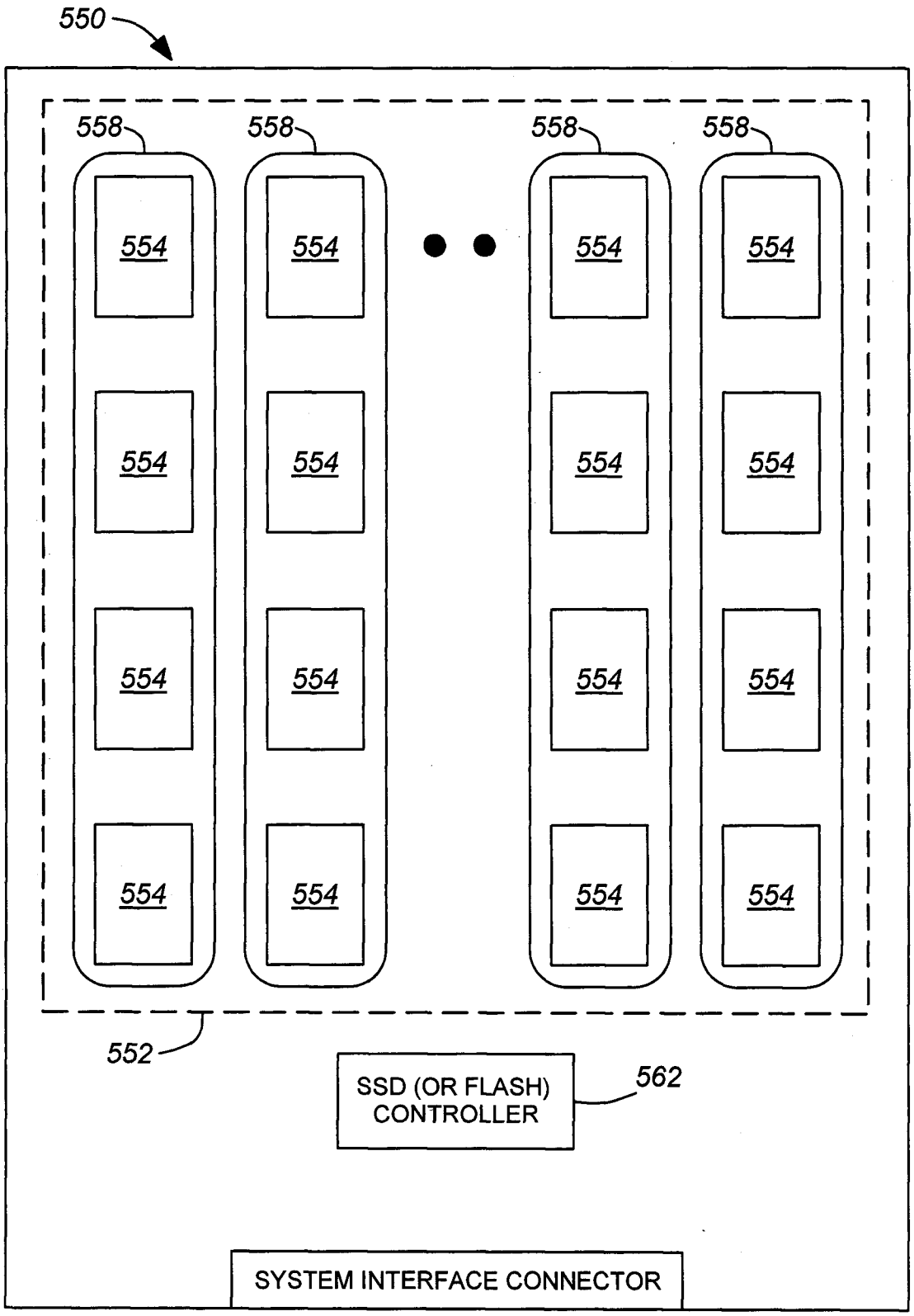
508
502
SSD (OR FLASH) CONTROLLER
512
SYSTEM INTERFACE CONNECTOR

FIG. 6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558
558
558
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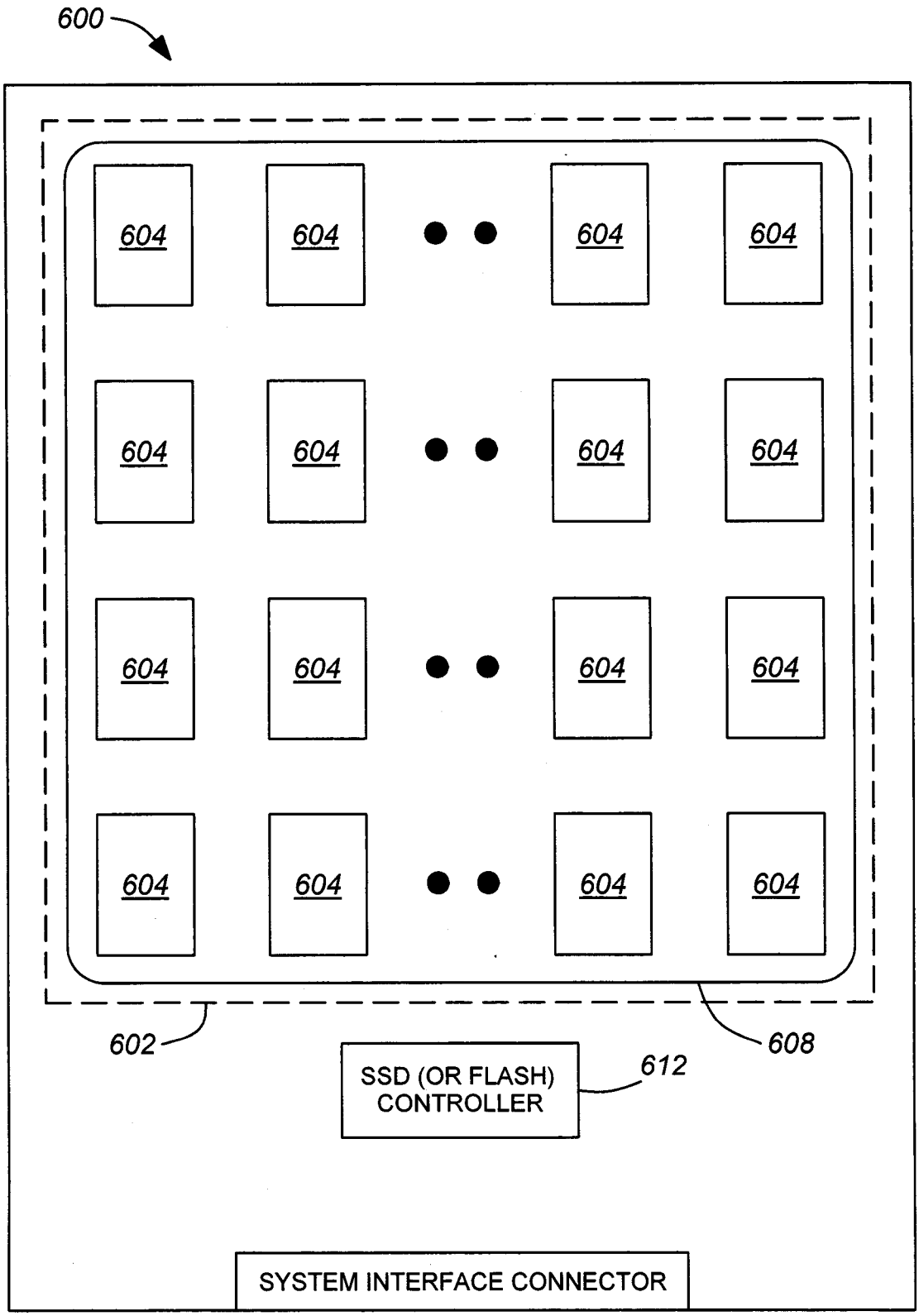
552
SSD (OR FLASH) CONTROLLER
562
SYSTEM INTERFACE CONNECTOR

FIG. 7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604
602
608
SSD (OR FLASH) CONTROLLER
612
SYSTEM INTERFACE CONNECTOR

FIG. 8

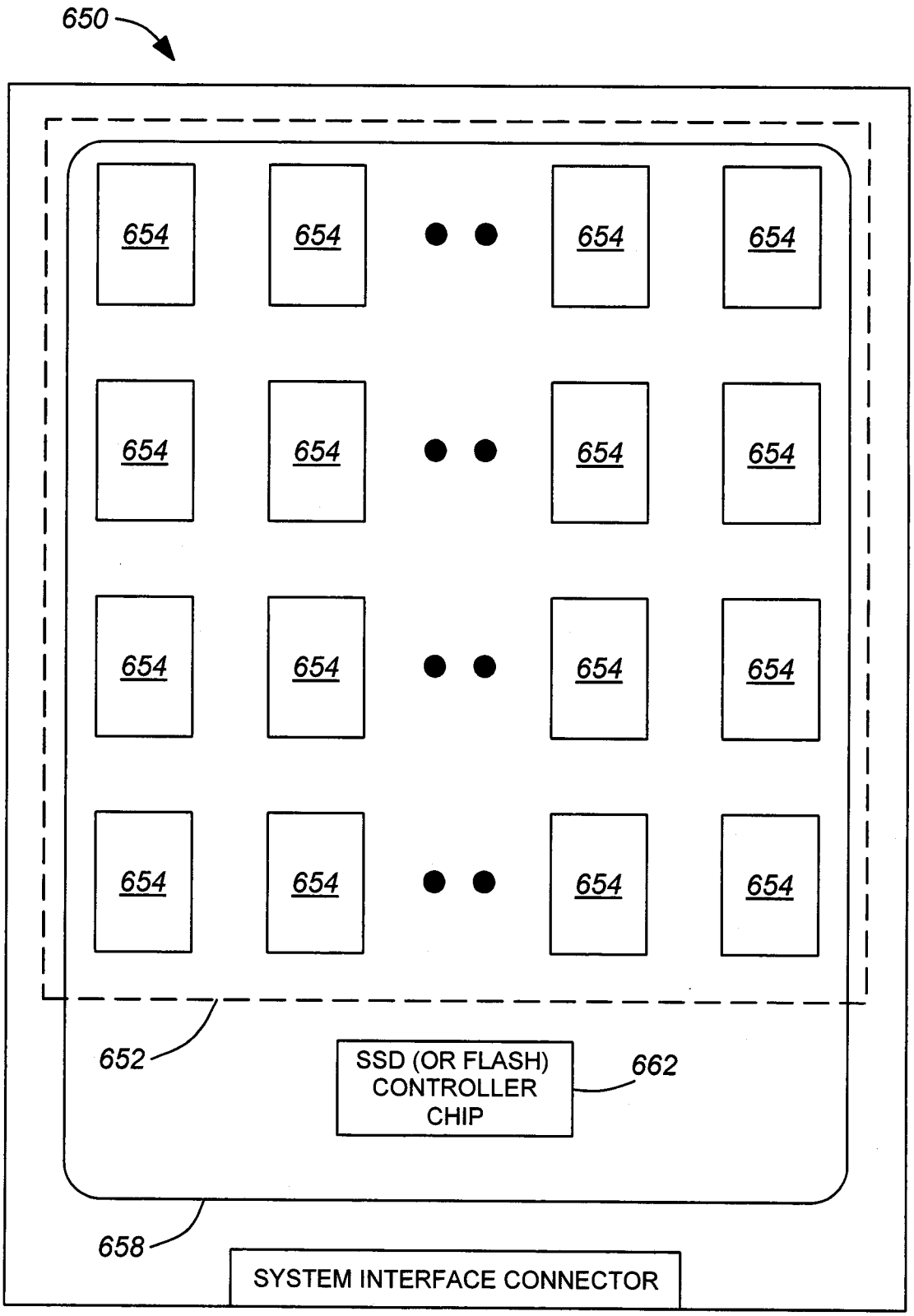
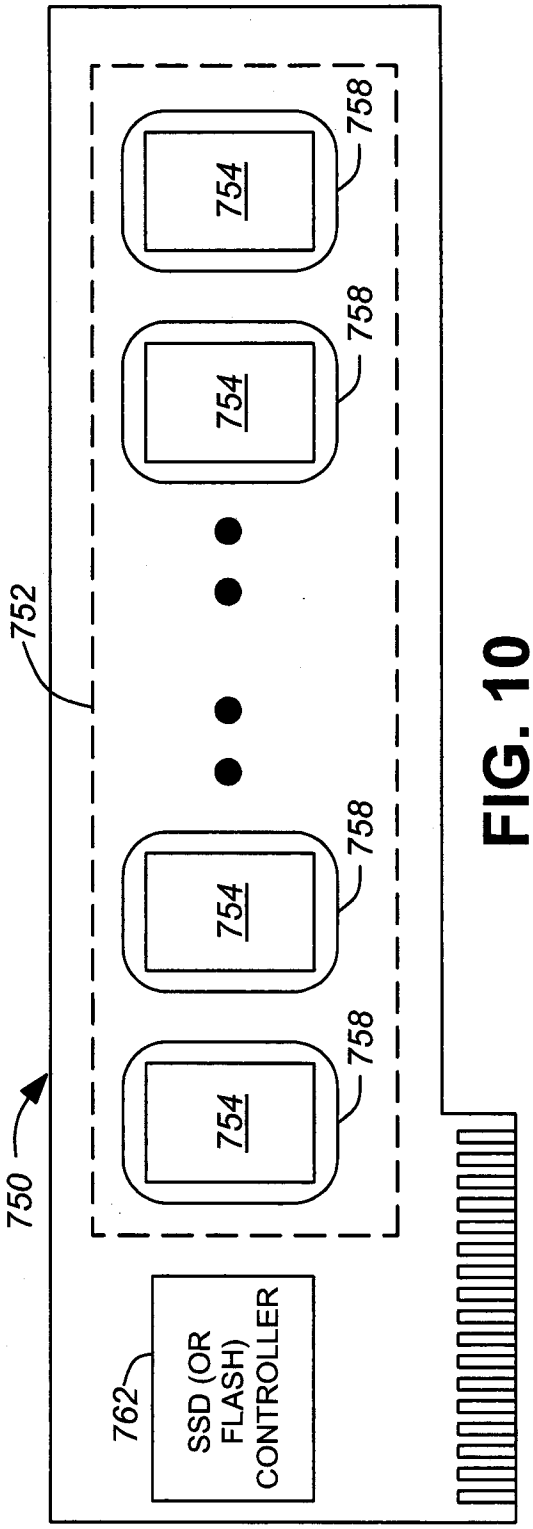

650
654
652
SSD (OR FLASH) CONTROLLER CHIP
662
658
SYSTEM INTERFACE CONNECTOR

FIG. 9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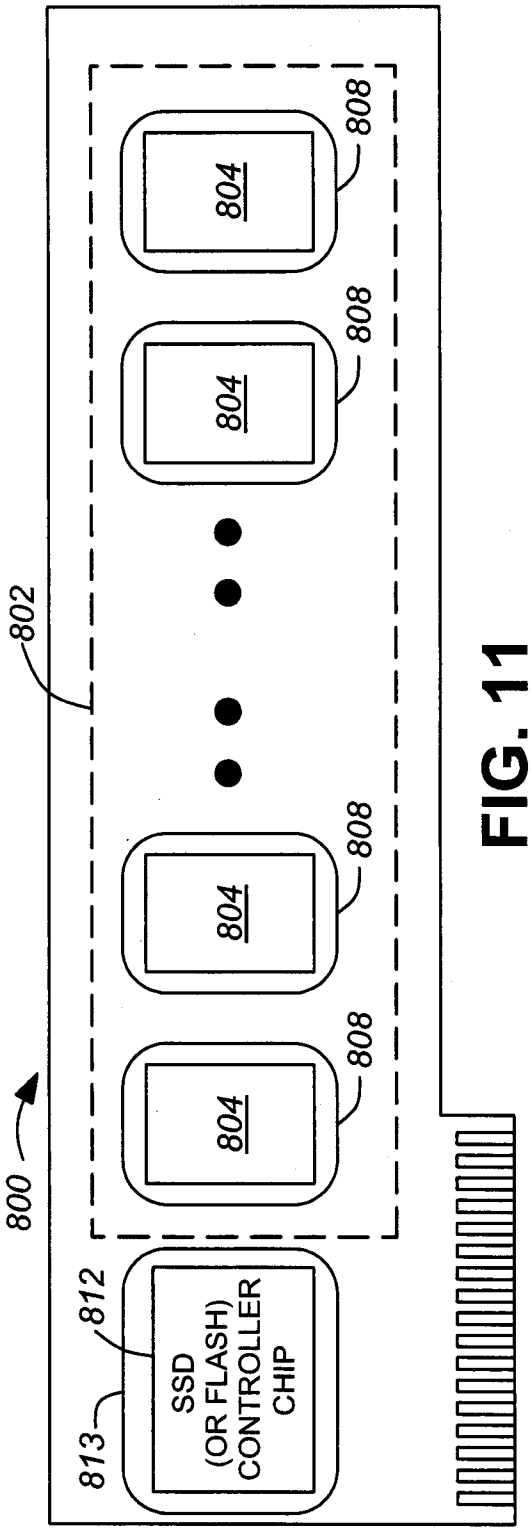
754
758
762
SSD (OR FLASH) CONTROLLER

FIG. 10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808
812
813
SSD (OR FLASH) CONTROLLER CHIP

FIG. 11

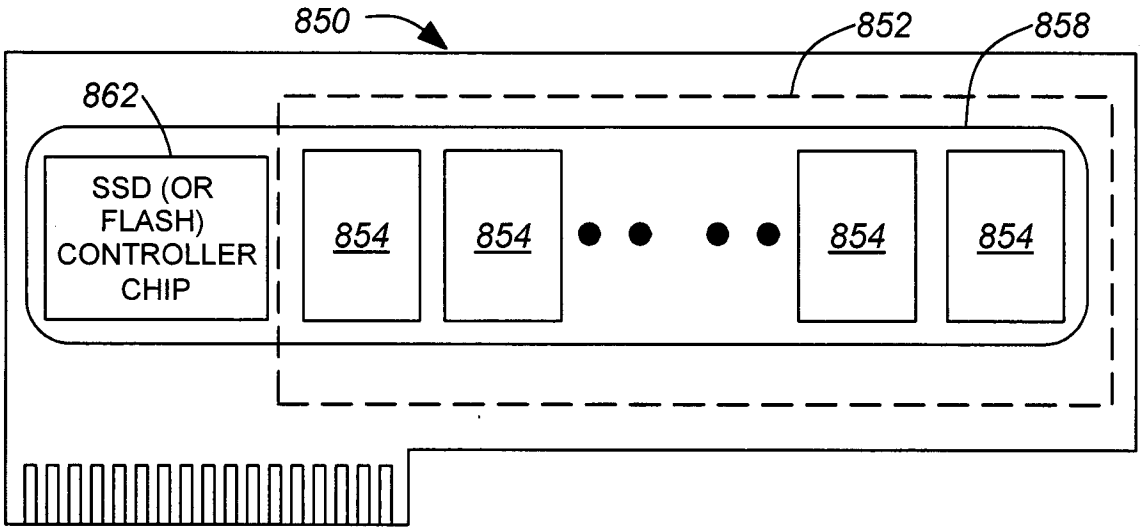
850
852
858
862
SSD (OR FLASH) CONTROLLER CHIP
854
854
854
854

FIG. 12

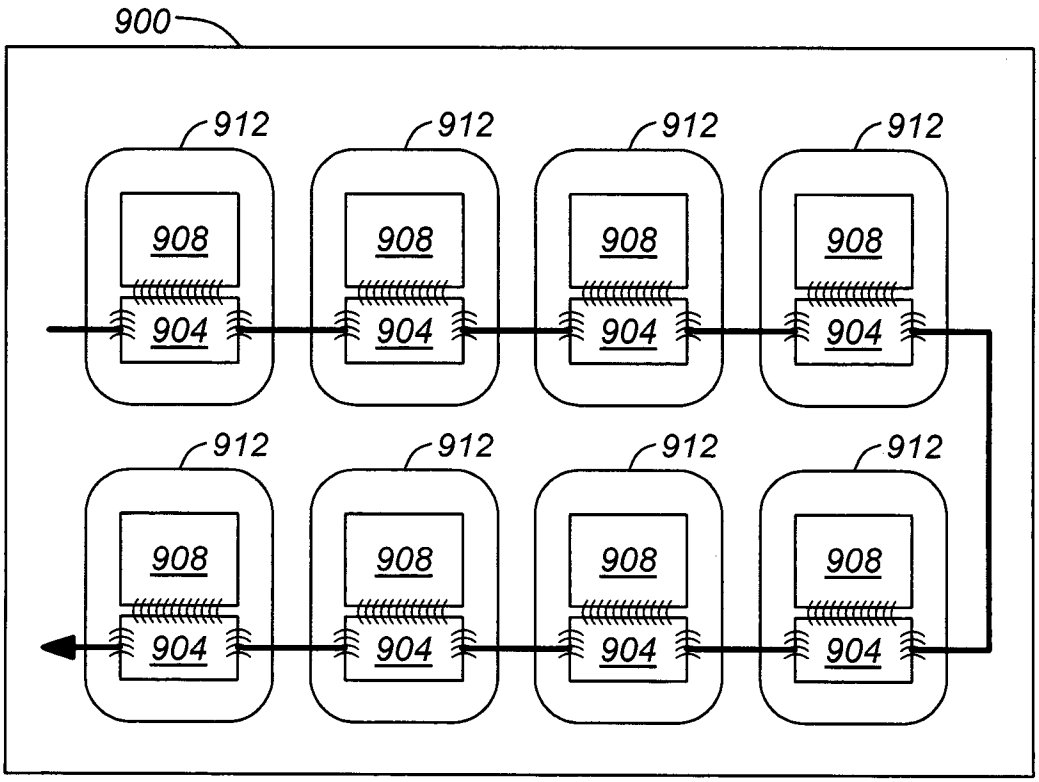
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FIG. 13

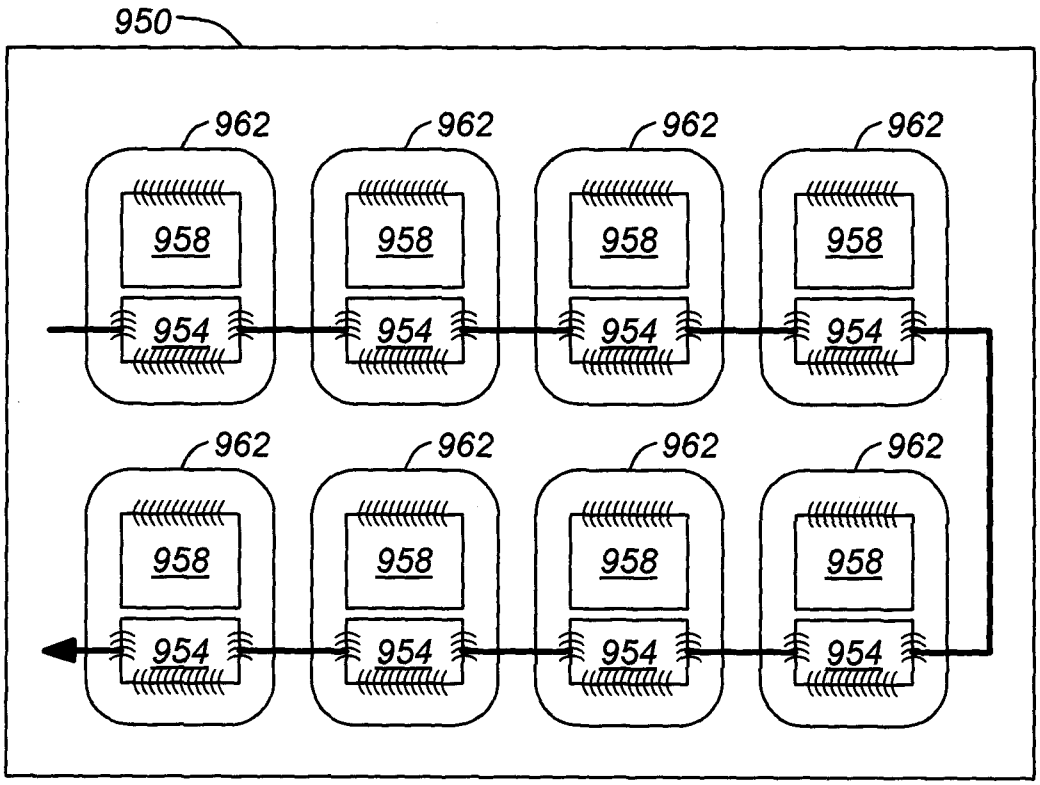
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FIG. 14

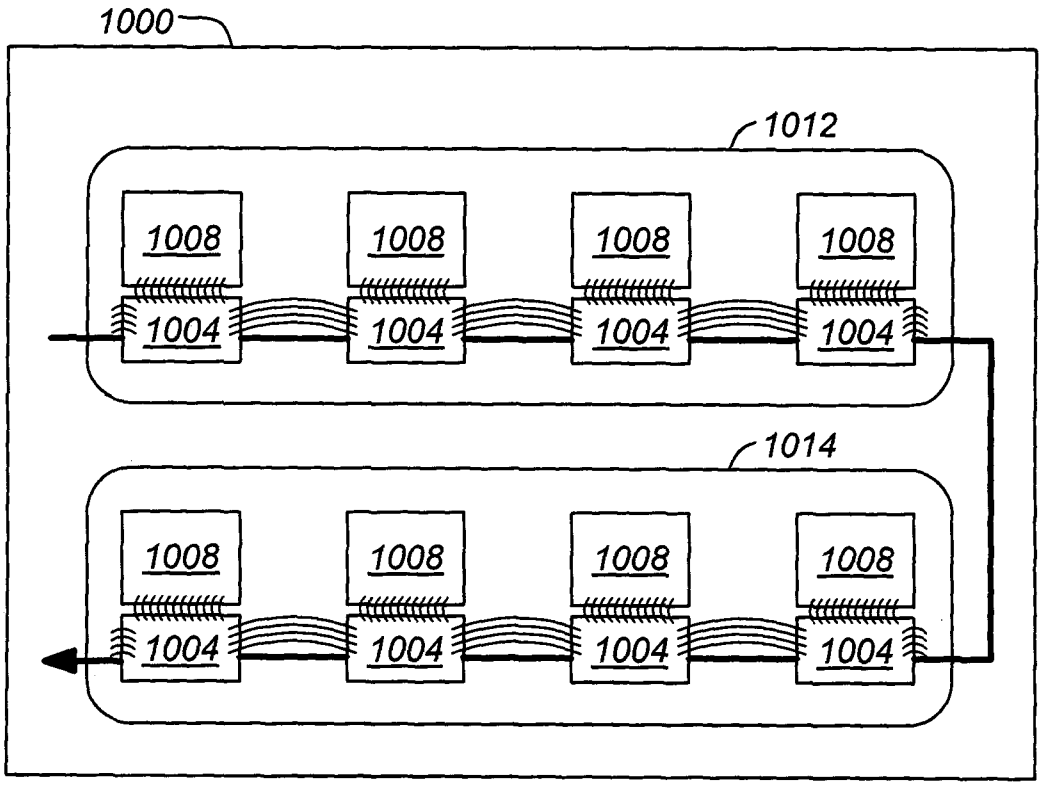
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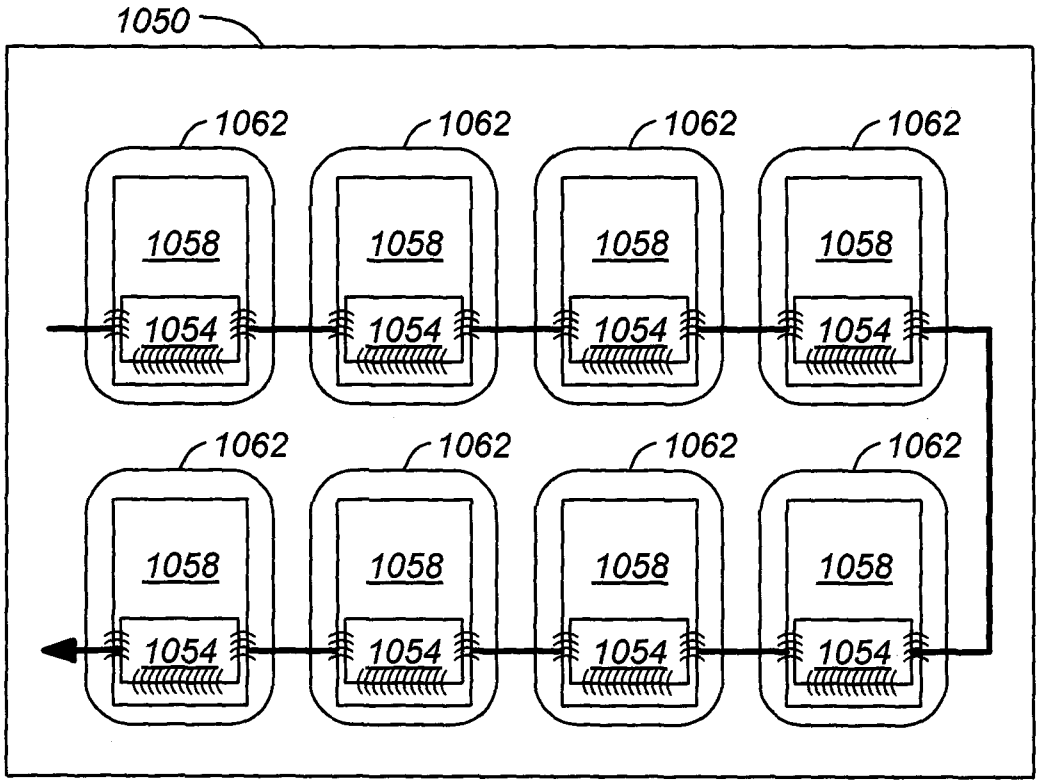
FIG. 15


1050
1062
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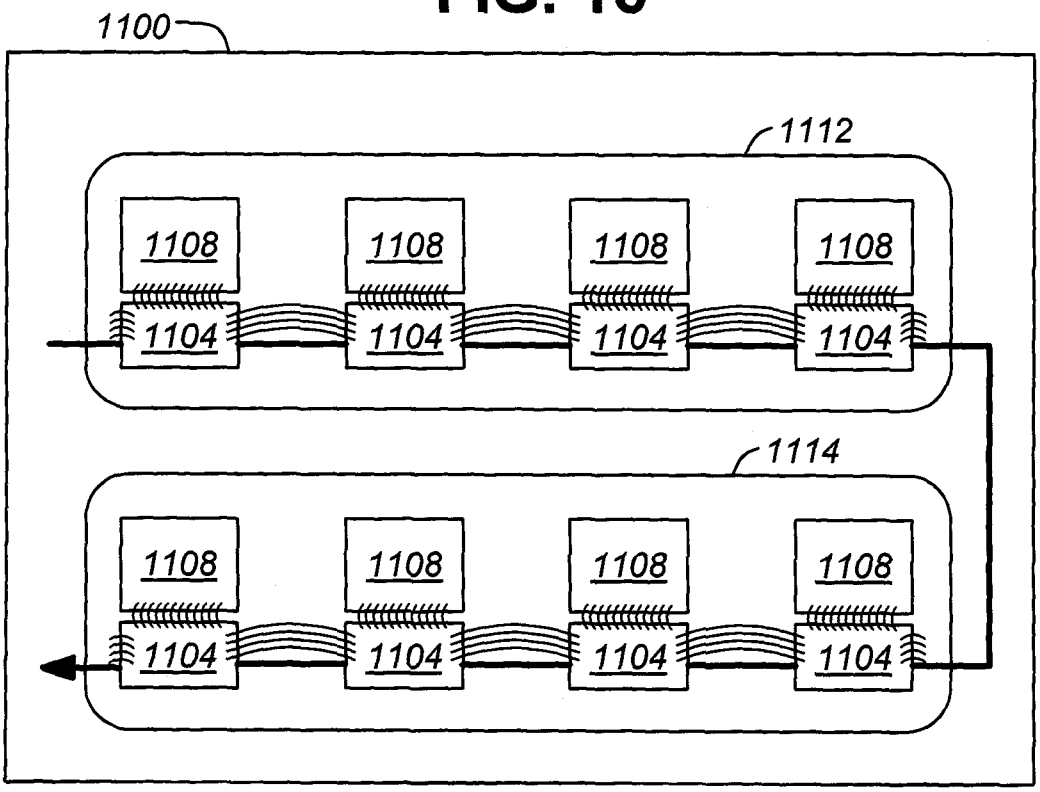
1054

FIG. 16


1100
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1114
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FIG. 17

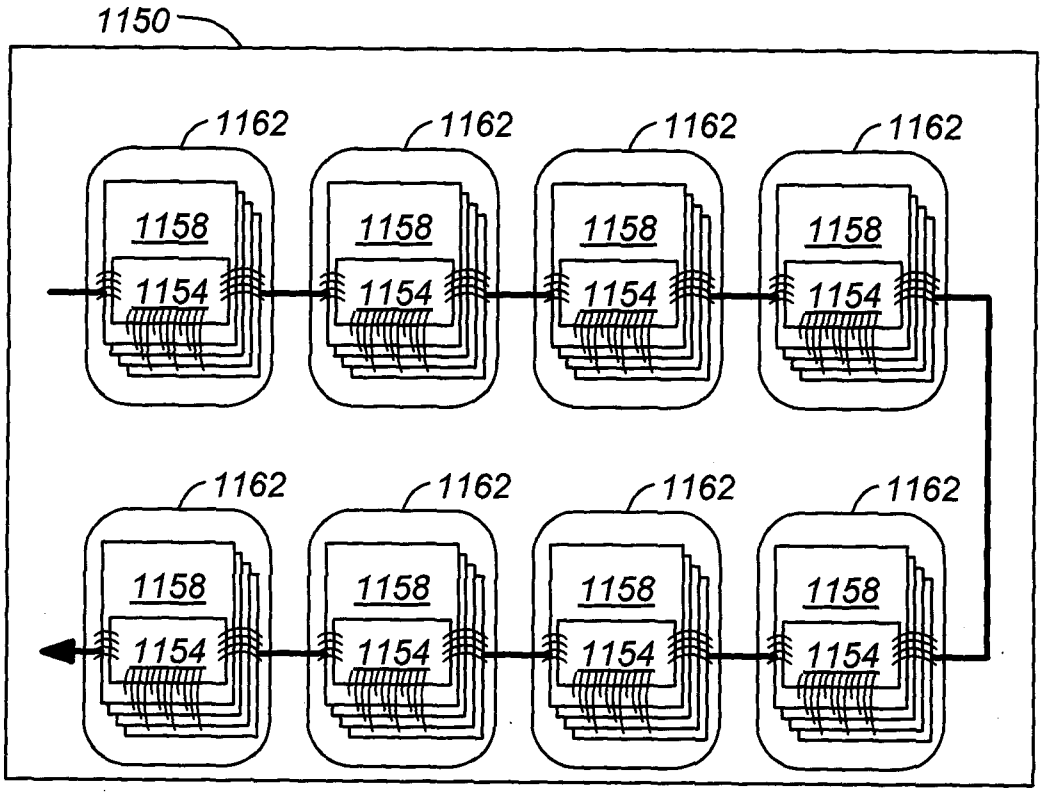

FIG. 18

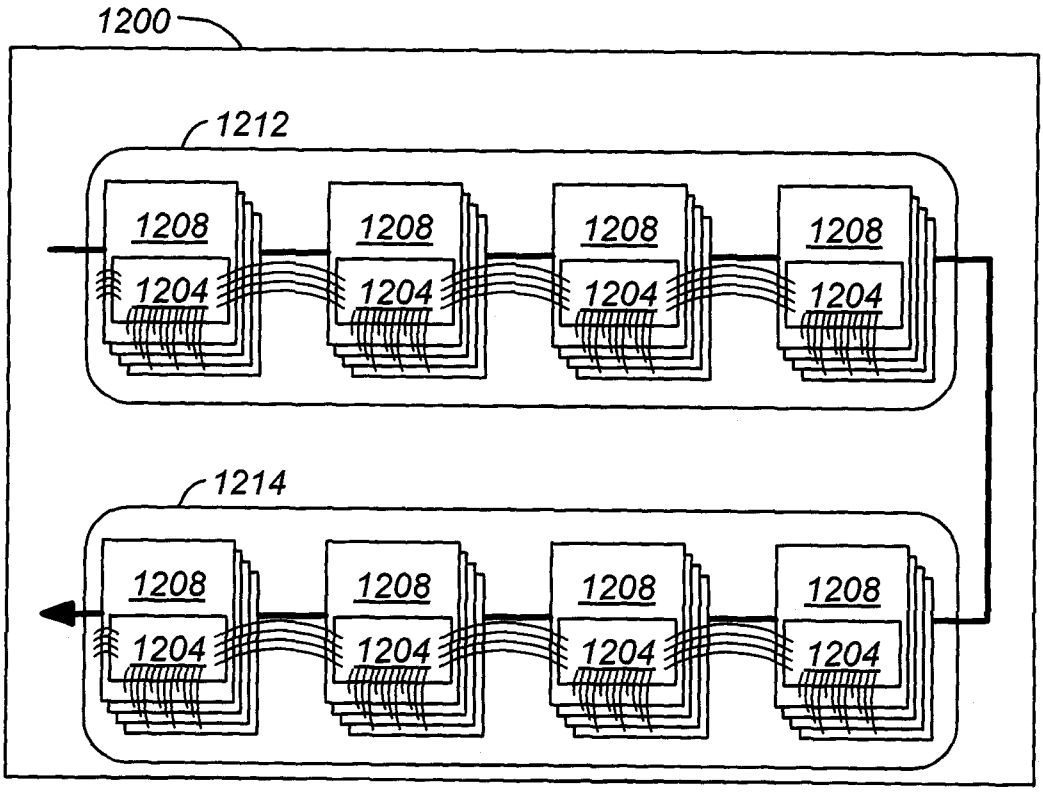

FIG. 19

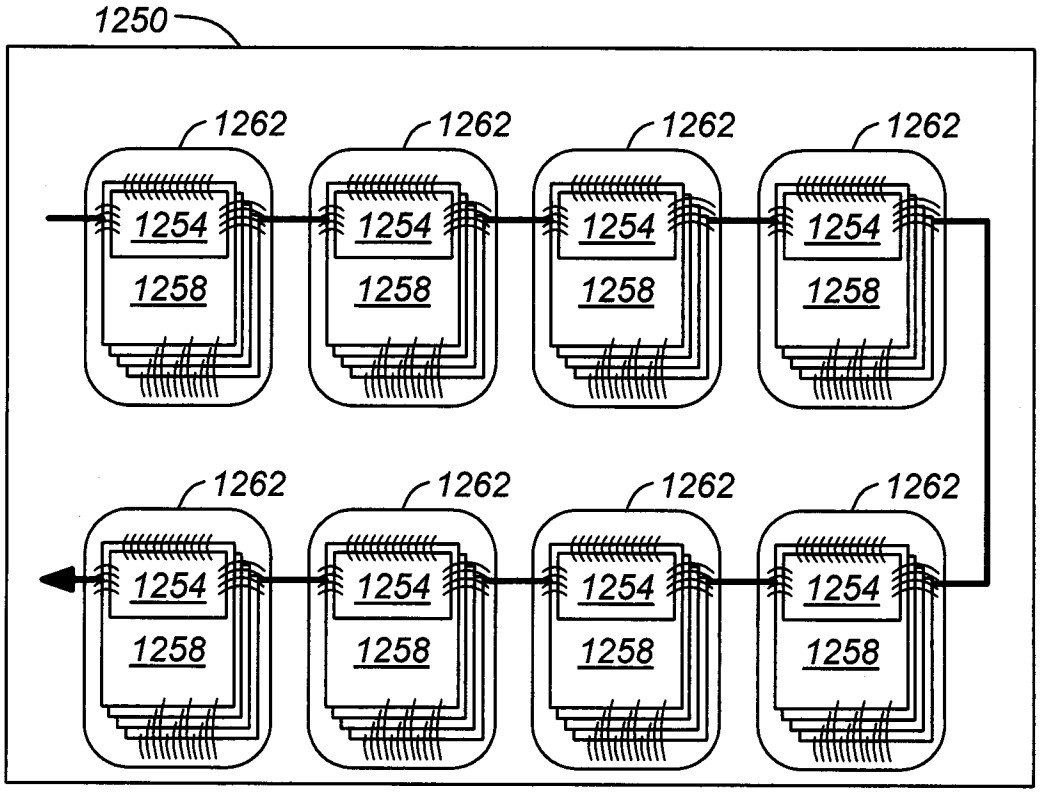
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FIG. 20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2009/001638

A. CLASSIFICATION OF SUBJECT MATTER

IPC: ***H01L 25/065*** (2006.01) , ***G06F 3/06*** (2006.01) , ***G11C 16/02*** (2006.01) , ***G11C 5/02*** (2006.01) , ***G11C 7/10*** (2006.01) , ***H01L 27/115*** (2006.01) , ***H05K 3/36*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: ***H01L 25/065*** (2006.01) , ***G06F 3/06*** (2006.01) , ***G11C 16/02*** (2006.01) , ***G11C 5/02*** (2006.01) , ***G11C 7/10*** (2006.01) , ***H01L 27/115*** (2006.01) , ***H05K 3/36*** (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)

EPOQUE (x-full (all english databases), WPI, EPODOC), IEEE

keywords - chip, board, circuit board, PCB, card, encapsul+, seal+, coat+, mold+, solid state, SSD, memory, chip on board, COB, resin, epoxy, glob top+, controller, array, row?, column?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US6040622 (Wallace) 21 March 2000 (21-03-2000) ** abstract; figs. 7, 10, 11; col. 1, lines 32-40; col. 3, lines 5-11and 30-43; col. 4, lines7-15 **	18, 19 1, 2, 5, 6, 8, 12, 15-17, 25-32
X Y	US20080235939 (Hiew et al.) 2 October 2008 (02-10-2008) ** abstract, pars. 7, 49-52, 54, 65, 70-73 **	18, 19, 21 1-5, 6, 8, 12, 15, 17, 2532
X Y	Wei Koh, "Digital Memory Card Market and Technology", 2005 Conference on High Density Microsystems Design and Packaging and Component Failure Analysis, 27-29 June 2005, p. 1-5. ** abstract, sections 4, 4.2, 4.2, 4.3, 4.4, 5 **	18, 19, 21-24 1-10, 12-17, 19-20, 25-32
Y	US20080266816 (Ni at al.) 30 October 2008 (30-10-2008) ** abstract, pars. 4, 6, 8, 38-39 **	1, 2, 5, 11, 25-32
Y	US5956233 (Yew et al.) 21 September 1999 (21-09-1999) ** abstract, col. 1, line 66 to col. 2, line 20; col. 5, lines 61-65; col. 8, line 64 to col. 9, line 65 **	12-17

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2010 (29.01.2010)	5 February 2010 (05-02-2010)
Name and mailing address of the ISA/CA Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	Authorized officer Leah Smith (819) 956-9966

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	US2003/0002262 (Benisek et al.) 2 January 2003 (02-01-2003) ** See parragraphs 2-3, 6-7, 36-37 **	12-17

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