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Tanzawa

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(54) **RANDOM TELEGRAPH SIGNAL NOISE REDUCTION SCHEME FOR SEMICONDUCTOR MEMORIES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(22) Filed: **Jul. 14, 2014**

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US 2014/0321216 A1 Oct. 30, 2014

Related U.S. Application Data

(60) Continuation of application No. 13/971,626, filed on Aug. 20, 2013, now Pat. No. 8,780,638, which is a continuation of application No. 13/480,378, filed on May 24, 2012, now Pat. No. 8,537,620, which is a continuation of application No. 13/047,562, filed on Mar. 14, 2011, now Pat. No. 8,194,459, which is a division of application No. 12/020,460, filed on Jan. 25, 2008, now Pat. No. 7,916,544.

(51) **Int. Cl.**

G11C 16/10	(2006.01)
G11C 16/04	(2006.01)
G11C 16/12	(2006.01)
G11C 16/26	(2006.01)
G11C 7/00	(2006.01)

(52) **U.S. Cl.**
CPC ***G11C 16/0408*** (2013.01); ***G11C 7/00*** (2013.01); ***G11C 16/12*** (2013.01); ***G11C 16/26*** (2013.01)

(58) **Field of Classification Search**
CPC G11C 16/10; G11C 16/12
USPC 365/185.19, 185.24
See application file for complete search history.

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Primary Examiner — Michael Tran
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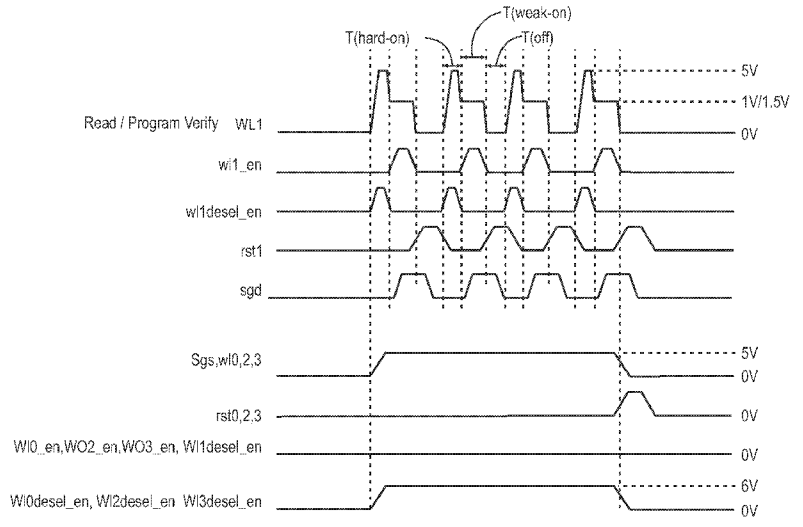
(57) **ABSTRACT**

Embodiments are provided that include a method including providing a first pulsed gate signal to a selected memory cell, wherein the pulsed gate signal alternates between a first voltage level and a second voltage level during a time period and sensing a data line response to determine data stored on the selected memory of cells. Further embodiments provide a system including a memory device, having a regulator circuit coupled to a plurality of access lines of a NAND memory cell, and a switching circuit configured to sequentially bias at least one of the plurality of the access lines between a first voltage level and a second voltage level based on an input signal.

20 Claims, 18 Drawing Sheets



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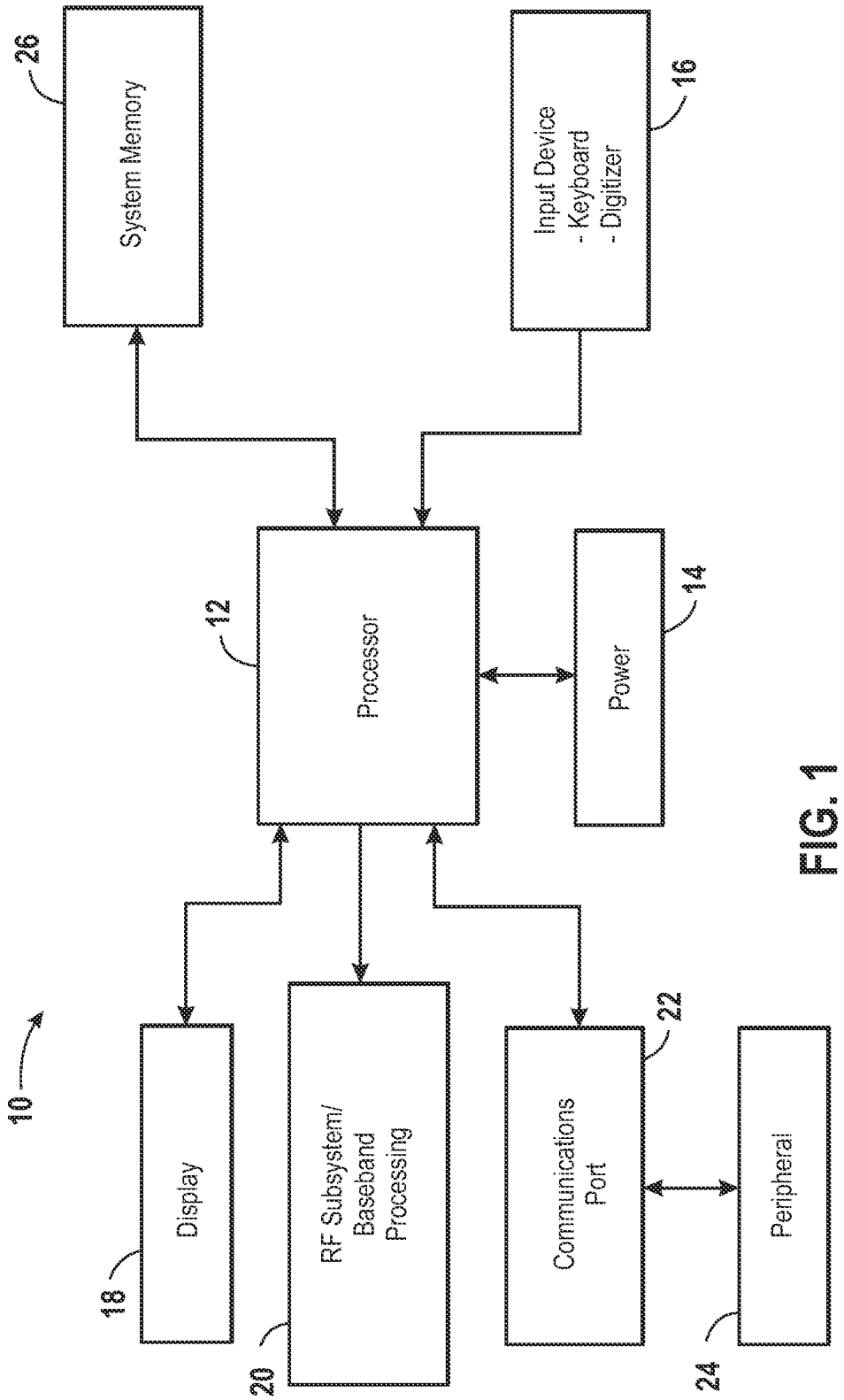
10
12
Processor
14
Power
16
Input Device
- Keyboard
- Digitizer
18
Display
20
RF Subsystem/
Baseband
Processing
22
Communications
Port
24
Peripheral
26
System Memory

FIG. 1

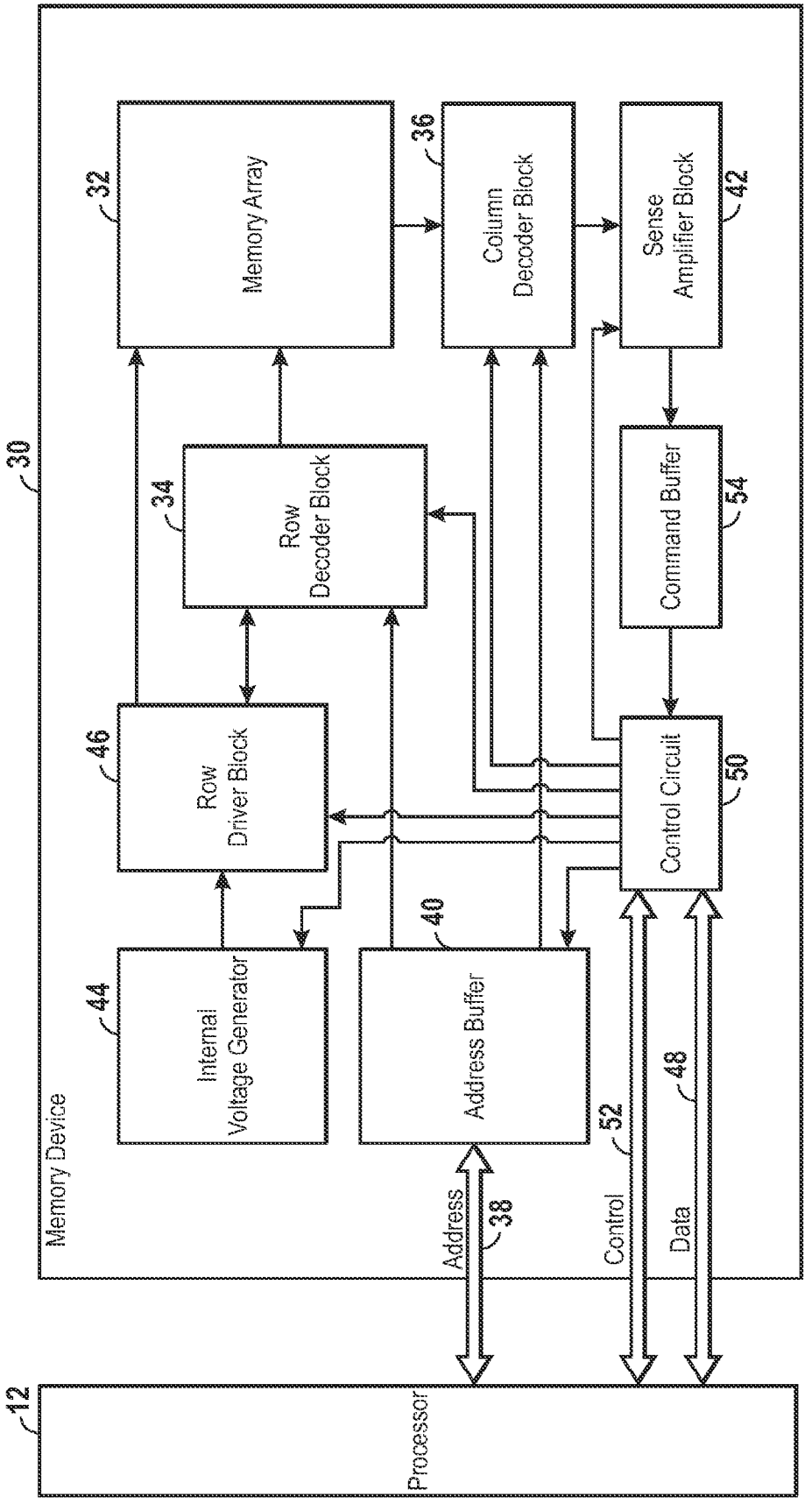
12
Processor
30
Memory Device
32
Memory Array
34
Row Decoder Block
36
Column Decoder Block
38
Address
40
Address Buffer
42
Sense Amplifier Block
44
Internal Voltage Generator
46
Row Driver Block
48
Data
50
Control Circuit
52
Control
54
Command Buffer

FIG. 2

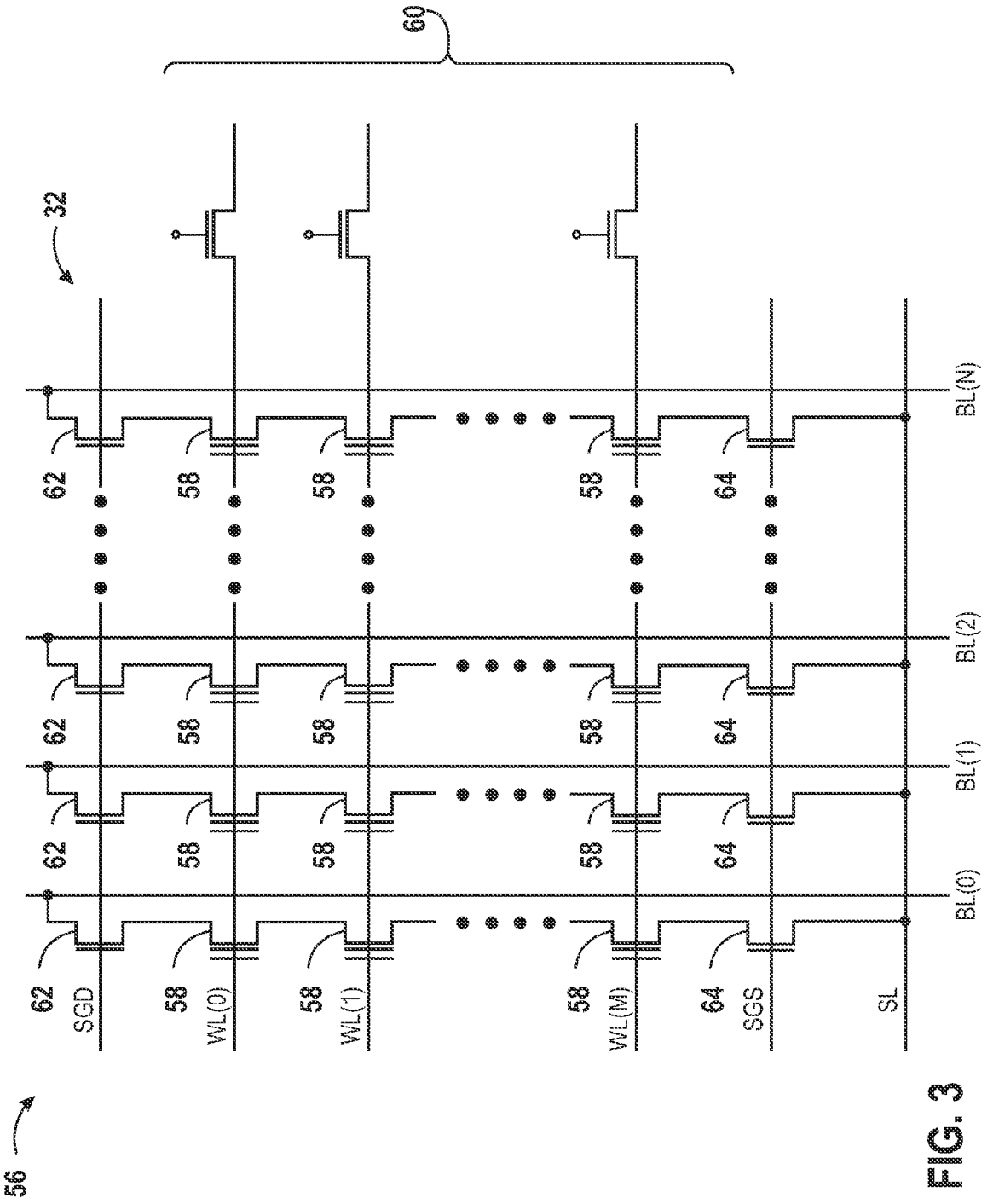

FIG. 3

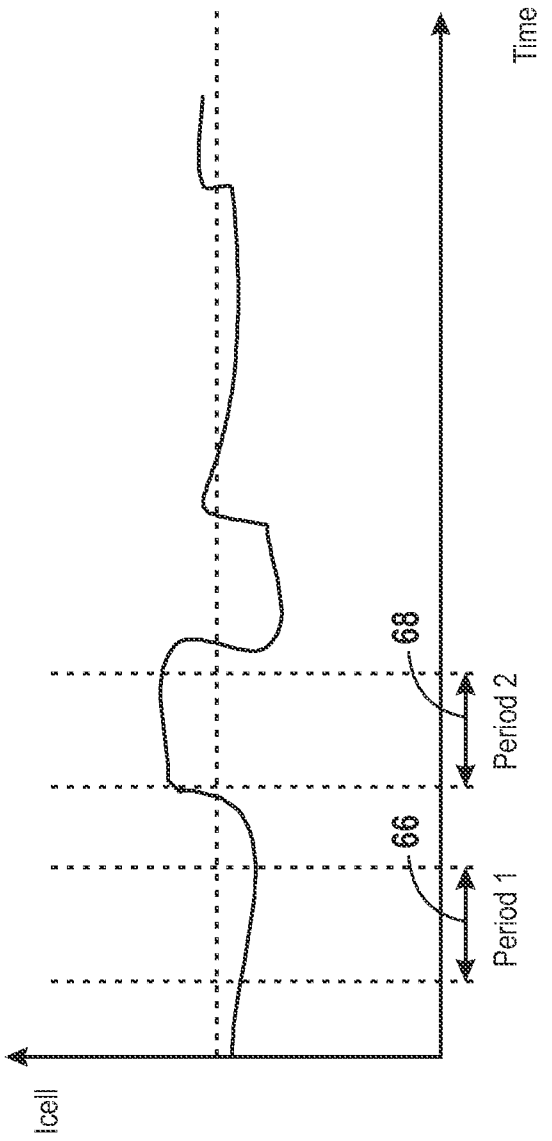

FIG. 4

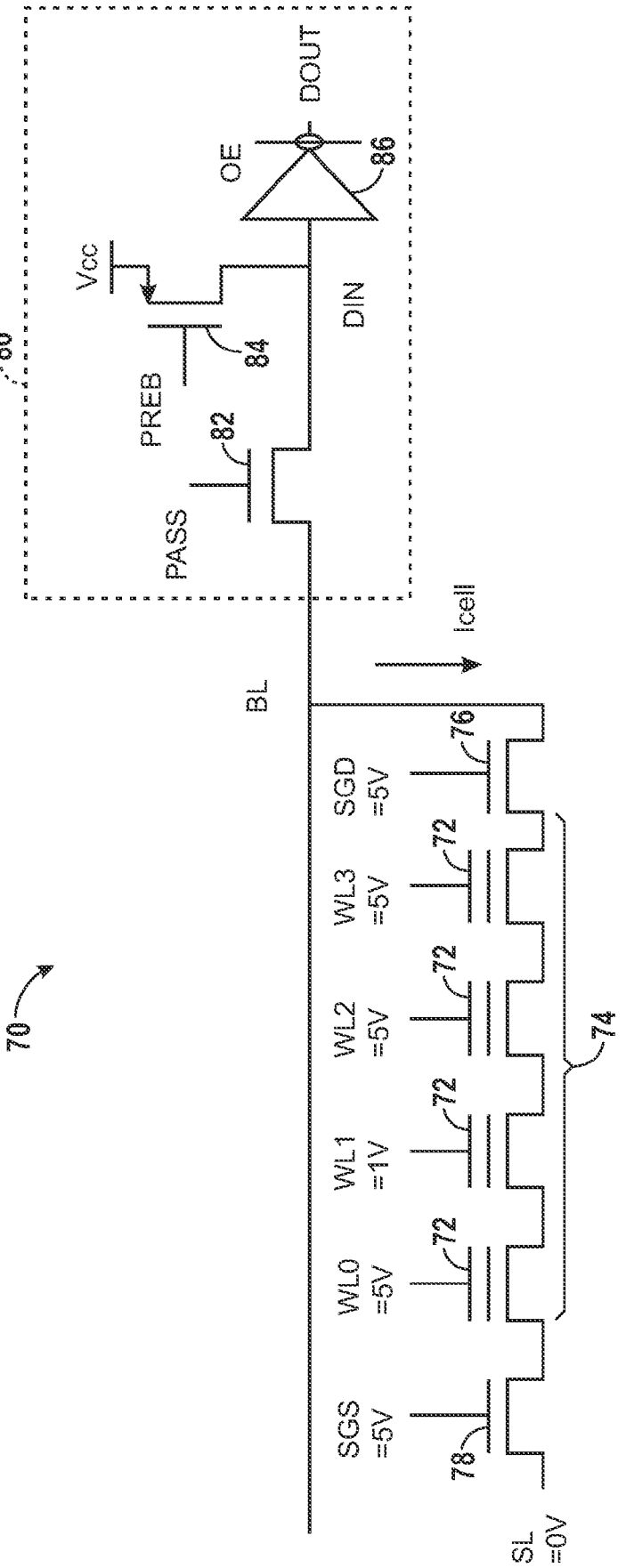
70
80
Vcc
PREB
84
82
PASS
DIN
OE
DOUT
86
BL
Icell
SGD
=5V
76
WL3
=5V
72
WL2
=5V
72
WL1
=1V
72
WL0
=5V
72
SGS
=5V
78
74
SL
=0V

FIG. 5

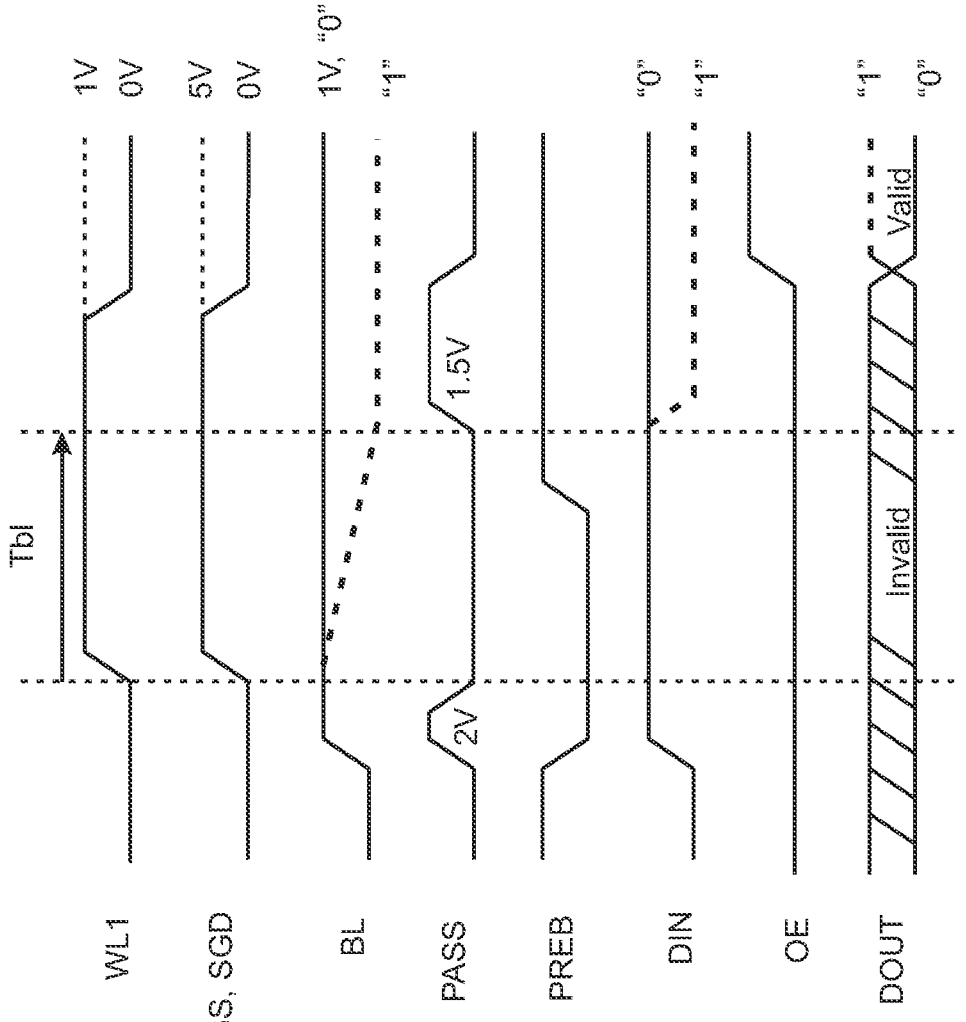
Tbl
WL1
1V
0V
WL0,WL2,WL3, SGS, SGD
5V
0V
BL
1V, "0"
"1"
PASS
2V
1.5V
PREB
DIN
"0"
"1"
OE
DOUT
"1"
"0"
Invalid
Valid

FIG. 6

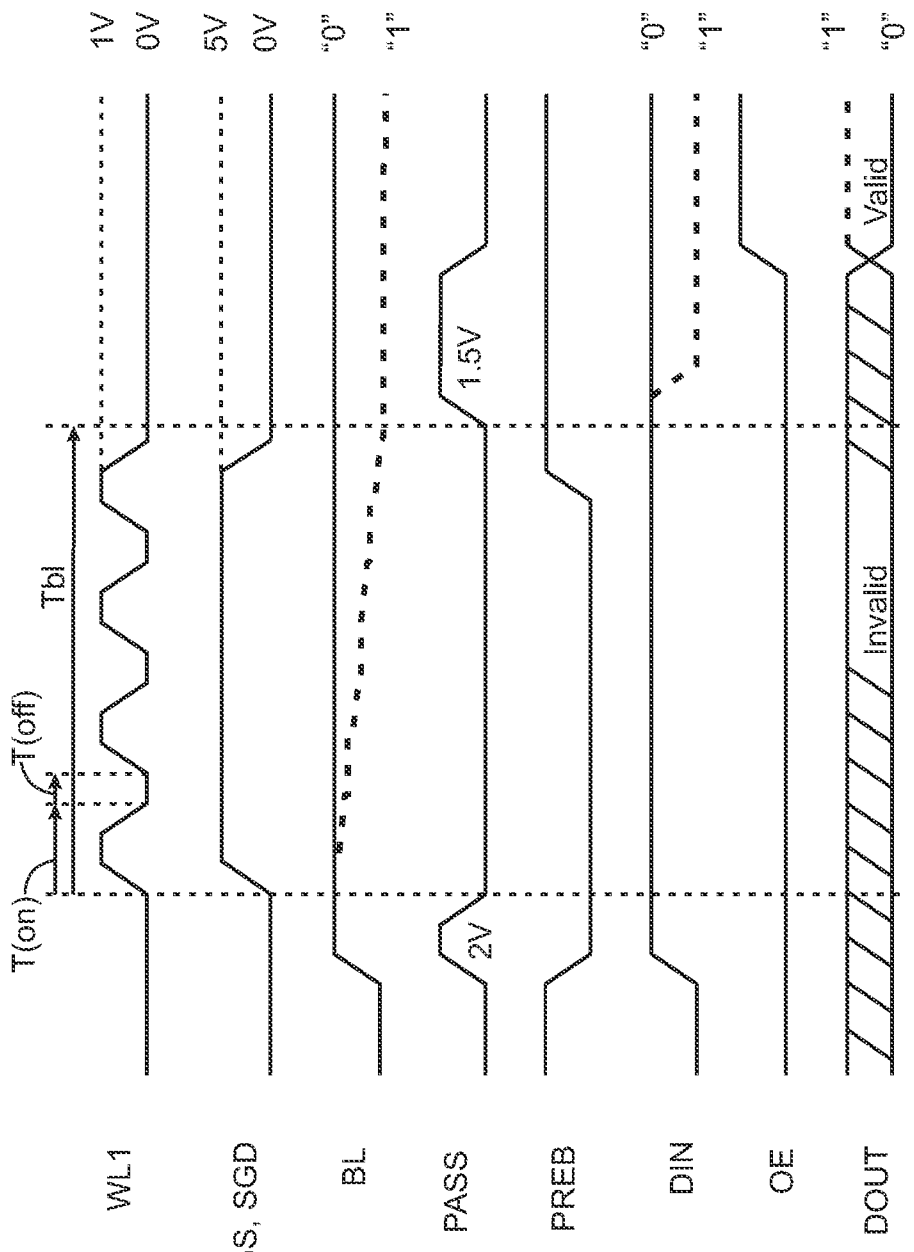
WL1
WL0,WL2,WL3, SGS, SGD
BL
PASS
PREB
DIN
OE
DOUT
T(on)
T(off)
Tbl
1V
0V
5V
0V
"0"
"1"
2V
1.5V
"0"
"1"
"1"
"0"
Invalid
Valid

FIG. 7A

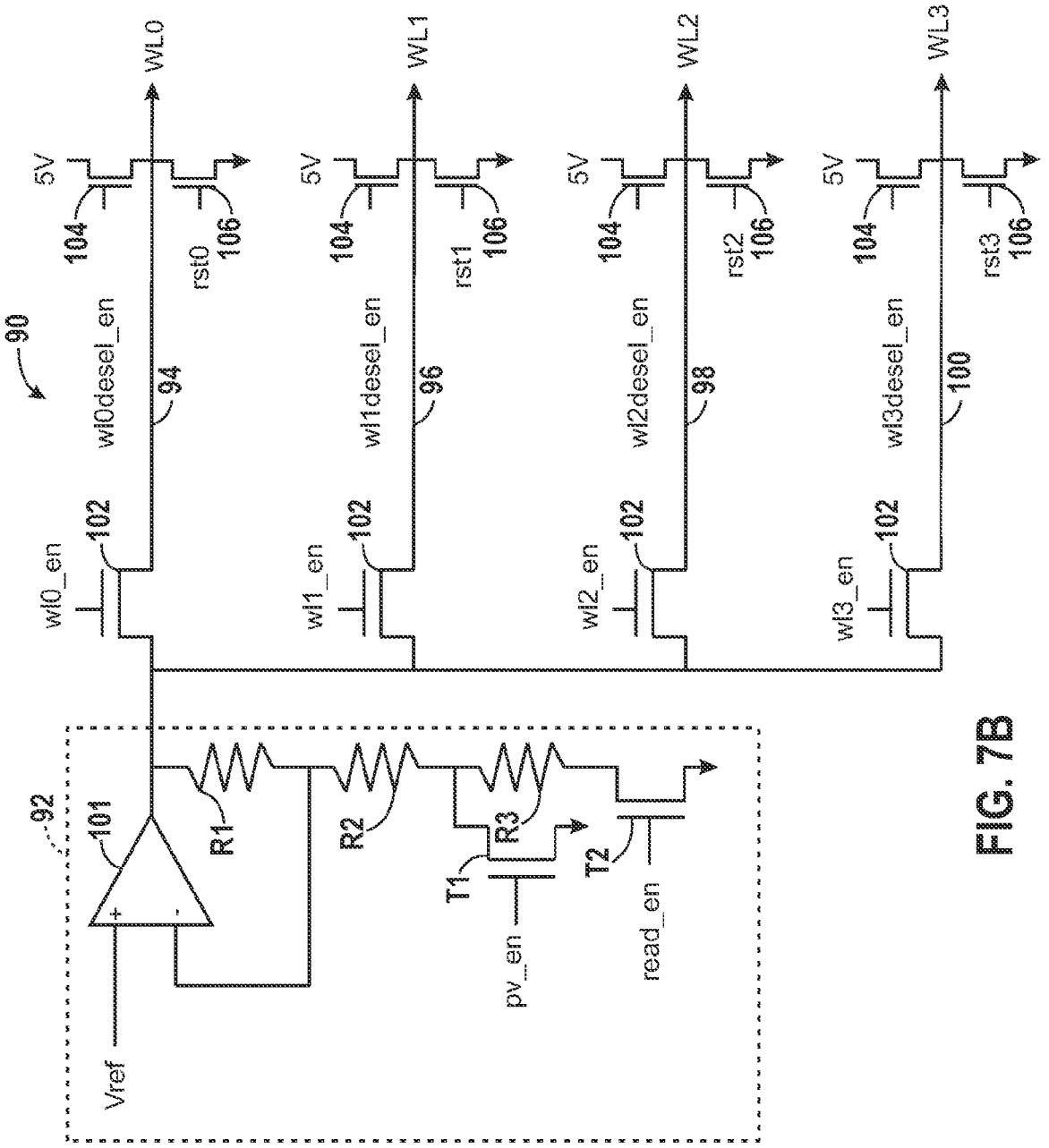
90
92
101
Vref
R1
R2
R3
T1
T2
pv_en
read_en
wl0_en
wl1_en
wl2_en
wl3_en
102
wl0desel_en
wl1desel_en
wl2desel_en
wl3desel_en
94
96
98
100
5V
104
rst0
rst1
rst2
rst3
106
WL0
WL1
WL2
WL3

FIG. 7B

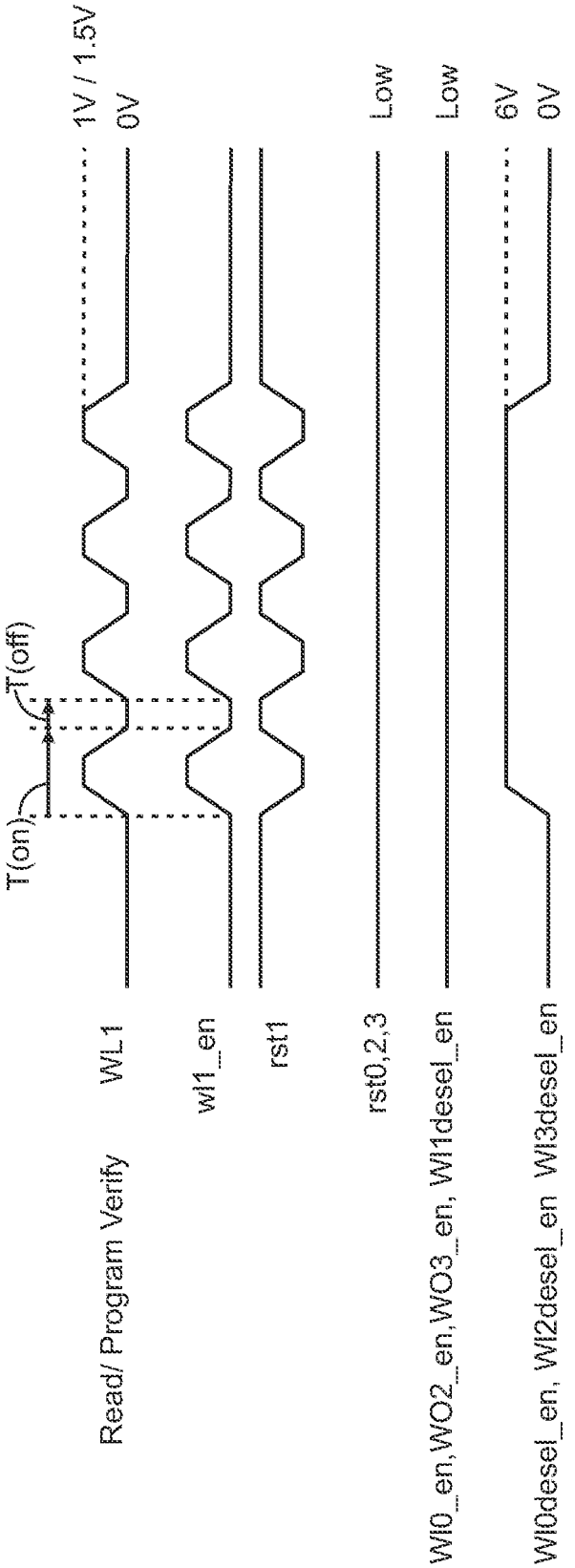
T(on)
T(off)
Read/ Program Verify
WL1
1V / 1.5V
0V
wl1_en
rst1
rst0,2,3
Low
Wl0_en,WO2_en,WO3_en, Wl1desel_en
Low
Wl0desel_en, Wl2desel_en Wl3desel_en
6V
0V

FIG. 7C

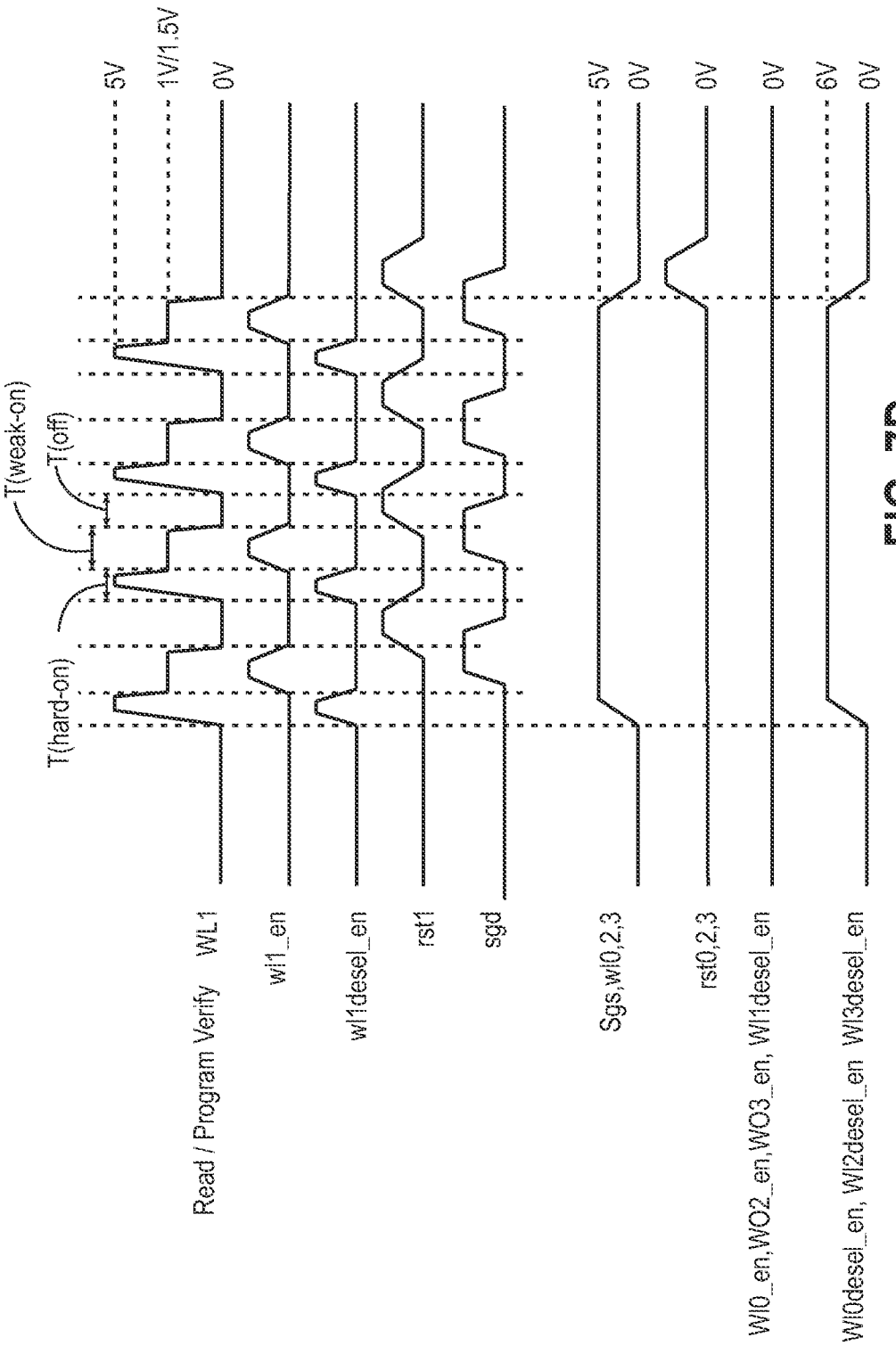
T(hard-on)
T(weak-on)
T(off)
5V
1V/1.5V
0V
Read / Program Verify WL1
wl1_en
wl1desel_en
rst1
sgd
Sgs,wl0,2,3
rst0,2,3
Wl0_en,WO2_en,WO3_en, Wl1desel_en
Wl0desel_en, Wl2desel_en Wl3desel_en
5V
0V
0V
0V
6V
0V

FIG. 7D

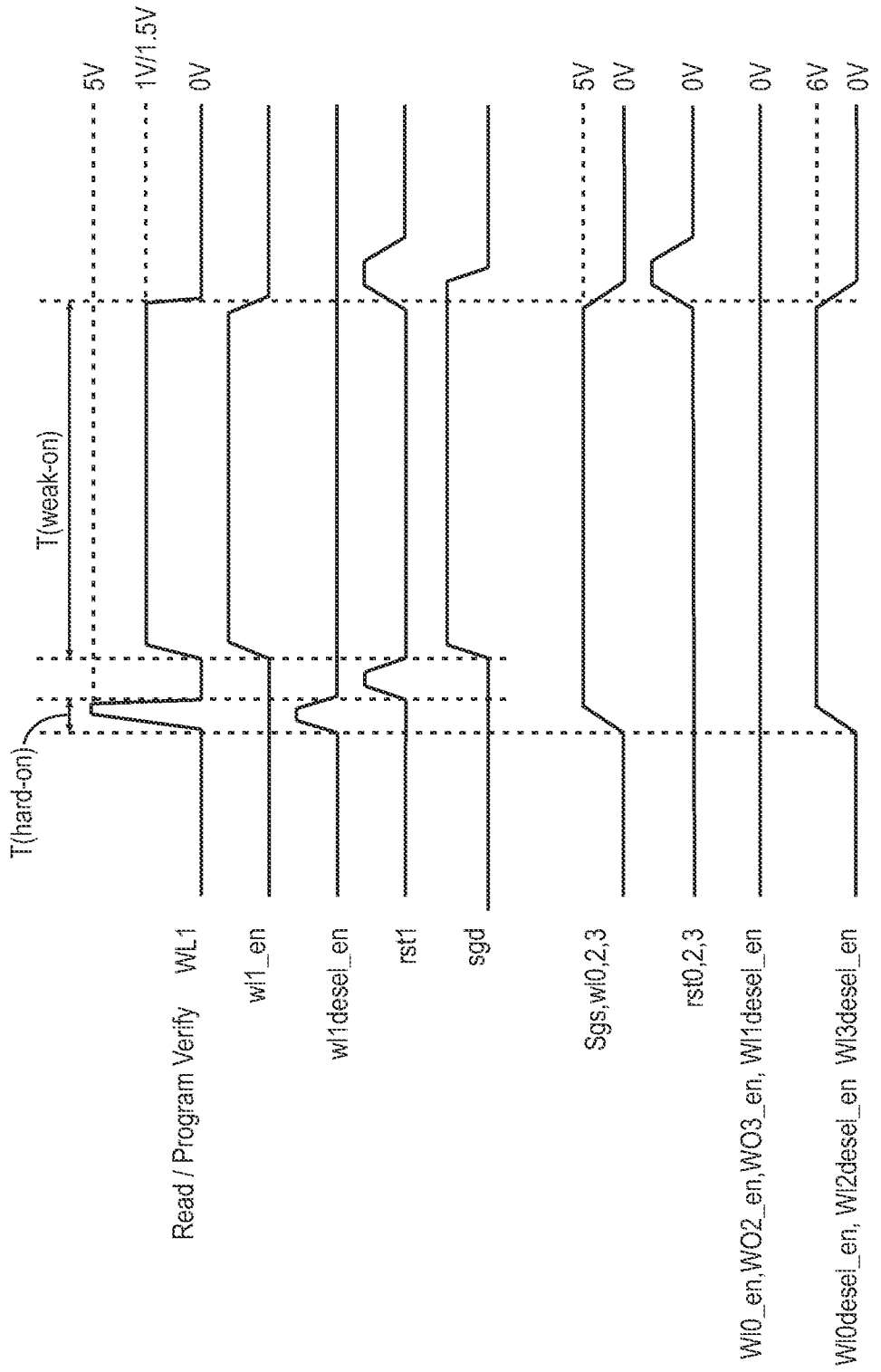
T(hard-on)
T(weak-on)
5V
1V/1.5V
0V
Read / Program Verify WL1
wl1_en
wl1desel_en
rst1
sgd
Sgs,wl0,2,3
rst0,2,3
Wl0_en,WO2_en,WO3_en, Wl1desel_en
Wl0desel_en, Wl2desel_en Wl3desel_en
5V
0V
0V
0V
6V
0V

FIG. 7E

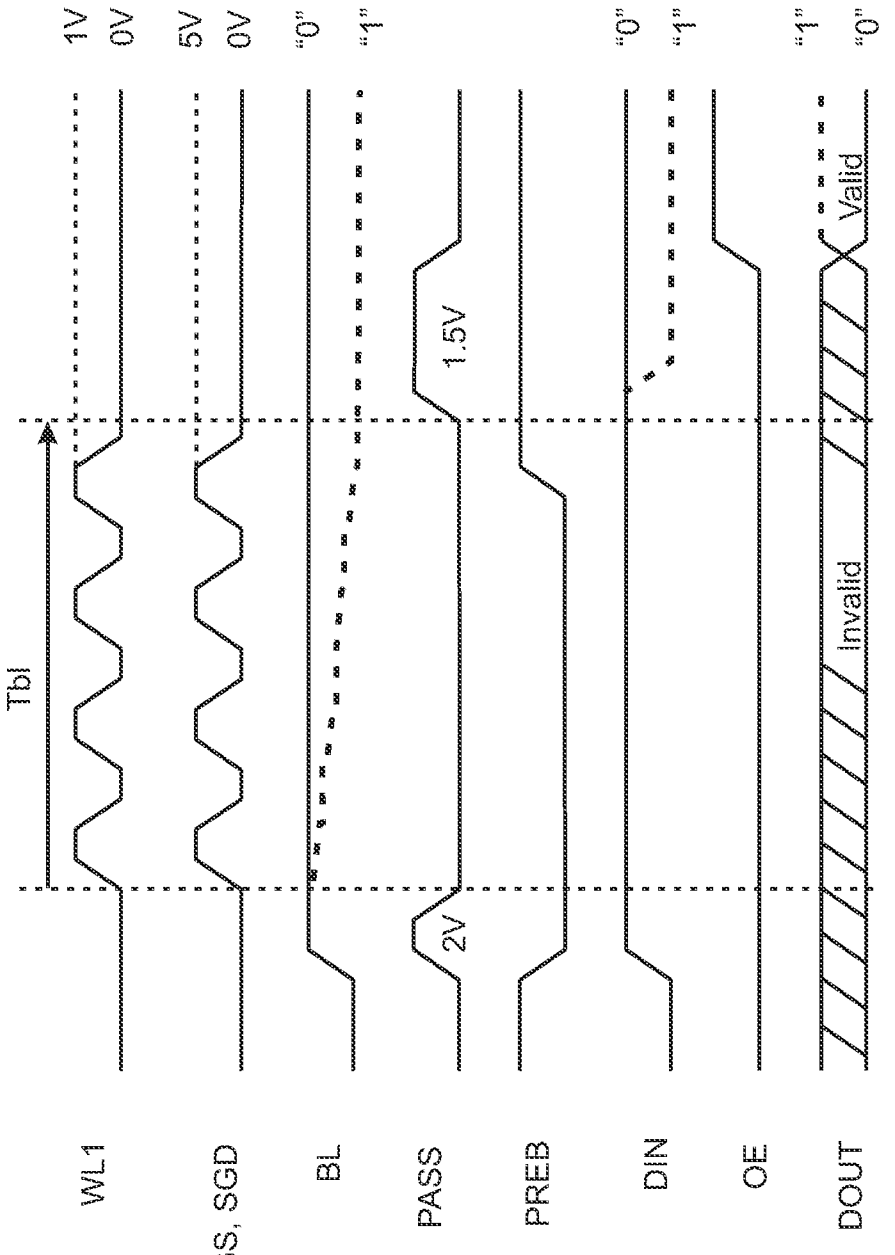
WL1
WL0,WL2,WL3, SGS, SGD
BL
PASS
PREB
DIN
OE
DOUT
Tbl
1V
0V
5V
0V
"0"
"1"
2V
1.5V
"0"
"1"
"1"
"0"
Invalid
Valid

FIG. 8

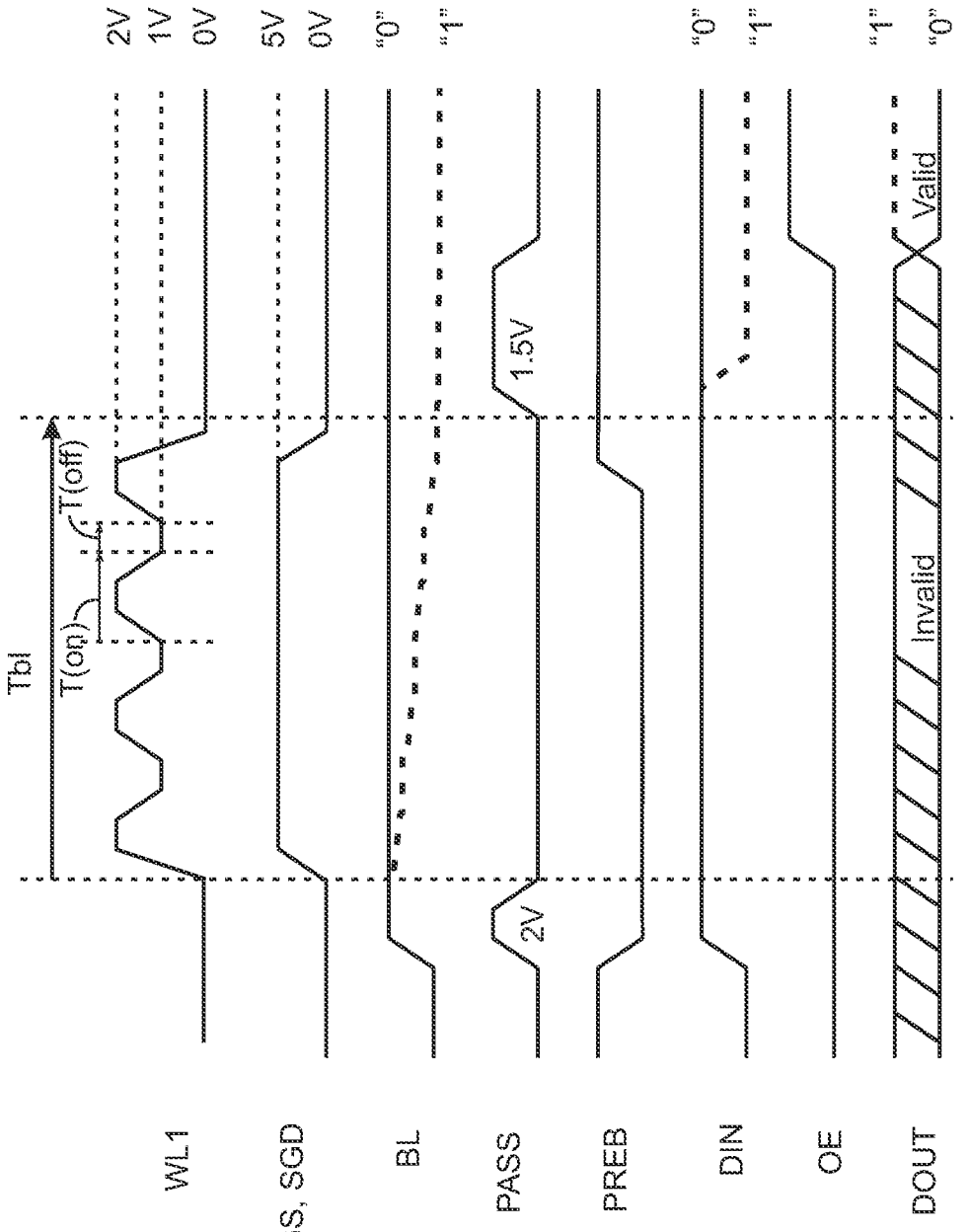
Tbl
T(on)
T(off)
2V
1V
0V
5V
0V
"0"
"1"
1.5V
2V
"0"
"1"
"1"
"0"
Invalid
Valid
WL1
WL0,WL2,WL3, SGS, SGD
BL
PASS
PREB
DIN
OE
DOUT

FIG. 9A

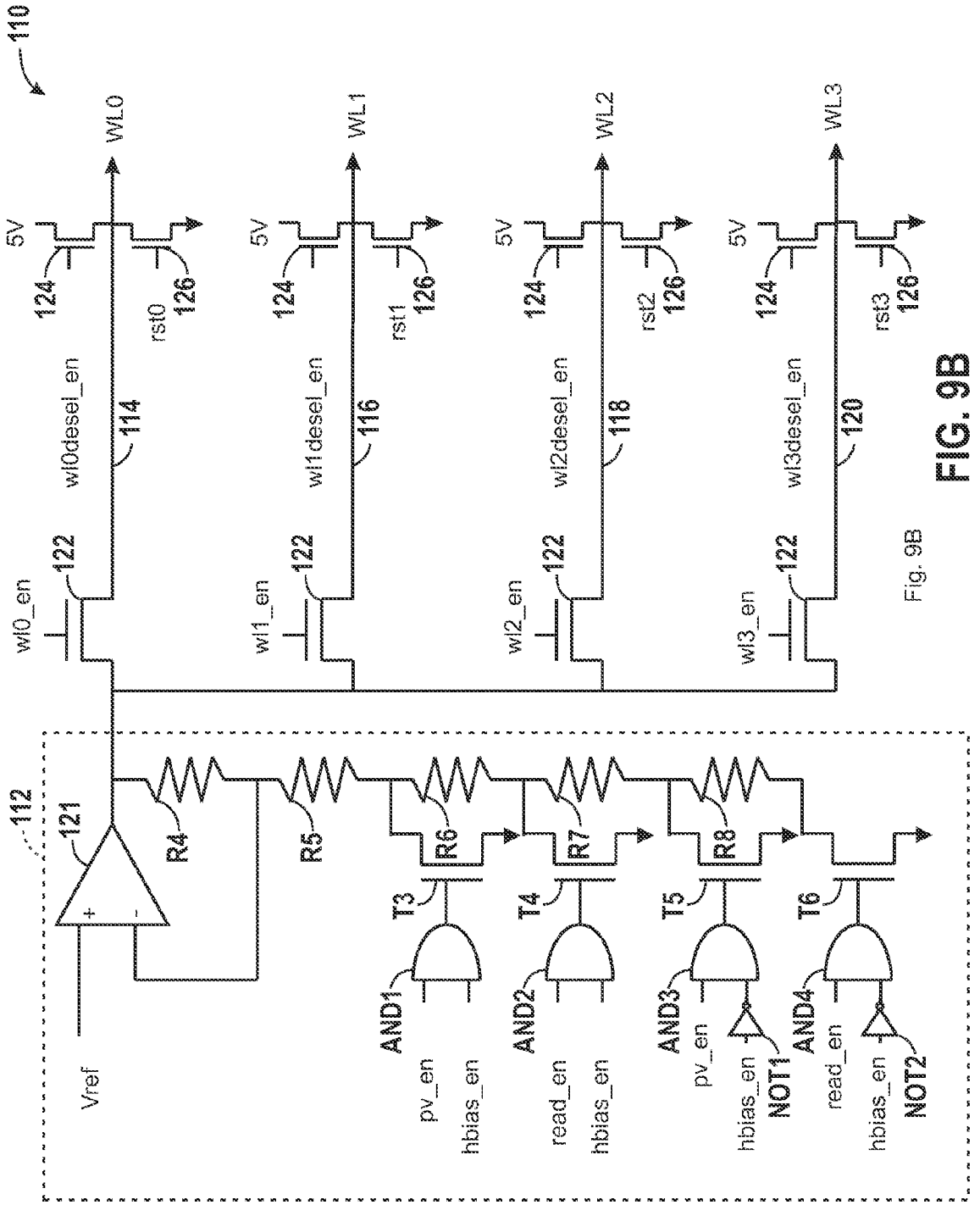
110
WL0
WL1
WL2
WL3
5V
124
126
rst0
rst1
rst2
rst3
wl0desel_en
wl1desel_en
wl2desel_en
wl3desel_en
114
116
118
120
122
wl0_en
wl1_en
wl2_en
wl3_en
112
121
Vref
R4
R5
R6
R7
R8
T3
T4
T5
T6
AND1
AND2
AND3
AND4
pv_en
hbias_en
read_en
NOT1
NOT2

Fig. 9B

FIG. 9B

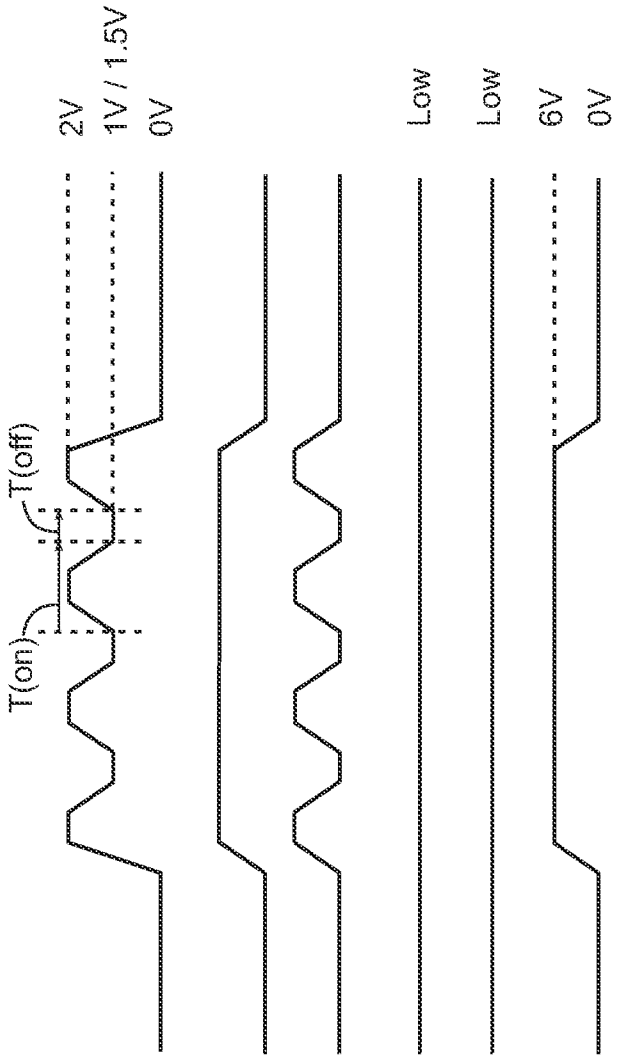
T(on)
T(off)
2V
1V / 1.5V
0V
Read/Program Verify WL1
wl1_en
hbias_en
rst0, rst1, rst2, rst3
Low
wl0_en,wl2_en,wl3_en, wl1desel_en
Low
wl0desel_en, wl2desel_en, wl3desel_en
6V
0V

FIG. 9C

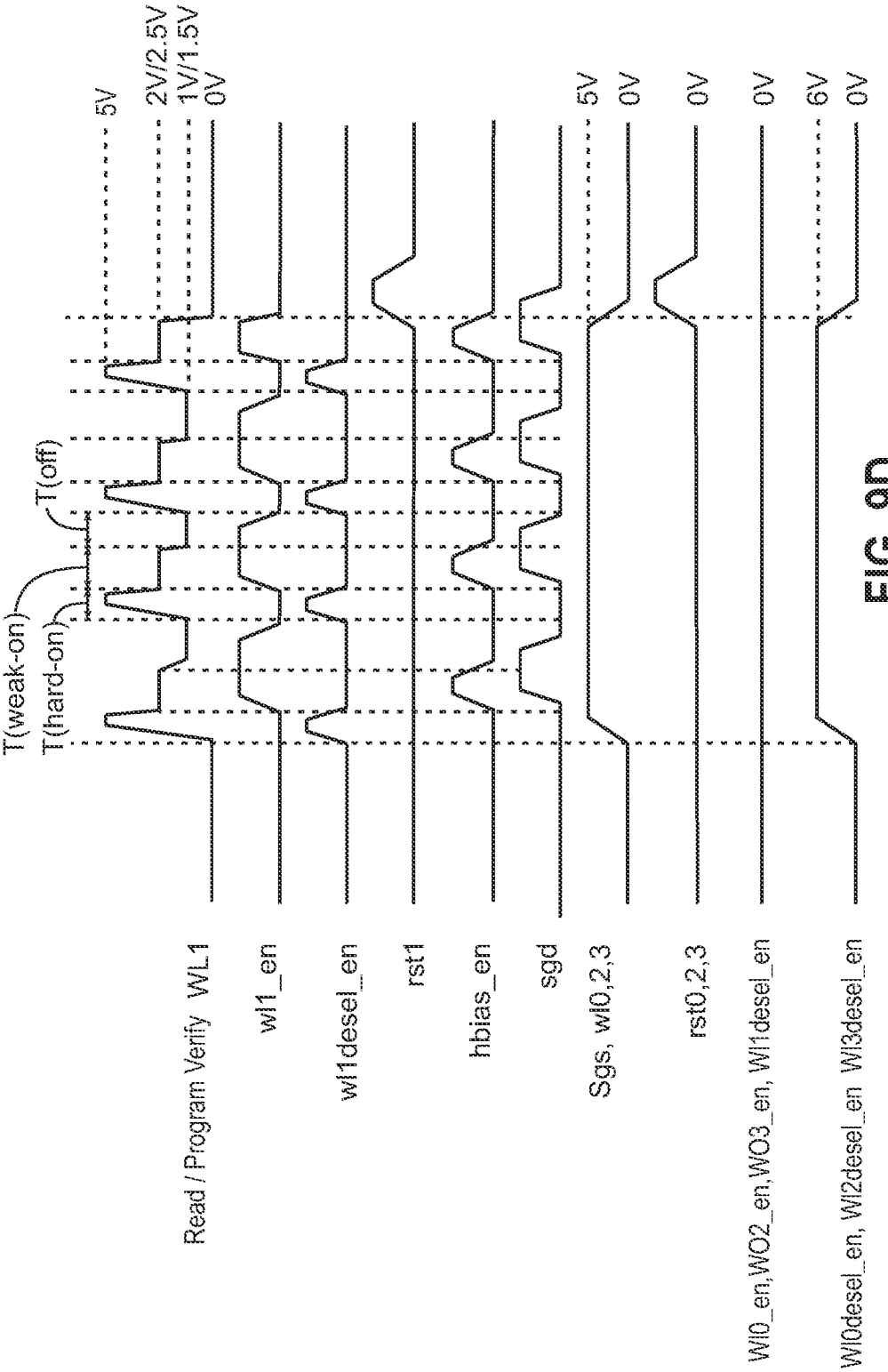
T(weak-on)
T(hard-on)
T(off)
5V
2V/2.5V
1V/1.5V
0V
Read / Program Verify WL1
wl1_en
wl1desel_en
rst1
hbias_en
sgd
Sgs, wl0,2,3
rst0,2,3
Wl0_en,WO2_en,WO3_en, Wl1desel_en
Wl0desel_en, Wl2desel_en Wl3desel_en
5V
0V
0V
0V
6V
0V

FIG. 9D

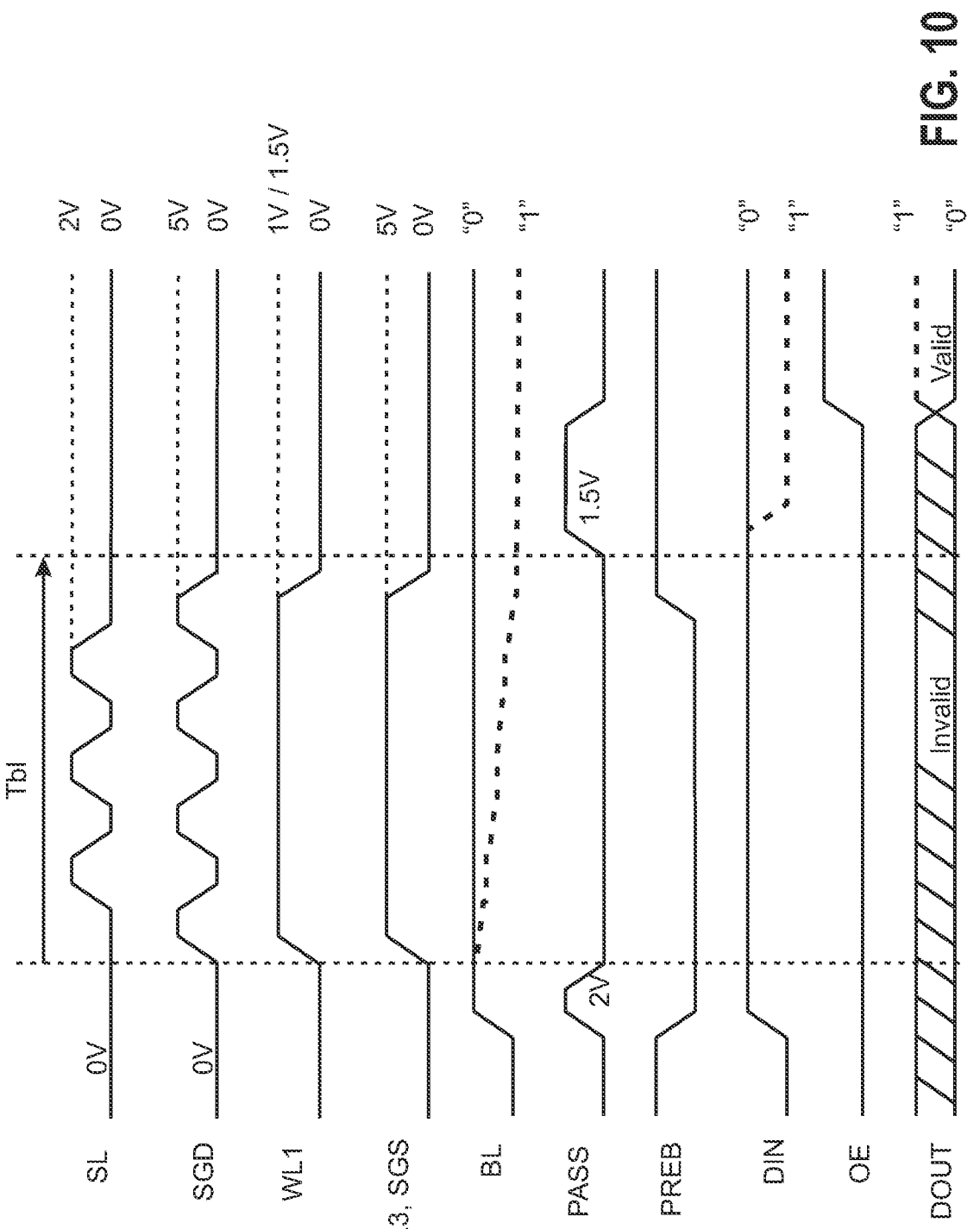
Tbl
SL
SGD
WL1
WL0, WL2, WL3, SGS
BL
PASS
PREB
DIN
OE
DOUT
0V
2V
0V
5V
0V
1V / 1.5V
0V
5V
0V
"0"
"1"
2V
1.5V
"0"
"1"
"1"
"0"
Invalid
Valid

FIG. 10

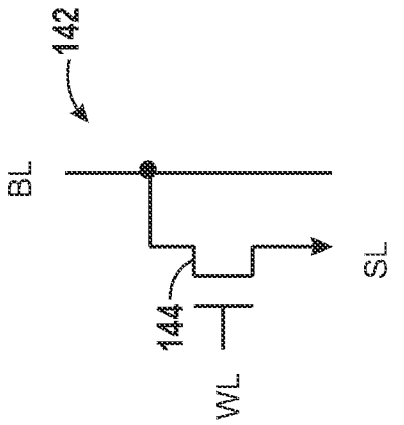

FIG. 11C

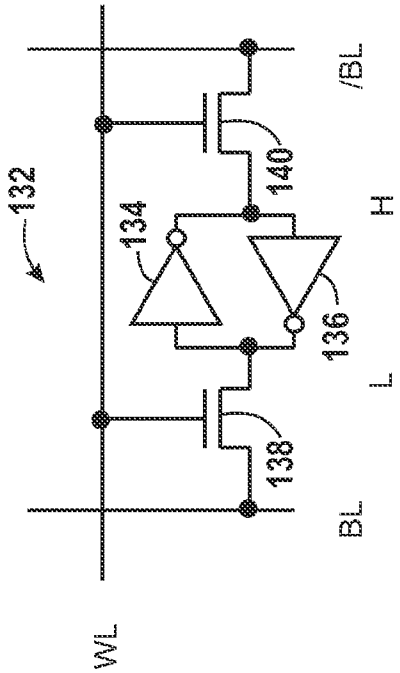

FIG. 11B

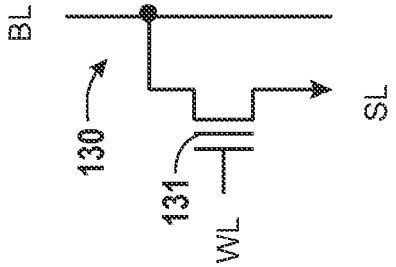

FIG. 11A

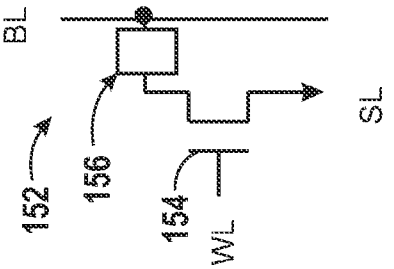

FIG. 11E

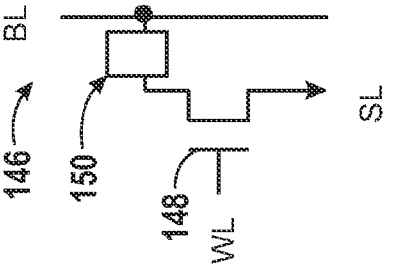

FIG. 11D

RANDOM TELEGRAPH SIGNAL NOISE REDUCTION SCHEME FOR SEMICONDUCTOR MEMORIES

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. patent application Ser. No. 13/971,626, which was filed on Aug. 20, 2013, now U.S. Pat. No. 8,780,638, which issued on Jul. 15, 2014, which is a continuation of U.S. patent application Ser. No. 13/480,378, which was filed on May 24, 2012, now U.S. Pat. No. 8,537,620, which issued on Sep. 17, 2013, which is a continuation of U.S. patent application Ser. No. 13/047,562, which was filed on Mar. 14, 2011, now U.S. Pat. No. 8,194,459, which issued on Jun. 5, 2012, which is a divisional of U.S. patent application Ser. No. 12/020,460, which was filed on Jan. 25, 2008, now U.S. Pat. No. 7,916,544, which issued on Mar. 29, 2011.

BACKGROUND

1. Field of the Invention

Embodiments of the invention relate generally to the field of memory devices and more particularly, to reducing the effect of random telegraph signal noise (RTS noise) in semiconductor memories.

2. Description of the Related Art

Flash memory is a non-volatile memory that can be electrically erased and reprogrammed. It is primarily used in memory cards, USB flash drives, and the like for storage of data in computer systems. Generally, flash memory stores information in an array of floating gate transistors, called "cells", each of which traditionally stores one bit of information that is represented as a "0" or a "1". Each cell is characterized by a threshold voltage (Vt) that varies based on the data stored in the cell. For example, during program and erase operations, charge is added or removed from a floating gate to change the cell's threshold voltage, thereby defining whether the cell is programmed or erased. During a read operation, a read voltage is applied to the cell and a response of the cell (e.g., a current across the cell) is monitored to determine whether the threshold voltage is above or below the read voltage. In other words, the read operation can determine if the cell is programmed as a 1 or a 0 value. Multi-level cells may include multiple threshold voltage ranges that are representative of additional values, such as two or more bits of information.

Flash memories may also employ a verify operation that ensures that each cell is programmed as a given state, such as a 1 or a 0. The verify operation may provide a sufficient margin between the 1 and 0 states such that a cell is charged to a given range and does not charge to an intermediate state where the cell may be read incorrectly. However, when the memory cells are programmed at one temperature and are read out at another temperature, the margin may decrease, potentially causing the value of the cell to be read incorrectly. For example, when the read operation is executed during a first period at a first temperature, the data may tend to be a 0, and when the read operation is executed during a second period at a second temperature, the data may tend to be a 1. This is prevalent where a word line voltage is a constant voltage value over the range of temperatures. The variations may be attributed to random telegraph noise (RTS noise) and the resulting time dependency of the current that passes through the memory cell. The RTS noise can be attributed to the trap and detrap of electrons or the recombination of electrons with holes. Unfortunately, the presence of the RTS noise and the resulting inaccuracies in reading the memory cells may produce inaccurate and/or less reliable memory devices.

Embodiments of the present invention may be directed to one or more of the problems set forth above.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram that illustrates a processor-based device having a memory that includes memory devices fabricated in accordance with one or more embodiments of the present invention;

FIG. **2** is a block diagram that illustrates a memory device having a memory array fabricated in accordance with one or more embodiments of the present invention;

FIG. **3** is a schematic diagram of a NAND flash memory array having memory cells fabricated in accordance with one or more embodiments of the present invention;

FIG. **4** is a graph that illustrates the variation in a cell current over various periods;

FIG. **5** is a schematic diagram of a column of the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **6** is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **7**A is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **7**B is a schematic diagram of a regulator circuit in accordance with one or more embodiments of the present invention.

FIG. **7**C is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **7**D is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **7**E is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **8** is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **9**A is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **9**B is a schematic diagram of a regulator circuit in accordance with one or more embodiments of the present invention;

FIG. **9**C is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **9**D is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention;

FIG. **10** is a timing diagram of operating the NAND flash memory in accordance with one or more embodiments of the present invention; and

FIGS. **11**A-**11**E are schematic diagrams of devices that can employ techniques in accordance with one or more embodiments of the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

As discussed in further detail below, the disclosed systems and methods relate to a random telegraph noise (RTS noise)

reduction scheme for semiconductor memory devices. In certain embodiments, signals to the word line and/or the select gate are pulsed to enable trapped electrons in the semiconductor to recombine with holes (i.e., detrap) during an accumulation period, to reduce the electron trap for the next inversion period. Detrap should reduce the RTS noise, thereby increasing the verify margin between states. In other words, the uncertainty that is present due to RTS noise during read and verify operations should be reduced. Before a detailed discussion of the system and methods described in accordance with various embodiments of the present invention, it may be beneficial to discuss embodiments of memory devices that may incorporate the devices described herein, in accordance with embodiments of the present technique.

Turning now to the figures, FIG. **1** includes a block diagram depicting a processor-based system, generally designated by reference numeral **10**. The system **10** may be any of a variety of types such as a computer, pager, cellular phone, personal organizer, control circuit, etc. In a typical processor-based device, a processor **12**, such as a microprocessor, controls the processing of system functions and requests in the system **10**. Further, the processor **12** may comprise a plurality of processors that share system control.

The system **10** typically includes a power supply **14**. For instance, if the system **10** is a portable system, the power supply **14** may advantageously include permanent batteries, replaceable batteries, and/or rechargeable batteries. The power supply **14** may also include an AC adapter, so that the system **10** may be plugged into a wall outlet, for instance. The power supply **14** may also include a DC adapter such that the system **10** may be plugged into a vehicle cigarette lighter, for instance.

Various other devices may be coupled to the processor **12** depending on the functions that the system **10** performs. For instance, a user interface **16** may be coupled to the processor **12**. The user interface **16** may include buttons, switches, a keyboard, a light pen, a mouse, and/or a voice recognition system, for instance. A display **18** may also be coupled to the processor **12**. The display **18** may include an LCD display, a CRT, LEDs, and/or an audio display, for example.

Furthermore, an RF sub-system/baseband processor **20** may also be couple to the processor **12**. The RF sub-system/baseband processor **20** may include an antenna that is coupled to an RF receiver and to an RF transmitter (not shown). A communications port **22** may also be coupled to the processor **12**. The communications port **22** may be adapted to be coupled to one or more peripheral devices **24** such as a modem, a printer, a computer, or to a network, such as a local area network, remote area network, intranet, or the Internet, for instance.

Because the processor **12** controls the functioning of the system **10** by implementing software programs, memory is used in conjunction with the processor **12**. Generally, the memory is coupled to the processor **12** to store and facilitate execution of various programs. For instance, the processor **12** may be coupled to system memory **26**, which may include volatile memory, such as Dynamic Random Access Memory (DRAM) and/or Static Random Access Memory (SRAM). The system memory **26** may also include non-volatile memory, such as read-only memory (ROM), EEPROM, and/or flash memory to be used in conjunction with the volatile memory. As discussed in further detail below, the system memory **26** may include one or more memory devices, such as flash memory devices, that include a floating gate memory array fabricated and implementing techniques in accordance with one or more embodiments of the present invention.

FIG. **2** is a block diagram that illustrates a flash memory device **30** that may be included as a portion of the system memory **26** of FIG. **1**. As will be discussed in further detail with respect to FIG. **3**, the flash memory device **30** may be a NAND flash memory device. The flash memory device **30** generally includes a memory array **32**. The memory array **32** generally includes many rows and columns of conductive traces arranged in a grid pattern. "Access lines" are used to access cells and generally correspond to the rows or "row lines" of the memory array **32**. In the conventional art, they are generally referred to as "word lines." "Data lines" generally correspond to the columns or "column lines." In the conventional art, they are generally referred to as "digit (e.g., bit) lines." The size of the memory array **32** (i.e., the number of memory cells) will vary depending on the size of the flash memory device **30**.

To access the memory array **32**, a row decoder block **34** and a column decoder block **36** are provided and are configured to receive and translate address information from the processor **12** via the address bus **38** and the address buffer **40** and to access a particular memory cell in the memory array **32**. A sense amplifier block **42**, having a plurality of the sense amplifiers, is also provided inline with the column decoder **36** and the memory array **32**. The sense amplifier block **42** senses and amplifies individual values stored in the memory cells. A row driver block **46** is provided to activate a selected word line in the memory array according to a given row address.

An internal voltage source **44**, such as a voltage generator, is provided to deliver voltages for use within the memory device **30**. The internal voltage source **44** may provide voltage levels for program, program, read, verify, and erase operations. The internal voltage source **44** may include a trimming circuit to accurately regulate the voltage level output by the internal voltage source **44**.

During read and program operations, data may be transferred to and from the flash memory device **30** via the data bus **48**. The coordination of the data and address information may be conducted through a control circuit **50**. The control circuit **50** may be configured to receive control signals from the processor **12** via the control bus **52**. A command buffer **54** may be configured to temporarily store commands of the control circuit **50**. The control circuit **50** is coupled to each of the row decoder block **34**, the column decoder block **36**, the address buffer **40**, the sense amplifier block **42**, the internal voltage generator **44**, the row driver block **46**, and the command buffer **54**, and is generally configured to coordinate timing and control among the various circuits in the flash memory device **30**.

FIG. **3** illustrates an embodiment of the memory array **32**, of FIG. **2**. In the illustrated embodiment, the memory array **32** includes a NAND memory array **56**. The NAND memory array **56** includes word lines WL(**0**)-WL(M) and intersecting local bit lines BL(**0**)-BL(N). As will be appreciated, for ease of addressing in the digital environment, the number of word lines WL and the number of bit lines BL are each a power of two (e.g., 256 word lines (WL) by 4,096 bit lines (BL)). The local bit lines BL are coupled to global bit lines (not shown) in a many-to-one relationship.

The NAND memory array **56** includes a floating gate transistor **58** located at each intersection of a word line (WL) and a local bit line (BL). The floating gate transistors **58** serve as non-volatile memory cells for storage of data in the NAND memory array **56**, as previously discussed. As will be appreciated, each floating gate transistor includes a source, a drain, a floating gate, and a control gate. The control gate of each floating gate transistor **58** is coupled to a respective word line (WL). The floating gate transistors **58** are connected in series,

source to drain, to form a NAND string **60** formed between gate select lines. Specifically, the NAND strings **60** are formed between the drain select line (SGD) and the source select line (SGS). The drain select line (SGD) is coupled to each NAND string **60** through a respective drain select gate **62**. Similarly, the source select line (SGS) is coupled to each NAND string **60** through a respective source select gate **64**. The drain select gates **62** and the source select gates **64** may each comprise a field-effect transistor (FET), for instance. A column of the memory array **56** includes a NAND string **60** and the source select gate **64** and drain select gate **62** connected thereto. A row of the floating gate transistors **58** are those transistors commonly coupled to a given word line (WL).

The source of each source select gate **64** is connected to a common source line (SL). The drain of each source select gate **64** is coupled to the source of a floating gate transistor **58** in a respective NAND string **60**. The gate of each source select gate **64** is coupled to the source select line (SGS).

The drain of each drain select gate **62** is connected to a respective local bit line (BL) for the corresponding NAND string **60**. The source of each drain select gate **62** is connected to the drain of a floating gate transistor **58** of a respective NAND string **60**. Accordingly, as illustrated in FIG. **3**, each NAND sting **60** is coupled between a respective drain select gate **62** and source select gate **64**. The gate of each drain select gate **62** is coupled to the drain select line (SGD).

During operation of the flash memory device **30**, multiple voltages are generated within the memory device **30** to accomplish various tasks. For example, the memory device **30** may employ multiple voltage levels applied to the word lines, bit lines, and the like, to program, read, erase and verify values stored in the cells of the memory array **32**. Specifically, the flash memory device **30** may employ a verify operation that ensures that each cell is programmed as in a given state, such as a 1 or a 0. The verify operation may provide a sufficient margin between the 1 and 0 states such that a selected cell is charged into a given range and does not charge to an intermediate state that may cause the selected cell to be read incorrectly. However, when the memory cells are programmed at one temperature and are read out at another temperature, the margin may decrease, leading to a possibility that the value of the selected cell may be read incorrectly.

For example, as illustrated in FIG. **4**, when the read operation is executed during a first period **66** at a first temperature, the level of a sensed current (Icell) across the selected cell may be indicative of a 0 value, and when the read operation is executed during a second period **68** at a second temperature, the level of the sensed current (Icell) across the selected cell may be indicative of a 1 value. This is prevalent where a word line voltage is a constant voltage value over the range of temperatures. The variations may be attributed, at least partially, to random telegraph noise (RTS noise) and the resulting time dependency of the current that passes through the memory cell. The RTS noise can be attributed to the trap and detrap of electrons or the recombination of electrons with holes. Unfortunately, the presence of the RTS noise and the resulting inaccuracies in reading the memory cells may produce inaccurate results and/or reduce the reliability of the memory device. The following techniques for reducing RTS noise are discussed in the context of a NAND flash memory device and, to simplify the discussion, are discussed in the context of a single column of a NAND memory array.

FIG. **5** is a schematic diagram of a column **70** of a NAND memory array. The column **70** includes a floating gate transistor (i.e., a cell) **72** located at each intersection of a word line (WL) (e.g., WL**0**, WL**1**, WL**2**, WL**3**) and a local bit line (BL). The control gate of each cell **72** is coupled to a respective word line (WL).

The cells **72** are connected in series, source to drain, to form a NAND string **74** formed between a drain select line (SGD) and a source select line (SGS). The drain select line (SGD) is coupled to the NAND string **74** through a respective drain select gate transistor **76**, and the source select line (SGS) is coupled to the NAND string **74** through a respective source select gate transistor **78**. The source of the source select gate transistor **78** is connected to a common source line (SL), the drain of the source select gate transistor **78** is coupled to the source of a cell **72** of the NAND string **74**, and the gate of the source select gate transistor **78** is coupled to the source select line (SGS). The drain of the drain select gate transistor **76** is connected to the local bit line (BL) of the NAND string **74**, the source of the drain select gate transistor (SGD) **76** is connected to the drain of a cell **72** of the NAND string **74**, and the gate of the drain select gate transistor **76** is coupled to the drain select line (SGD).

The local bit line (BL) is coupled to a sense amplifier **80**. The sense amplifier **80** includes a PASS transistor **82**, a PREB transistor **84**, and an inverter **86**. The bit line (BL) is coupled to a source of the PASS transistor **82**. The gate of the PASS transistor **82** is coupled to a PASS line (PASS), and the drain of the PASS transistor **82** is coupled to a data-in node (DIN). A drain of a PREB transistor **84** is coupled to the data-in node (DIN), a source of the PREB transistor **84** is coupled to a common voltage (Vcc), and a floating gate of the PREB transistor **84** is coupled to a PREB line (PREB). The data-in node (DIN) is coupled to an input of the inverter **86** that is coupled to an output enable (OE) signal. The inverter **86** has an output on a data-out line (DOUT).

FIG. **6** is a timing diagram that illustrates signals in accordance with an operation of sensing (e.g., reading or verifying) cell data. This figure may be reviewed in conjunction with FIG. **5**, for example. The bit line (BL) is precharged to about 1V(volt) with the PASS line (PASS) biased with 2V. At the beginning of a discharging period (Tbl), the word lines (WL) and the select gate signals (SGS and SGD) are transition from a low voltage to a high voltage. For example, the word line of the selected cell (WL**1**) is raised to about 1V. The word line to the unselected cells (WL**0**, WL**2**, and WL**3**) and the select gate signals (SGS and SGD) are raised to a high level, such as 5V.

After the bit line (BL) is precharged, the PASS line (PASS) is grounded to disconnect the data-in node (DIN) from the bit line (BL). Depending on the memory data, the bit line (BL) voltage is reduced or remains high. For example, where the data stored on the selected cell is "1" the bit line (BL) voltage lowers, as indicated by the dashed line that lowers to a "1" state. Where the data stored on the selected cell is "0" the bit line (BL) voltage remains high, at 1V, as indicated by the bit line (BL) signal maintaining a "0" state. During this period, the data-in node (DIN) voltage is forced to Vcc, for example 3V. At the end of the discharging period (Tbl), the PASS line (PASS) voltage is raised to 1.5V.

Where the data stored on the cell is "0", if the bit line (BL) is maintained at 1V, the gate-source voltage (Vgs) of the PASS transistor **82** is 0.5V (0.5V=1.5V−1V) and the PASS transistor **82** is in an off state, assuming the threshold voltage (Vt) of the PASS transistor **82** is about 1V. The data-in node (DIN) voltage is also maintained high as 3V. The data-out line (DOUT) voltage goes low with the output enable (OE) high. The data on the data-out line (DOUT) is transferred to a DQ pad and the resultant data represents "0".

Where the data stored on the cell is "1", if the bit line (BL) is discharged according to the cell current (Icell), the bit line (BL) voltage lowers to about 0V. The gate-source voltage (Vgs) of the PASS transistor **82** is 1.5V (1.5V=1.5V−0V) so that the PASS transistor **82** is on. The data-in node (DIN) voltage is discharged to a bit-line (BL) capacitance, resulting in a data-in (DIN) voltage of 0V. The data-out line (DOUT) transitions to high with the output enable (OE) high. The data on the data-out line (DOUT) is transferred to the DQ pad and the resultant data represents "1".

It should be noted that a similar technique may be used for a verify operation, wherein the voltage on the word line of the selected cell (WL**1**) is driven to a higher voltage, such as 1.5V.

As discussed previously, if the memory device **30** operates in accordance with the embodiments of FIG. **6**, it may be susceptible to RTS noise that is attributable, at least in part, to the trap and detrap of electrons or a recombination of electrons with holes in the cell. The following embodiments include a method and system that includes providing a pulsed signal (rather than a constant signal) to at least one of the plurality of cells (e.g., the selected cell) and sensing a bit line current to determine whether data is stored on one of the plurality of cells. The pulsed signal(s) alternates between a high voltage level and a low voltage level to reduce the RTS noise.

FIG. **7**A is a timing diagram that illustrates signals in accordance with an embodiment of a method of operating the memory device **30**. The method includes providing a pulsed (e.g., sequentially biased) signal to the selected cell. For example, in the illustrated embodiment, the word line to the selected cell (WL**1**) is pulsed between a low state and a high state during the discharging period (Tbl). The discharging period (Tbl) is extended for a period such that the word line signal to the selected cell (WL**1**) is in the high state for a total time that is approximately equal to the time period that the word line to the selected cell (WL**1**) is held high in an embodiment where they are not being pulsed. In other words, the total time the word line to the selected cell (WL**1**) is high in the discharge period (Tbl) is about the same amount of time the word line to the selected cell (WL**1**) is high in the illustration of FIG. **6**. Where the word line to the selected cell (WL**1**) is pulsed, the current across the bit line (BL) is integrated over the discharging period (Tbl) to determine whether data is stored on the cell and/or to identify data stored on the cell.

During the discharging period (Tbl), the pulsed word line signal to the selected cell (WL**1**) alternates between a high voltage level, where the cell is on, and a low voltage level, where the cell is off. For example, in the illustrated embodiment, the high voltage level is about 1V and the low voltage level is about 0V. While the word line signal to the selected cell (WL**1**) is supplied with the low voltage level, the memory cell connected to (WL**1**) gets accumulated to detrap electrons that trap while the word line signal to the selected cell (WL**1**) is supplied with the high voltage level. The other signals operate similar to those discussed above with regard to FIG. **6**, and incorporate a longer discharging period (Tbl). For example, the word lines to the unselected cells (WL**0**, WL**2**, and WL**3**) and the select gate signals (SGS and SGD) are raised to a high level, such as 5V, and are not pulsed (i.e., they are held at a constant voltage level).

Further, it is noted that the word line (WL**1**) is pulsed during a first time period (T(on)) and maintained in a low state during a second period (T(off)) that occurs between each of the pulses. In the illustrated embodiment the ratio of the duration of the first period to the duration of the second period (T(on)/T(off)) may be greater than 1. In other words, the duration of the first period (T(on)) may be greater than the duration of the second period (T(off)).

FIG. **7**B is a schematic diagram of a regulator circuit **90** that is configured to provide voltages to the various lines of the column **70** of the memory device **30**, in accordance with the technique discussed previously with regard to FIG. **7**A. Specifically, the regulator circuit **90** is configured to output a pulsed signal to a selected word line and to provide constant voltages to unselected word lines. The regulator circuit **90** includes a voltage input circuit **92** coupled in parallel to output **94**, **96**, **98**, and **100** that are coupled to the word lines (WL**0**, WL**1**, WL**2**, and WL**3**). In the illustrated embodiment, the voltage input circuit **92** includes a comparator **101**, three resistors R**1**, R**2**, and R**3**, and two transistors T**1** and T**2**. A reference voltage (Vref) is input to one node of the comparator **93**. Control signals program verify enable (pv_en) and read enable (read_en) are input to control gate of the transistors T**1** and T**2**, respectively.

Each of the outputs **94**, **96**, **98**, and **100** includes an enable transistor **102**, a deselect transistor **104**, and a reset transistor (RST) **106**. Enable signals (wl**0**_en, wl**1**_en, wl**2**_en, and wl**3**_en) are input to the control gate of the enable transistors **102** on the outputs **94**, **96**, **98**, and **100**, respectively. Disable signals (wl**0**desel_en, wl**1**desel_en, wl**2**desel_en, and wl**3**desel_en) are input to the control gate of the deselect transistor **104** on the outputs **94**, **96**, **98**, and **100**, respectively. RST signals (rst**0**, rst**1**, rst**2**, and rst**3**) are input to the reset transistor (RST) **106** on the outputs **94**, **96**, **98**, and **100**, respectively. The wordlines can be grounded with the input to the reset transistor (RST) high.

FIG. **7**C is a timing diagram that illustrates signals in accordance with an embodiment of method of operating the regulator circuit **90**. The diagram illustrates embodiments including, a read operation (e.g., WL1 is pulsed between 0V and 1V) or a verify operation (e.g., WL1 is pulsed between 0V and 1.5V) where the output **96** is coupled to the selected cell via the word line of the selected cell (WL**1**). The word line coupled to the selected cell (WL**1**) is pulsed as discussed above with regard to FIG. **7**A. The enable signal (wl**1**_en) is also pulsed between a low and a high state, with a profile similar to that of the word line (WL**1**) coupled to the selected cell. The RST signal (rst**1**) input to the reset transistor (RST) **106** of the outputs **96** is also pulsed during the period when the word line (WL**1**) and the enable signal (wl**1**_en) are pulsed. However, the profile of the RST signal (rst**1**) is the inverse of the word line (WL**1**) and the enable signal (wl**1**_en). In other words, the RST signal (rst**1**) is in a low state while the word line (WL**1**) and the enable signal (wl**1**_en) are in a high state, and the RST signal (rst**1**) is in a high state while the word line (WL**1**) and the enable signal (wl**1**_en) are in a low state. The RST signals (rst**0**, rst**2**, and rst**3**), the enable signals of the unselected word line/outputs (wl**0**_en, wl**2**_en, and wl**3**_en), and the disable signal (wl**1**desel_en) of the selected word line/outputs remain in the low state. The disable signals (wl**0**desel_en, wl**2**desel_en, and wl**3**desel_en) of the unselected word line/outputs are driven high (e.g. to about 6V) during the period when the world line (WL**1**) of the selected cell is pulsed. In one embodiment, when the word line capacitance is 10 picofarad (pF), a read time is 50 microseconds (us), the number of rise and falls (pulses) for the selected word line is 10, the average current is 2 microamps (uA) ((10 pF×1 V)/(50 us×10)=2 microamps (uA)), less than 1% of the total read current.

Once again, it is noted that the wordline (WL**1**) is pulsed during a first time period (T(on)) and maintained in a low state during a second period (T(off)) that occurs between each of the pulses. In the illustrated embodiment the ratio of the

duration of the first period to the duration of the second period (T(on)/T(off)) may be greater than 1. In other words, the duration of the first period (T(on)) may be greater than the duration of the second period (T(off)).

FIG. **7**D is a timing diagram that illustrates signals in accordance with another embodiment of method of operating the regulator circuit **90**. The diagram illustrates embodiments including, a read operation (e.g., word line (WL**1**) is pulsed between 0V and 1V) or a verify operation (e.g., word line (WL**1**) is pulsed between 0V and 1.5V) and having an additional voltage spike (e.g., an excited pulse) that includes a period in which the cell voltage level is strong (e.g., above the read or program verify voltage). In such embodiments, a trap site can be filled with electrons, and the subsequent read or program verify can be performed with the trap sites filled. For example, an embodiment may include a read or verify pulse that includes consecutive pulses wherein one or more of the pulses includes a first period in which the cell is subject to a strong (e.g., trap) voltage, a second period include the cell is subject to the read or verify voltage, and a third period in which the cell is turned off (e.g., subject to a low voltage, such as 0V). As is discussed in further detail below, each of the periods may be varied in duration to achieve desired results.

In the illustrated embodiment, the signals are controlled in a similar manner as to those discussed with regard to FIG. **7**C. However, the word line (WL**1**) includes a multi-level pulse having a spike in the voltage level substantially above level of the read voltage level (1V) and/or the program verify voltage level (1.5V). For example, in the illustrated embodiment, the pulse of the word line (WL**1**) transitions to a trap voltage level (5V) during a first time period (T(hard-on)), the voltage level of the pulse transitions to read voltage level (1V) and/or the program verify voltage level (1.5V) during a second time period (T(weak-on)), and the pulse ends as the voltage level transitions back to approximately 0V during a third time period (T(off)). The enable signal (wl**1**_en) is high during the second period (T(weak-on)), the deselect line (wl**1**desel_en) is high during the first period (T(hard-on)), the RST signal (rst**1**) is high during the third period (Toff), and the drain select line (SGD) transitions to a high state during the second period (T(weak-on)) and transitions back to a low state during the third period (T(off)). For example, in the illustrated embodiment, the drain select line (SGD) transitions from a low state to a high state after the transition of the word line (WL**1**) from the trap voltage level (5V) to the read voltage level (1V) and/or the program verify voltage level (1.5V), and transitions back to a low state before the next pulse in the sequence. Discharge may occur when the word line (WL**1**) is 1V or 1.5V and the gate signal (SGD) is high.

It is also noted that in the illustrated embodiment the ratio of the duration of the second time period to the duration of the third time period (T(weak-on)/T(off)) may be greater than 1. In other words, the duration of the second time period (T(weak-on)) may be greater than the duration of the third time period (T(off)). Further, the ratio of the duration of the first time period to the duration of the third time period (T(hard-on)/T(off)) may be greater than 1 or less than 1. In other words, the duration of the first time period (T(hard-on)) may be greater than or less than the duration of the third time period (T(off)).

FIG. **7**E is a timing diagram that illustrates signals in accordance with another embodiment of method of operating the regulator circuit **90**. The diagram illustrates an embodiment wherein prior to a read operation (e.g., word line (WL**1**) is pulsed between 0V and 1V) or a verify operation (e.g., word line (WL**1**) is pulsed between 0V and 1.5V) a voltage spike (e.g., an excited pulse) is applied to the selected word line (WL**1**) to fill electrons in trap sites. In such embodiments, a trap site can be filled with electrons, and the subsequent read or program verify can be performed with the trap sites filled. For example, in the illustrated embodiment, a first period (T(hard-on) includes the word line (WL**1**) being excited to a trap voltage level (5V) during a first time period (T(hard-on)), the voltage level transitions back to approximately 0V during a second time period, and the voltage level of the pulse transitions to read voltage level (1V) and/or the program verify voltage level (1.5V) during a third time period (T(weak-on)). The enable signal (wl**1**_en) is high during the third period (T(weak-on)), the deselect line (wl**1**desel_en) is high during the first period (T(hard-on)), the RST signal (rst**1**) is high during the second period, and the drain select line (SGD) transitions to a high state during the third period (T(weak-on)) and transitions back to a low state after the third period (T(weak-on)). Discharge may occur when the word line (WL**1**) is 1V or 1.5V and the gate signal (SGD) is high.

FIG. **8** is a timing diagram that illustrates signals in accordance with another embodiment of operating the memory device **30**. The method includes providing a pulsed signal to the word line of the selected cell (WL**1**), as well as providing pulsed signals to other inputs of the column **70**. For example, the word line signals to the unselected cells (WL**0**, WL**2**, and WL**3**) and the select signals (SGS and SGD) are pulsed. Similar to the embodiments discussed with regard to FIG. **7**A, during the discharging period (Tbl), the word line to the selected cell (WL**1**) is pulsed between a low state, where the cell is off, and a high state, where the cell is on. For example, the high voltage level is about 1V and the low voltage level is about 0V. While the word line signal to the selected cell (WL**1**) is supplied with the low voltage level, the memory cell connected to the word line (WL**1**) is accumulated to detrap electrons that are trapped during the period where the word line signal to the selected cell (WL**1**) is at the high voltage level. Further, during the discharging period (Tbl), the word line signals to the unselected cells (WL**0**, WL**2**, and WL**3**) and the select signals (SGS and SGD) are pulsed between a low state, where the cells/transistors are on, and a high state, where the cells/transistors are off. In the illustrated embodiment, the high voltage level is about 5V and the low voltage level is about 0V. Each of the signals (WL**0**, WL**2**, WL**3**, SGS and SGD) can be generated via a regulator circuit that is the same or similar to the regulator circuit **90** discussed with to FIG. **7**B.

FIG. **9**A is a timing diagram that illustrates signals in accordance with another embodiment of operating the memory device **30**. The method includes a read operation that may detect whether the threshold voltage (Vt) of the selected cell is lower than a high voltage level or higher than a low voltage level. In other words, the read operation determines whether the threshold voltage (Vt) of the selected cell falls within a given voltage range. The method includes providing a pulsed (e.g., sequentially biased) signal (WL**1**) to the selected cell. The signal is driven from a low state and is pulsed between a first high voltage level and a second high voltage level. For example, during the discharging period (Tbl), the pulsed word line signal to the selected cell (WL**1**) alternates between a first high voltage level of about 2V and a second high voltage level of about 1V. While the word line signal to the selected cell (WL**1**) is supplied with the low voltage level, the memory cell connected to the word line (WL**1**) gets accumulated to detrap electrons that are trapped during the period where the word line signal to the selected cell (WL**1**) is at the high voltage level. As mentioned previously, the method enables the memory device **30** to detect whether the threshold voltage (Vt) of the selected cell is

below the first high voltage level (2V) and/or higher than the second high voltage level (1V). The other signals operate similar to those discussed above with regard to FIGS. **6** and **7**A. For example, the word line to the unselected cells (WL**0**, WL**2**, and WL**3**) and the select gate signals (SGS and SGD) are driven to a high voltage level, such as 5V, and are not pulsed (i.e., they are held at a constant voltage level). Further, the discharging period (Tbl) is extended such that the word line signal to the selected cell (WL**1**) is in the high state for a total time that is approximately equal to the time period that the word line (WL**1**) is held high in an embodiment where the word line (WL**1**) is not being pulsed.

Further, it is noted that the wordline (WL**1**) is pulsed during a first time period (T(on)) and maintained in a low state during a second period (T(off)) that occurs between each of the pulses. In the illustrated embodiment the ratio of the duration of the first period to the duration of the second period (T(on)/T(off)) may be greater than 1. In other words, the duration of the first period (T(on)) may be greater than the duration of the second period (T(off)).

FIG. **9**B is a schematic diagram of a regulator circuit **110** that may provide voltages to the various lines of the column **70**, in accordance with the techniques discussed with regard to FIG. **9**A. Specifically, the regulator circuit **110** may output a pulsed signal to a selected word line and output constant voltages to unselected word lines. The pulsed signal alternates between a first high voltage level and a second high voltage level (e.g., between 2V and 1V). The regulator circuit **110** includes a voltage input circuit **112** having a high-bias enable input (hbias_en) and an output coupled in parallel to outputs **114**, **116**, **118**, and **120**. In the illustrated embodiment, the voltage input circuit **112** includes a comparator **121**, five resistors R**4**, R**5**, R**6**, R**7**, and R**8**, four AND logic gates AND**1**, AND**2**, AND**3**, and AND**4**, two inverters NOT**1** and NOT**2**, and four transistors T**3**, T**4**, T**5**, and T**6**. A reference voltage (Vref) is input to one node of the comparator **93**. Control signals program verify enable (pv_en), bias enable (hbias_en), and read enable (read_en) are coupled to the inputs of the AND logic gates AND**1**, AND**2**, AND**3**, and AND**4** and the inverters NOT**1** and NOT**2**, as depicted. Outputs of the four AND logic gates AND**1**, AND**2**, AND**3**, and AND**4** are coupled to the control gate of the four transistors T**3**, T**4**, T**5**, and T**6**, respectively. The outputs **114**, **116**, **118**, and **120** are coupled to the word lines WL**0**, WL**1**, WL**2**, and WL**3**, respectively. Each of the outputs **114**, **116**, **118**, and **120** includes an enable transistor **122**, a deselect transistor **124**, and a reset transistor (RST) **126**. Enable signals (wl**0**_en, wl**1**_en, wl**2**_en, and wl**3**_en) are input to control gates of the enable transistors **122** on the outputs **114**, **116**, **118**, and **120**, respectively. Disable signals (wl**0**desel_en, wl**1**desel_en, wl**2**desel_en, and wl**3**desel_en) are input to control the gate of the deselect transistor **124** of the outputs **114**, **116**, **118**, and **120**, respectively. RST signals (rst**0**, rst**1**, rst**2**, and rst**3**) are input to the control gate of the reset transistor (RST) **126** of the outputs **114**, **116**, **118**, and **120**, respectively.

FIG. **9**C is a timing diagram that illustrates signals in accordance with an embodiment of operating the regulator circuit **110** of FIG. **9**B. The diagram illustrates an embodiments of a read operation (e.g., an operation where WL**1** is pulsed between 2V and 1V) and/or verify operation (e.g., an operation where WL**1** is pulsed between 2V and 1.5V) where the output **116** is coupled to the selected cell via the word line WL**1**. The word line of the selected cell (WL**1**) is pulsed as discussed above with regard to FIG. **9**A. The enable signal (wl**1**_en) is driven to a high state/voltage level and is held constant while the word line of the selected cell (WL**1**) is pulsed. The high-bias enable input (hbias_en) is pulsed between a high voltage level and a low voltage level, with a profile similar to that of the word line of the selected cell (WL**1**). The RST signals (rst**0**, rst**1**, rst**2**, and rst**3**), the enable signals of the unselected word line/outputs (wl**0**_en, wl**2**_en, and wl**3**_en), and the disable signal (wl**1**_desel_en) of the selected word line/outputs remain at a low voltage/state during the period when the word line of the selected cell (WL**1**) is pulsed. The disable signals (wl**0**desel_en, wl**2**desel_en, and wl**3**desel_en) of the unselected word line/outputs are driven high during the period when the world line of the selected cell (WL**1**) is pulsed. In one embodiment, when the word line capacitance is 10 pF, a read time is 50 us, the number of rise and falls (pulses) for the selected word line is 10, the average current is 2uA ((10 pF×1 V)/(50 us×10)=2 uA, less than 1% of the total read current.

Once again, it is noted that the wordline (WL**1**) is pulsed during a first time period (T(on)) and maintained in a low state during a second period (T(off)) that occurs between each of the pulses. In the illustrated embodiment the ratio of the duration of the first period to the duration of the second period (T(on)/T(off)) may be greater than 1. In other words, the duration of the first period (T(on)) may be greater than the duration of the second period (T(off)).

FIG. **9**D is a timing diagram that illustrates signals in accordance with another embodiment of method of operating the regulator circuit **90**. The diagram illustrates an embodiment including, a read operation (e.g., word line (WL**1**) is pulsed between 1V and 2V) and/or a verify operation (e.g., word line (WL**1**) is pulsed between 1.5V and 2.5V) and having an additional voltage spike (e.g., excited pulse) that occurs at the beginning of the high state of the pulse. In such embodiments, a trap site can be filled with electrons during the spike, and the subsequent read or program verify can be performed with the trap sites filled.

In the illustrated embodiment, the signals are controlled in a similar manner as to those discussed with regard to FIG. **9**C. However, the word line (WL**1**) includes a multi-level pulse that first transitions to a trap voltage level, and returns to the high voltage level before returning to the low voltage level (e.g., above 0V) between the pulses. For example, in the illustrated embodiment, the pulses of the word line (WL**1**) transition from 0V or the low voltage level (1V or 1.5V) to the trap voltage level (5V) during a first time period (T(hard-on) (during which the trap sites may be filled with electrons), the voltage level of the pulse transitions back to the high level (2V or 2.5V) of the read or verify voltage pulse during a second period (T(weak-on)), and voltage level transitions back to the low voltage level (1V or 1.5V) of the read or verify voltage pulse (e.g., the voltage level between the pulses) during a third period (T(off)).

The enable signal (wl**1**_en) is low during the first period (T(hard-on), transitions to high during the second period (T(weak-on) and transitions back low during the third period (T(off)). The deselect line (wl**1**desel_en) is high during the first period (T(hard-on)) and is low during the second period (T(weak-on)) and the third period (T(off)). The RST signal (rst**1**) transitions to high after the series of pulses (e.g., when the word line (WL**1**) returns to 0V). The high-bias enable input (hbias_en) is high during the second period (T(weak-on). The drain select line (SGD) transitions to a high state during the second period (T(weak-on)) and transitions back to a low state during the third period (T(off)). The drain select line (SGD) transitions to a high state after the deselect line (wl**1**desel_en) goes low, and the drain select line (SGD) transitions to a low state before the deselect line (wl**1**desel_en) goes high. Discharge may occur when the word line (WL**1**) is 2V or 2.5V and the gate signal (SGD) is high.

It is also noted that in the illustrated embodiment the ratio of the duration of the second time period to the duration of the third time period (T(weak-on)/T(off)) may be greater than 1. In other words, the duration of the second time period (T(weak-on)) may be greater than the duration of the third time period (T(off)). Further, the ratio of the duration of the first time period to the duration of the third time period (T(hard-on)/T(off)) may be greater than 1 or less than 1. In other words, the duration of the first time period (T(hard-on)) may be greater than or less than the duration of the third time period (T(off)).

FIG. **10** is a timing diagram that illustrates another embodiment of a method of operating the memory device **30**, in accordance with the present techniques. The method includes providing a constant voltage to the selected cell, and pulsing other signals coupled to the column **70**. Specifically, the embodiment includes pulsing the source-line (SL) and the drain-select line (SGD), while the voltage level of the signals to the cells **72** (WL**0**, WL**1**, WL**2**, and WL**3**) and the signal to the source select gate transistor **78** (SGS) remain at a constant voltage level. During the discharging period (Tbl) the source line (SL) is pulsed between a low state and a high state and the drain-select line (SGD) is pulsed between a high state when the source line (SL) is low and a low state when the source line (SL) is high. For example, in the illustrated embodiment, the source line (SL) alternates between a low voltage level of about 0V and a high voltage level of about 2V, and the source-line (SL) alternates between a low voltage level of 0V and a high voltage level of 5V. The source-line (SL) and the drain select line (SGD) are pulsed between high and low states during the period when the word lines (WL**0**, WL**1**, WL**2**, and WL**3**) and the source select line (SGS) are driven to a high state. For example, the word line of the selected cell (WL**1**) is driven to 1.0V during a read operation or 1.5V during a verify operation, and the remaining word lines to the unselected cells (WL**0**, WL**2**, and WL**3**) and to the source select line (SGS) are driven to 5V. During the period when the source line (SL) is driven high (e.g., to 2V), the cells connected to the word line of the selected cell (WL**1**) are accumulated to detrap electrons that are trapped in cell. It is again noted, that the discharging period (Tbl) is extended for a period such that the word line signal of the selected cell (WL**1**) is in the high state for a total time that is approximately equal to the time period that the word line (WL**1**) is held high in an embodiment where the word line (WL**1**) is not being pulsed (e.g., the time period Tbl of FIG. **6**). In one embodiment, when the source line (SL) and the drain select line (SGD) capacitance are 1 nanofarad (nF) and 10 pF, respectively, a read time is 50 us, the number of rise and falls (pulses) for the selected word line is 10, the current efficiency of a 5V generation charge pump circuit is 20%, the average current is 500 uA ((1 nF×2V+(10 pF×5V)/2)/(50 us×10)=2 uA, approximately 10% of the total read current.

Although the previous embodiments are discussed in the context of a NAND flash memory device **30**, the systems and methods can be applied to other types of memory where stored data is read by cell current as well. FIGS. **11**A-**11**E include schematic diagrams of other memory devices that may employ techniques similar to those discussed above. For example, FIG. **11**A illustrates a NOR flash memory cell **130**. The NOR flash memory cell **130** includes a transistor **131** coupled between a bit line (BL) and a source line (SL) of a memory array, and a control gate of the transistor **131** coupled to a word line (WL) of the memory array. FIG. **11**B illustrates a static random access memory (SRAM) cell **132**. The SRAM cell **132** includes two cross-coupled inverters **134** and **136** and two access transistors **138** and **140**. A control gate of each of the transistors **138** and **140** is coupled to a word line (WL) of a memory array. Further, the source and drain nodes of the access transistors **138** and **140** are coupled between the cross-coupled inverters **134** and **136** and complementary bit lines BL and /BL of the memory array. FIG. **11**C illustrates a floating body cell **142**. The floating body cell **142** includes a transistor **144** coupled between a bit line (BL) and a source line (SL) of a memory array, and a control gate of the transistor **144** coupled to the word line (WL) of the memory array. FIG. **11**D illustrates a phase change memory cell **146**. The phase change memory cell **146** includes a transistor **148** coupled between a bit line (BL) and a source line (SL) of a memory array, and a phase change material **150** disposed between a drain node of the transistor **148** and the bit line (BL) of the memory array. Further, a control gate of the transistor **148** is coupled to a word line (WL) of the memory array. FIG. **11**E illustrates a magnetoresistive random access memory (MRAM) cell **152**. The MRAM cell **152** includes a transistor **154** coupled between a bit line (BL) and a source line (SL) of a memory array, and a magnetic material **156** disposed between a drain node of the transistor **154** and the bit line (BL) of the memory array. Further, a control gate of the transistor **154** is coupled to a word line (WL) of the memory array.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and will be described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

1. A memory device comprising:

a memory array including a plurality of access lines and data lines; and

a circuit coupled to the plurality of access lines, and configured to sequentially bias at least a selected one of the plurality of access lines between a first voltage level and a second voltage level during a single read operation, wherein the first voltage level is substantially greater than the second voltage level, and the second voltage level is a read voltage level.

2. The memory device of claim **1**, wherein the circuit is configured to provide a first enable signal to a first transistor to enable the first voltage level to be provided to the selected one of the plurality of access lines.

3. The memory device of claim **2**, wherein the circuit is configured to provide a second enable signal to a second transistor to enable the second voltage level to be provided to the selected one of the plurality of access lines.

4. The memory device of claim **1**, wherein the circuit is configured to provide an enable signal to a transistor to enable the second voltage level to be provided to the selected one of the plurality of access lines.

5. The memory device of claim **1**, wherein the second voltage level is greater than 0 volts and less than 2.0 volts, and the first voltage level is at least approximately 1 volt greater than the read voltage level.

6. The memory device of claim **1**, wherein the circuit is configured to provide a third voltage level to the selected one of the plurality of access lines.

7. The memory device of claim **6**, wherein the third voltage level is approximately 0 volts.

8. A system comprising:

a memory device comprising:

a memory array including a plurality of access lines and data lines; and

a circuit coupled to the plurality of access lines, and configured to provide a first voltage level and a second voltage level to a selected one of the plurality of access lines during a single read or verify operation, wherein the first voltage level is substantially greater than the second voltage level, and the second voltage level is a read voltage level or a verify voltage level.

9. The system of claim **8**, wherein the selected one of the plurality of access lines comprises an access line coupled to a control gate of one of the plurality of memory cells.

10. The system of claim **8**, wherein the circuit comprises a voltage input configured to provide the second voltage level to the selected one of the plurality of access lines.

11. The system of claim **8**, wherein the second voltage level is between 0.5 and 1.5 volts during a read operation, and the second voltage level is between 1.0 and 2.0 volts during a verify operation.

12. The system of claim **8**, wherein the circuit comprises a plurality of transistors configured to enable the first voltage level and the second voltage level.

13. A flash memory device, comprising:

a memory cell comprising a gate, wherein the flash memory device is configured to apply a trap voltage level to the gate that is above a read voltage level prior to applying the read voltage level to the gate during a read operation.

14. The flash memory device of claim **13**, wherein the trap voltage level is configured to fill a trap site with electrons.

15. The flash memory device of claim **13**, wherein the trap voltage level is at least approximately 1 volt greater than the read voltage level.

16. The flash memory device of claim **13**, wherein the flash memory is configured to apply a low voltage level to the gate after the read voltage level, or between application of the trap voltage level and the read voltage level.

17. A flash memory device configured to apply a trap voltage level to a gate of a memory cell that is above a program verify voltage level prior to applying the program verify voltage level to the gate of the memory cell during a program verify operation.

18. The flash memory device of claim **17**, wherein the trap voltage level is configured to fill a trap site with electrons.

19. The flash memory device of claim **17**, wherein the trap voltage level is at least approximately 1 volt greater than the verify voltage level.

20. The flash memory device of claim **17**, wherein the flash memory is configured to apply a low voltage level to the gate after the verify voltage level, or between application of the trap voltage level and the verify voltage level.

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