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[54]   **VOTING SYSTEM**

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[57]   **ABSTRACT**

A voting system for totaling aye and nay votes and abstentions from a plurality of voting stations. Each station includes an aye and a nay vote switch for casting aye and nay votes respectively. Each vote switch is coupled to a register for storing a vote cast by the switch coupled thereto. Aye and nay multiplexers are respectively coupled to the register coupled to the aye and nay vote switches. The multiplexer sequentially and cyclically passes the contents, vote-cast and vote-not-cast signals, of the registers coupled thereto to an aye vote recording circuit, to a nay vote recording circuit, and to an abstention vote recording circuit. The aye and nay multiplexers operate in synchronism so that an abstaining voting station will simultaneously pass an aye vote-not-cast signal and a nay vote-not-cast signal through the aye and nay multiplexers. The abstention vote recording section treats such simultaneous receipt of aye and nay vote-not-cast signals as an abstention.
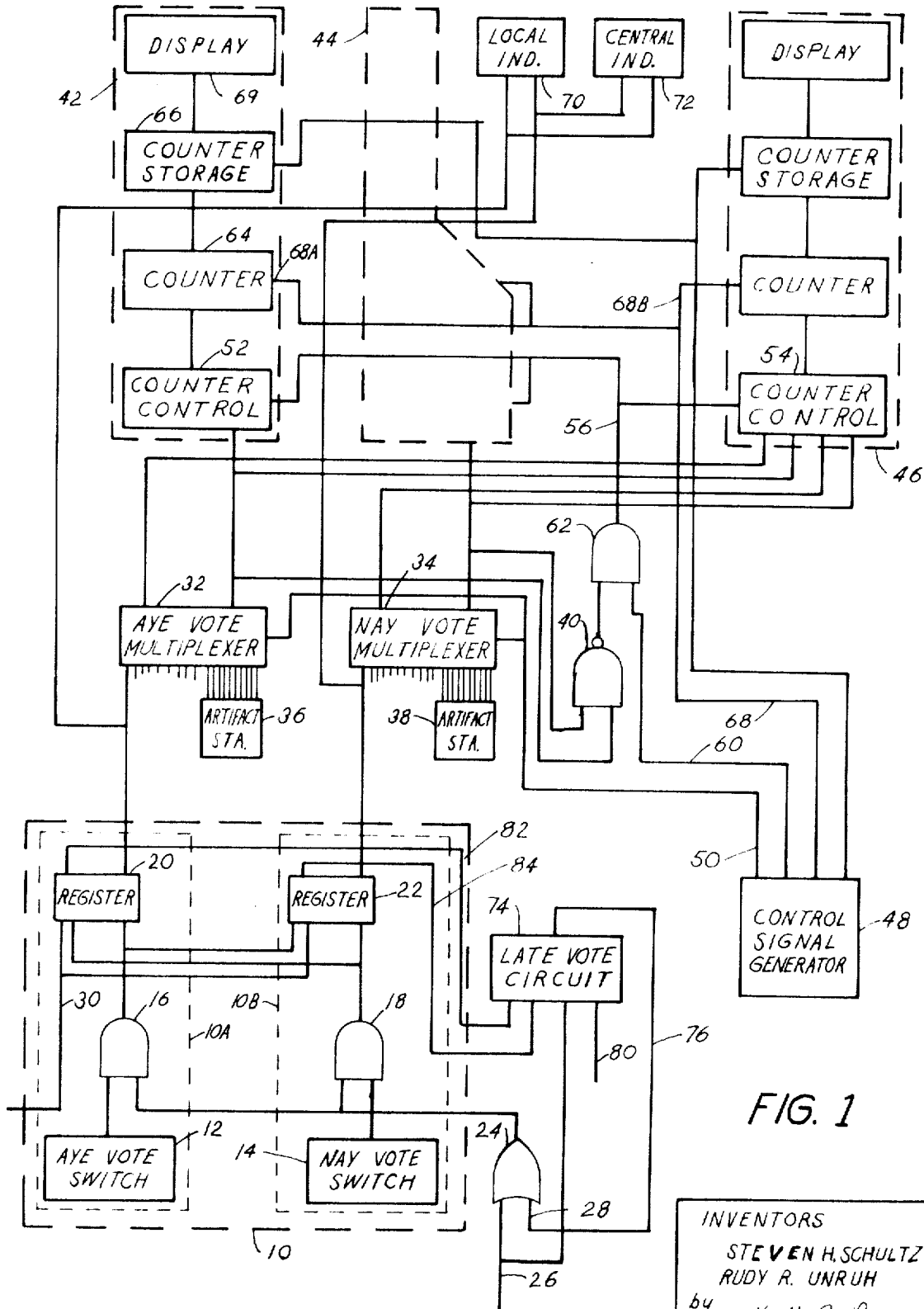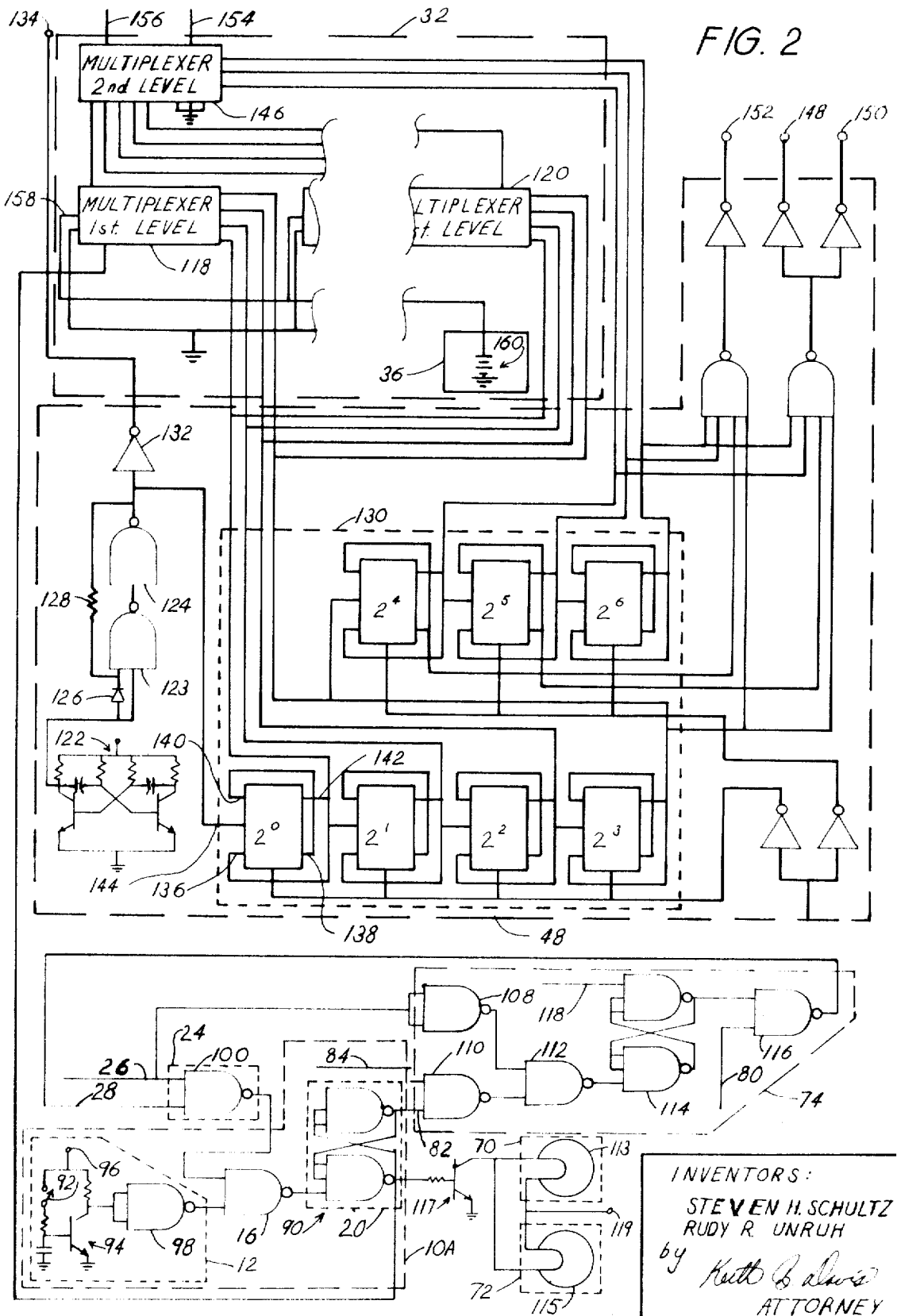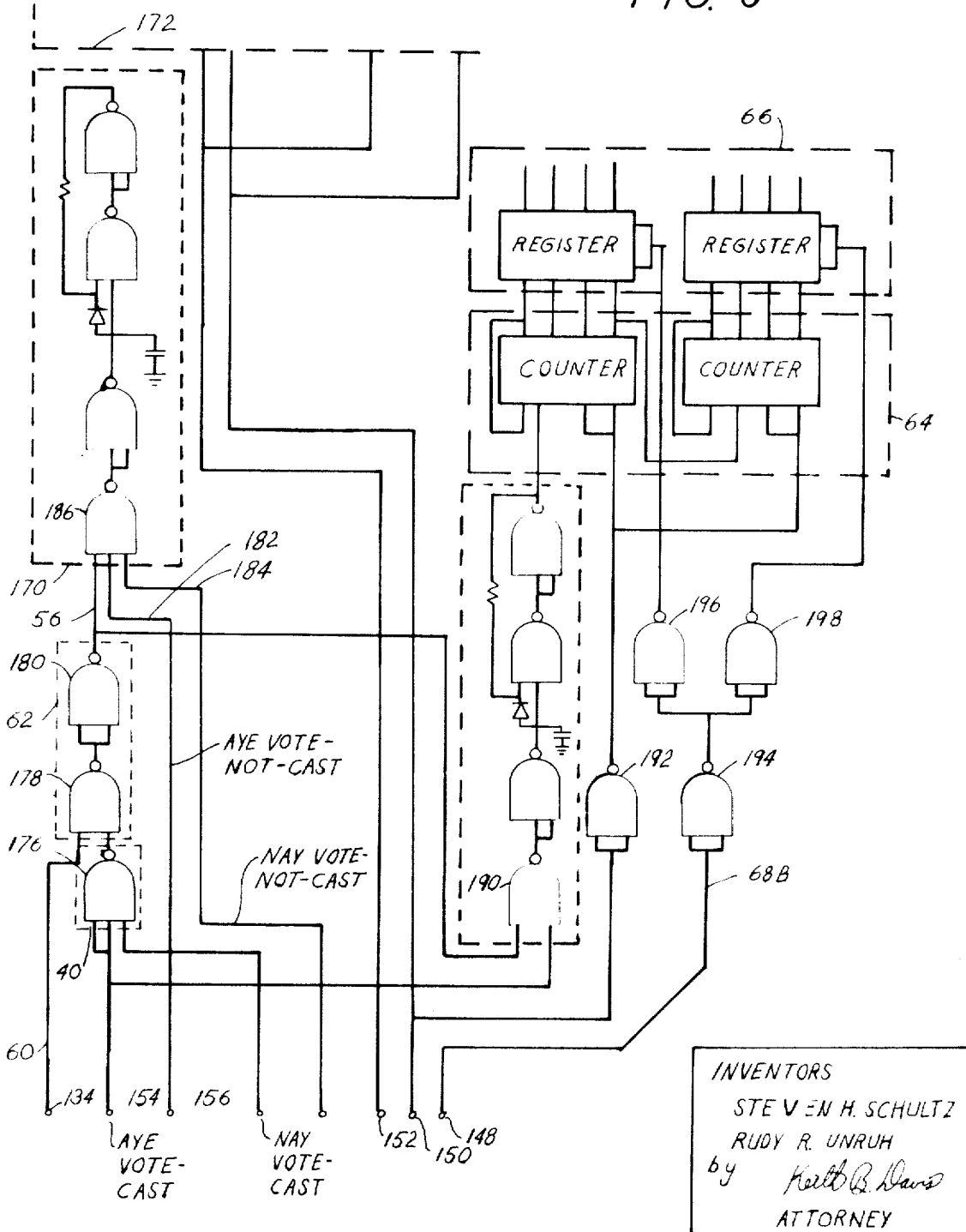
15 Claims, 3 Drawing Figures
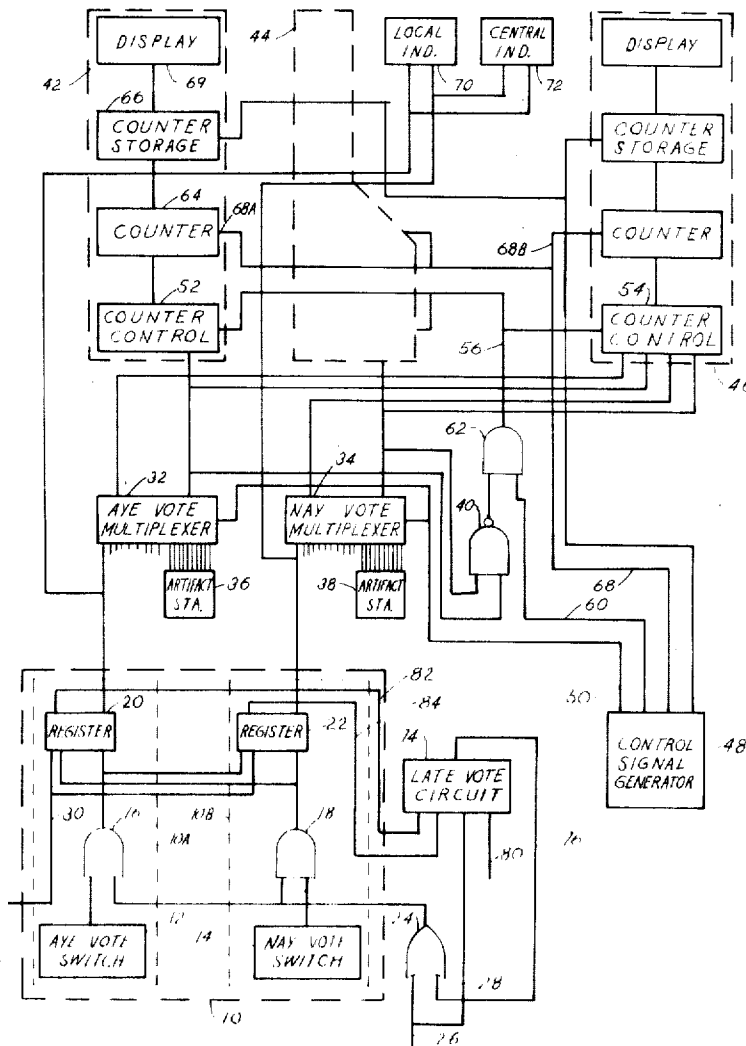
FIG. 1

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VOTING SYSTEM

BACKGROUND AND FIELD OF INVENTION

This invention relates to voting systems in general and in particular to general assembly voting systems such as those of the various governmental legislative bodies. Typically these latter types of systems consist of a voting station for each legislator, each voting station having an aye and a nay vote switch for voting in favor of or against each issue. Voting systems in general usually include a combination of switches for voting for or against a proposal. For example, voting systems used in general elections frequently have such switches for voting on referendums, bond issues and the like.

Frequently, the number of voting stations of a voting system vary from time to time so that it is desirable to be able to conveniently increase or decrease the number of stations. This is true even of legislative voting systems. It is not uncommon for the number of stations of a legislative system to change following a census and reapportionment may also result in a change in the number of members of a legislative body and hence a change in the number of voting stations.

Briefly, the present invention provides a voting system in which the number of voting stations can be easily increased or decreased and which provides for rapid and accurate totaling of aye and nay votes and of the number of abstaining voting stations as well.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a basic logic diagram of a voting system according to the present invention;

FIG. 2 is a partial schematic and partial detailed logic diagram of a portion of the voting system of FIG. 1; and

FIG. 3 is a detailed logic diagram of a portion of the voting system of FIG. 1.

The logic symbols employed in the figures of the drawings, and the definitions used in the descriptions thereof, are standard graphic symbols and definitions for logic diagrams as set forth in MIL-STD-806B dated Feb. 26, 1962, copies of which may be obtained from the Department of Defense, Washington 25, D.C. A definition of the standards specifically applicable to FIG. 2 is that of a "basic" logic diagram which means a logic diagram im which the logic symbols depict logic relationships as simply and understandably as possible without necessarily corresponding literally to physical implementations. Specific examples of depiction of logic relationships are the OR gate 24 is shown in FIGS. 2 and 3 to take the form of a NAND 100.

DETAILED DESCRIPTION

Referring now to FIG. 1, there is shown a preferred embodiment of the invention which includes a voting station 10. In FIG. 1 only one voting station 10 is shown though it is to be understood that the invention contemplates a plurality of such voting stations, the exact number not being critical to the invention. Voting station 10 includes an aye section 10A and nay section 10B and comprises a pair of voting switches, aye vote switches 12 and nay vote switch 14 and a pair of dual input AND gates 16 and 18 which respectively couple switches 12 and 14 to the set inputs of a pair of flip-flop registers 20 and 22. The remaining input of both AND 16 and AND 18 is the output of a two input OR gate 24. Inputs 26 and 28 of OR 24 carry signals respectively corresponding to a normal voting period and a

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late voting period. With a signal present on either lead, ANDs 16 and 18 are pre-conditioned to pass a vote-cast signal initiated by actuation of their associated vote switches to set the corresponding aye or nay register as the case may be and store a vote. When set, registers 20 and 22 provide signals representative of a vote-cast on their outputs; conversely, when cleared, they provided output signals representative of a vote-not-cast. The registers are shown to have a clear input coupled to receive the set input of the other register to insure that at any given time only one of the registers provides a vote-cast output signal. Each register also is coupled to receive a clear signal from register-clear lead 30. Coupled to the vote-case outputs of the aye and nay registers are an aye vote multiplexer 32 and a nay vote multiplexer 34. As shown both multiplexers have a plurality of data inputs some of which are coupled to the registers of other voting stations (not shown) and others of which are unused. As will be subsequently explained in greater detail, the unused data inputs are connected to "artifact" stations, 36 and 38, which are of a very simple and straight forward construction and which appear when sensed by the multiplexer as though they are always presenting a vote-cast signal on the unused data inputs. The system ignores such artifact votes by means of a double-vote-inhibit circuit 40, shown as a NAND gate in FIG. 1, which operates in a manner which will be set forth following a brief consideration of the system vote recording circuits which consist of aye, nay, and abstention vote recording circuits 42, 44, and 46, respectively, and the system control signal generator 48. Among other things, control signal generator (CSG) 48 provides a timing signal to the aye and nay multiplexers via lead 50. The multiplexers are responsive to the timing signal to sequentially and cyclically enable each of their data inputs, including the unused inputs from artifact stations 36 and 38, to pass aye and nay vote-case signals to the aye vote recording circuit 42, nay vote recording circuit 44, to pass both the aye and nay vote-cast signals to the double vote inhibit means NAND gate 40 and to pass both vote-not-cast signals to abstention counter 46. Recording of a vote-cast signal as a vote is under control of aye counter control 52 and a like nay counter control (not shown) for aye and nay vote-cast signals respectively. Abstention votes are recorded under control of counter control 54. The counter controls are in turn subject to a count-control signal on lead 56, which count-control signal originates at CSG 48 as a timing wavetrain. The wavetrain is carried via a lead 60 to an AND gate 62; passage of the wavetrain through, and conversion into a count-control signal by, AND 62 is subject to an active state of double vote inhibit means 40, which as previously stated is illustrated in FIG. 1 as a NAND gate having the aye and nay multiplexer vote-cast outputs as its two inputs. Accordingly, double vote inhibit means 40 is active to enable AND 62 and permit conversion of a wavetrain into a count-control signal whenever neither or either of the aye and nay multiplexers pass a vote-cast signal but is inactive to disable AND 62, and block conversion of a wavetrain into a count-control signal, whenever both multiplexers pass a vote-cast signal to prevent counting of erroneous double votes, and as shall be subsequently shown, and of no lesser importance, to facilitate adding voting stations to or subtracting them from the system. Actual recording of a vote, e.g. recording of an aye vote, results when the counter

control 52 passes a vote-cast signal to counter 64, the count of which is periodically transferred or "strobed" into a counter storage circuit 66 by means of a strobe control signal on leads 68 and 68A from CSG 48. Also included in each vote recording circuit is a display coupled to each counter storage circuit. An example of such a display is the aye vote display 69. These displays conveniently can be readout devices such as conventional digital readouts in which numerals are formed by illumination of selected lamps in an array, each lamp of which is coupled through a lamp driver, and/or decoder driver circuit to the counter storage circuit. The illustrated system of FIG. 1 also includes a local vote indicator 70, and a central vote indicator 72. Such indicators may each conveniently take the form of a pair of lamps, one lamp corresponding to an aye vote, the other to a nay vote, with the local indicator being mounted proximate the voting station to provide vote confirmation for the voter and the central indicator and all like indicators being located at a central location to provide an overall indication of how all voting stations have voted on an issue. The lamps literally provide vote "confirmation," as they indicate how the system has registered a vote.

For the illustrated preferred embodiment, the system also includes a late vote circuit 74 associated with each voting station. If a voting station did not cast a vote during a normal voting period, its associated late vote circuit 74 allows the station to cast a vote during a late voting period. The late vote circuit 74 couples, via lead 28, and enabling signal to OR 24, which in turn conditions ANDs 16 and 18 for activation whenever normal vote closed and late vote enable control signals are present on leads 26 and 80 respectively, provided vote-not-cast signals from aye and nay registers 20 and 22 are also present on leads 82 and 84.

Having thus described the general structure of and principles underlying the different features of the present invention by means of the illustrative embodiment of FIG. 1, an embodiment of the invention specifically intended for use as the voting system of a general assembly, such as a legislative body, shall now be described in detail with the aid of FIGS. 2 and 3. In the illustrations of FIGS. 2 and 3, positive NAND logic is used exclusively. Consequently, the figures differ slightly from the basic logid diagrams of FIG. 1; in particular, the OR gate 24 is effected a NAND gate.

FIG. 2 is a partial schematic and partial detailed logic diagram of a voting station aye section 10A, a late vote circuit 74, control signal generator 48, and aye vote multiplexer 32.

Aye section 10A is shown to include a conventional NAND flip-flop (FF) 90 as the aye vote register 20 and a normally open switch 92 and normally non-conducting NPN transistor 94 as the aye vote switch 12. When closed, switch 92 couples positive potential (not shown) from terminal 96 to the base of transistor 94, causing it to conduct whereupon the transistor collector goes from a high to a low potential, about plus 5 and zero volts, respectively. An inverter is formed from NAND 98 and couples the inverted transistor output to NAND 16 which is controlled by its other input which is coupled to the output of OR gate 24. OR 24 is a NAND gate 100 the inputs of which are the normal voting period input 26 and the output of late vote circuit 74. Normally, i.e. when it is neither a normal nor a late voting period, both inputs are high and NAND

100 is active to place a low signal to NAND 16 and thereby prevent it from being activated upon activation of switch 92 and to thus prevent setting of FF 90. During either a normal or a late voting period, a low signal is provided to the NAND 100, by normal voting period input lead 26 in the one case and the input lead 28 from late vote circuit 74 in the other, to, in both cases, inactivate NAND 100 and couple a high signal to NAND 16 permitting it to become activated and set FF 90 upon casting of a vote by actuation of switch 92. The late vote circuit 74 accomplishes this result when a low signal is placed on a late vote lead 80, provided a vote had not been cast by the station during the preceding normal voting period. The late vote circuit consists of NANDS 108, 110 and 112, FF 114, and NAND 116. The FF 114 registers a vote cast during a normal voting period to prevent a repeat vote being cast from the station during a late voting period. When a vote is cast, one of the inputs 82 or 84 of NAND 110 goes low to couple a high signal to NAND 112 the other input of which is already high by virtue of NAND 108 which inverts the low normal voting period signal. With both inputs of NAND 112 high, a low input is coupled to the set input of FF 114 to set the FF. With FF 114 set, NAND 116 receives a low input and is inactivated. Resetting of the FF is accomplished via a low signal on clear input lead 118 but, resetting is not initiated until after a late voting period, should there be one. If a late voting period is initiated and a station has cast a vote, NAND 116 is held inactive by the set FF 114 to block passage of the late vote signal to NAND 100 and thus prevents voting during the late voting period; conversely, if a vote has not been cast, FF 114 is cleared and NAND 116 will be activated by the re-open voting signal to apply a low signal to NAND 100 and thereby condition aye NAND 16 (and nay NAND 18 which is not shown) to pass a vote-cast signal to FF 90. Storing of the vote in FF 90 does not set FF 114 to prevent changing of the vote, however, as NAND 112 is disabled by means of a normal voting closed (high) signal which is low (after inversion by NAND 108) when applied to NAND 112.

Also shown in FIG. 2 are the local and main indicators 70 and 72 which are shown to be simply a pair of lamps 113 and 115 coupled in parallel to the collector of an NPN transistor 117 the base of which is coupled to the set output of FF 90. When the FF 90 is set by a vote-cast signal, the resulting high output on its set lead forward biases transistor 117 to draw current through lamps 113 and 115 from a source of positive potential (not shown) connected to terminal 119. It can thus be seen that transistor 117 "interprets" the vote stored in voting section 10A.

Turning now to consideration of the aye multiplexer 32, it comprises two levels of integrated circuit multiplexers, the first level consisting of five discrete multiplexers each having 16 data inputs and the second level consists of a signal eight data input multiplexer, five data inputs of which are coupled to the first level multiplexer outputs and the other three of which are grounded. It is assumed for purposes of this disclosure that only 70 of the total of 80 first level multiplexer inputs are connected to voting stations, the remaining 10 being unused inputs coupled to what shall be referred to herein as "artifact" stations. In FIG. 2, only two of the first level multiplexers are shown to any appreciable extent, a first stage 118 having its first data input

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coupled to the aye voting register 20 and its remaining data inputs connected to aye registers of other voting stations (not shown). For the assumed system of 70 voting stations, data inputs of the second, third, and fourth stages of the first level multiplexers are also each connected to a voting station. For the sake of clarity, they have been omitted. The fifth stage of the first level is identified by reference numeral 120 and is partially shown in such a manner to indicate that its first 10 data inputs are coupled to voting stations whereas its last six inputs are coupled to artifact stations.

Turning for a moment to consideration of CSG 48, it is shown to comprise a clock pulse generator in the form of a conventional free running multivibrator 122. For the assumed embodiment, multivibrator 122 runs at a frequency of about 1000 hz. and has its output coupled through a signal shaping circuit comprising NANDS 123 and 124, diode 126 and resistor 128 to a timing counter 130 and an inverter 132 the output of which is a notclock ($\overline{\text{Clock}}$) signal which is provided to terminal 134 and is used for controlling the vote counters in a manner which shall be explained in greater detail hereinafter. The timing counter 130 is a seven stage binary counter (128) count), the stages of which therefore correspond to binary digits $2°-2°$, inclusive, and which in the illustrated embodiment are cascaded toggle flip-flops, which flip-flops are formed by crosscoupling the "J" and "K" inputs and outputs of a conventionl "JK" FF. In the Figure, the digit position of each of the seven stages is identified by a binary digit placed within the rectangular FF symbol. Cross-coupling of the inputs and outputs is the same for all stages; to illustrate the cross-coupling, the 2° stage inputs and outputs have been assigned reference numbers. The "K" input has been designated 136, the "clear output" 138, the "J" input 140, the "set output" 142, and the "toggle" input 144. Resetting of each stage is accomplished by a reset signal applied to the "reset" lead, such as reset lead 145 of stage 2^4, which reset leads are illustrated as coming into the bottom of the rectangular FF symbols. As indicated, the set outputs of stages $2°-2^3$ control sequencing of the first level multiplexer data inputs and the set outputs of stages 2^4, 2^5 and 2^6 control second level multiplexer 146. Various set and clear outputs of this latter group of stages are used to generate the CSG strobe and reset control signals, the former of which appears at both of terminals 148 and 150 and is produced during counts 80–95 of the timing counter and the latter of which is produced during the last 16 counts of each timing counter cycle, counts 112–127.

The first level multiplexers are each responsive to timing counter signals to each sequentially enable their 16 data inputs, for purposes of this discussion, arbitrarily defined from left to right in the figure as data inputs one through 16. The first level multiplexers are synchronously enabled by the timing counter signals and thus there are five aye registers whose outputs are simultaneously sampled by the first level multiplexers. However, at any given time only one data input of the second level multiplexer 146 is enabled and thus only one out of the five aye register outputs are passed through both the first and second level multiplexers. Vote-cast signals are passed via leads 154 and vote-not-cast signals via lead 156. At this pont it should be noted that an identical multiplexer is provided for the voting station nay registers. Because of identical connections with timing counter 130, the aye and nay multiplexers

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operate in synchronism which as previously stated makes it possible to avoid counting double votes and to conveniently provide unused data inputs, or artifact stations 36, which provide flexibility in the number of stations of the system.

For the particular illustrated embodiment, the multiplexers employed makes it particularly convenient to effect artifact stations. The multiplexers are Texas Instrument (TM) types SN 74150 and SN 74151. Both of these types are provided with an input pin, such as input 158 of the first level first stage multiplexer, intended for coupling to a source of positive potential (schematically illustrated as source of positive potential 160). Internally the multiplexers couple the positive potential such that if an input is left unconnected, i.e., an unused input, when the multiplexer enables that input in the multiplexing sequence the multiplexer provides a vote-cast output signal. Accordingly, the positive potential applied to input 158 effectively provides an artifact vote-cast signal to each unused multiplexer input. By simply defining a vote-cast signal (at the multiplexer input) as a low signal, leaving each unused input unconnected, and synchronizing multiplexing of corresponding aye and nay unused inputs to simultaneously enable corresponding unused aye and nay inputs, only an exclusive OR gate is required to prevent both of simultaneously occurring artifact vote-cast signals from being counted and thus provide a convenient and uncomplicated system in which the number of voting stations can be readily increased or decreased. Should one wish to employ a multiplexer not having the aforedescribed internal connections to an input pin such as pin 158, the artifact stations 36 could easily be formed by connecting each unused data input through a current limiting resistor to the source of potential.

Taking up consideration of FIG. 3, a double vote inhibit means 40, AND 62, abstention vote counter control 170, and an aye vote counter control 52, counter 64, and counter storage 66 are shown in detailed logic form.

The double vote inhibit means 40 is accomplished by means of NAND 40 which by definition is active whenever neither or either one but not both of its inputs are carrying a vote-cast signal, i.e., high at this point in the logic. When active, NAND 40 provides an enabling signal to AND circuit 62 and conversely, when inactive, provides a disabling signal to AND 62, the latter state occurring, for example, when an artifact station is being sensed by the multiplexer. The physical implementation of AND 62 consists of two series coupled NANDS 178 and 180, the former of which performs the enablement/disablement function just discussed, and the latter of which also functions as an inverter. The AND 62 output is thus the $\overline{\text{Clock}}$ CSG lead 60 output. This $\overline{\text{Clock}}$ signal is applied via lead 56 to abstention vote counter control 170 the two data inputs of which, 182 and 184, are respectively derived from the aye and nay vote multiplexer vote-not-cast outputs. Whenever neither vote storage register of a voting station is storing a vote, both inputs 182 and 184 carry a high signal which, together with the $\overline{\text{Clock}}$ signal, enable an input gate NAND 186 of counter control 170 to ultimately store a vote in counter 172. The output of NAND 186 is coupled to counter 172 by a signal shaping and filtering circuit 188 which consists of the three illustrated NANDS and their associated diode, resistor, and capacitor. The abstention counter and counter

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storage are not shown as they are identical to their aye vote counterparts described hereinafter.

The aye vote counter control is the same as the abstention control 170 with the obvious exception that its input gate 190 has only a signal data input, the aye vote-cast-input. Counter 64 is formed by series coupling a pair of Texas Instrument SN 7490 integrated circuit counters. The counter outputs are coupled to counter storage 66, for the preferred embodiment illustrated, a pair of Texas Instrument SN 7475 IC registers. Transfer of data from the counters to the registers is effected by a strobe signal from CSG 48 on lead 68B. A strobe signal enables the counter storage inputs to accept data from the counter. Also associated with the strobe and reset inputs of the aye counter 64 and counter storage 66 are NANDs 192, 194, and 196 and 198. These NANDs are included with the aye vote recording circuit to provide additional current sinking capacity since the aye strobe and reset inputs are also applied to the nay vote counter and counter storage.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention.

What is claimed is:

1. A voting system for totaling aye, nay and abstention votes from a plurality of voting stations, comprising, in combination:

a plurality of voting stations, each station including an aye vote switch, a nay vote switch, and an aye and a nay vote register, which registers each have a set and a clear input and have their respective set inputs coupled to the aye and nay vote switches, each of which registers has at least one output and provides an output signal representative of a vote-not-cast in response to an input signal applied to its clear input but which provides an output signal representative of a vote-cast in response to an input signal applied to its set input by actuation of its associated vote switch, and which registers each have their clear input coupled to receive the set input of the other register to insure that at any given time only one of the registers provides a vote-cast output signal;

an aye vote counter and a nay vote counter, each of which counters are responsive to a vote-cast signal to increment its count;

an abstention vote counter responsive to simultaneous receipt of an aye vote-not-cast and a nay vote-not-cast signal to increment its count;

an aye vote multiplexer having a plurlaity of data inputs at least equal in number to the number of voting stations, a vote-cast output coupled to the aye vote counter, and a vote-not-cast output coupled to the abstention vote counter, each aye register being coupled to provide its output signals to an aye vote multiplexer data input, and which multiplexer is responsive to a timing signal to sequentially and cyclically enable its data inputs to pass each aye register vote-cast output signal to the aye vote counter and vote-not-cast signal to the abstention vote counter;

a nay vote multiplexer having a plurality of data inputs at least equal in number to the number of voting stations, a vote-cast output coupled to the nay vote counter, and a vote-not-cast output coupled to

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the abstention vote counter, each nay register being coupled to provide its output signals to a nay vote multiplexer data input, and which multiplexer is responsive to a timing signal to sequentially and cyclically enable its data inputs to pass each nay register vote-cast output signal to the nay vote counter and vote-not-cast output signal to the abstention vote counter; and

a control signal generator for generating the timing signal and for providing the timing signal to each of the aye and nay multiplexers to operate the multiplexers in synchronism whereby during each cycle for each voting station vote-not-cast output signals of a voting station aye and nay registers are simultaneously provided to the abstention vote counter or a vote-cast signal from one of the registers is provided to the appropriate aye or nay counter to provide composite counts of all voting station aye, nay and abstention votes.

2. A voting system according to claim 1 further comprising:

a coincidence gate coupled between each multiplexer and counter, each of which gates when enabled applies a register output signal passed by a multiplexer to a counter but prevents such application when disabled; and

double vote inhibit means coupled to receive both the aye and nay vote-cast output signals passed by the aye and nay vote multiplexers and is activated in response to receipt of one or the other or neither of said vote-cast signals to enable the logic gate, but is deactivated by simultaneous receipt of both of said vote-cast signals to disable the gate.

3. A voting system according to claim 2 wherein the aye and nay vote multiplexers have an equal number of data inputs, wherein there are fewer voting stations than the number of multiplexer data inputs, wherein the inputs not coupled to voting stations of the aye and nay multiplexers are unused inputs and the aye and nay unused inputs correspond to each other in the multiplexing sequence, and in which system during a cycle each of the multiplexer data inputs are enabled, and further comprising: means for effectively applying an artifact vote-cast signal to each unused multiplexer input to effectively provide both an aye and a nay vote-cast signal when each of the unused multiplexer inputs are enabled and thereby disable the logic gates and prevent counting of such artifact vote-cast signals.

4. A voting system according to claim 3 wherein relatively high and relatively low signals are respectively representative of vote-cast and vote-not-cast signals, wherein each multiplexer is provided with an artifact vote input pin for receiving a relatively high potential and which multiplexer includes internal connections which couple a high potential received at said artifact-vote input to provide a vote-cast output signal from the multiplexer when a multiplexer unused input is enabled during the multiplexing sequence, and wherein the means for applying a vote-cast signal is a source of relatively high potential connected to said multiplexer artifact vote input pin.

5. A voting system according to claim 2 wherein each multiplexer has n control inputs, where n is an integer number, and has 2^n data inputs, each of which data inputs is enabled by a unique set of binary signals received by the control signal inputs, and wherein the control generator has n outputs coupled to the n

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multiplexer inputs and cyclically provides to the multiplexer via the outputs a series of binary signal sets, each set of which represents one pulse of the timing wavetrain, each pulse corresponding to a count of the multiplexing sequence and consisting of equal length positive and negative going phases, and which sets comprise all possible combinations of n binary signals to enable each multiplexer data input once during each multiplexing sequence.

6. A voting system according to claim 5 wherein each counter continuously provides output signals representative of a count stored therein on n data outputs and is responsive to a re-set signal to clear itself to zero, wherein at least two of said multiplexer data inputs are unused inputs, and further comprising:

a count storage register for each counter, which storage register has its inputs coupled to the counter outputs and is responsive to a strobe signal to enable its inputs to receive and store the counter output signals;

strobe signal generating means for producing and coupling to the count storage registers a strobe signal in response to a binary signal set corresponding to an unused multiplexer data input; and

re-set signal generating means for producing and coupling to the counters a re-set signal in response to a binary signal set following said set for which a strobe signal is produced and corresponding to an unused input.

7. A voting system according to claim 2 further comprising for each voting station a duel input AND gate coupled between said logic gates and said double vote inhibit means, which dual input AND has one input coupled to receive a timing wavetrain, and has its other input coupled to receive the output of the double vote inhibit means, the output of which double vote inhibit means when activated satisfies one of the conditions for activating said AND to pass said wavetrain through said AND as said timing signal.

8. A voting system according to claim 1 which provides for re-opening voting following expiration of a voting period to provide a late voting period, comprising:

means for generating a signal representative of and the duration of which corresponds to a normal voting period;

means for generating a re-open voting signal the duration of which corresponds to a late voting period;

a first OR gate which when active provides an output signal representative of a voting period open, which OR gate has one input coupled to receive and be activated by said signal representative of a normal voting period and another input coupled to receive and be activated by said signal representative of a late voting period;

a coincidence gate coupled between each multiplexer and each counter, each of which gates when enabled applies a register output signal passed by a multiplexer to a counter but prevents such application when disabled, and each of which gates has one input coupled to receive said signal representative of a voting period open; and

a second OR gate having said aye and nay register outputs of a voting station as its inputs and responsive to either an aye or a nay vote-cast signal to become active;

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a re-vote inhibit register for preventing during a late voting period the casting of a vote from a station from which a vote was cast during a normal voting period, which register has an input coupled to receive said second OR gate output and is responsive when said output is active to provide an inhibit re-voting signal; and

a duel input AND gate one input to which is coupled to receive said re-open voting signal and the other input of which is coupled to receive the output of said re-vote inhibit register, which AND gate is active in response to a said re-open voting signal and the absence of an inhibit re-voting signal to produce as an output signal a said signal representative of a late voting period, but which AND gate is deactivated in response to an inhibit revoting signal to prevent production of a said signal representative of a late voting period.

9. A voting system according to claim 8 for permitting a voter to change his vote as often as he wishes throughout a late voting period:

a fourth second dual input AND gate coupled between said OR gate and said revote inhibit register, one input of which second AND gate is the OR gate output and the other of which is coupled to receive the normal voting period signal, a said normal voting period signal conditioning said second AND gate to pass set output of said OR representative of a vote-cast to et said re-vote inhibit register but said fourth NAND being inactive during a late voting period as a result of the absence of a normal voting period signal to prevent setting of said re-vote inhibit register and thus permit changing of the vote cast during a late voting period.

10. A voting system according to claim 8 further comprising double vote inhibit means coupled to receive both the aye and nay vote-cast output signals passed by the aye and nay vote multiplexers and is activated in response to receipt of one or the other of a said vote-cast signals to enable the coincidence gate, but is deactivated by simultaneous receipt of both of said vote-cast signals to disable the coincidence gate.

11. A voting system according to claim 8 wherein the aye and nay vote multiplexers have an equal number of data inputs, wherein there are fewer voting stations than the number of multiplexer data inputs, wherein the inputs not coupled to voting stations of the aye and nay multiplexers are unused inputs and the aye and nay unused inputs correspond to each other in the multiplexing sequence, and in which system during a cycle each of the multiplexer data inputs are enabled, and further comprising: means for effectively applying an artifact vote-cast signal to each unused multiplexer input to effectively provide both an aye and a nay vote-cast signal when each of the unused multiplexer inputs are enabled and thereby disable the logic gates and prevent counting of such artifact vote-cast signals.

12. A voting system according to claim 11 further comprising:

double vote inhibit means coupled to receive both the aye and nay vote-cast output signals passed by the aye and nay multiplexers and is activated in response to receipt of one or the other or neither of said vote-cast signals to enable said coincidence gate but is deactivated by simultaneous receipt of both of said vote-cast signals to disable the coicidence gate.

13. A voting system according to claim 1 further comprising a coincidence gate coupled between each multiplexer and counter, each of which gates when enabled applies a register output signal passed by a multiplexer to a counter but prevents such application when disabled; and, wherein the aye and nay vote multiplexers have an equal number of data inputs, wherein there are fewer voting stations than the number of multiplexer data inputs, wherein the inputs not coupled to voting stations of the aye and nay multiplexers are unused inputs and the aye and nay unused inputs correspond to each other in the multiplexing sequence, and in which system during a cycle each of the multiplexer data inputs are enabled, and further comprising: means for effectively applying an artifact vote-cast signal to each unused multiplexer input to effectively provide both an aye and a nay vote-cast signal when each of the unused multiplexer inputs are enabled and thereby disable the logic gates and prevent counting of such artifact vote-cast signals.

14. A process of registering absention indications in a voting system wherein the status of aye and nay vote switches of each voting station are coupled to the respective inputs of aye and nay vote multiplexers and the aye vote multiplexer and nay vote multiplexer outputs are respectively coupled to the inputs of aye and nay vote counters and to aye vote-not-cast and nay vote-not-cast outputs of an abstention indication counter, the steps comprising:

1. producing an output signal from the aye vote switch and the nay vote switch of each voting system;

2. sequentially and cyclically enabling the aye and nay vote multiplexers in synchronism to simultaneously provide aye multiplexer and nay multiplexer outputs respectively representative of the status of the aye and nay vote switches of a voting

station; and

3. registering an indication of an abstention in said abstention counter in response to simultaneous receipt at said counter inputs from said multiplexer outputs of aye and nay vote-not-cast signals from aye and nay voting switches of a voting station.

15. In a voting system for accumulating aye, nay, and abstention indications, the system including a voting station having an aye vote switch and a nay vote switch and including an aye vote counter, and a nay vote counter, the improvement comprising:

an aye vote multiplexer having an input coupled to each aye vote switch, having a vote cast output coupled to the aye vote counter and having a vote-not-cast output coupled to the abstention vote counter;

a nay vote multiplexer having an input coupled to each nay vote switch, having a vote cast output coupled to the nay vote counter and having a vote-not-cast output coupled to the abstention vote counter;

an abstention vote counter having as its inputs the aye vote multiplexer and nay vote multiplexer vote-not-cast outputs, which abstention vote counter is responsive to simultaneous occurrence of aye and nay vote-not-cast signals at its inputs to increment its count; and

a control signal generator for providing a timing signal to the aye vote and nay vote multiplexers to cyclically and sequentially enable the aye vote and nay vote multiplexers in synchronism whereby aye vote-not-cast and nay vote-not-cast signals are simultaneously presented to the abstention counter for each voting station from which a vote was not cast.

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