

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
27 September 2007 (27.09.2007)

PCT

(10) International Publication Number
WO 2007/108561 A1

(51) International Patent Classification:

G02F 1/133 (2006.01) G09G 3/36 (2006.01)
G09G 3/20 (2006.01)

(21) International Application Number:

PCT/JP2007/057006

(22) International Filing Date: 23 March 2007 (23.03.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

0605744.2 23 March 2006 (23.03.2006) GB

(71) Applicant (for all designated States except US): **SHARP KABUSHIKI KAISHA** [JP/JP]; 22-22, Nagaike-cho, Abeno-ku, Osaka-shi, Osaka, 5458522 (JP).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **BROWN, Christopher J.**

(74) Agent: **HARAKENZO WORLD PATENT & TRADE-MARK**; Daiwa Minamimorimachi Building, 2-6, Tenjinbashi 2-chome Kita, Kita-ku, Osaka-shi, Osaka 5300041 (JP).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

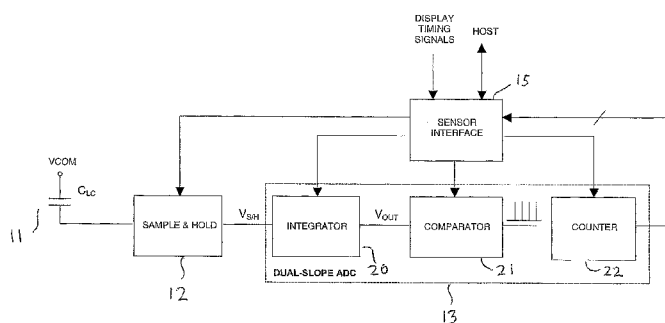
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ACTIVE MATRIX LIQUID CRYSTAL DEVICE



(57) **Abstract:** An active matrix liquid crystal device (AMLCD) comprises an active matrix substrate (1) having an active matrix area (2) and a counter electrode substrate carrying a common electrode whose voltage may vary so as to reduce liquid crystal degradation. A layer of liquid crystal material is disposed between the substrates and a temperature measuring arrangement (10) is provided on the active matrix substrate (1). This arrangement (10) comprises a temperature sensing liquid crystal capacitor (11) which in turn comprises a first electrode formed on the active matrix substrate (1) outside the image generating region of the active matrix area (2) and separated from the common electrode, which forms the second electrode of the capacitor, by the liquid crystal layer, which forms the capacitor dielectric. During operation of the active matrix, a measuring circuit (12, 13, 15) repeatedly performs a precharging step, in which the capacitor (11) is precharged to a fixed stable known voltage magnitude, and a step in which a signal representing the capacitance is formed. For example, the charge stored in the capacitor (11) may be charge-shared with a transfer capacitor to form thereacross a voltage representing the capacitance of the liquid crystal capacitor (11) and hence representing the liquid crystal temperature. The sampling is performed repeatedly, preferably in synchronism with addressing performed by the active matrix of the device. The resulting temperature measurement may be used, for example, to compensate the AMLCD for the effects of temperature variation in the liquid crystal properties.

- 1 -

DESCRIPTION

ACTIVE MATRIX LIQUID CRYSTAL DEVICE

5 TECHNICAL FIELD

The present invention relates to an active matrix liquid crystal device (AMLCD).

BACKGROUND ART

10 Display devices utilising liquid crystal (LC) have historically suffered degraded image quality through loss of contrast ratio as a result of temperature-induced changes in the optical properties of the liquid crystal material. In particular, the voltage-transmission curve of a liquid crystal
15 is related to its temperature, as shown in Figure 1 of the accompanying drawings.

A well-known solution for this degradation in image quality is to provide a temperature controlled contrast ratio compensation system comprising means for measuring the
20 temperature of the display and means for altering the voltages applied to the display based on this measurement. Such a system is disclosed for a segmented liquid crystal display in EP0012479 and for an AMLCD in US 5,926,162.

Alternatively, a temperature control system may be
25 provided comprising means for measuring the temperature of

- 2 -

the display and a heating element to maintain the display at a constant temperature. Such a system is disclosed in JP7230079. In general, systems based on the heating element method are undesirable compared to the driving voltage compensation method due to the increased power consumption associated with the heating element.

Conventional solutions for measuring the temperature rely on attaching a discrete temperature detection element to the display, for example as disclosed in US 5,029,982. Disadvantages of this method include: indirect measurement of the liquid crystal temperature (it is the temperature of the glass, or substrate on which the detection element is mounted, that is actually being measured and not the LC); extra connections to the display reducing reliability; and extra components and fabrication steps raising the cost.

In order to reduce fabrication cost, a liquid crystal temperature sensor may be fabricated with the temperature detection element integrated on the display substrate itself, as disclosed in US 6,414,740. In this disclosure, the temperature detection element is a thin-film diode or thin-film transistor that has a temperature related drain current measured by circuitry separate to the display substrate. Thus the device still has the disadvantages of performing indirect measurement of temperature and requiring extra connections to the display. An additional

- 3 -

disadvantage is that the process variation typical of elements integrated onto the display substrate limits the accuracy of such systems.

US 6,333,728 discloses an improved arrangement in which the temperature detection element is formed as a liquid crystal capacitor. The advantage of using a liquid crystal capacitor as the temperature detection element is that it has a one to one transfer function when relating the sensed temperature to the optical performance of the display pixels. The transient response of the liquid crystal capacitor to an input ramp voltage is used as a measure of temperature. In a first embodiment, a differentiator is used to detect the maximum rate of change of this transient response and a peak detection circuit is subsequently used to generate a voltage corresponding to the location of the maximum rate. This voltage is compared with a reference and a heating element is switched on/off according to the relative value. In a second embodiment, a switch arrangement is used to sample the transient response at a defined time. The voltage sampled at this defined time is a function of the capacitance of the liquid crystal element and hence of the temperature. A differential integrator compares the sampled voltage with a reference and its output is used to control the heating element.

In both above embodiments, the system supplies an

- 4 -

output voltage corresponding to the difference between a measured temperature-dependant voltage and a reference voltage. Whilst this is suitable for on/off control of a heating element, as in a control loop, disadvantageously the system does not supply a measure of absolute temperature as would be required in a preferred driving voltage compensation system. It is unlikely that this system may be modified to achieve accurate absolute temperature measurements in a practical display system for the following reasons:

- the transient response approach to measuring the capacitance of the liquid crystal element requires a ramp input voltage of constant slope. This is difficult to achieve in practice requiring a significant increase in complexity of the display driving circuits;

- it is difficult to accurately define capacitor values, including the liquid crystal capacitor element, in practice. Reference voltages and timing signals supplied to the system therefore need to be uniquely calibrated for each display.

DISCLOSURE OF INVENTION

According to the invention, there is provided an active matrix liquid crystal device comprising: an active matrix first substrate having an active matrix area; a second substrate carrying a common electrode for the active matrix; a layer of liquid crystal material between the first and second

- 5 -

substrates; a temperature sensing first capacitor comprising a first electrode outside the image generating region of the active matrix area on the first substrate separated from the common electrode, which forms a second electrode of the first capacitor, by the liquid crystal layer, which forms the first capacitor dielectric; and a capacitance measuring circuit arranged, during operation of the active matrix, repeatedly to perform the steps of precharging the first capacitor to a substantially fixed stable known first precharge voltage magnitude and forming a signal representing the capacitance of the first capacitor.

The measuring circuit may be formed on the first substrate.

It is thus possible to provide an arrangement in which more accurate measurement of the capacitance of a liquid crystal capacitor forming part of an AMLCD may be achieved. The liquid crystal capacitor has access to only one of the terminals thereof as the other terminal is formed by the device common electrode, whose potential V_{com} may be modulated in order to avoid degradation of the liquid crystal material. By making a measurement following precharging of the liquid crystal capacitor to a fixed stable known magnitude of voltage, the voltage dependency of the capacitance can be substantially eliminated; the capacitance is not generally dependent on the polarity of the precharge voltage.

- 6 -

The measuring circuit may be arranged to charge the first capacitor to the same magnitude of voltage during each precharging step. The measuring circuit may be arranged to charge the first capacitor to the same polarity of voltage during each precharging step.

The measuring circuit may be arranged to perform each precharging step at a same part of an active matrix addressing cycle. The same part may comprise the same part of a line addressing period.

The active matrix and the common electrode may be arranged periodically to invert the polarity of drive voltages applied to pixel cells of the device. The active matrix and the common electrode may be arranged to invert the polarity during alternate line addressing periods. The measuring circuit may be arranged to perform the precharging step during alternate line addressing periods.

The forming step may measure the charge stored in the first capacitor during the precharging step. The measuring circuit may be arranged to measure the stored charge by charge-sharing. The measuring circuit may be arranged, during each forming step of a first part of a conversion cycle, to share the stored charge with a transfer second capacitor during a first forming phase, and to make the first resulting voltage across the second capacitor available during a second forming phase. The measuring circuit may be arranged to

- 7 -

charge a reference third capacitor to a second precharge voltage during the precharging step, to share the stored charge with a transfer fourth capacitor during the first forming phase, and to make the second resulting voltage across the fourth capacitor available during the second forming phase. The third capacitor may have a value less than or equal to a lowest-expected value of the first capacitor. The device may comprise means for forming the difference between the first and second resulting voltages. The means may comprise a summation fifth capacitor arranged to be connected temporarily between the second and fourth capacitors. As an alternative, the means may comprise a differential input of a following stage.

The measuring circuit may comprise an analog/digital converter. The converter may be an integrating converter. The converter maybe a dual-slope converter.

The measuring circuit may be arranged, during each of repeated discharge cycles of a second part of the conversion cycle, to charge a discharge sixth capacitor to a third precharge voltage during a third phase, to share the stored charge with a transfer seventh capacitor during a fourth phase, and to make the third resulting voltage across the seventh capacitor available during a fifth phase. The measuring circuit may be arranged to charge the third capacitor to a fourth precharge voltage during the third phase,

- 8 -

to share the stored charge with the fourth capacitor during the fourth phase, and to make the fourth resulting voltage across the fourth capacitor available during the fifth phase. The sixth capacitor may have a value less than that of the third capacitor.

At least one said precharge voltage may be derived from a complement of the voltage on the common electrode.

At least one said precharge voltage may be derived from a matrix element drive voltage.

The measuring circuit may be arranged, during each of repeated calibration cycles of an initial part of the conversion cycle, to charge a calibration eighth capacitor to a fifth precharge voltage during a sixth phase, to share the stored charge with a transfer ninth capacitor during a seventh phase, and to make the fifth resulting voltage across the ninth capacitor available during an eighth phase. The measuring circuit may be arranged to charge the third capacitor to a sixth precharge voltage during the sixth phase, to share the stored charge with the fourth capacitor during the seventh phase, and to make the sixth resulting voltage across the fourth capacitor available during the eighth phase.

The measuring circuit may comprise a reference voltage generator for generating a reference voltage from the fifth resulting voltage. The generator may comprise a tenth capacitor arranged to integrate the fifth resulting voltages

- 9 -

from the calibration cycles. The generator may be arranged to supply the reference voltage to a comparator of the converter during the second part of the conversion cycle.

The signal representing the capacitance may provide a measure of the liquid crystal material temperature. The device may comprise an arrangement, responsive to the measure of the liquid crystal material temperature, for supplying temperature-compensated drive signals to the cells of the matrix.

It is thus possible to provide an arrangement in which more accurate measurement of the temperature of the liquid crystal material may be achieved. The temperature sensing capacitor is a liquid crystal capacitor with access to only one of the terminals thereof as the other terminal is formed by the device common electrode, whose potential V_{COM} may be modulated in order to avoid degradation of the liquid crystal material. By making a measurement following precharging of the liquid crystal capacitor to a fixed stable known magnitude of voltage, the voltage dependency of the capacitance can be substantially eliminated; the capacitance is not generally dependent on the polarity of the precharge voltage. The measurement is directly related to the actual temperature of the liquid crystal material, which may therefore be determined.

By performing the measurement in synchronism with the

- 10 -

addressing performed by the active matrix, it is possible to provide a measure of the sensing capacitance, and hence of the liquid crystal material temperature, with a constant voltage magnitude across the sensing capacitor. The effects of variation in capacitance with applied voltage are therefore substantially reduced or eliminated so as to provide a more accurate measure of capacitance and hence liquid crystal temperature without any disruption of the active matrix addressing.

The resulting measure may be used to compensate for the effects of temperature, for example in the case of a liquid crystal display. Where such displays are used in environments with substantially varying temperatures, compensation can be provided so as to reduce any loss in display quality such as reduction in contrast ratio. It is possible for all of the circuitry associated with measuring the capacitance to be formed within the device so that no additional connections between the device and other components are required. This arrangement may be incorporated with no modification to the design or operation of, for example, device driver circuits or the pixel matrix. A relatively accurate measure of the liquid crystal material temperature may therefore be obtained and may be used to provide high quality compensation for temperature variations in the display performance.

BRIEF DESCRIPTION OF DRAWINGS

The invention will be further described, by way of example, with reference to the accompanying drawings, in
5 which:

Figure 1 is a graph of transmittance in percentage of maximum transmittance against pixel drive voltage illustrating the transfer characteristics for several different temperatures of an active matrix liquid crystal device
10 (AMLCD);

Figure 2 is a graph of (normalised) capacitance against applied voltage of a liquid crystal sensing capacitor in an AMLCD for a plurality of temperatures;

Figure 3 illustrates diagrammatically consecutive frames
15 of a row inversion addressing scheme for an AMLCD;

Figure 4 comprises waveform diagrams illustrating the voltage or potential of a common or counter electrode for the row inversion scheme illustrated in Figure 3;

Figure 5 illustrates diagrammatically the layout of an
20 AMLCD constituting an embodiment of the invention;

Figure 6 is a block schematic diagram illustrating a temperature sensing arrangement of the AMLCD of Figure 5;

Figure 7 is a diagram illustrating waveforms occurring in the arrangement shown in Figure 6;

25 Figure 8 is a circuit diagram illustrating a first example

- 12 -

of the arrangement shown in Figure 6;

Figure 9 is a waveform diagram illustrating operation of the example shown in Figure 8;

Figure 10 is a timing diagram illustrating the timing of
5 signals in the example shown in Figure 8;

Figures 11 and 12 correspond to Figures 9 and 10, respectively, but illustrate an alternative mode of operation;

Figure 13 is a circuit diagram illustrating a second example of the arrangement shown in Figure 6;

10 Figure 14 is a timing diagram illustrating operation of the example shown in Figure 13;

Figure 15 is a circuit diagram illustrating a third example of the arrangement shown in Figure 6;

15 Figures 16 and 17 are waveform and timing diagrams illustrating operation of the example shown in Figure 15;

Figure 18 is a circuit diagram illustrating a fourth example of the arrangement shown in Figure 6;

Figure 19 is a timing diagram illustrating operation of the example shown in Figure 18;

20 Figure 20 is a circuit diagram illustrating a fifth example of the arrangement shown in Figure 6;

Figure 21 is a circuit diagram illustrating a reference voltage generator of the arrangement shown in Figure 6;

25 Figure 22 is a circuit diagram illustrating a comparator of the arrangement shown in Figure 6;

- 13 -

Figure 23 is a circuit diagram of a modified comparator of the type shown in Figure 22; and

Figure 24 is a circuit diagram illustrating an offset cancellation circuit of the arrangement of Figure 6.

5 Like reference numerals refer to like parts throughout the drawings.

BEST MODE FOR CARRYING OUT THE INVENTION

As mentioned hereinbefore, the performance of an active
10 matrix liquid crystal device (AMLCD), such as the display performance of a display, varies with the temperature of the liquid crystal material of the device. Figure 1 illustrates how the transfer function between pixel drive voltage and pixel transmittance varies for a range of temperatures to which
15 such a device may be subjected during operation. For example, such devices may be used to provide displays in vehicles and may be subjected to a very wide range of temperatures. In order to reduce the effects of temperature variations on display performance, compensation has to be provided.

20 As mentioned hereinbefore, the capacitance of a liquid crystal capacitor whose dielectric is formed by the liquid crystal material of the device may be used to provide a measure of the actual temperature of the liquid crystal material and this measure may be used in an arrangement for
25 providing temperature compensation. However, the

- 14 -

capacitance of such a liquid crystal capacitor is also dependent on the voltage applied across the liquid crystal layer and Figure 2 illustrates this variation for a range of temperatures.

5 In order to avoid or greatly reduce degradation of the liquid crystal material of such a device, it is known to reverse periodically the polarity of the drive signals applied to the individual pixel cells so that, over a period of operation, there is substantially no net direct component of the applied
10 voltage and hence of the applied field. A known technique for achieving this is referred to as "row inversion" and this is illustrated in Figure 3. The device is refreshed a frame at a time and, within each frame, the pixels are refreshed with display data a row at a time. In the first frame of each
15 consecutive pair of frames, positive drive signals are supplied to the odd-numbered rows $ROW_1, \dots, ROW_M$ and negative drive signals are supplied to the even-numbered rows. In the second frame of the consecutive pair, the polarities of the row drive signals are inverted so that each row receives positive
20 drive signals in one frame and negative drive signals in the next frame during operation of the device.

Figure 4 illustrates the voltage or potential V_{COM} , and its inverse or complement V_{COMB} , as used in a row inversion addressing scheme of the type illustrated in Figure 3. The
25 potential is switched between a maximum positive value V_{COM}

- 15 -

and a minimum zero value. This potential is supplied to a common or "counter" electrode which is common to all of the pixels and forms a continuous layer on a substrate facing an active matrix substrate of the device with the liquid crystal layer between the substrates. Drive signals are supplied to the individual pixel electrodes on the active matrix substrate to select the desired transmittance and these drive signals vary between a highest voltage V_H and a lowest voltage V_L in order to achieve the desired pixel transmittance. During row periods when the counter electrode potential is at V_{COM} , V_H represents maximum pixel transmittance whereas V_L represents minimum transmittance (or white and black, respectively). During row periods when the counter electrode potential is zero, V_H represents minimum transmittance and V_L represents maximum transmittance. Intermediate drive voltages provide grey scale display and image data for display are generated and supplied in accordance with the row inversion scheme.

Figure 5 illustrates schematically the layout of an AMLCD constituting an embodiment of the invention. In particular, Figure 5 illustrates the layout of an active matrix display first substrate 1, which hides from view a counter second substrate carrying a plane, common electrode covering substantially the whole area of the counter substrate and arranged to receive the voltage V_{COM} illustrated in Figure 4.

- 16 -

The substrates carry other layers, for example alignment layers, and are spaced apart to define a cavity containing a liquid crystal material. Polarises, colour filters, retarders, and other components may be provided as necessary in order to
5 form a complete device such as a display.

The display substrate 1 comprises a pixel matrix area 2 over most of the area of the substrate. A display source driver 3 and a display gate driver 4 are disposed along two adjacent edges of the substrate 1 and perform active matrix addressing
10 of the pixel matrix. A display timing and control arrangement 5 controls refreshing of image data, which it receives from a "host" at an input 6. Such arrangements are well known and will not be described further.

The device shown in Figure 5 also comprises a
15 temperature measurement apparatus 10 in the form of a capacitance measuring circuit. The apparatus comprises a temperature sensing first liquid crystal capacitor 11, which comprises a first electrode formed on the substrate 1 outside the image generating region of the active matrix pixel area 2.
20 The first electrode cooperate with the common electrode on the counter substrate forming the second capacitor electrode and with the liquid crystal layer providing the capacitor dielectric. The capacitor 11 is connected to a sample and hold circuit 12, which repeatedly precharges the capacitor 11 to a
25 fixed stable known magnitude of voltage constituting a first

- 17 -

precharge voltage, and measures the capacitance of the capacitor 11, in synchronism with addressing of the pixel matrix. The output signal of the circuit 12 is an analog signal representing the capacitance of the capacitor 11. The voltage dependency of the capacitor 11 may thus be accounted for and a more accurate measure of capacitance, and hence temperature, may be obtained. For convenience, the capacitance may be measured with the same voltage magnitude, and maybe polarity, across the liquid crystal capacitor 11 so as to avoid the voltage-dependent effects illustrated in Figure 2. The capacitance of the capacitor 11 is thus substantially only a function of the liquid crystal temperature, with voltage-dependent effects greatly reduced or eliminated, and thus provides a measure of the actual liquid crystal temperature.

The output of the circuit 12 is supplied to an analog/digital converter (ADC) 13, which converts the measured signal to a corresponding digital value. A control signal generator 14 generates control signals for controlling the operation of the apparatus 10. The output of the ADC 13 is supplied to a sensor interface 15, which supplies control signals to the apparatus 10 from the host and from the arrangement 5. The measure of the liquid crystal temperature is used to compensate for the temperature variations illustrated in Figure 1. For example, the measured

- 18 -

temperature may be supplied to the host, which generates the appropriate image data so as to compensate for differences in temperature of the liquid crystal material from the nominal working temperature of the device.

5 As shown in Figure 6, only the electrode of the capacitor 11 on the display substrate 1 is accessible and this is connected to the input of the sample and hold circuit 12. The capacitance of the capacitor 11 is denoted by C_{LC} and varies with the liquid crystal material temperature. The output $V_{S/H}$ of the circuit 12 is supplied to the ADC 13, which is in the form of a dual-slope ADC. Thus, the ADC comprises an integrator 20, whose output V_{OUT} is supplied to a comparator 21. The output of the comparator 21 is supplied to a counter 22, which forms the digital output signals of the ADC 13. The basic operation and structure of a dual-slope ADC are well known and only those aspects of structure and performance which are relevant to the use of such a device in the AMLCD shown in Figure 5 will be described in detail hereinafter.

20 Vertical and horizontal synchronising signals VSYNC and HSYNC are illustrated in Figure 7 together with the output of the integrator 20 and the output of the comparator 21. Each vertical and horizontal synchronising signal marks the start of an active matrix addressing cycle comprising a frame and line addressing period, respectively. During a first frame refresh operation of the AMLCD forming a "sampling"

25

- 19 -

frame of the apparatus 10, the sample and hold circuit 12 generates the voltage $V_{S/H}$ proportional to the capacitance C_{LC} of the liquid crystal capacitor 11. During 2^N row refresh periods, where N is the number of bits of the counter 22, the integrator 20 increments its output voltage by $kV_{S/H}$, where k is the integrator constant, so that, after the 2^N selected rows, which are the last 2^N refreshed rows in the frame, the output voltage V_{OUT} of the integrator is equal to $2^N.kV_{S/H}$. In practice and as described in more detail hereinafter, the integrator 20 actually integrates a difference signal representing the difference between the capacitance C_{LC} of the capacitor 11 and the capacitance C_{REF} of a reference capacitor, whose capacitance is independent of temperature and is arranged to be less than or equal to the minimum value of the capacitance C_{LC} . The integrator 20 thus receives a positive signal at its input and produces an up-slope at its output.

During the second "conversion" frame, the sample and hold circuit 12 generates a voltage which is proportional to the difference between the capacitance of the reference capacitor and that of a discharge capacitor, whose capacitance is independent of temperature and is arranged to be a known amount less than the reference capacitor. The input signal for the integrator 20 is thus negative and the integrator produces a down-slope at its output.

The comparator 21 compares the output voltage V_{OUT} of

- 20 -

the integrator 20 with a reference voltage V_{REF} and produces an output pulse for each row refresh period during which the output voltage is greater than the reference voltage. The reference voltage V_{REF} may be a known fixed potential or may
5 be generated during an additional calibration frame as described hereinafter. For each output pulse from the comparator 21, the counter 22 is incremented by one count so that, at the end of the conversion frame, the output of the counter 22 is proportional to the difference in capacitance
10 between the liquid crystal capacitor 11 and the reference capacitor.

The whole of the apparatus 10 is formed on the display substrate 1 so that only minimal external connections are required. For example, the apparatus 10 may be formed from
15 transistors and other components integrated on the display substrate in the form of polycrystalline silicon thin-film transistor circuitry.

A first example of the apparatus is shown in more detail in Figure 8. The sensor interface 15 comprises a timing
20 generator, which supplies multiple phase clock signals $\Phi_1, \dots, \Phi_{DCB}$, some or all of which are used by the sample and hold circuit 12 and the ADC 13. The clock signals divide each row refresh period into a plurality of phases for performing the measurement.

25 The liquid crystal first capacitor 11 is shown as part of

- 21 -

the circuit 12 within a liquid crystal capacitor branch 25. The branch 25 comprises electronic switches (for example formed by thin film transistors). A switch S_{1A} is closed only during a clock phase signal Φ_{1A} to charge the available plate of the capacitor 11 to the first precharge voltage comprising the voltage of the complement V_{COMB} of the potential V_{COM} supplied to the common electrode. A switch S_{2A} is closed only during a clock phase signal Φ_{2A} to connect a transfer second capacitor of capacitance C_0 to the liquid crystal capacitor 11 so as to perform charge transfer such that the voltage across the transfer capacitor, constituting a first resulting voltage, is proportional to the charge held in the previous phase in the liquid crystal capacitor 11 and hence is proportional to the capacitance C_{LC} of the liquid crystal capacitor. During the clock phase signal Φ_{1A} , a switch S_{4A} is closed so as to discharge the transfer capacitor in readiness for charge transfer. During a clock phase signal Φ_{3A} , the switch S_{3A} is closed so as to connect the transfer capacitor to a non-inverting or "positive" input of the integrator 20.

A reference capacitor branch 26 is connected to the "negative" or inverting input of the integrator 20 and comprises the reference third capacitor of capacitance C_{REF} , a transfer fourth capacitor of capacitance C_0 , switches S_1 and S_4 controlled by the clock phase signal Φ_1 , and switches S_2 and S_3 controlled by clock phase signals Φ_2 and Φ_3 ,

- 22 -

respectively. The circuit 12 further comprises a discharge capacitor branch 27 comprising a discharge sixth capacitor of capacitance C_{DIS} , a transfer seventh capacitor of capacitance C_O , switches S_{1B} and S_{4B} controlled by a clock phase signal Φ_{1B} , and switches S_{2B} and S_{3B} controlled by clock phase signals Φ_{2B} and Φ_{3B} , respectively. The output of the discharge capacitor branch 27 is also connected to the non-inverting input of the integrator 20. The inputs of the integrator 20 are connected to ground during the clock phase signal Φ_1 by switches S_5 and S_6 .

The integrator 20 is illustrated as a differential integrator having integrating capacitors 28 and 29 of capacitance C_F . The output of the integrator is provided with a reset switch S_7 for resetting the integrator at the start of each cycle of operation.

Each complete conversion cycle of operation takes place in two consecutive frame refresh periods of the AMLCD. Two full conversion cycles are illustrated by the waveform diagram of Figure 9 and Figure 10 illustrates the clock phase timing during a first frame and part of a second frame of a conversion cycle.

A signal from the display gate driver 4 may be used to select the rows in which the sample and hold circuit 12 is active. For example, the $(M-2^N)$ th row scan signal of the display gate driver may be used to initiate the up and down

- 23 -

slopes of the integrator 20 as illustrated in Figure 9, where M is the number of rows of the AMLCD and N is the number of output bits of the counter 22. Alternatively, the signals may be supplied externally although this is less desirable because the number of connections to the AMLCD would have to be increased.

During the first "sampling" frame of each conversion cycle, the liquid crystal capacitor branch 25 and the reference capacitor branch 26 are active. The clock phase signals Φ_1 - Φ_3 and Φ_{1A} - Φ_{3A} comprise two sets of non-overlapping clock phase signals for the switches of the sample and hold circuit 12 and are enabled in turn during the last 2^N display row periods as illustrated in Figure 9. The timing of the individual clock phase signals is illustrated in Figure 10.

When the clock phase signals Φ_1 and Φ_{1A} are simultaneously active, the switches S_1 , S_{1A} , S_4 , S_{4A} , S_5 and S_6 are closed whereas the other switches are open. The voltage V_{COMB} is transferred to the first electrodes of the liquid crystal capacitor 11 and the reference capacitor C_{REF} so that the voltages across both capacitors are equal to $V_{COM}-V_{COMB}$, constituting first and second precharge voltages on the capacitors 11 and C_{REF} , respectively. These voltages are illustrated in Figure 4. The transfer capacitors C_0 and the integrator input terminals are reset to ground potential during this phase.

- 24 -

During the next phase corresponding to clock phase signals Φ_2 and Φ_{2A} , the switches S_2 and S_{2A} are closed whereas the other switches are open so that charge sharing occurs between the liquid crystal and reference capacitors and the corresponding transfer capacitors in the branches 25 and 26. The terminals of the transfer capacitors connected during this phase to the liquid crystal and reference capacitors rise to potentials given by $C_{LC} \cdot V_{COMB} / (C_{LC} + C_O)$ and $C_{REF} \cdot V_{COMB} / (C_{REF} + C_O)$, constituting first and second resulting voltages, respectively. The output voltage of the sample and /hold circuit 12 is the difference between these voltages and is positive because C_{REF} is less than or equal to the minimum expected liquid crystal capacitance C_{LC} . This output voltage is approximately proportional to the difference between the capacitance C_{LC} of the liquid crystal capacitor and the capacitance C_{REF} of the reference capacitor.

During the clock phase signals Φ_3 and Φ_{3A} , the switches S_3 and S_{3A} are closed whereas the other switches of the circuit 12 are open. The output voltage of the circuit 12 is applied between the differential inputs of the integrator 20 and this results in the output V_{OUT} of the integrator being incremented by the product of the sample and hold circuit output voltage and (C_O / C_F) , where C_F is the capacitance of the integrating or feedback capacitor 28. This process is repeated for the 2^N row periods of the sampling frame, at the end of

- 25 -

which the output voltage of the integrator 20 is equal to $2^N (C_O/C_F) V_{IN}$, where V_{IN} is the input voltage supplied to the integrator 20.

During the following "conversion" frame, the reference
5 capacitor branch 26 and the discharge capacitor branch 27
are active. As shown in Figures 9 and 10, during the last 2^N
row periods of the conversion frame, the clock phase signals
 Φ_1 - Φ_3 and Φ_{1B} - Φ_{3B} control the switches of the sample and
hold circuit 12. During the clock phase signals Φ_{1B} and Φ_1 ,
10 the capacitors, respectively, C_{REF} and C_{DIS} are charged to
third and fourth precharge voltages, respectively. Charge
sharing takes place during the clock phase signals Φ_{2B} and Φ_2
and third and fourth resulting voltages are made available
across the capacitors C_O of the branches 27 and 26 during the
15 clock phases signals Φ_{3B} and Φ_3 , respectively. Thus, during
each active row period of the conversion frame, a negative
voltage substantially proportional to the difference between
the capacitances C_{REF} and C_{DIS} of the reference and discharge
capacitors is decremented from the output voltage V_{OUT} of the
20 integrator 20.

During each active row period of the conversion frame,
the comparator 21 is enabled by a sampling pulse SAM whose
timing is illustrated in Figure 10. When enabled by this pulse,
the comparator 21 compares the output V_{OUT} of the integrator
25 20 with a reference voltage V_{REF} and supplies an output pulse

- 26 -

for each sampling period when the integrator output voltage is greater than the reference voltage. The reference voltage V_{REF} may be any suitable voltage, for example ground potential or a potential derived as described hereinafter. At
5 the end of the conversion frame, the counter 22 holds a value, for example in binary code, proportional to the capacitance of the liquid crystal capacitor 11 and hence representing a measure of the temperature of the liquid crystal material. The integrator 20 is re-set by means of a re-set pulse RST which
10 closes the switch S_7 so that the apparatus is ready to repeat the whole conversion cycle whenever required.

The apparatus thus provides an accurate measurement of the actual temperature of the liquid crystal material and, as described hereinbefore, this may be used in a temperature
15 compensation arrangement, for example to vary the pixel drive voltages so as to reduce the dependence of image appearance and quality on temperature. The temperature sensing arrangement is operated in synchronism with the AMLCD timing so that measurement of the liquid crystal
20 capacitance occurs when the display common electrode is at a known settled potential. Thus, the effects of voltage-dependence are substantially reduced or eliminated. Further, because the complement or inverse of the common electrode potential is used for charging the liquid crystal
25 capacitor, DC balance is maintained across the liquid crystal

- 27 -

capacitor 11 so as substantially to avoid degradation of the liquid crystal material forming the capacitor dielectric.

A possible reduction in accuracy of measurement of the example illustrated in Figure 8 results from the fact that the row periods during which the voltage VCOMB is at ground potential are used in the conversion cycle. Thus, during the even-numbered row periods of the first frame shown in Figure 3, the output voltage of the sample and hold circuit 12 is nominally zero volts. However, because of errors caused by parasitic effects, such as charge injection from the electronic switches of the sample and hold circuit 12, the output voltage may differ sufficiently significantly from zero to affect the accuracy of the capacitance, and hence temperature, measurement.

In order to avoid this possible disadvantage, the example shown in Figure 8 may be arranged to perform the sampling only during row periods where the voltage VCOMB is at its high level as illustrated in Figure 4.

The waveform diagram of Figure 11 illustrates this mode of operation and the modified clock phase timing is illustrated in the timing diagram of Figure 12. The individual sampling and conversion operations are thus performed for every second row period when the liquid crystal, reference and discharge capacitors are charged to the higher potential of the signal VCOMB. Because 2^N row periods are required to be

- 28 -

active for generating the up and down slopes of the N-bit ADC 13, the sampling and conversion periods occupy the last 2^{N+1} row periods of the sampling and conversion frames.

In order to maintain DC balancing of the liquid crystal capacitor 11, its first electrode is connected to receive the signal VCOMB during the active row periods of the second or conversion frame of each conversion cycle.

The example illustrated in Figure 8 requires that the additional signal VCOMB be generated and supplied to the AMLCD. However, this may be avoided, in the case of an AMLCD with digital driver circuits integrated onto the display substrate, as shown in the example illustrated in Figure 13. In particular, the voltages V_H and V_L are supplied as reference voltages for digital-to-analog converters forming part of the AMLCD and these voltages are symmetrical around the voltage VCOM of the common terminal so that DC balance of the liquid crystal material in each pixel may be maintained by means of a suitable modulation scheme. Thus, as shown in Figure 13, the upper voltage V_H may be used for charging the liquid crystal, reference and discharge capacitors in the branches 25-27 during the clock phase signals Φ_1 , Φ_{1A} and Φ_{1B} . In order to provide DC balancing of the liquid crystal capacitor 11, an additional switch S_{DCB} is provided and controlled by a clock phase signal Φ_{DCB} as shown in Figure 14. Where the reference and discharge capacitors are not of the

- 29 -

liquid crystal type but employ conventional dielectrics, they do not require such DC balancing.

The example illustrated in Figure 15 differs from that illustrated in Figure 13 in that the positive or non-inverting input of the integrator 20 is connected to a known reference voltage, such as ground potential, and a summation fifth capacitor C_1 is connected between the negative or inverting input of the integrator 20 and the outputs of the liquid crystal capacitor and discharge capacitor branches 25 and 27. Also, the switches S_5 and S_6 are controlled by the second clock phase signal Φ_2 and two further switches S_8 and S_9 are controlled by a further clock phase signal Φ_4 . The switch S_9 is connected between the inverting input of the integrator 20 and the first terminal of the capacitor C_1 whereas the switch S_8 is connected between the second terminal of the capacitor C_1 and ground.

The operation of this example during each row period is the same as described hereinbefore to the point where the clock phase signals Φ_3 and Φ_{3A} or Φ_{3B} are active, at which point the output voltage of the sample and hold circuit 12 is transferred to the summation capacitor C_1 , which was previously fully discharged by the switches S_5 and S_6 during the clock phase signal Φ_2 .

An advantage of this example with the summation capacitor C_1 is that the overall size of the apparatus 10 may

- 30 -

be reduced. In the examples illustrated in Figures 8 and 13, the ratios of the capacitances C_{LC} , C_{DIS} and C_{REF} to the transfer capacitance C_O and of the transfer capacitance to the feedback capacitance C_F must be such that, for example, C_{LC}
5 $= C_O = kC_F$, where $1/k$ determines the gradient of the upslope produced by the integrator 20. It is desirable to make C_{LC} relatively large so as to reduce process mismatch errors and, for a high output bit resolution, k must be made greater than unity to avoid saturation of the integrator 20. For example, a
10 typical value of k is 5. Thus, the capacitors which are required are relatively large compared with the accompanying active circuitry so that a relatively large area is needed in which to integrate the apparatus 10.

The apparatus 10 is required to be integrated on a fringe
15 area of the display substrate and it is desirable to minimise the required area in order to reduce the fringe size of the AMLCD. The use of the summation capacitor C_1 removes the need for the feedback capacitor 29 at the non-inverting integrator input and removes the dependency of the
20 capacitance C_F of the capacitor 28 on the capacitance C_O of the transfer capacitors. The capacitance of the summation capacitor is not directly related to, for example, the liquid crystal capacitance C_{LC} and may be made substantially smaller than C_O without increasing the effect of process
25 mismatch errors. The feedback capacitor 28 still has a value

- 31 -

related to that of the summation capacitor and so may also be reduced in size. Also, with such an arrangement, it is easier to provide offset removal or compensation for the integrator 20.

5 Figures 16 and 17 are waveform and timing diagram which illustrate the operation of the example shown in Figure 15. Figure 16 is similar to Figure 11 but shows the output signal $V_{S/H}$ of the circuit 12 instead of the switch timing signals. Figure 17 differs from Figure 14 in that it shows the
10 clock phase signal Φ_4 .

 Figure 18 illustrates another example of the apparatus 10 which differs from that shown in Figure 15 in that a calibration capacitor branch 30 is provided and comprises a calibration eighth capacitor C_{CAL} , a transfer ninth capacitor
15 C_O , and switches $S_{1C} - S_{4C}$ controlled by clock phase signal $\Phi_{1C} - \Phi_{3C}$. The output of the branch 30 is connected to the same terminal of the summation capacitor C_1 as the liquid crystal and discharge capacitor branches 25 and 27. Also, the integrator comprises an operational amplifier 31 provided
20 with a feedback network 32, which replaces the feedback capacitor 28 and includes a reference voltage generator for providing the reference voltage V_{REF} to the comparator 21.

 As illustrated by the timing diagram in Figure 19, each conversion cycle includes an initial frame period during which
25 calibration is performed and a final frame period during

- 32 -

which DC balancing is performed, with the sampling and conversion frames being disposed therebetween. During the calibration frame, the calibration and reference capacitor branches 30 and 26 are active and the feedback network 32 is
5 arranged to present a capacitance C_F between the inverting input and the output of the operational amplifier 31. The capacitor charging, charge transfer, difference forming and integrating operations are as described hereinbefore so that, during the active row periods, the integrator 20 provides an
10 output voltage V_{OUT} which is dependent on the difference between the values C_{REF} and C_{CAL} of the reference and calibration capacitors. For example, during the clock phase signals Φ_{1C} and Φ_1 , the capacitors C_{CAL} and C_{REF} are charged to fifth and sixth precharge voltages, respectively, and, during
15 the clock pulse signals Φ_{3C} and Φ_3 , fifth and sixth resulting voltages are available across the capacitors C_O in the branches 30 and 26, respectively. The calibration and reference capacitors are of nominally equal capacitance so that, in the absence of any errors introduced by the practical
20 implementation of this example, the output voltage of the integrator 20 would be zero.

However, errors are introduced by such a practical implementation. For example, such errors are caused by charge-injection effects resulting from finite parasitic
25 capacitances of the transistor-based switches so that the

- 33 -

actual output voltage of the integrator 20 during the calibration frame provides a voltage which may be used as the reference voltage for the comparator 21 in order to reduce or eliminate such errors.

5 During the sampling and conversion frame periods, a capacitor (which forms part of the reference voltage generator but is not shown in Figure 18) storing the reference voltage is disconnected from the operational amplifier 31 and used to provide the reference voltage to the comparator 21. Another
10 feedback capacitor (not shown in Figure 18) of the same capacitance C_F is connected by the feedback network 32 between the inverting input and the output of the operational amplifier 31 and the sampling and conversion operations described hereinbefore are performed. The compensating
15 voltage reference supplied to the comparator 21 at least partially compensates for the errors mentioned above so as to provide a more accurate measure of the liquid crystal capacitance and hence of the temperature of the liquid crystal material.

20 In order to provide DC balancing so as to reduce or avoid degradation of the liquid crystal layer, a fourth "balancing" frame is required as illustrated in Figure 19. In the first calibration frame, the switch $S_{1A(B)}$ is closed by the clock phase signal $\Phi_{1A(B)}$ to connect the liquid crystal
25 capacitor 11 to the lower drive voltage V_L during each active

- 34 -

row period. During the row periods, the common electrode is at the higher voltage.

During the second sampling frame, the liquid crystal capacitor is connected to the higher drive voltage V_H and the common electrode is at its lower voltage during the active row periods. During the conversion frame, the liquid crystal capacitor is at the lower drive voltage and the common electrode is at the higher voltage during the active rows. Accordingly, in order to provide DC balancing during the active rows of the balancing frame, the liquid crystal capacitor is charged to the higher drive voltage and the common electrode is at the lower voltage.

The example illustrated in Figure 20 differs from that shown in Figure 18 in that the calibration and discharge capacitors C_{CAL} and C_{DIS} are embodied as liquid crystal capacitors biased to operate in the temperature independent region. In particular, the timing is such that the calibration and discharge capacitors C_{CAL} and C_{DIS} are "measured" with a relatively low voltage across them. This low voltage is selected to be in the voltage range where capacitance is substantially independent of temperature, for example as illustrated in Figure 2 for voltages below about 1.5 volts.

The basic operation of this example is the same as for that of Figure 18 except that DC balancing has to be provided in respect of the calibration and discharge capacitors. This is

- 35 -

achieved by providing switches $S_{1A(B)} - S_{1C(B)}$ controlled by clock phase signals $\Phi_{1A(B)} - \Phi_{1C(B)}$, respectively, for connecting the capacitors to the lower drive voltage V_L . The waveform diagram of Figure 19 applies to the example of Figure 20.

5 However, the additional clock phase signals are such that:

- the liquid crystal capacitor 11 is connected to the lower drive voltage V_L during the calibration and conversion frames and to the higher voltage V_H during the sampling and balancing frames;

10 • the calibration capacitor is connected to the higher voltage V_H during the calibration and conversion frames and to the lower voltage V_L during the sampling and balancing frames; and

15 • the discharge capacitor is connected to the higher voltage V_H during the calibration and conversion frames and to the lower voltage V_L during the sampling and balancing frames.

20 An advantage of this example is that accuracy of measurement is increased because of improved matching of capacitors of similar construction. In particular, the liquid crystal, discharge and calibration capacitors are all liquid crystal capacitors and may be matched more closely than for the previous examples, in which the liquid crystal capacitor is of a different construction from the conventional dielectric

25 discharge and calibration capacitors. Although the reference

- 36 -

capacitance C_{REF} should be of a value similar to the liquid crystal capacitance C_{LC} , the reference capacitor should not be a liquid crystal capacitor because any mismatch is removed by means of the calibration frame.

5 Figure 21 illustrates an example of the feedback network
32 connected between the inverting input and the output of
the operational amplifier 31 and supplying the reference
voltage V_{REF} to the comparator 21. The feedback network 32
comprises electronic switches $S_{FB,1} - S_{FB,7}$ and capacitors
10 $C_{FB,1}$ and $C_{FB,2}$. The switches $S_{FB,1}-S_{FB,4}$ and the tenth
capacitor $C_{FB,1}$ form the reference voltage generator. This
arrangement allows a calibration voltage to be generated
during the calibration frame and subsequently stored as a
reference voltage for the comparator 21 during the third
15 conversion frame. During each of the frames of each
conversion cycle, the feedback network 32 presents a
capacitance C_F between the inverting input and the output of
the operational amplifier 31.

 During the calibration frame, the switches $S_{FB,1}$ and
20 $S_{FB,2}$ are closed so that the capacitor $C_{FB,1}$ is connected
between the inverting input and the output of the operational
amplifier 31. The switches $S_{FB,7}$ and S_7 are briefly closed so as
to reset the terminals of the capacitor $C_{FB,1}$ to ground
potential. The calibration frame then proceeds as described
25 hereinbefore so that, at the end of the calibration frame, the

- 37 -

voltage stored across the capacitor $C_{FB,1}$ is equal to the integrator output error voltage.

During the next three frames, the switches $S_{FB,1}$ and $S_{FB,2}$ are opened whereas the switches $S_{FB,3} - S_{FB,6}$ are closed.

5 The switches $S_{FB,7}$ and S_7 are briefly closed to reset the terminals of the capacitor $C_{FB,2}$ to ground potential. The integrator output voltage during the calibration frame is thus supplied to the comparator 21 as the reference voltage V_{REF} for use during the conversion frame. The capacitor $C_{FB,2}$ acts
10 as the integrating capacitor during the sampling, conversion and balancing frames of each conversion cycle.

Figure 22 illustrates an example of the comparator 21 including offset correction circuitry, for example of the type disclosed in R. Gregorian "Introduction to CMOS Op Amps
15 and Comparators", John Wiley and Sons, 1999. The reference voltage supplied by the feedback network of the integrator 20 is additionally used to provide a reference voltage for offset removal.

The comparator 21 comprises cascaded operational
20 amplifiers 40, 41 and 42, a dynamic latch 43 which receives the sampling pulse SAM, offset storage capacitors $C_{CP,1} - C_{CP,6}$, electronic switches $S_{CP,1}$ and $S_{CP,2}$ controlled by the clock phase signal Φ_2 , and electronic switches $S_{CP,3} - S_{CP,10}$ controlled by the clock phase signal Φ_1 .

25 The offsets of the amplifiers 40, 41 and 42 may vary with

- 38 -

their respective input voltages. For example, if the offsets are removed at a particular voltage, then residual offset errors may exist at other operational voltages. For improved accuracy, such offsets should be removed under the same conditions as will prevail during operation. In this example, the offsets are removed at the reference voltage so as to improve conversion accuracy.

During a first phase of offset removal, the switches $S_{CP,3}$ - $S_{CP,10}$ are closed so that the offsets of the individual stages are measured and stored on the capacitors $C_{CP,1}$ - $C_{CP,6}$. The amplifier offset voltages are measured at the operating point specified by the reference voltage V_{REF} .

During the second phase of offset removal, the switches $S_{CP,3}$ - $S_{CP,10}$ are opened and the switches $S_{CP,1}$ and $S_{CP,2}$ are closed so that the input of the first amplifier 40 is connected to the comparator input. The comparator thus operates as normal and, because the individual offset voltages remain stored across the capacitors $C_{CP,1}$ - $C_{CP,6}$, errors arising from the amplifier offset voltages are substantially eliminated or greatly reduced.

The comparator offset removal cycle need only be performed once at the start of each conversion frame, alternatively, in order to reduce errors caused by leakage from the offset storage capacitors $C_{CP,1}$ - $C_{CP,6}$, the offset removal cycle may be performed at the beginning of every row

- 39 -

period of the conversion frame.

The arrangement illustrated in Figure 23 differs from that shown in Figure 22 in that a unity gain buffer 45 buffers the reference voltage generator $S_{FB,1}$ - $S_{FB,4}$, $C_{FB,1}$ in the integrator 20 from loading effects of the comparator 21. Thus, the integrator output error voltage stored on the capacitor $C_{FB,1}$ is not substantially disturbed by the comparator offset removal cycle and by measurement operations. A similar offset removal arrangement may be provided for the unity gain buffer 45 and a suitable arrangement is disclosed in G. Carins et la "Multi-Format Digital Display with Content Driven Display Format", Society for Information Display Technical Digest, 2001 pp. 012-105.

Figure 24 illustrates an offset cancellation arrangement forming part of the integrator 20. Such an arrangement is provided in order to compensate for variations in transistor characteristics within the operational amplifier 31 which might otherwise cause the amplifier to exhibit an input offset error voltage, which may result in conversion error and amplifier saturation. The arrangement comprises an offset storage capacitor C_{OS} , electronic switches $S_{OS,1}$ - $S_{OS,4}$ controlled by a clock phase signal Φ_1 , and electronic switches $S_{OS,5}$ and $S_{OS,6}$ controlled by a clock phase signal Φ_2 . When used in conjunction with the feedback network 32 described hereinbefore, the switch $S_{OS,1}$ may be embodied by the switch

- 40 -

 $S_{FB,7}$.

Operation of the offset cancellation arrangement occurs in two phases. In the first phase, the amplifier offset is sampled. In particular, the switches $S_{OS,1} - S_{OS,4}$ are closed so that the operational amplifier 31 is connected in a unity gain configuration and the amplifier offset is stored on the capacitor C_{OS} . In particular, the output of the amplifier 31 is connected to the inverting input of the amplifier 31 via the switch $S_{OS,1}$ so that the amplifier 31 has a voltage gain of unity to provide the unity gain configuration. The non-inverting input of the amplifier 31 is connected to ground via the switch $S_{OS,3}$ so that the input offset error voltage appears between the inverting and non-inverting inputs of the amplifier 31. The input offset error voltage appears at the output of the amplifier 31 and hence across the capacitor C_{OS} via the switches $S_{OS,2}$ and $S_{OS,4}$. In the second phase, the switches $S_{OS,5}$ and $S_{OS,6}$ are closed so that the sampled offset voltage is inverted and applied to the non-inverting input terminal of the amplifier 31. Following offset sampling, offset correction is maintained during subsequent operation of the integrator 20.

The amplifier offset voltage may be sampled once during a conversion cycle, for example before the calibration frame when present. The offset voltage then remains stored on the capacitor C_{OS} until a subsequent offset sampling phase.

- 41 -

Alternatively, the offset voltage may be sampled at the beginning of each frame of the conversion cycle. As a further alternative, the offset voltage may be sampled at the beginning of each active row period during which the
5 integrator 20 is in operation. This more frequent offset sampling and correction is preferable if charge leakage from the capacitor C_{os} would result in an error in the stored offset voltage accumulating with time.

The temperature measurement of the liquid crystal
10 material is used to effect a change in the operation of the AMLCD. For example, the driving voltages applied to pixels of the AMLCD may be adjusted in order to compensate the display for temperature-induced changes in the properties of the liquid crystal material. Means for adjusting the display
15 driving voltages may comprise a look-up table and one or more digital/analog converters (DACs) for controlling reference voltages used in display driving circuits. Values stored in the look-up table may be predetermined by experiment to allow the generation of appropriate driving
20 voltages for the measured temperature.

For example, a set of liquid crystal voltage transmission curves for a range of temperatures may be stored in the look-up table and the appropriate or closest curve may be selected on the basis of the measured temperature of the
25 liquid crystal material. Alternatively, a limited set of points

- 42 -

may be stored with intermediate values being interpolated so as to generate the appropriate curve for any liquid crystal temperature. A further possibility, as disclosed in US 5,926,162, is to alter the voltage of the common electrode in accordance with the measured temperature.

The temperature of the liquid crystal material in an AMLCD is not a rapidly changing variable. Accordingly, it may be sufficient to perform temperature measurements relatively infrequently in order to reduce power consumption. The frequency of measurement may be predetermined or may be variable and may be set externally by a user or host. Alternatively, the user or host may supply a signal requesting that a temperature measurement cycle be performed. In response to such a request, the apparatus begins a measurement cycle as described hereinbefore at the start of a frame period with the common electrode at a suitable polarity. At the end of the measurement cycle, the output of the counter 22 is stored and made available for providing AMLCD temperature compensation or for any other desired purpose.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

The invention being thus described, it will be obvious that the same way may be varied in many ways. Such

- 43 -

variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

- 44 -

CLAIMS

1. An active matrix liquid crystal device comprising: an active matrix first substrate having an active matrix area; a
5 second substrate carrying a common electrode for the active matrix; a layer of liquid crystal material between the first and second substrates; a temperature sensing first capacitor comprising a first electrode outside the image generating region of the active matrix area on the first substrate
10 separated from the common electrode, which forms a second electrode of the first capacitor, by the liquid crystal layer, which forms the first capacitor dielectric; and a capacitance measuring circuit arranged, during operation of the active matrix, repeatedly to perform the steps of precharging the
15 first capacitor to a substantially fixed stable known first precharge voltage magnitude and forming a signal representing the capacitance of the first capacitor.

2. A device as claimed in claim 1, in which the
20 measuring circuit is formed on the first substrate.

3. A device as claimed in claim 1, in which the measuring circuit is arranged to charge the first capacitor to the same magnitude of voltage during each precharging step.

- 45 -

4. A device as claimed in claim 3, in which measuring circuit is arranged to charge the first capacitor to the same polarity of voltage during each precharging step.

5 5. A device as claimed in claim 1, in which the measuring circuit is arranged to perform each precharging step at a same part of an active matrix addressing cycle.

10 6. A device as claimed in claim 5, in which the same part comprises the same part of a line addressing period.

15 7. A device as claimed in claim 1, in which the active matrix and the common electrode are arranged periodically to invert the polarity of drive voltages applied to pixel cells of the device.

20 8. A device as claimed in claim 4, in which the active matrix and the common electrode are arranged to invert the polarity during alternate line addressing periods.

 9. A device as claimed in claim 8, in which the measuring circuit is arranged to perform the precharging step during alternate line addressing periods.

25 10. A device as claimed in claim 1, in which the forming

- 46 -

step measures the charge stored in the first capacitor during the precharging step.

11. A device as claimed in claim 10, in which the
5 measuring circuit is arranged to measure the stored charge by charge-sharing.

12. A device as claimed in claim 11, in which the
measuring circuit is arranged, during each forming step of a
10 first part of a conversion cycle, to share the stored charge with a transfer second capacitor during a first forming phase, and to make the first resulting voltage across the second capacitor available during a second forming phase.

13. A device as claimed in claim 12, in which the
15 measuring circuit is arranged to charge a reference third capacitor to a second precharge voltage during the precharging step, to share the stored charge with a transfer fourth capacitor during the first forming phase, and to make
20 the second resulting voltage across the fourth capacitor available during the second forming phase.

14. A device as claimed in claim 13, in which the third
capacitor has a value less than or equal to a lowest-expected
25 value of the first capacitor.

15. A device as claimed in claim 13, comprising means for forming the difference between the first and second resulting voltages.

5

16. A device as claimed in claim 15, in which the means comprises a summation fifth capacitor arranged to be connected temporarily between the second and fourth capacitors.

10

17. A device as claimed in claim 15; in which the means comprises a differential input of a following stage.

18. A device as claimed in claim 1, in which the measuring circuit comprises an analog/digital converter.

15

19. A device as claimed in claim 18, in which the converter is an integrating converter.

20

20. A device as claimed in claim 19, in which the converter is a dual-slope converter.

21. A device as claimed in claim 12, in which the measuring circuit comprises a dual-slope analog/digital converter and is arranged, during each of repeated discharge

25

- 48 -

cycles of a second part of the conversion cycle, to charge a
discharge sixth capacitor to a third precharge voltage during
a third phase, to share the stored charge with a transfer
seventh capacitor during a fourth phase, and to make the
5 third resulting voltage across the seventh capacitor available
during a fifth phase.

22. A device as claimed in claim 21, in which the
measuring circuit is arranged to charge the third capacitor to
10 a fourth precharge voltage during the third phase, to share
the stored charge with the fourth capacitor during the fourth
phase, and to make the fourth resulting voltage across the
fourth capacitor available during the fifth phase.

15 23. A device as claimed in claim 22, in which the sixth
capacitor has a value less than that of the third capacitor.

24. A device as claimed in claim 1, in which at least one
said precharge voltage is derived from a complement of a
20 voltage on the common electrode.

25. A device as claimed in claim 1, in which at least one
said precharge voltage is derived from a matrix element drive
voltage.

- 49 -

26. A device as claimed in claim 12, in which the measuring circuit is arranged, during each of repeated calibration cycles of an initial part of the conversion cycle, to charge a calibration eighth capacitor to a fifth precharge
5 voltage during a sixth phase, to share the stored charge with a transfer ninth capacitor during a seventh phase, and to make the fifth resulting voltage across the ninth capacitor available during an eighth phase.

10 27. A device as claimed in claim 26, in which the measuring circuit is arranged to charge the third capacitor to a sixth precharge voltage during the sixth phase, to share the stored charge with the fourth capacitor during the seventh phase, and to make the sixth resulting voltage across the
15 fourth capacitor available during the eighth phase.

28. A device as claimed in claim 26, in which the measuring circuit comprises a reference voltage generator for generating a reference voltage from the fifth resulting voltage.

20 29. A device as claimed in claim 28, in which the generator comprises a tenth capacitor arranged to integrate the fifth resulting voltages from the calibration cycles.

25 30. A device as claimed in claim 21, in which the

- 50 -

measuring circuit is arranged, during each of repeated calibration cycles of an initial part of the conversion cycle, to charge a calibration eighth capacitor to a fifth precharge voltage during a sixth phase, to share the stored charge with
5 a transfer ninth capacitor during a seventh phase, and to make the fifth resulting voltage across the ninth capacitor available during an eighth phase.

31. A device as claimed in claim 30, in which the
10 measuring circuit comprises a reference voltage generator for generating a reference voltage from the fifth resulting voltage.

32. A device as claimed in claim 31, in which the generator is arranged to supply the reference voltage to a
15 comparator of the converter during the second part of the conversion cycle.

33. A device as claimed in claim 1, in which the signal representing the capacitance provides a measure of the liquid
20 crystal material temperature.

34. A device as claimed in claim 33, comprising an arrangement, responsive to the measure of the liquid crystal material temperature, for supplying temperature-compensated
25 drive signals to the cells of the matrix.

FIG. 1
Liquid Crystal Voltage-Transmission Curve

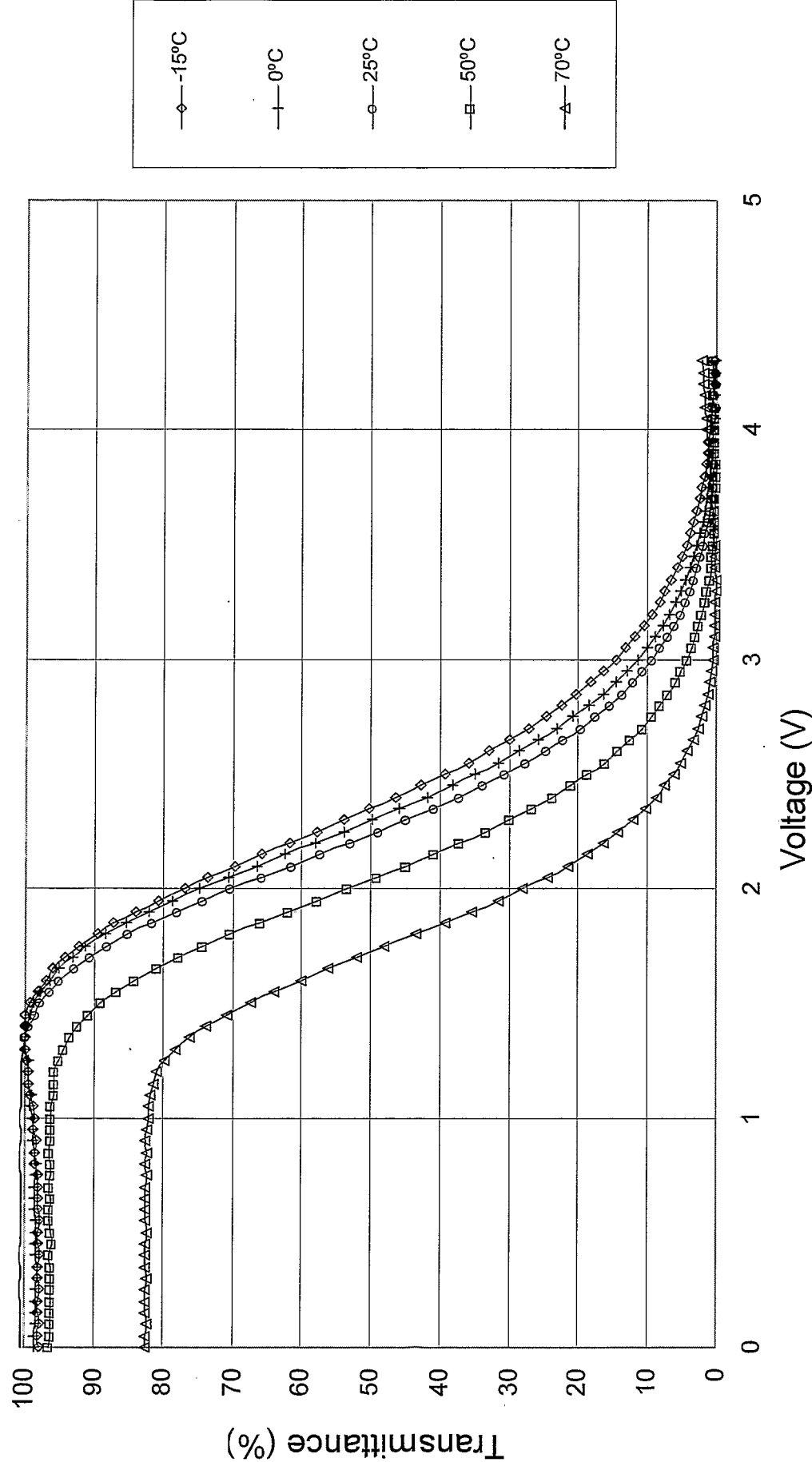
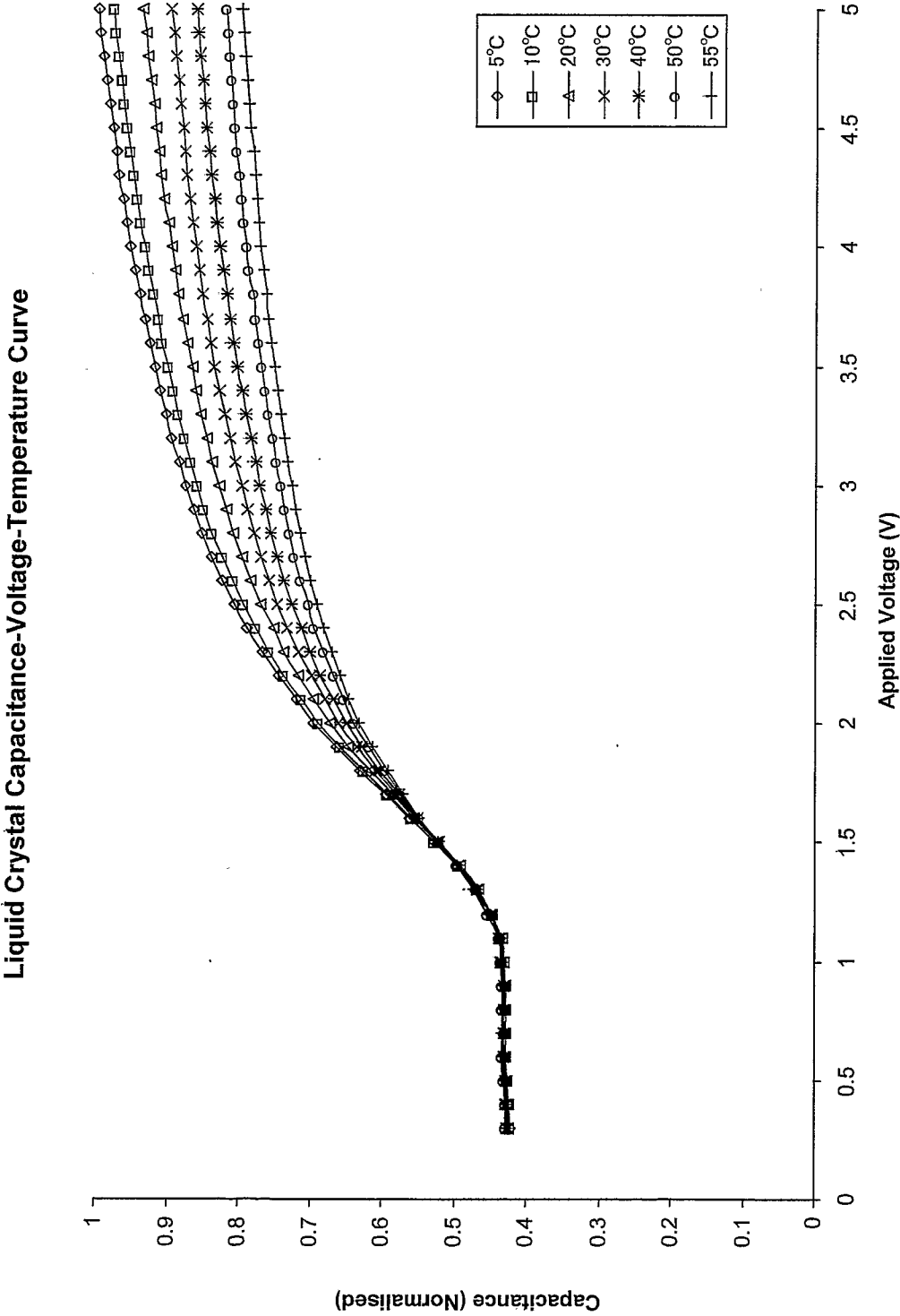


FIG. 2



3 / 2 4

FIG. 3

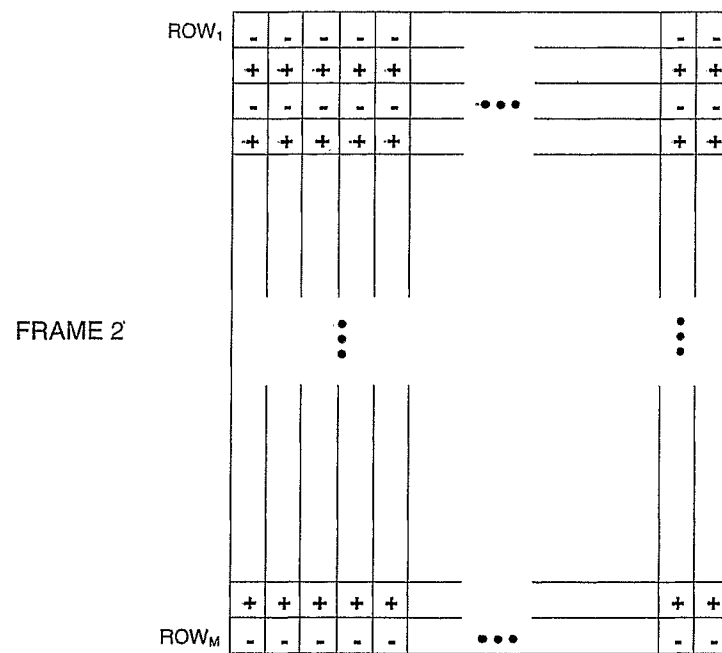
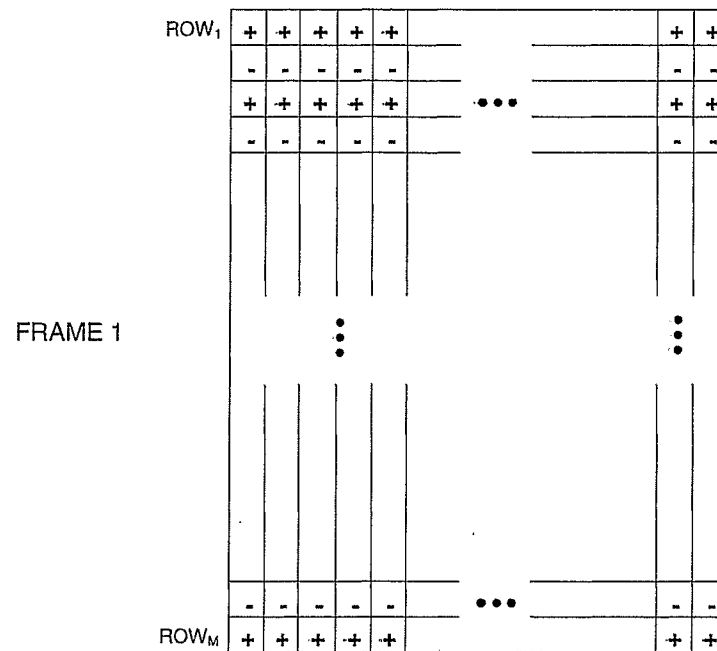
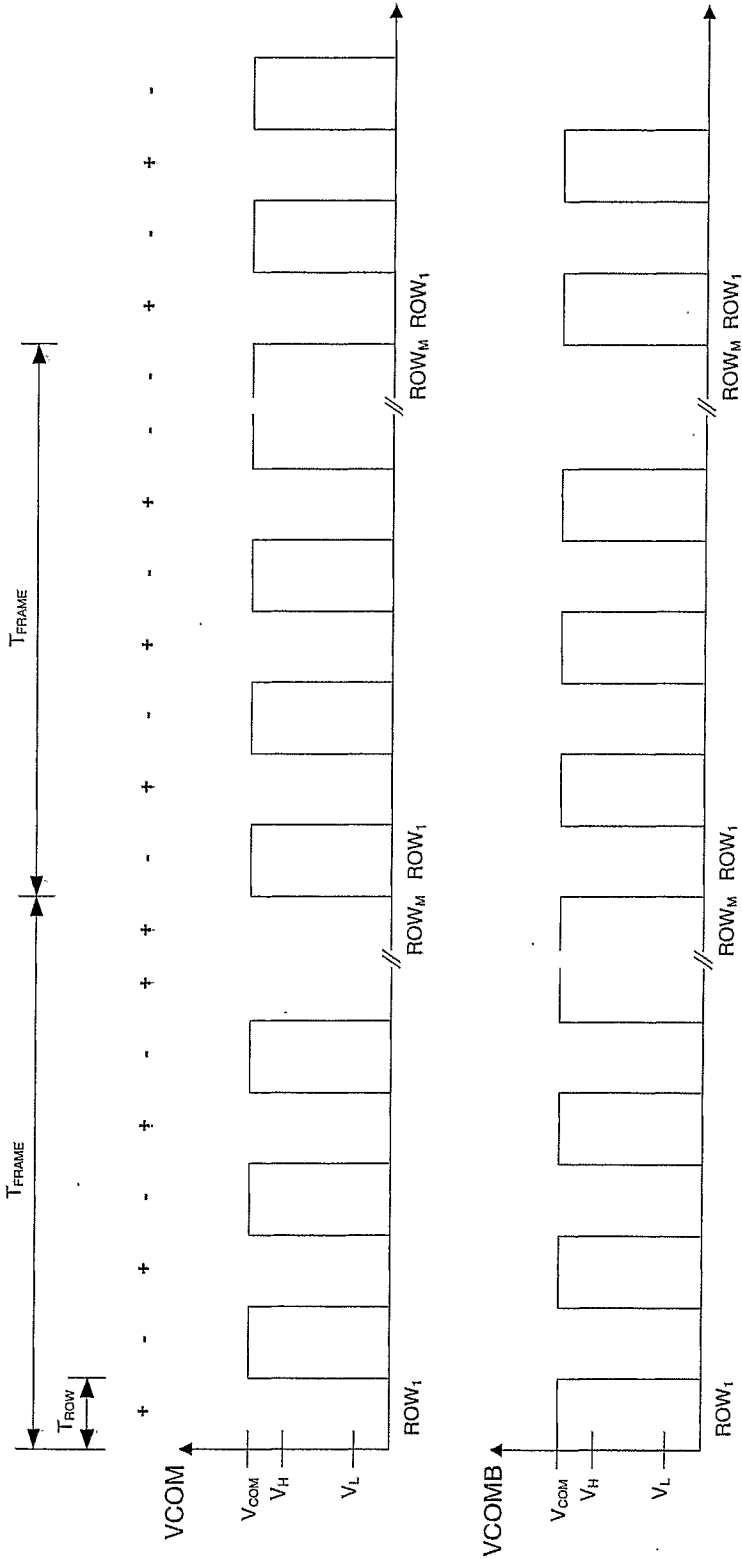


FIG. 4



5/24

FIG. 5

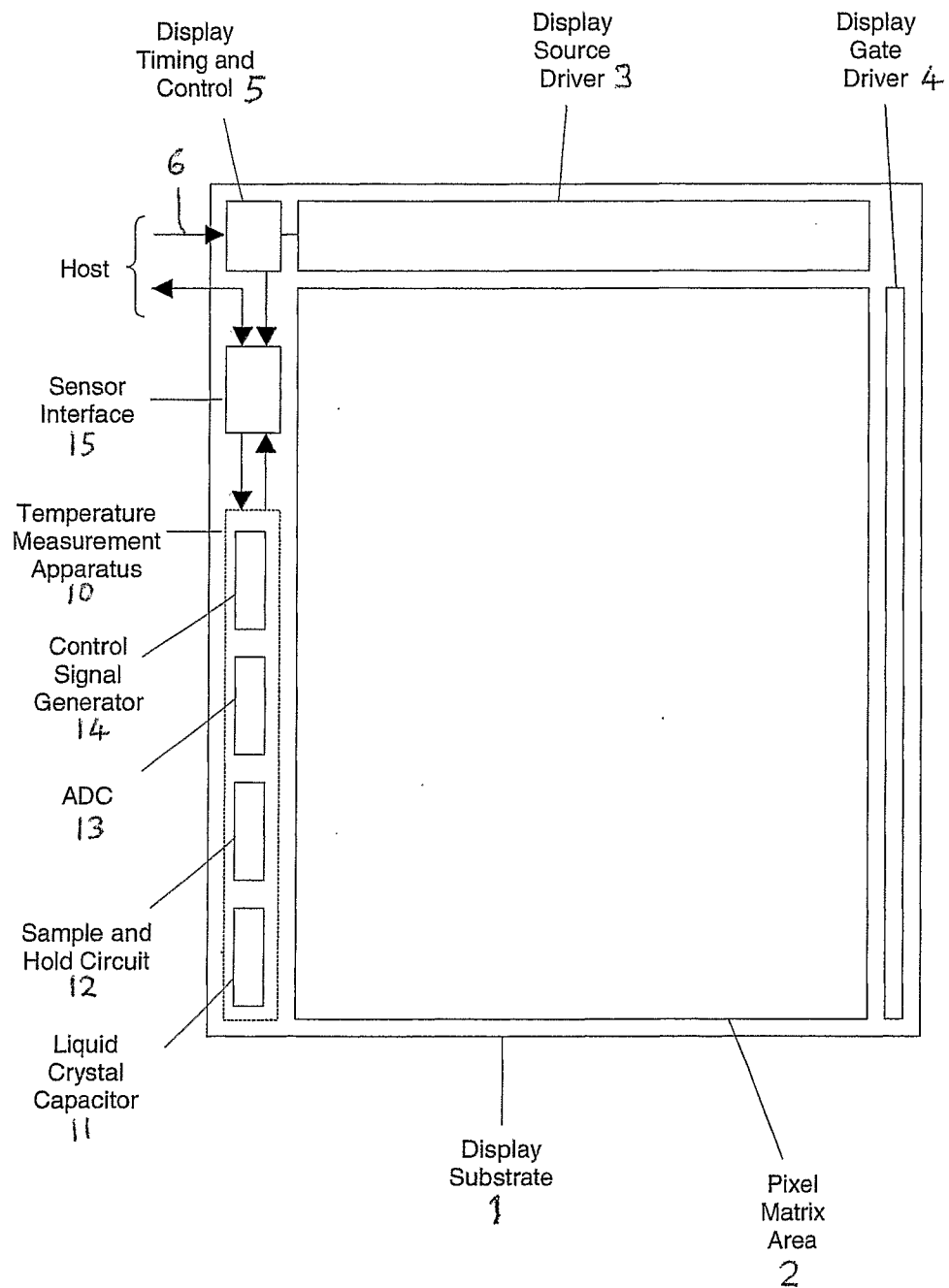


FIG. 6

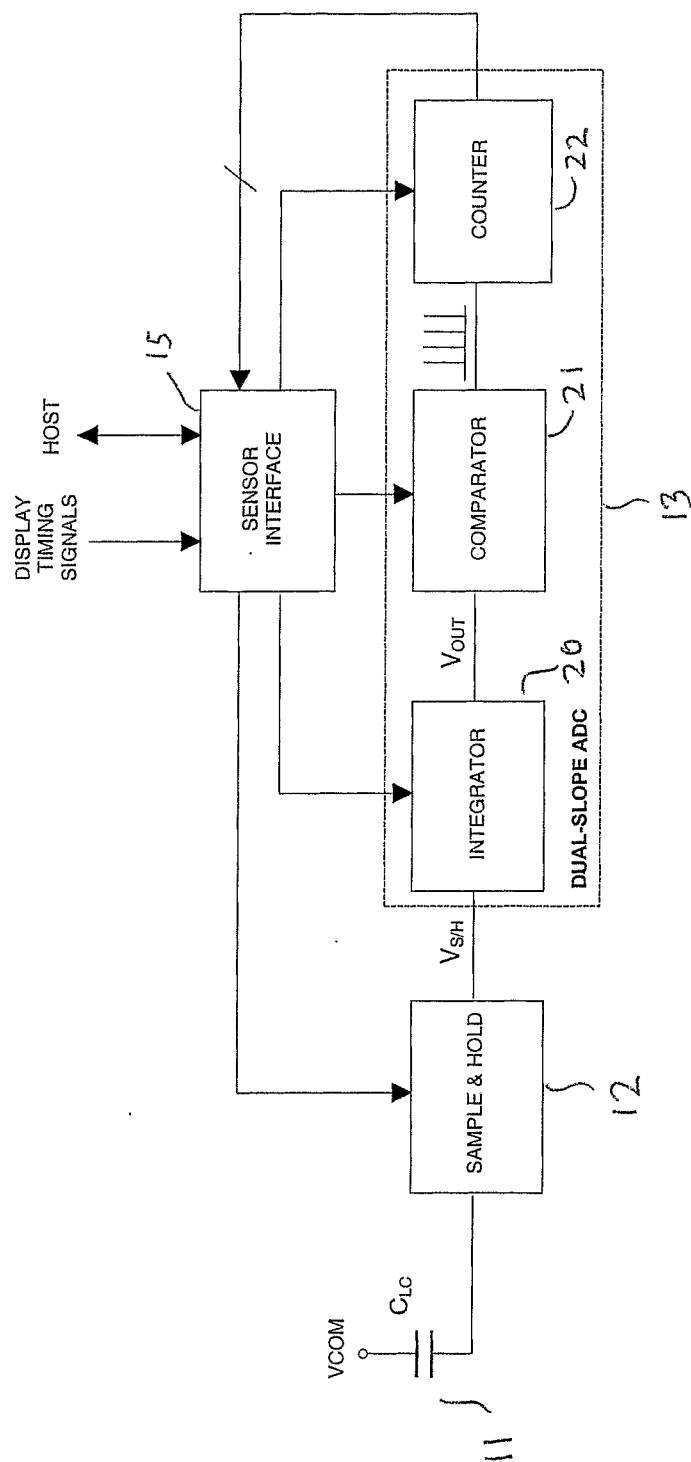


FIG. 7

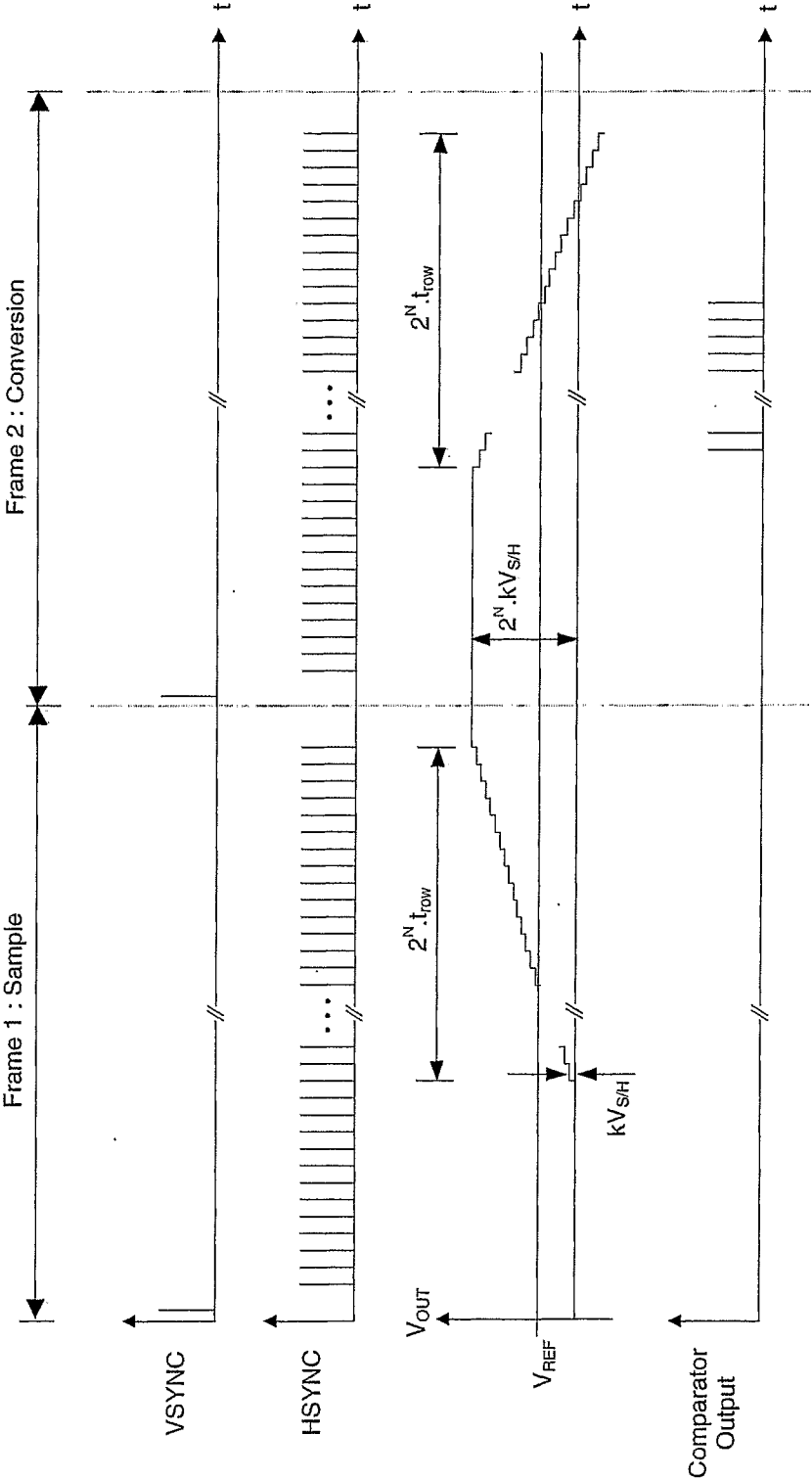
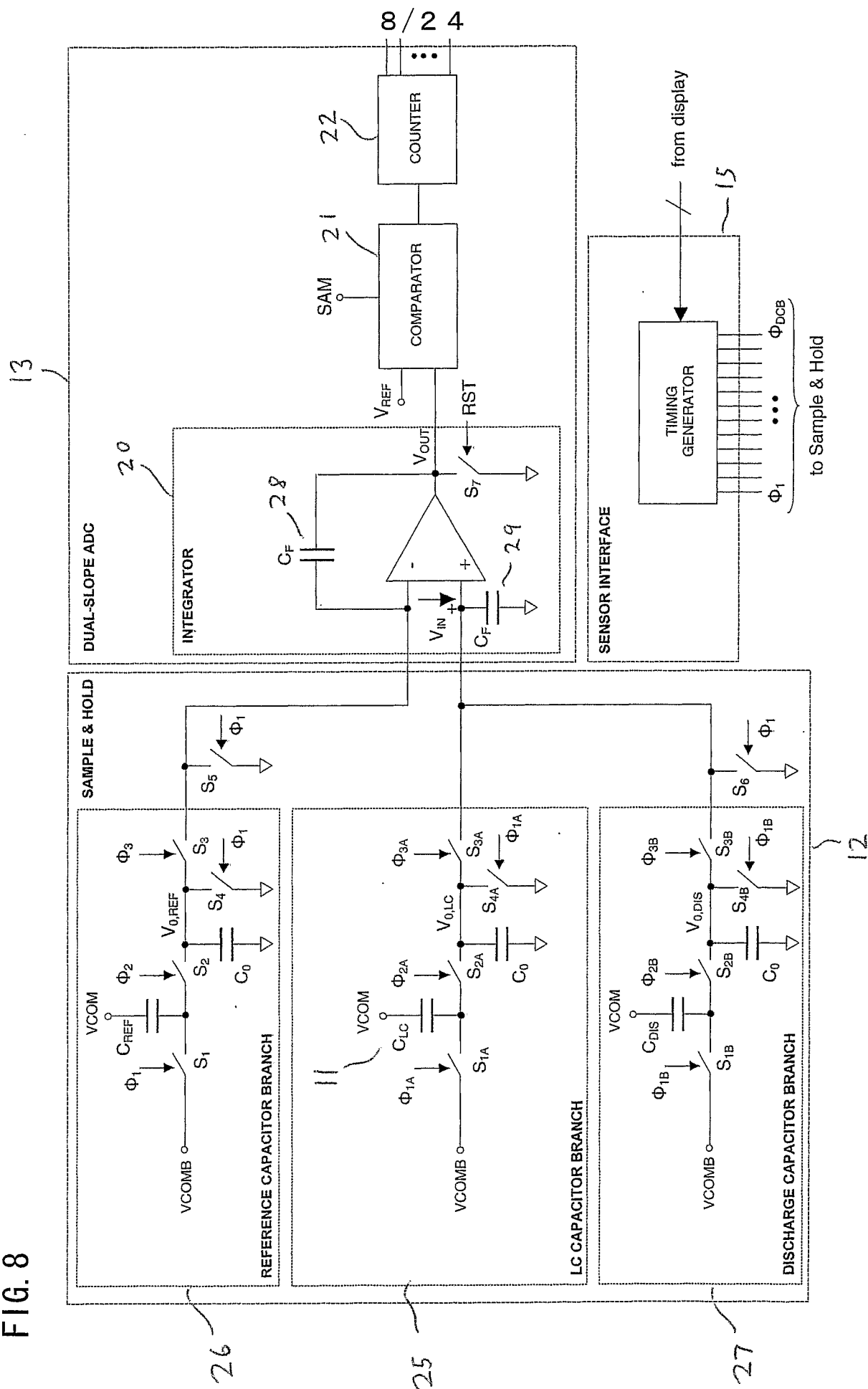
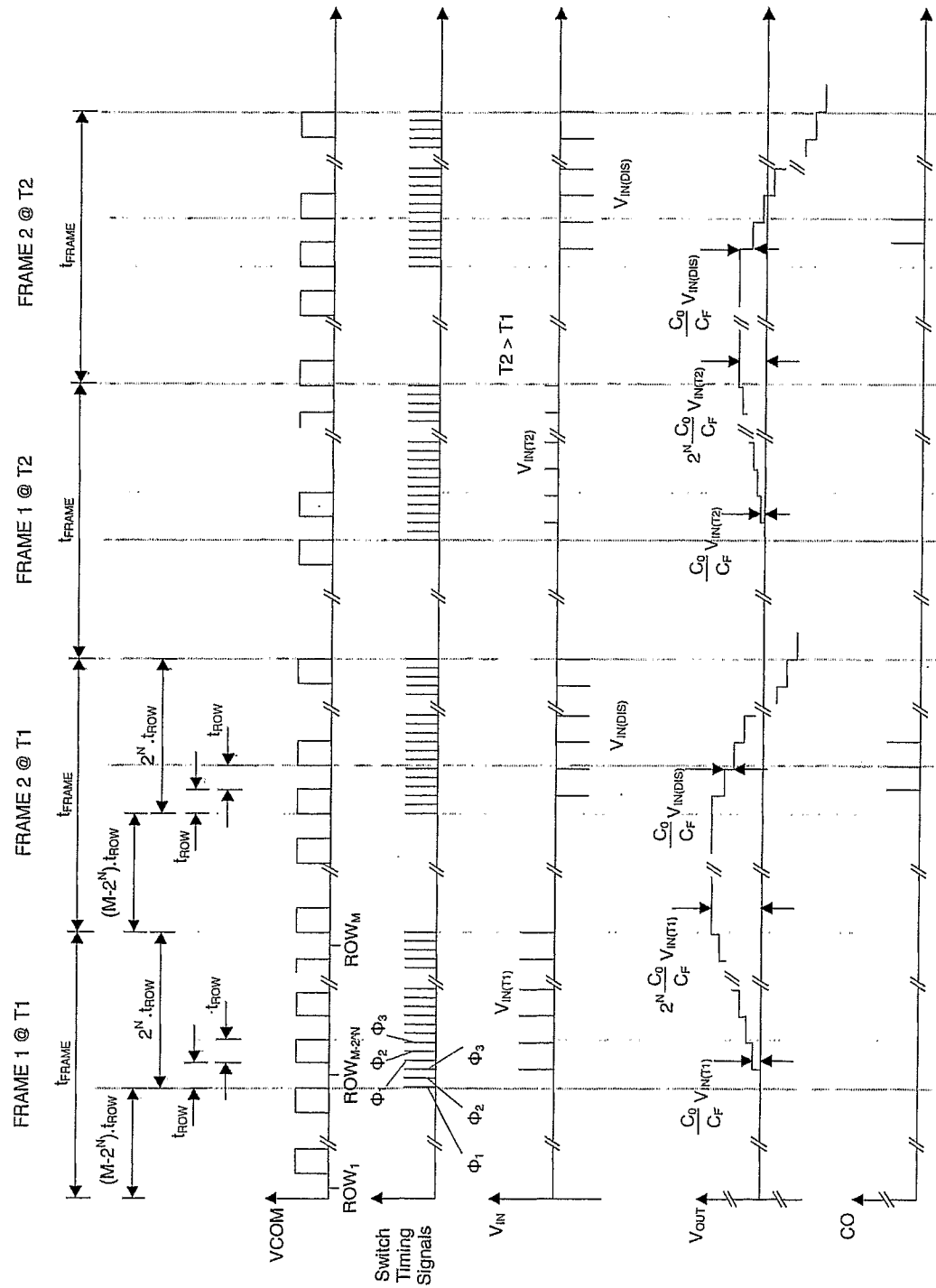


FIG. 8



9/24

FIG. 9



10/24

FIG. 10

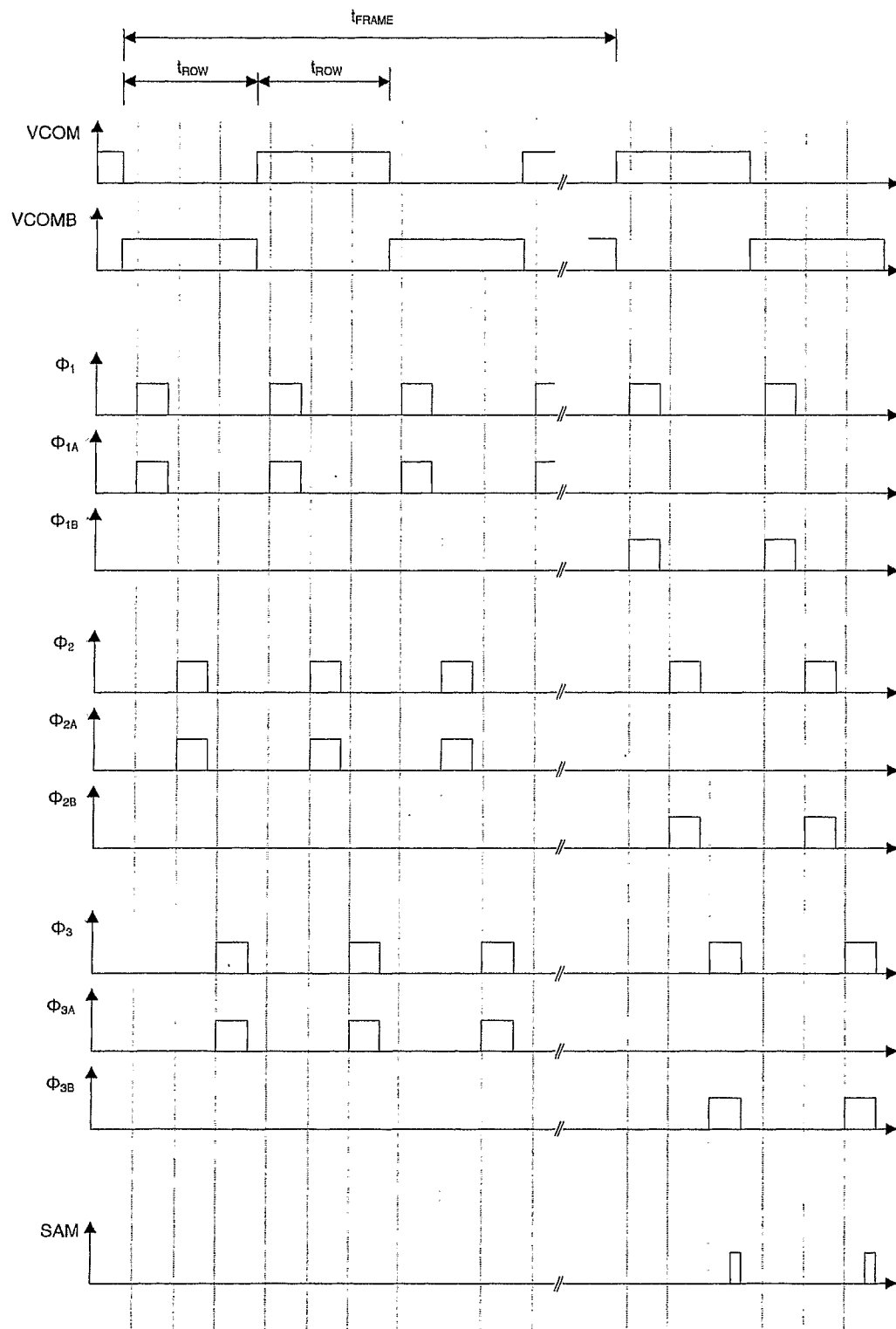


FIG. 11

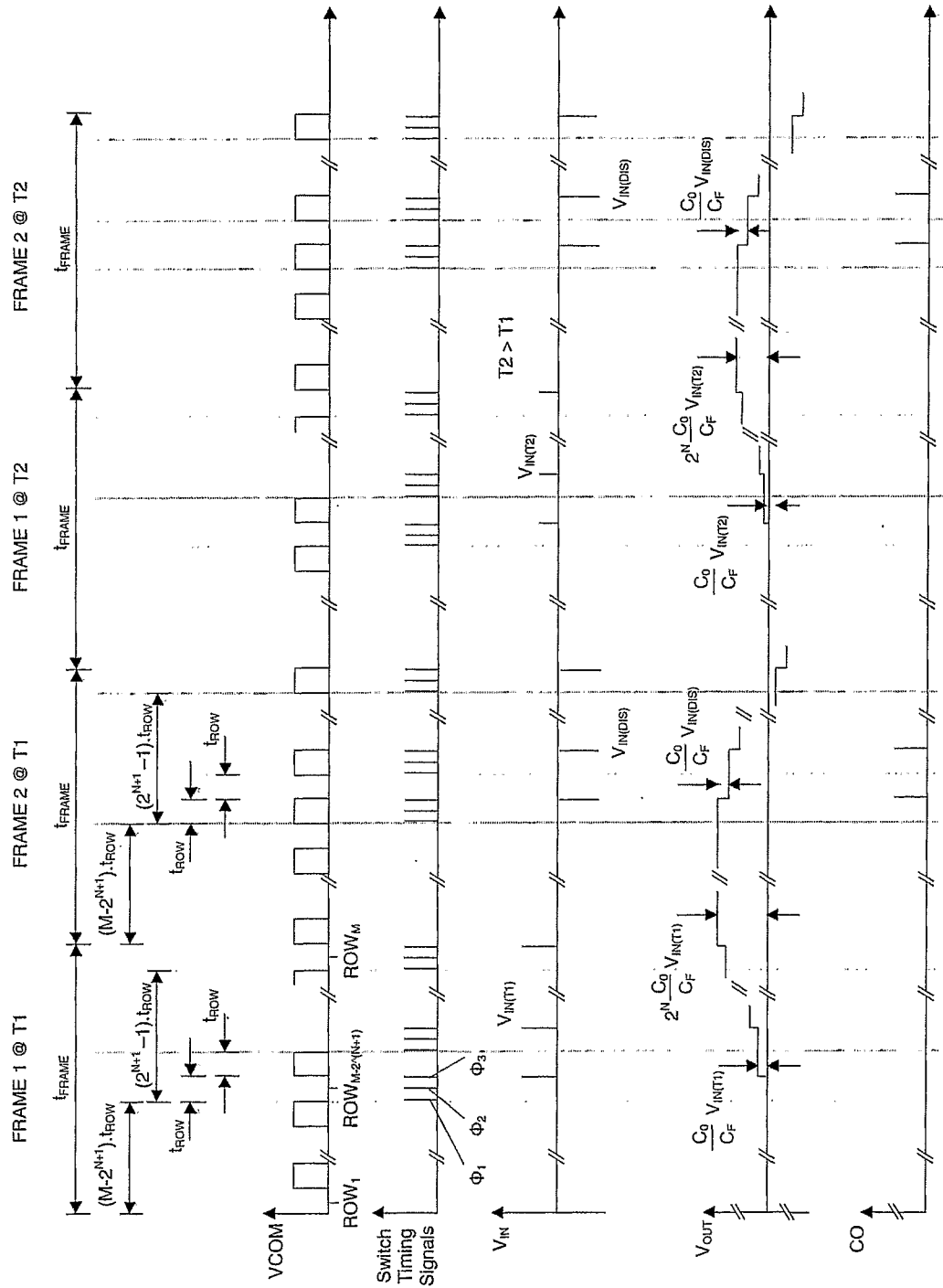


FIG. 12

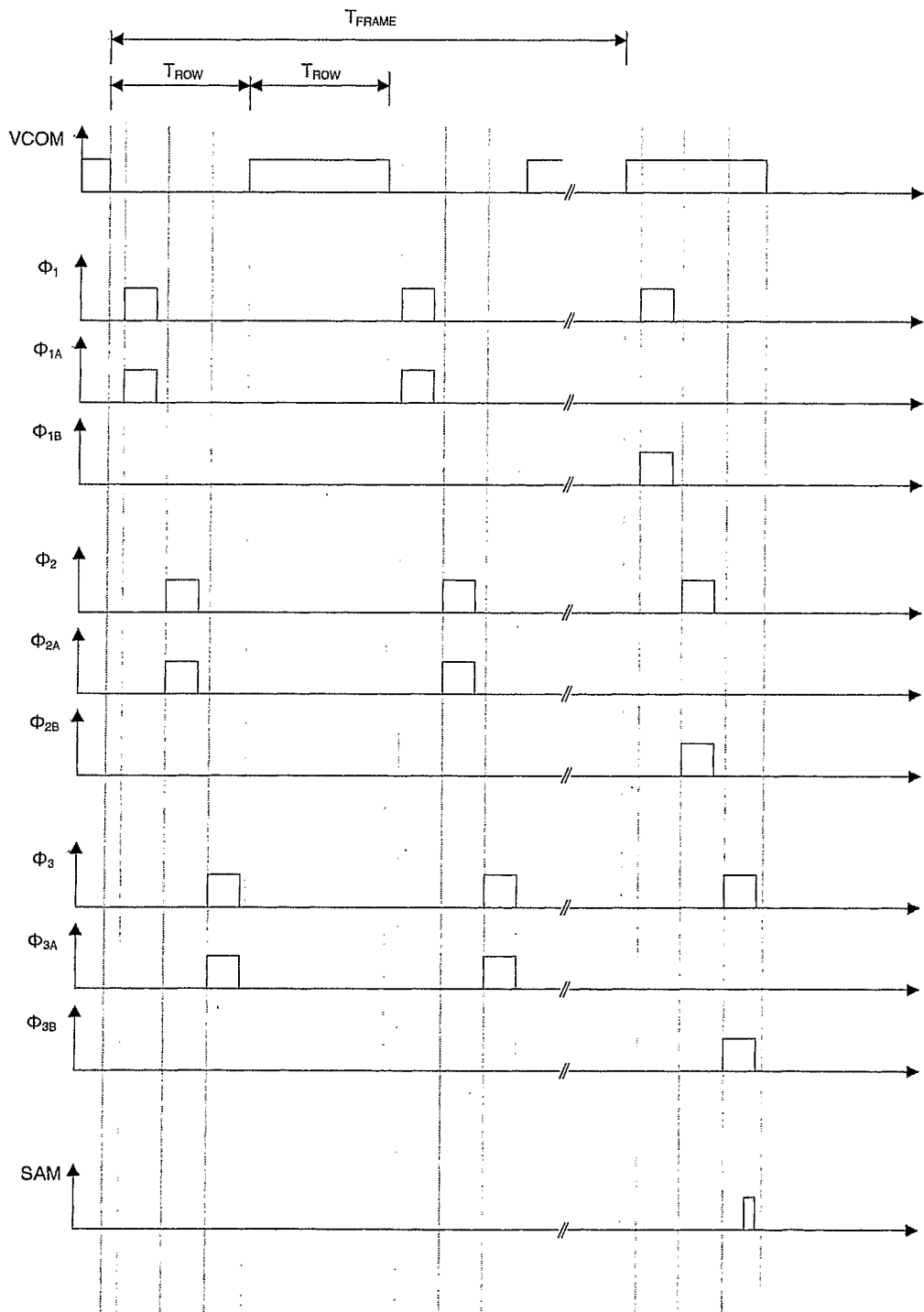


FIG. 13

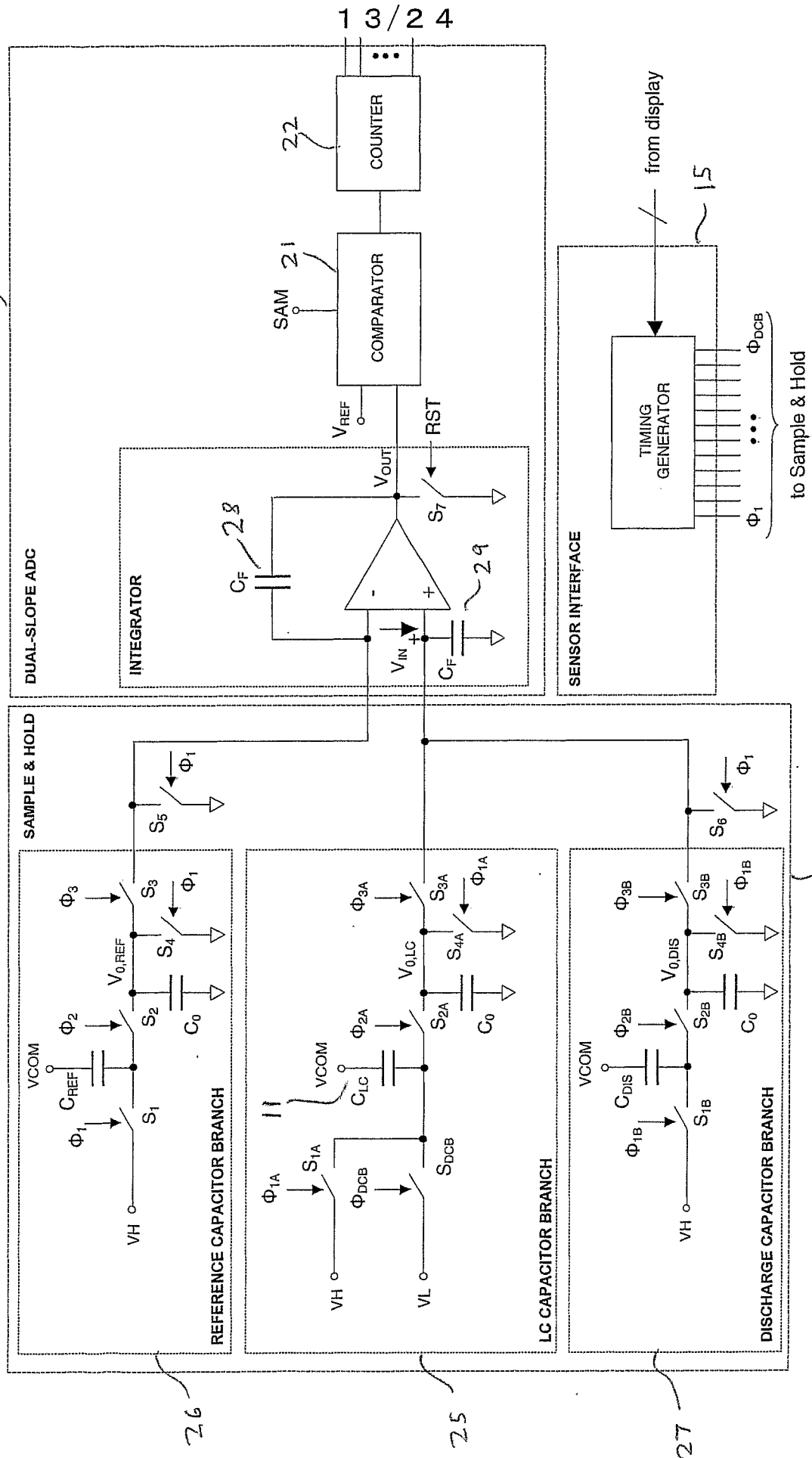


FIG. 14

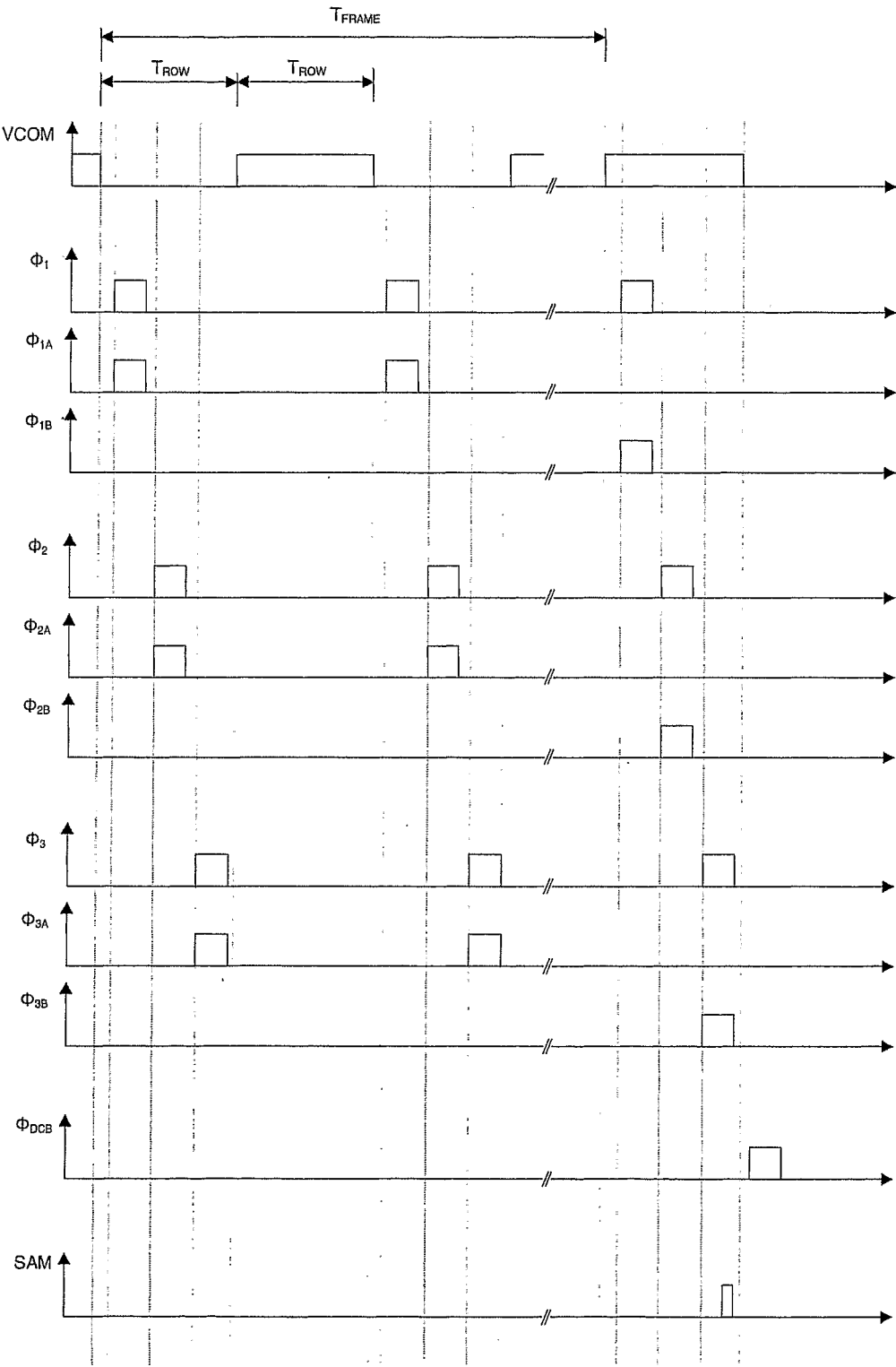


FIG. 15

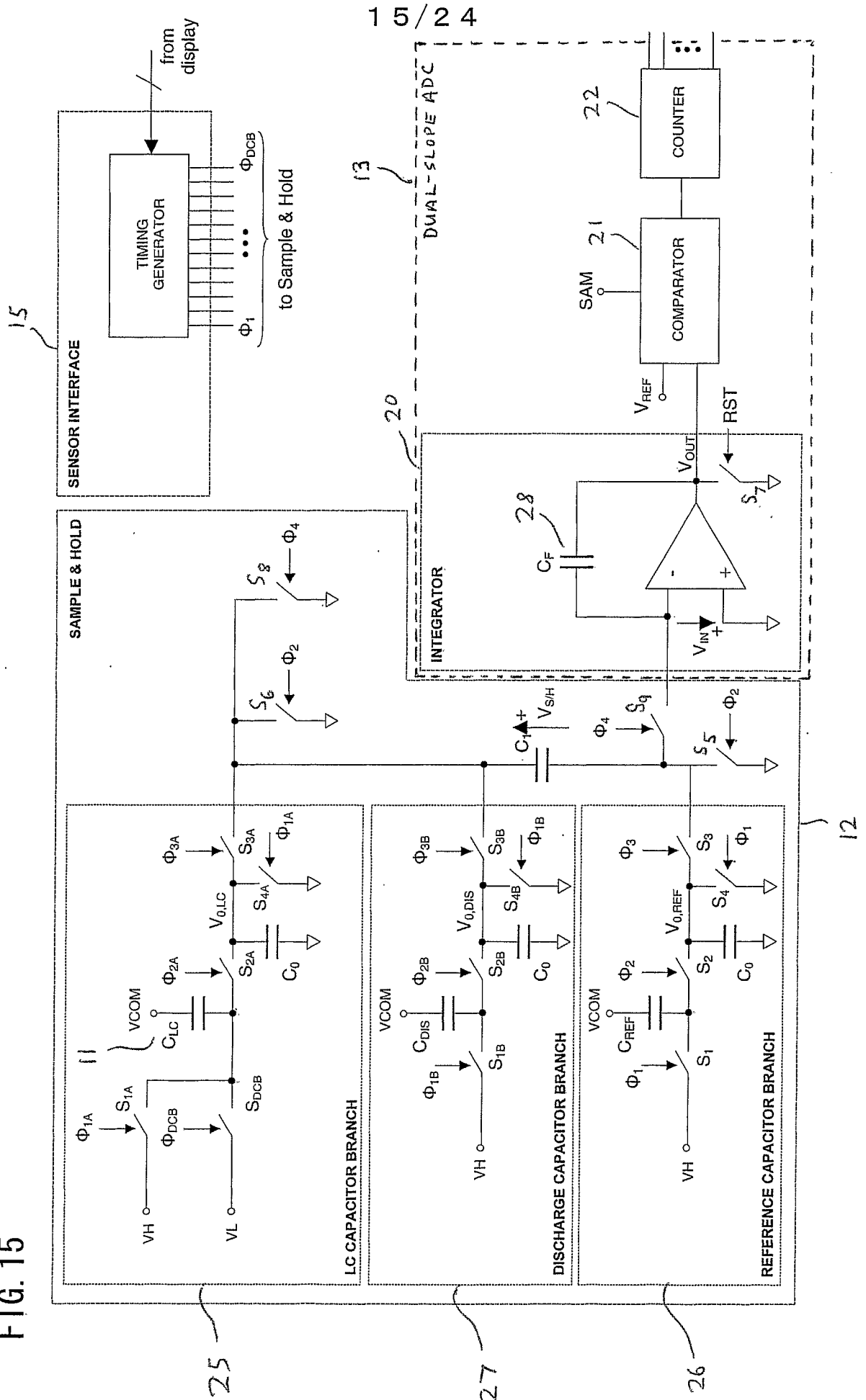
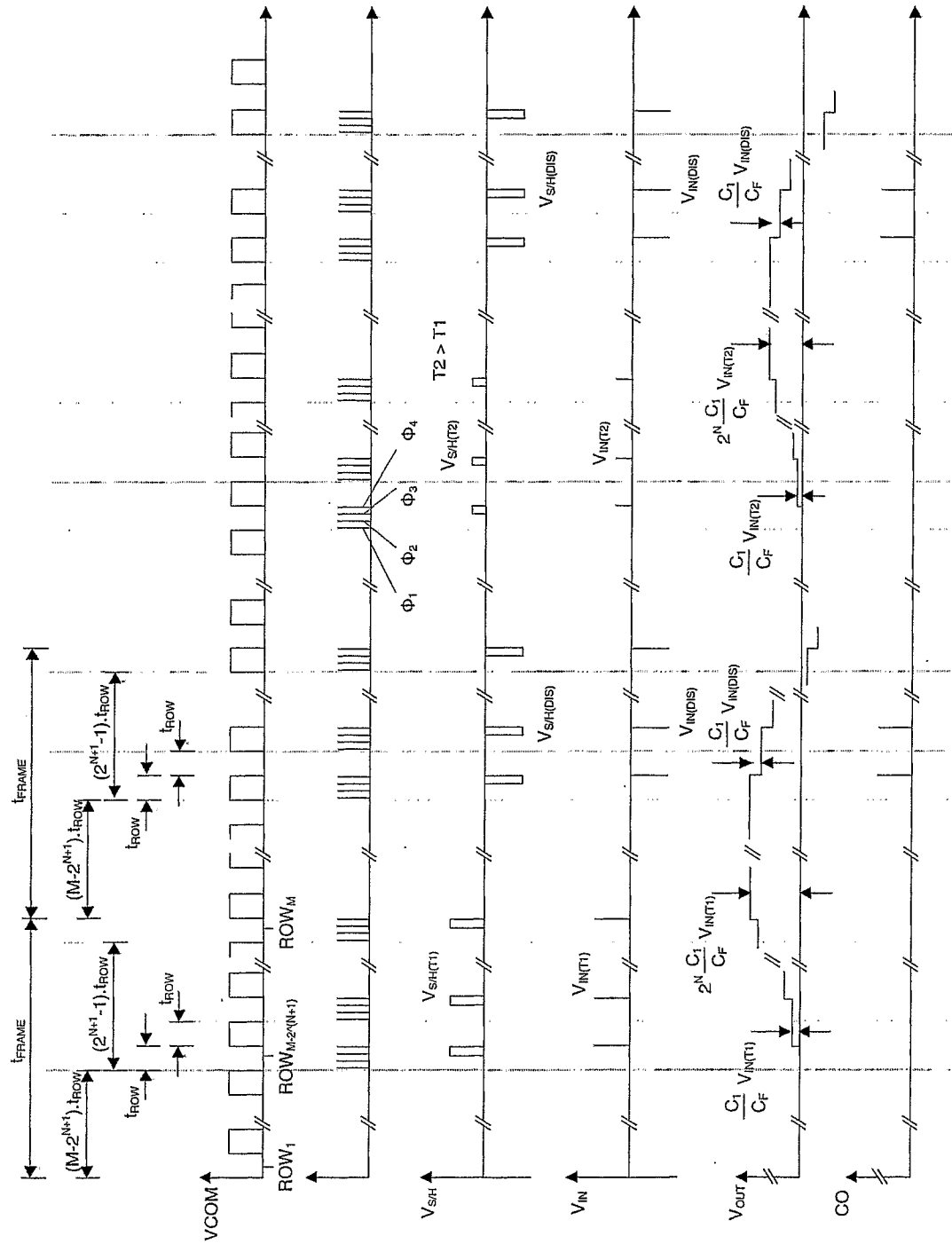


FIG. 16



17/24

FIG. 17

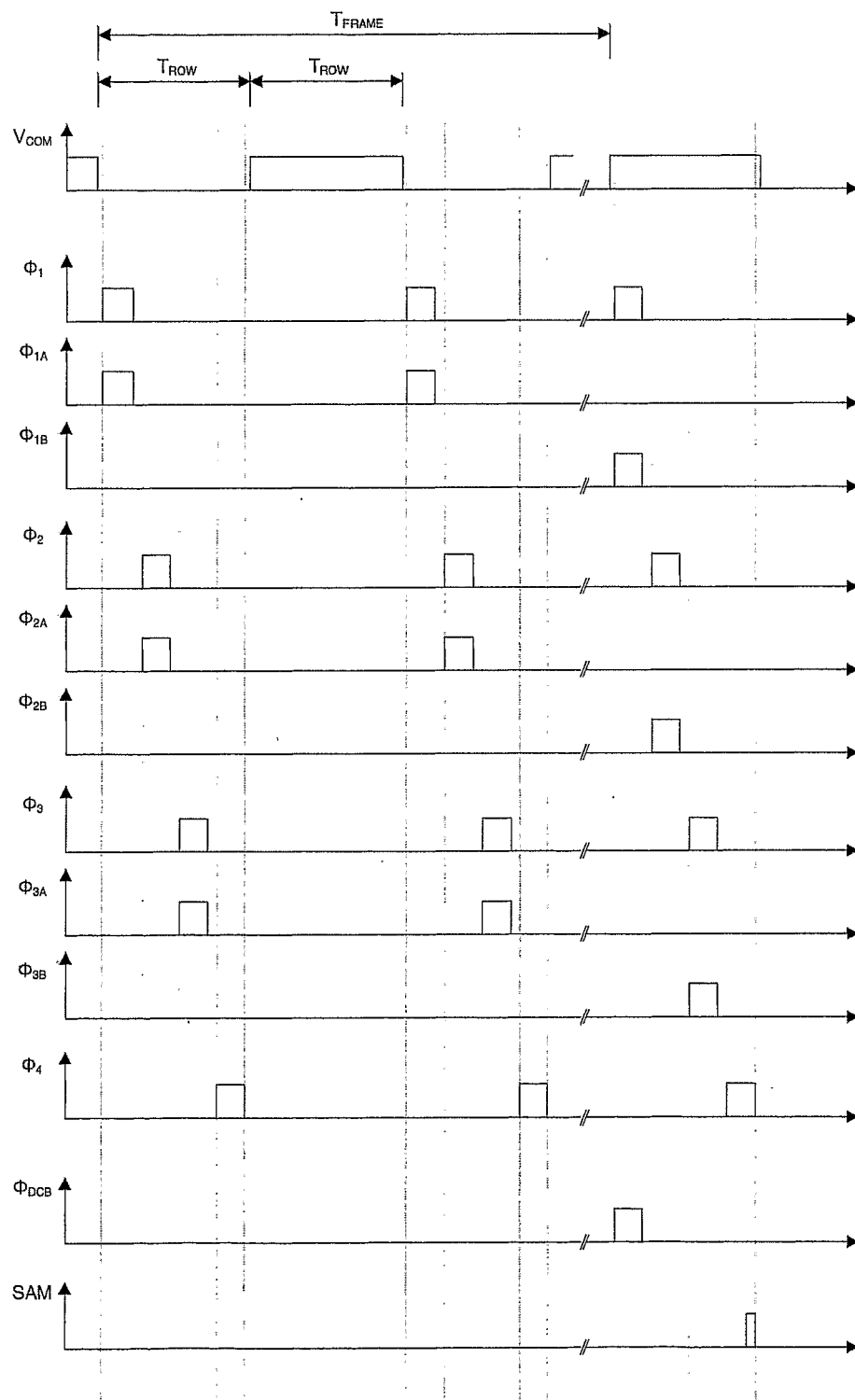
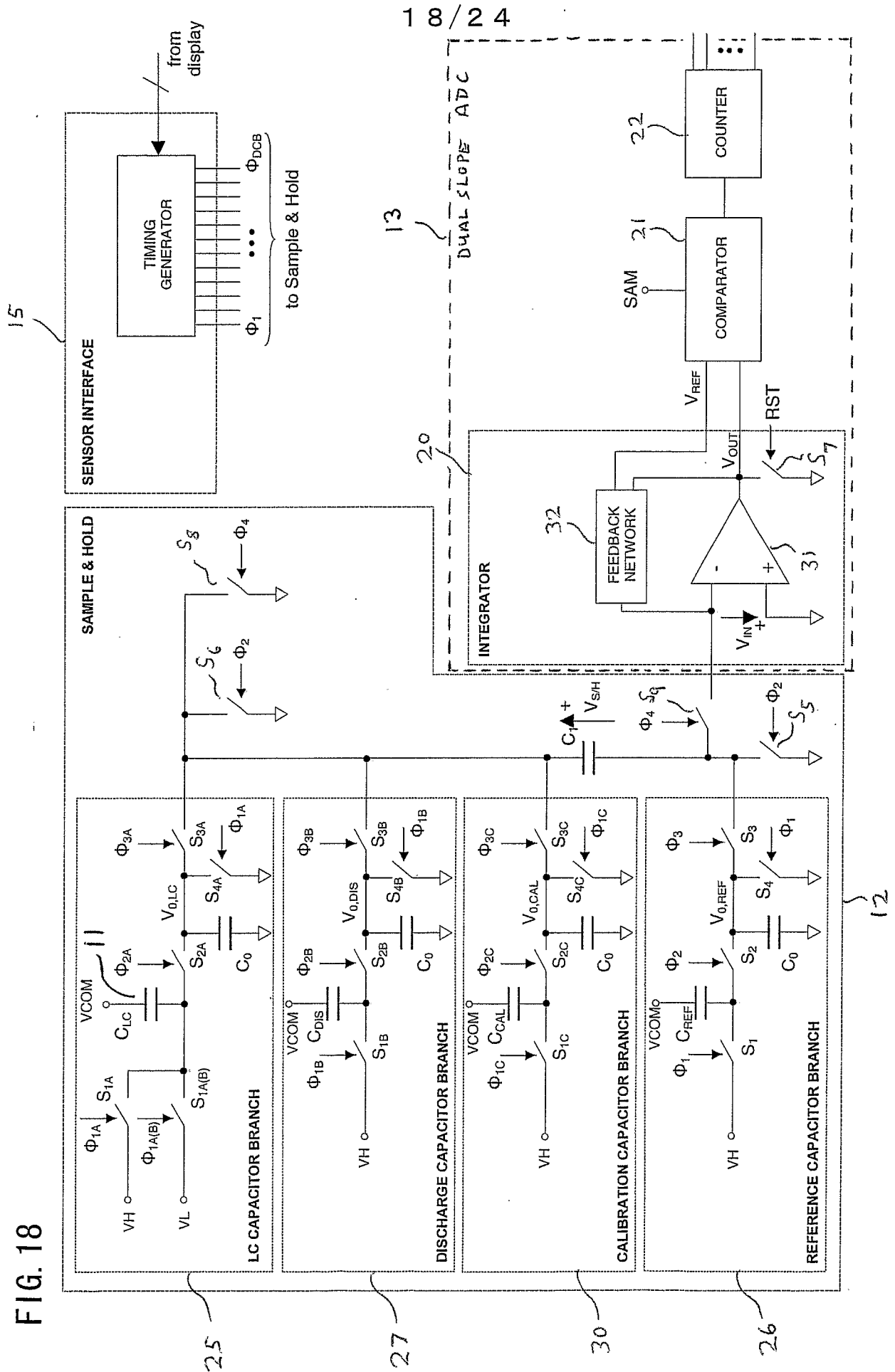


FIG. 18



19/24

FIG. 19

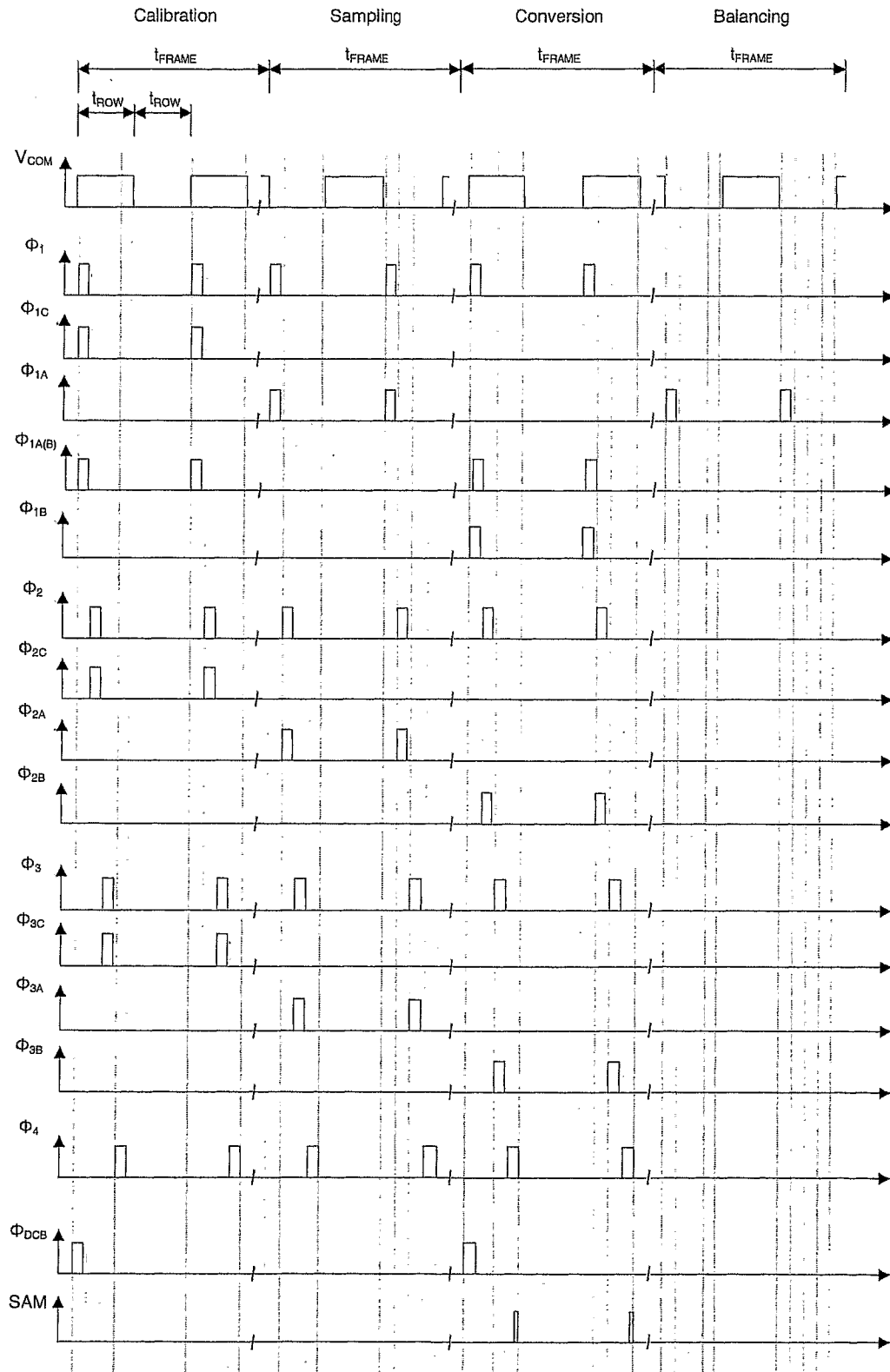


FIG. 20

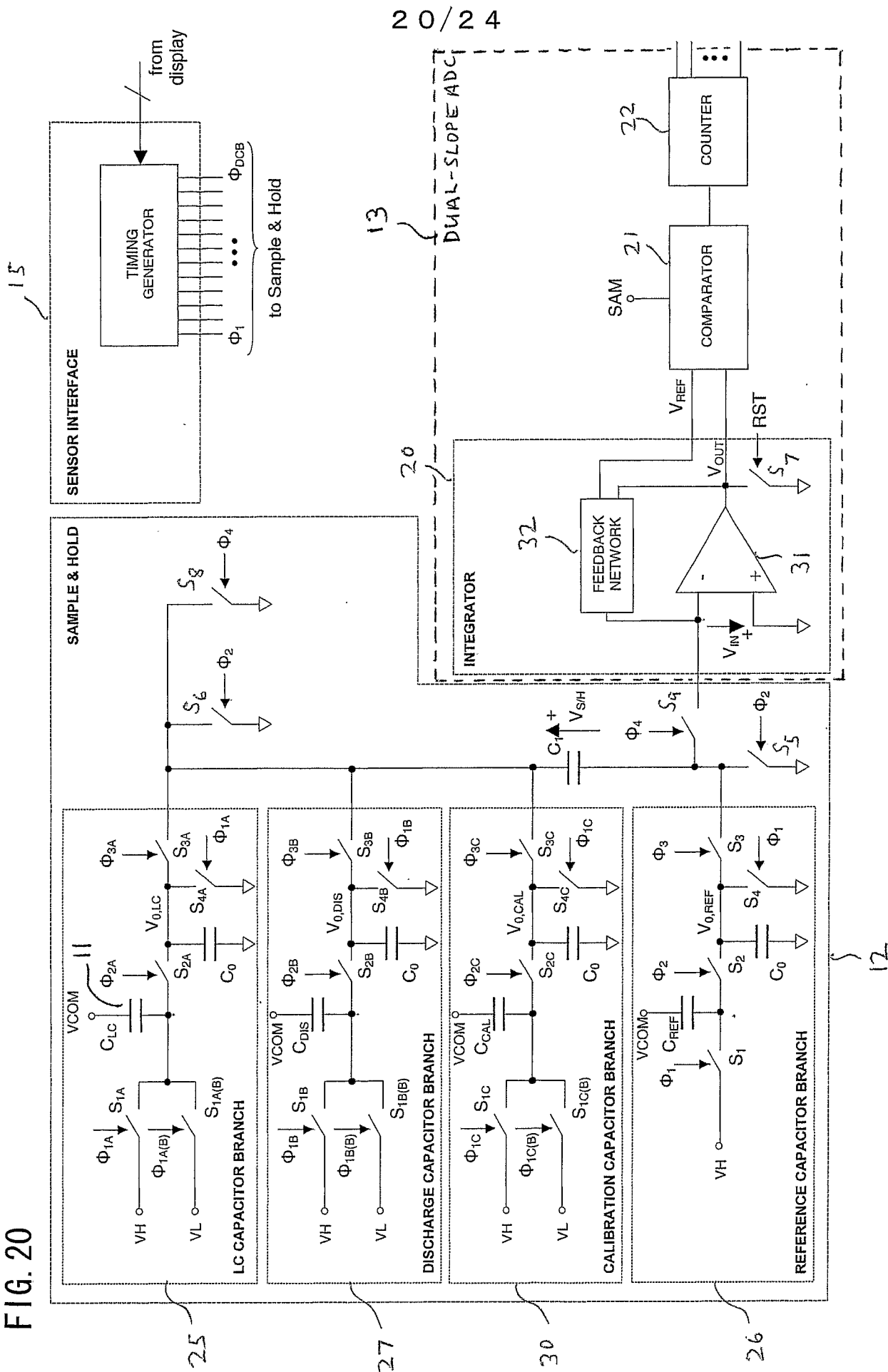
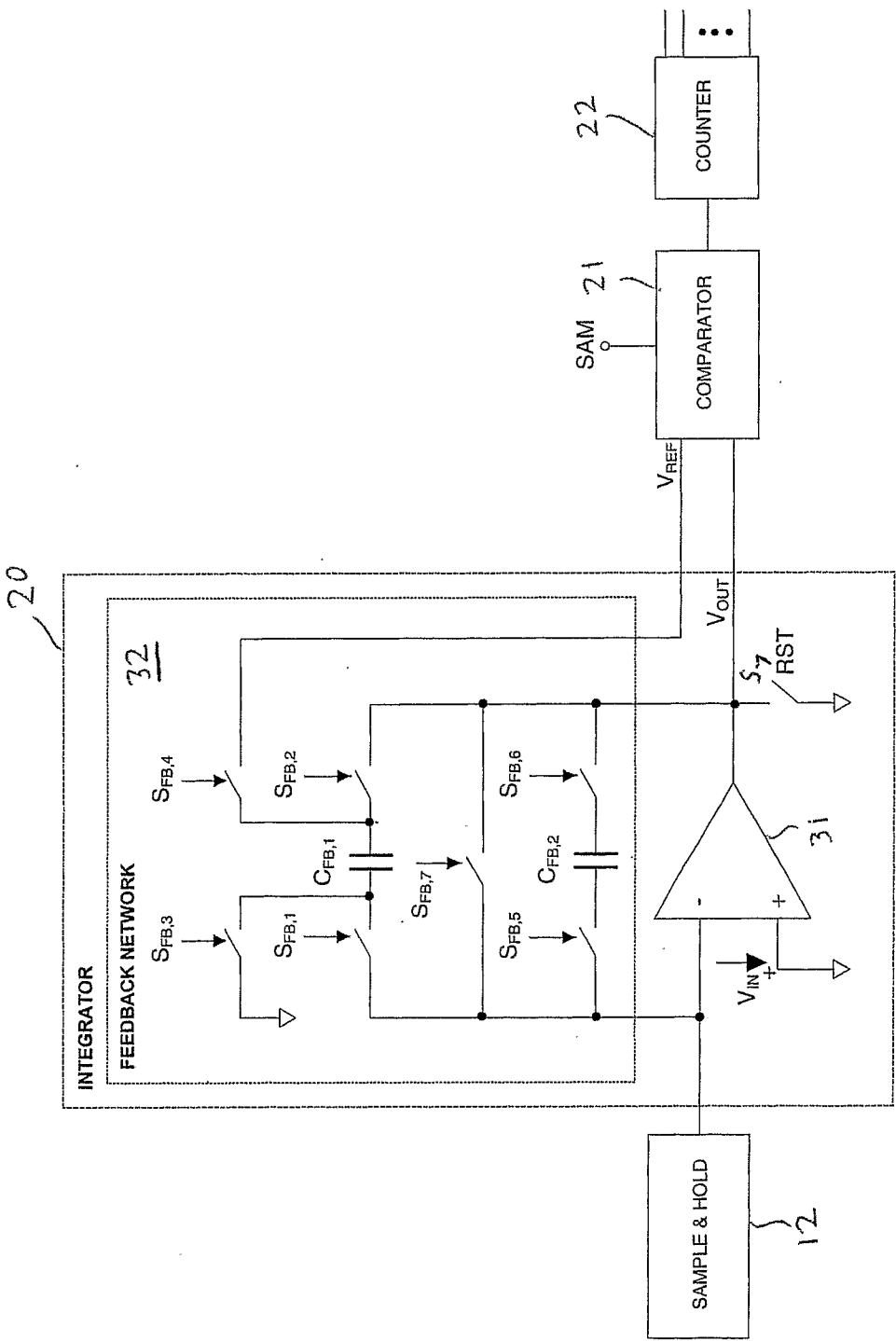


FIG. 21



22/24

FIG. 22

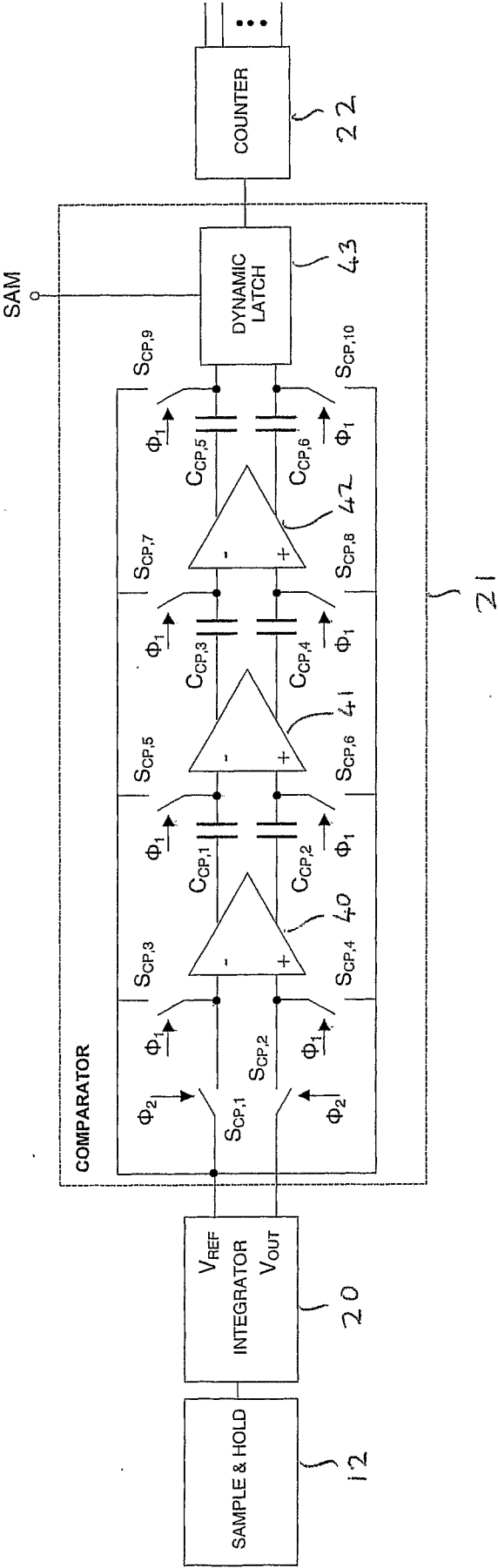
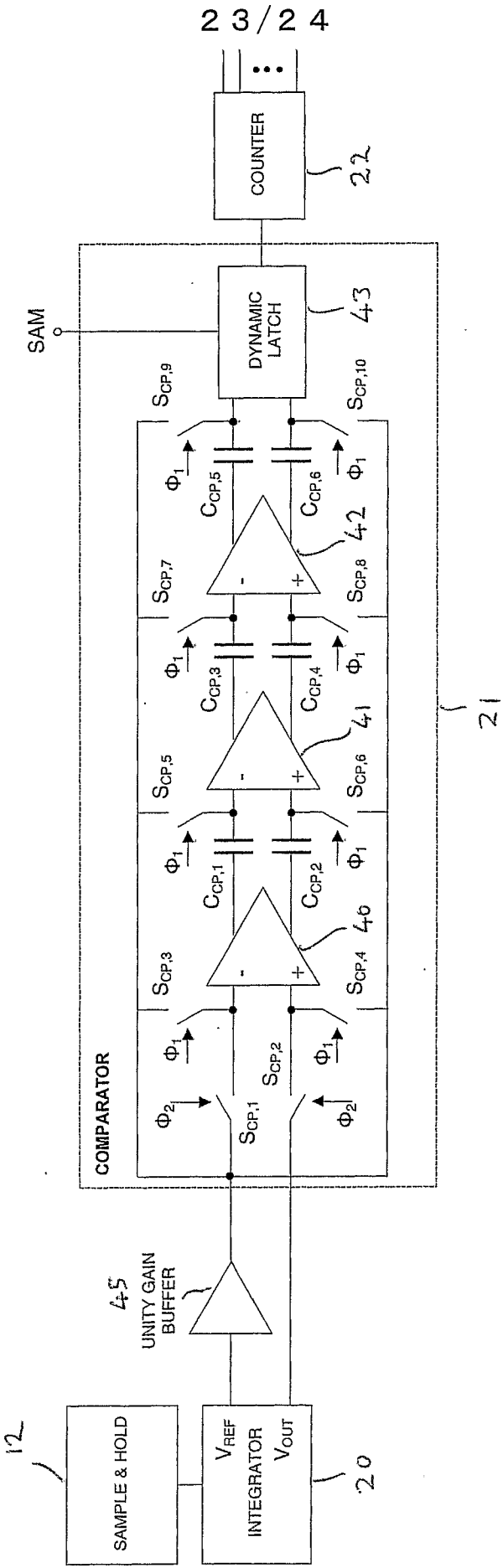
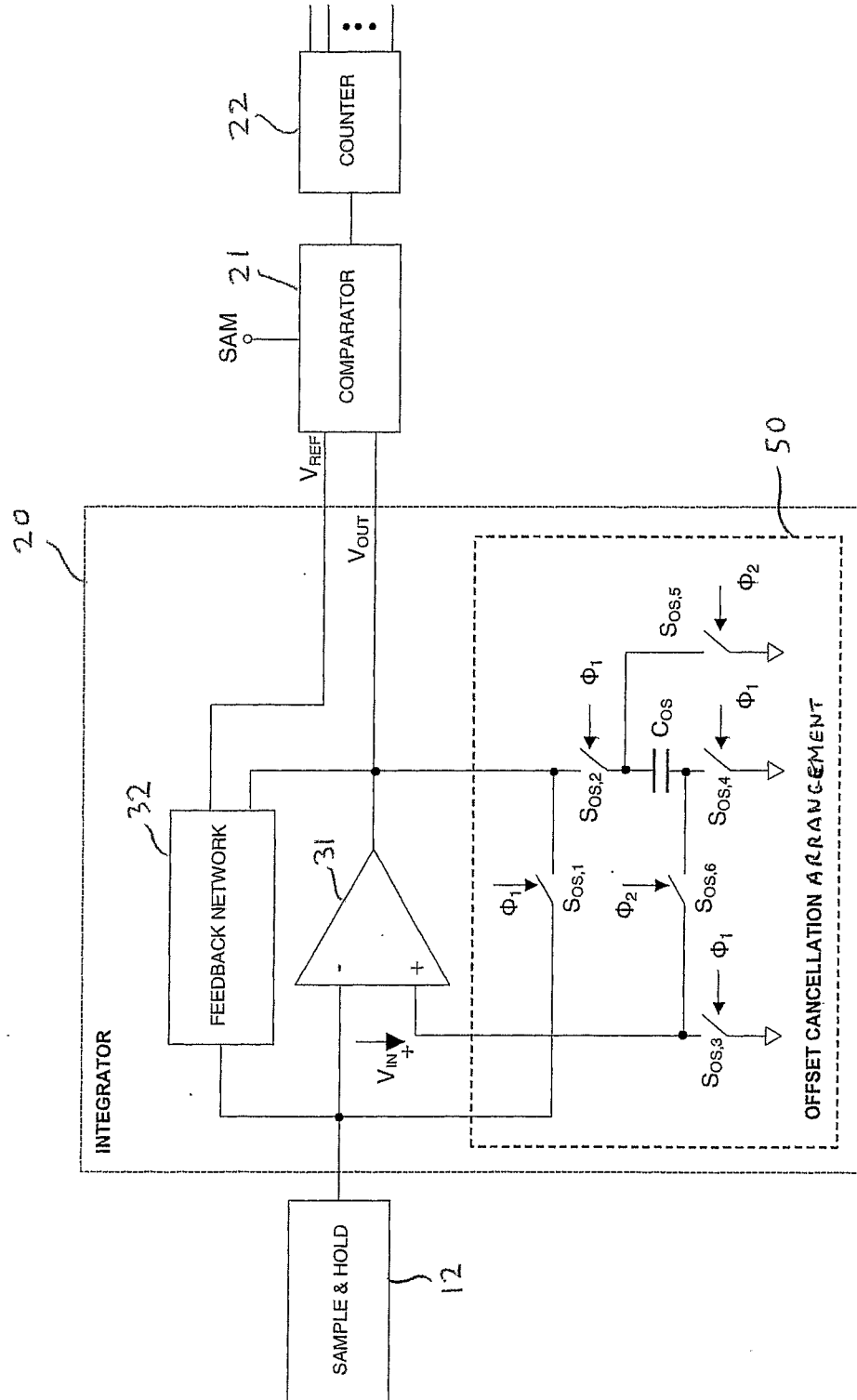


FIG. 23



24/24

FIG. 24



INTERNATIONALSEARCHREPORT

International application No.

PCT/JP2007/057006

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. G02F1/133 (2006.01) i, G09G3/20 (2006.01) i, G09G3/36 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. G02F1/133, G09G3/20, G09G3/36

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2007
 Registered utility model specifications of Japan 1996-2007
 Published registered utility model applications of Japan 1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2003-248209 A (SEIKO EPSON CORPRATION) 2003.09.05, Full text, all drawings (Family: none)	1
Y		2

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

01.06.2007

Date of mailing of the international search report

12.06.2007

Name and mailing address of the ISA/JP

Japan Patent Office

3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer

Koji Fukushima

Telephone No. +81-3-3581-1101 Ext. 3255

21 9018

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

The same or corresponding matters (A) between the inventions of claims Nos. 1-34 are the subject matter of claim 1.

However, after taking the prior art into consideration, it became apparent that the matters(A) were mentioned in a document JP 2003-248209 A (SEIKO EPSON CORPORATION) 2003.09.05. Therefore, the matters (A) makes no contribution over the prior art.

Consequently, there is no same or corresponding "special technical features" which is the expression in the PCT Rule 13.2. Therefore, there is no technical relationship between the inventions of claims Nos. [1, 2], [3, 4, 8, 9], 5, 6, 7, [10-17, 21-23, 26-32], [18-20], 24, 25, and [33, 34].

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.