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INTEGRATED CIRCUIT WITH CLOCK SIGNAL MODIFICATION

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(57) Abstract:
An integrated circuit (100) has a clock signal distribution network (140) for distributing a parent clock pulse signal that is provided through a conductor (102). At the inputs, the clock distribution network (140) is coupled to a clock signal modifying circuit (120) and on the outputs the clock distribution network (140) is coupled to a reference generating circuit (160). The reference generating circuit (160) is arranged to provide the clock signal modifying circuit (120) with a direct current voltage that is proportional to the duty cycle of the clock pulse signal that is distributed through the clock distribution network (140). The clock signal modifying circuit (120) is arranged to alter the duty cycle of the incoming parent clock pulse signal responsive to the direct current voltage. The arrangement implements a feedback mechanism for reducing deviations from a 50% duty cycle of a clock pulse signal distributed through the clock distribution network (140).
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.
Integrated circuit with clock signal modification

The invention relates to an integrated circuit with clock signal modification.

The ongoing downscaling of semiconductors technologies has led to a dramatic increase of the complexity of an integrated circuit (IC). For instance, nowadays integrated circuits typically contain hundreds of millions of transistors that are being operated at frequencies of a GigaHertz (GHz) order. However, a downside of this increase in performance of the IC is the increase in the associated power consumption, which for instance is detrimental to the lifetime of batteries of battery-powered devices including ICs. A large part of this power is being consumed during the generation and propagation of the clock signals. Such signals typically have a rising or falling edge that is used to trigger the switching behavior on the IC.

In order to reduce the power consumption associated with the generation and propagation of the clock signal, a lot of effort is being put in developing circuits which are capable of switching at a double frequency by utilizing both edges of the clock signal, e.g. dual-edge triggering. Consequently, such circuits consume only roughly 50% of the energy of a circuit using a single clock edge for its switching behavior. Unfortunately, the use of both edges of the clock signals poses additional constraints on the shape of the clock signal. In order to assure the correct switching behavior on the IC and to maximize the performance, the time periods between two contiguous edges, should be approximately the same, e.g. its duty cycle should be around 50%. Although the generation of such a clock signal is relatively simple, the propagation of the 50% duty cycle signal through a clock signal distribution network can lead to a deformation of the signal at the output end of the clock signal distribution network, which can be introduced by variations in the IC technology process parameters.

In the Japanese patent application JP 2001024487 a correction to this deviation is provided; clock signal distribution network output signal is delayed, evaluated and subsequently turned into a reference signal by a reference generating circuit having a plurality of delay circuits and having a phase comparator circuit. The amount of introduced
delay depends on the shape of the output signal. This reference signal is then compared with
an inverted clock signal distribution network output signal by a second phase comparator in
the clock signal modifying circuit, which produces an output signal that is processed by the
clock signal modifying signal by a further delay circuit in combination with a narrow pulse
signal that is generated in a differential circuit. The outputs of the differential circuit and the
further delay circuit are fed to an R,S latch for generating the desired clock signal
characteristics.

The above described solution has the disadvantage that the required hardware
arrangement for generating a 50% duty cycle clock signal at the outputs of the clock signal
distribution network is very complex, which consequently leads to the introduction of
relatively large amounts of dedicated hardware to implement the desired functionality, which
adds to the total silicon real estate and the associated cost of the IC.

Inter alia, it is an object of the invention to provide an IC of the kind described
in the opening paragraph that provides an improved duty cycle at the output of the clock
signal distribution network requiring only limited hardware resources.

The invention is defined by the independent claims. Advantageous
embodiments are defined in the dependent claims.

The invention is based on the realization that, in contrast to the solution
presented in JP 2001024487, where the edges of the clock pulse signal were analyzed and
mapped on a reference signal to evaluate the shape of the duty cycle of the signal, the area of
the clock pulse can provide the same information, and can be correlated to a discrete direct
current (DC) voltage value, which, as a reference, can be used to drive the signal generating
means in order to obtain a desired duty cycle at the outputs of the clock signal distribution
network. This has the advantage that no comparison has to be made between a collected
output clock signal and a generated delayed clock signal, which drastically simplifies the
required hardware for implementing the duty cycle control circuitry and reduces the amount
of hardware required for this implementation. In addition, by using a reference in the form of
a DC voltage instead of a pulse signal, no comparison between the reference and a generated
clock signal has to be made in the clock signal modifying means, thus also simplifying the
required functionality and reducing the hardware resources of the clock signal modifying
means.

It is an advantage if the signal integration means comprise an inverter loaded
by a capacitance. This results in a very simple implementation of a signal integration means,
which will produce a reference of larger than half of the supply voltage, e.g. \(> \frac{V_{dd}}{2}\), when the duty cycle is less than 50%, and vice versa.

The direct current voltage can be used to control the control terminals of a set of transistors of a logic circuit. Combined with the use of a parent clock signal to control the control terminals of a second set of transistors, a logic circuit can be designed that outputs a clock signal that leads to the desired duty cycle characteristics at the outputs of the clock signal distribution network, and wherein the transistors being controlled by the reference modulate the parent clock signal into the intended shape.

Claim 4 has the advantage that a very simple logic circuit, having a minimum of only four transistors, is obtained.

It is an advantage if the output of the logic circuit is coupled to the output of the signal modifying means via a further inverter. The use of such an arrangement enables the use of a simple inverting integrator as the reference generating means, which contributes to the overall reduction of required hardware.

The invention is described in more detail and by way of non-limiting examples with reference to the accompanying drawings, wherein:

Fig. 1 depicts an embodiment of the integrated circuit according to the present invention;

Fig. 2 depicts an embodiment of a part of the integrated circuit according to the present invention;

Fig. 3 depicts an embodiment of another part of the integrated circuit according to the present invention; and

Fig. 4 shows a graph of a simulation result of the effect of the present invention on the duty cycle of an integrated circuit.

In Fig. 1, integrated circuit 100 has a clock signal generator not shown for generating a parent clock pulse signal. The parent clock pulse signal is fed to a clock signal modifying circuit 120 through signal conductor 102, which modifies the parent clock pulse signal into a modified clock pulse signal. The modified clock pulse signal is outputted to a clock distribution network 140 through conductor 104. The clock distribution network 140 is, by way of example, depicted as a balanced clock tree including buffering elements 142,
e.g. inverters. At the output end of the clock distribution network 140, i.e. where the clock pulse signal is distributed to the various integrated circuit elements not shown that are response to both edges of the pulse of the distributed clock pulse signal, e.g. double-edge flipflops, a distributed clock pulse signal is fed to the reference generating circuit 160 through conductor 106. The reference generating circuit 160 generates a reference in the form of a direct current (DC) voltage by integration of the pulses in the distributed clock pulse signal. Since the distributed clock pulse signal typically resembles the form of a block wave oscillating between 0 V and the supply voltage $V_{dd}$, the magnitude of the DC voltage corresponds with the area of the pulse, e.g. the pulse width, which, preferably, is $V_{dd}/2$ for a distributed clock pulse signal having a 50% duty cycle, although other reference voltages can be chosen. The reference in the form of a DC voltage is supplied to clock signal modifying circuit 120 through conductor 108, and the DC voltage is used to correct the parent clock pulse signal by an amount that correlates with the deviation of the reference from the $V_{dd}/2$ value indicating the deviation from the 50% duty cycle distributed clock pulse signal.

Now, the following Figs are described with backreference to Fig.1 Corresponding reference numerals have the same meaning as described for Fig.1, unless explicitly stated otherwise.

In Fig. 2, a very simple implementation of an integration circuit 170 enclosed in the reference generating circuit 160 is shown. Integration circuit 170 is an inverting integration circuit, which is formed by an inverter 172 and a capacitor 174. Inverter 172 has its control terminals coupled to conductor 106, making inverter 172 responsive to the distributed clock pulse signal. The capacitor 174 is coupled to conductor 108, which in its turn couples the output of inverter 172 to clock signal modifying circuit 120.

Capacitor 174 has a large enough capacity to limit the ripple on the DC voltage outputted by reference generating circuit 170. Typically, the capacitor has a capacitance in the sub-pF to pF range. When the duty cycle of the distributed clock pulse signal is close enough to 50%, capacitor 174 is charged to such an extent that the substantially constant direct current voltage has a value of about $V_{dd}/2$. However, if the distributed clock pulse signal has a duty cycle of substantially less than 50%, the output of inverter 172 will remain high for a longer period of the clock cycle, which will cause an increase in the direct current voltage outputted on conductor 108 because of the larger charge on capacitor 174. If the distributed clock pulse signal has a duty cycle of substantially more than 50%, the output of inverter 172 will remain low for a longer period of the clock cycle, which will cause an decrease in the DC voltage outputted on conductor 108 because of the
smaller amount of charge stored in capacitor 174. It will be obvious to those skilled in the art that other integration circuits can be thought of without departing from the teachings of the present invention.

Fig. 3 shows an embodiment of a very compact clock signal modifying circuit 120 including a logic circuit 130 and an optional inverter 122. Inverter 122 can be omitted when a non-inverted reference, e.g. a reference voltage that increases with an increasing duty cycle of the distributed clock pulse signal, is used to control a part of the logic circuit 130. In this embodiment, logic circuit 130 has four transistors coupled in series; a first transistor 132 of a first conductivity type having its control terminal coupled to conductor 102 making first transistor 132 responsive to the parent clock pulse signal; a second transistor 134 of the first conductivity type having its control terminal coupled to conductor 108, making second transistor 134 responsive to the reference, e.g. the direct current voltage generated by reference generating circuit 160; a third transistor 136 of a second conductivity type having its control terminal coupled to conductor 102 and a fourth transistor 138 of the second conductivity type having its control terminal coupled to conductor 108.

In Fig. 3, first and second transistors 132 and 134 are depicted as pMOS transistors, whereas third and fourth transistors 136 and 138 are depicted as nMOS transistors. It is emphasized that this is done by way of example only; it will be obvious to those skilled in the art that other arrangements of logic circuit 130 using transistors other than CMOS transistors are possible without departing from the teachings of the present invention.

In logic circuit 130, the time-dependent conductivity of second and fourth transistors 134 and 138, e.g. the conductivity within a complete clock cycle, will be near constant, because the control terminals of second and fourth transistors 134 and 138 are subjected to the substantially constant DC voltage reference from reference generating circuit 160. However, their relative conductivities can vary, since this is dependent on the value of the DC voltage reference. In contrast, since the control terminals of first and third transistors 132 and 136 are subjected to a parent clock pulse signal, the time-dependent conductivity of these transistors will vary as a function of the parent clock pulse signal. It will be obvious to those skilled in the art that second and fourth transistors 134 and 138 are used to introduce a reference dependent delay to the rising and falling edge of the parent clock pulse, respectively.

For instance, for a distributed clock pulse signal having a duty cycle close to 50%, second and fourth transistors 134 and 138 will be substantially equally conducting, since their control terminals are being subjected to a voltage of around V_{dd}/2. Consequently,
the shape of the clock pulse signal that is outputted by clock signal modifying circuit 120 is governed by the time-dependent conductivity of first and third transistors 132 and 136, e.g. by the shape of the parent clock pulse signal. However, when the duty cycle of the distributed clock pulse signal is substantially larger than 50%, the inverting integration circuit 170 will produce a lower DC voltage reference, making pMOS transistor 134 more conducting than nMOS transistor 138. Consequently, the rising edge of the clock pulse signal outputted by logic circuit 130 will be formed quicker than the falling edge, leading to an increase of the duty cycle of the clock cycle outputted by logic circuit 130. Inverter 122 will invert this signal and hence a clock pulse signal with a reduced duty cycle with respect to the distributed clock pulse signal is outputted to the clock distribution network 140. Obviously, the inverse applies to a distributed clock pulse signal that is substantially smaller than 50%; pMOS transistor 138 will be less conducting than nMOS transistor 138 because of a DC reference higher than \( V_{dd}/2 \), which will result in a broadening of the parent clock pulse by clock signal modifying circuit 120.

Fig. 4 shows the results of a PSTAR simulation of the impact of the application of the duty cycle control logic according to the present invention on an IC in CMOS18 technology having a five-inverter balanced clock tree. PSTAR is a Philips in-house simulation tool for simulating the conductivity characteristics of transistors. In this simulation, an offset has been added to the threshold voltage of the P and N transistors forming the inverters of the clock tree, to mimic the effect of IC fabrication process variations on the behavior of the clock pulse signal distribution. This offset is plotted on the X-axis in millivolts. On the Y-axis, the calculated duty cycle of the distributed clock pulse signal is represented in %. The dotted line represents the simulated duty cycle of a distributed clock pulse signal of an IC without duty cycle control logic, whereas the solid line represents the simulated duty cycle of a distributed clock pulse signal of an IC including the reference generating circuit 160 and the clock signal modifying circuit 120 as depicted in Fig. 2 and 3, respectively.

The effect of the duty cycle control logic according to the invention, e.g. the reference generating circuit 160 for providing a DC voltage reference and a clock signal modifying circuit 120 including a logic circuit being responsive to both the parent clock pulse signal and the DC voltage reference, is evident: a duty cycle in the range of 45-55% is obtained when applying the duty cycle control logic according to the invention even when an uncorrected duty cycle of just over 20% is obtained, e.g. for process variations leading to a threshold voltage offset of \(-400\) mV.
Thus, the use of a very simple hardware arrangement in comparison to the
arrangement disclosed in laid-open Japanese patent application JP 2001024487 still leads to a
corrected duty cycle close enough to 50% to guarantee the desired timing behavior of
synchronous elements coupled to the outputs of the clock signal distribution network 140 that
utilize both edges of the clock pulse, like dual-edge triggered flipflops.

At this point, it is emphasized that the simulations show that the feedback loop
from the outputs of the clock signal distribution network 140 to clock signal modifying
circuit 120 via reference generating circuit 160 does not lead to oscillations in the duty cycle
of the distributed clock pulse signal. These simulations have demonstrated that the distributed
clock pulse signal duty rapidly converges to a value between the value of the uncorrected
duty cycle and a duty cycle of 50%, thereby generally reducing the process technology
induced duty cycle deviation by at least a factor two.

Although a correction of the parent clock pulse signal by the clock signal
modifying circuit 120 on the basis of the DC voltage reference will lead to a modification of
the distributed clock pulse signal and, consequently, of the DC voltage generated by
reference generating circuit 160, it can be shown that in equilibrium all signals are stable.

With backreference to Fig. 1, the following expressions can be constructed:

\begin{align*}
(1) \quad & y = z + p; \\
(2) \quad & x = I(y) = k_d(1 - y) + k_i' \\
(3) \quad & z = DCC(x, 0.5) = k_d x + k_d'
\end{align*}

- with clock pulse signal \( z \) being the modified clock pulse signal on conductor 104 and DCC
  \((x, 0.5)\) being the function defining the shape of \( z \), e.g. the function describing the influence
  of the output signal from clock signal modifying circuit 120 on the incoming parent clock
  pulse signal, with \( k_d \) and \( k_d' \) being constants defining the slope and offset of DCC;
- signal \( x \) being the reference signal on conductor 108 and \( I(y) \) being the function defining the
  shape of \( x \), e.g. the function describing the influence of reference generating circuit 160 on
  the incoming clock signal \( y \), with \( k_i \) and \( k_i' \) being constants defining the slope and offset of \( I \);

and

- clock pulse signal \( y \) being the clock pulse signal on conductor 106, \( y \) being formed by the
  shape of modified clock pulse signal \( z \) and the deviation \( p \) introduced in the clock signal
distribution network 140.
Now, substitution of expression (2) into expression (3) can lead to the following expression for $z$:

$$(4) \quad z = k_d k_i' + k_d k_i (1 - y) + k_d';$$

and substitution of (4) into (1) leads to the following expression for $(y)$:

$$(5) \quad y = [k_d(k_i + k_i') + k_d' + p]/(1 + k_d k_i)$$

Expression (5) shows that $y$ is solely dependent on constants, hence $y$ is a constant. Therefore, both $z$ and $x$ are constant as well since they both depend on $y$, which demonstrates that a stable equilibrium can be obtained.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.
CLAIMS:

1. Integrated circuit, comprising:
   a clock signal modifying circuit for modifying a parent clock pulse signal into
   a clock pulse signal responsive to a reference;
   a clock signal distributing network for distributing the clock pulse signal; and
   a reference generating circuit for generating the reference in response to a
   distributed clock pulse signal received from the clock signal distributing network;
   characterized in that the reference generating circuit comprises signal
   integration means for integrating the distributed clock pulse signal to generate the reference
   as a direct current voltage.

2. An integrated circuit as claimed in claim 1, characterized in that the signal
   integration means comprise an inverter loaded by a capacitance.

3. An integrated circuit as claimed in claim 1 or 2, characterized in that the clock
   signal modifying circuit further comprise a logic circuit having:
   a first transistor and a second transistor of a first conductivity type coupled to
   a third transistor and a fourth transistor of a second conductivity type, the first transistor and
   the third transistor having a control terminal coupled to receive the parent clock pulse signal,
   and the second transistor and the fourth transistor having a control terminal coupled to
   receive the reference.

4. An integrated circuit as claimed in claim 3, characterized in that the first
   transistor is coupled in series with the second transistor; and the third transistor is coupled in
   series with the fourth transistor, with an output of the logic circuit being coupled between an
   output of the second transistor and an input of the third transistor.

5. An integrated circuit as claimed in claim 3, characterized in that an output of
   the logic circuit is coupled to the output of the signal modifying circuit via a further inverter.