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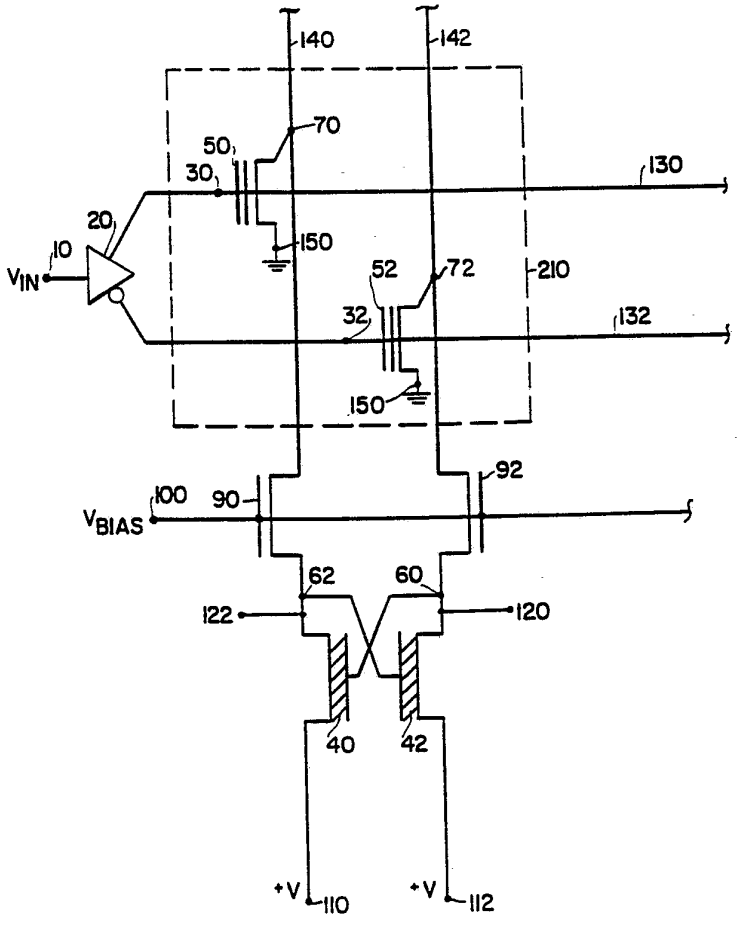
(54) Title: EPROM-BASED CROSSBAR SWITCH WITH ZERO STANDBY POWER

(57) Abstract

An EPROM-based crossbar switch (200) is disclosed that provides for the programmable interconnection of logic circuitry. Circuit layout and design features (210) reduce circuit real estate and bitline (140, 142) parasitic capacitances, allowing a high level of integration and faster switching speeds.



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EPROM-BASED CROSSBAR SWITCH WITH ZERO STANDBY POWER

Background of the Invention

This invention relates to the programmable interconnection of digital circuits. Particularly, the invention relates to programmable interconnections known as crossbar switches, which are used to switch N digital inputs into N digital outputs.

Various interconnection schemes are possible, for example, as described in Wong et al. U.S. Patent 4,871,930, blocks of programmable logic or logic array blocks (LABs) may be programmably interconnected using programmable interconnect arrays (PIAs). In this manner, relatively many small logic elements may be efficiently interconnected using a hierarchical method -- first, interconnecting primitive logic elements into LABs, and second, interconnecting LABs using PIAs. The PIAs accept all logic function outputs from the LABs, and provide the means to programmably interconnect a small subset of these back into the LABs.

However, it is often desirable to provide digital circuit interconnections that programmably switch a number of inputs into an equal number of outputs. Further, it is desirable that the switching circuit have low standby power and display relatively

small parasitic capacitance values. The switch should also be simple to program and low in cost.

Summary of the Invention

In view of the foregoing, it is an object of this invention to provide a programmable crossbar switch with low standby power consumption.

It is a further object of the invention to provide a crossbar switch that is based on erasable programmable read only memory (EPROM) transistors, and thus is relatively inexpensive and readily programmed.

It is a further object of this invention to provide an EPROM-based crossbar switch with low bitline parasitic capacitance.

The present invention provides the desired structure set out above. Namely, a crossbar switch is provided for programmably interconnecting N input nodes to N output nodes, allowing the interconnection of digital circuits, while adding relatively little parasitic capacitance to the overall circuit. Contributing to the low parasitic capacitance is the use of only two EPROM transistors for each intersection of two bitlines and two wordlines. As shown in commonly assigned, co-pending U.S. Patent Application Ser. No. 596,764, concerning sense amplifiers with complementary bitlines, prior art intersections typically have four EPROM transistors, resulting in greater bitline loading and slower circuit performance.

Brief Description of the Drawings

FIG. 1 is a schematic drawing of the circuit of one cell of an illustrative embodiment of the crossbar switch of this invention. Also shown are bias transistors and the pair of cross-coupled inverters this cell drives.

FIG. 2 is a schematic diagram of a representative 4x4 subsection of an illustrative embodiment of a crossbar switch circuit constructed in accordance with the principles of this invention, showing the matrix layout of the cells.

Detailed Description of the Preferred Embodiments

As shown in FIG. 1, a representative portion of a crossbar switch constructed in accordance with this invention includes complementary wordlines 130 and 132 intersecting complementary bitlines 140 and 142 via programmable EPROM transistors 50 and 52. In an NxN crossbar switch there will be N^2 such intersections, laid out as shown in part in FIG. 2. This allows one of N inputs to be programmably switched to any one of N outputs by the appropriate programming of the EPROM transistors. Specifically, if EPROM transistors 50 and 52 are programmed, they will not switch and the state of the input voltage, V_{IN}, at node 10 will not affect the output voltage, V_{OUT}, at node 120. However, if EPROM transistors 50 and 52 are erased (not programmed), the transistors will switch in response to changes in V_{IN}. By programming all but one pair of EPROM transistors on a pair of complementary wordlines, an input signal at an input node, such as node 10, will be output at the appropriate output node, such as 120. Various EPROM transistors may be employed. For example, EPROM transistors 50 and 52 may be UV-erasable EPROM transistors or electrically erasable programmable read only memory (E^2PROM) transistors.

Referring to FIG. 1, the propagation of an input signal at node 10 via erased EPROM transistors 50 and 52 to output node 120 is described as follows, for both low to high and high to low transitions. Note the power supply voltage at nodes 110 and 112 is

approximately 5.0 V, the bias voltage at node 100 is in the range of 3.0 V, and the potential of the ground nodes 150 is maintained in the range of 0 V. The bias transistor arrangement prevents nodes 70 and 72 from rising so high as to falsely program EPROM transistor 50 or 52.

For a low to high transition, the initial state of node 10 is low, thus EPROM transistor 50 is initially off, and node 70 high. The high signal of node 70 is communicated via n-type buffer transistor 90 to node 62, holding p-type transistor 42 off. The complement of the low node 10 voltage at node 52 holds EPROM transistor 52 on, holding node 72 low. As p-type transistor 42 is off, only a negligible current flows in bit line 142. The low signal at node 72 is communicated via buffer transistor 92 to node 60 where it holds p-type transistor 40 on. However, as EPROM transistor 50 is off, a negligible current flows in bit line 140. With no current flowing in bit lines 140 and 142, the standby power consumption of the circuit in FIG. 1 is near zero. Note the low signal at node 72 is communicated to output node 120 via buffer transistor 92.

A low to high transition at input node 10 causes EPROM transistor 50 to turn on, pulling node 70 low. This low voltage is transmitted to node 62 via buffer transistor 90, turning on p-type transistor 42. Low node 32, which is the complement of high node 10, has turned off EPROM transistor 52. Thus, the turn-on of p-type transistor 42 brings node 60, and therefore output node 120, high. Subsequently, p-type transistor 40 is turned off, blocking current flow in bit line 140. Since current flow is blocked in bit line 142 by turned off EPROM transistor 52, quiescent power

dissipation is negligible as in the previous state, where the voltage V_{IN} at node 10 was low.

A high to low transition at input node 10, takes node 32 high, turning EPROM transistor 52 on, and forcing node 72 low. This low voltage is transmitted via n-type buffer transistor 92 to node 60 and the output node 120, turning p-type transistor 40 on. Since node 30 is low, EPROM transistor 50 is off. Thus, as p-type transistor 40 turns on, it brings node 62 high, turning off p-type transistor 42 and blocking current flow in bit line 142. Current flow is blocked in bit line 140 by turned off EPROM transistor 50. The cell has now been returned to its original state.

As shown in FIG. 2, the crossbar switch may also include output buffers 215 to buffer and invert the output signal. Further, as shown in FIG. 1, it is also possible to provide output node 122, the complement of node 120.

From the above, it is apparent that not only does the circuit in FIG. 1 transmit input signals at node 10 to output node 120, but that the circuit also provides for zero quiescent power consumption.

As the structure of two-EPROM transistor cell 210 consumes less real estate on the chip, a higher level of integration is possible than if four EPROM transistors were committed to each cell. Two transistor cell 210 also does not load bit lines 140 and 142 and word lines 130 and 132 as much as would a four transistor cell. This reduced loading provides for faster switching in the crossbar circuit.

Although particular attention has been given to the operation of one cell of the crossbar switch circuit, it will be understood that the overall function of the chip is to programmably interconnect N inputs to N outputs, and that among other possible

variations within the scope of the invention that will occur to those skilled in the art, any number of inputs and outputs may be used.

We claim:

1. An EPROM-based crossbar switch for programmably interconnecting N input nodes to N output nodes comprising:

a plurality of complementary wordlines communicating with said input nodes;

a plurality of complementary bitlines;

a plurality of EPROM transistor pairs for interconnecting said complementary bitlines and said complementary wordlines; and

circuit means for communication between said complementary bitlines and said output nodes.

2. The apparatus of claim 1 wherein said transistor pairs comprise erased pairs and programmed pairs, said erased pairs providing communication between said complementary wordlines and said complementary bitlines, and said programmed pairs not providing communication between said complementary wordlines and said complementary bitlines.

3. The apparatus of claim 2 wherein:

a first transistor from one said erased pair provides communication between a first wordline and a first bitline;

a corresponding second transistor from said erased pair provides communication between a second wordline and a second bitline; and

said second wordline is the complement of said first wordline and said second bitline is the complement of said first bitline.

4. The apparatus of claim 3 wherein said first transistor comprises:

a gate connected to said first wordline;

a second terminal connected to said first bitline; and

a third terminal connected to a ground node.

5. The apparatus of claim 3 wherein said second transistor comprises:

a gate connected to said second wordline;

a second terminal connected to said second bitline; and

a third terminal connected to a ground node.

6. The apparatus of claim 1 wherein said circuit means comprises pairs of buffer transistors for limiting the excursion of voltages on said complementary bitlines.

7. The apparatus of claim 6 wherein said circuit means further comprises output buffers providing communication between said buffer transistors and said output nodes.

8. The apparatus of claim 6 wherein said circuit means further comprises cross-coupled inverters communicating with said complementary bitlines via said buffer transistors for limiting quiescent current flow in said complementary bitlines.

9. The apparatus of claim 8 wherein each of said cross-coupled inverters comprises:

a first p-type transistor having

(1) a first gate connected to a first bitline;

(2) a first terminal connected to a power supply; and

(3) a second terminal connected to a second bitline, said second bitline being the complement of said first bitline; and

a second p-type transistor having

(1) a second gate connected to said second bitline;

(2) a third terminal connected to said power supply; and

(3) a fourth terminal connected to said first bitline.

10. The apparatus of claim 1 wherein on each of said complementary wordlines, all but one of said pairs of EPROM transistor are programmed.

11. The apparatus of claim 1 wherein on each of said complementary bitlines, all but one of said pairs of EPROM transistors are programmed.

12. An EPROM-based crossbar switch for programmably interconnecting N input nodes to N output nodes comprising:

N complementary wordline pairs, each for communicating with a respective one of said N input nodes;

N complementary bitline pairs;

N^2 EPROM transistor pairs for interconnecting said complementary bitline pairs and said complementary wordline pairs, wherein:

said transistor pairs comprise erased pairs and programmed pairs, said erased pairs providing communication between said complementary wordline pairs and said complementary bitline pairs, and said

programmed pairs not providing communication between said complementary wordline pairs and said complementary bitline pairs; and wherein:

a first transistor from each said erased pair provides communication between a first wordline and a first bitline, said first transistor comprising:

a first gate connected to said first wordline;

a first drain connected to said first bitline;

a first source connected to a ground;

a corresponding second transistor from said erased pair provides communication between a second wordline and a second bitline, said second transistor comprising:

a second gate connected to said second wordline;

a second drain connected to said second bitline;

a second source connected to said ground; and

said second wordline is the complement of said first wordline, and said second bitline is the complement of said first bitline; and

circuit means for providing communication between each of said complementary bitlines and a respective one of said output nodes.

13. The apparatus of claim 12 wherein said circuit means comprises pairs of buffer transistors for limiting the excursion of voltages on said complementary bitlines.

14. The apparatus of claim 13 wherein said circuit means further comprises output buffers

providing communication between said buffer transistors and said output nodes.

15. The apparatus of claim 13 wherein said circuit means further comprises cross-coupled inverters communicating with said complementary bitlines via said buffer transistors for limiting quiescent current flow in said complementary bitlines.

16. The apparatus of claim 15 wherein each of said cross-coupled inverters comprises:

a first p-type transistor having

(1) a first gate connected to a first bitline;

(2) a first terminal connected to a power supply; and

(3) a second terminal connected to a second bitline, said second bitline being the complement of said first bitline; and

a second p-type transistor having

(1) a second gate connected to said second bitline;

(2) a third terminal connected to said power supply; and

(3) a fourth terminal connected to said first bitline.

17. The apparatus of claim 12 wherein on each of said complementary wordlines, all but one of said pairs of EPROM transistors are programmed.

18. The apparatus of claim 12 wherein on each of said complementary bitlines, all but one of said pairs of EPROM transistors are programmed.

19. Integrated circuitry for programmably connecting each of a plurality of input terminals to any respective one of a plurality of output terminals comprising:

a pair of wordline conductors associated with each of said input terminals;

means for applying true and complement versions of the signal applied to each input terminal to respective ones of the wordline conductors in the pair of wordline conductors associated with that input terminal;

a pair of bitline conductors associated with each of said output terminals;

means for programmably interconnecting each pair of wordline conductors to each pair of bitline conductors, said means for programmably interconnecting each pair of wordline conductors to a pair of bitline conductors consisting of a pair of EPROM transistors each having a gate and a source-drain channel, the gate of each EPROM transistor being connected to a respective one of the wordlines in the associated pair of wordline conductors, and the source-drain channel of each EPROM transistor being connected to a respective one of the bitlines in the associated pair of bitline conductors;

means for interconnecting the bitline conductors in each pair of bitline conductors so that the current supply to each bitline conductor to which an EPROM transistor which is conducting is connected is cut off by the absence of any conducting EPROM transistor connected to the other bitline conductor in said pair of bitline conductors.

20. The integrated circuitry defined in claim 19 wherein the source-drain channel of each EPROM

transistor is connected in series between the bitline conductor to which that EPROM transistor is connected and a source of ground potential.

21. The integrated circuitry defined in claim 20 wherein said means for interconnecting the bitline conductors in each pair of bitline conductors comprises:

a p-channel transistor having a source-drain channel connected in series between each bitline conductor and a source of logical 1 potential, each p-channel transistor also having a gate which is connected to the other bitline conductor in the associated pair of bitline conductors.

22. The integrated circuitry defined in claim 21 further comprising an n-channel transistor having a source-drain channel connected in series between each bitline conductor and the source-drain channel of the p-channel transistor associated with that bitline channel, each n-channel transistor also having a gate connected to a source of bias potential which is intermediate said ground potential and said logical 1 potential.

23. The integrated circuitry defined in claim 22 wherein the output terminal associated with each pair of bitline conductors is connected between the p-channel and n-channel transistors whose source-drain channels are connected in series with one of the bitline conductors in that pair of bitline conductors.

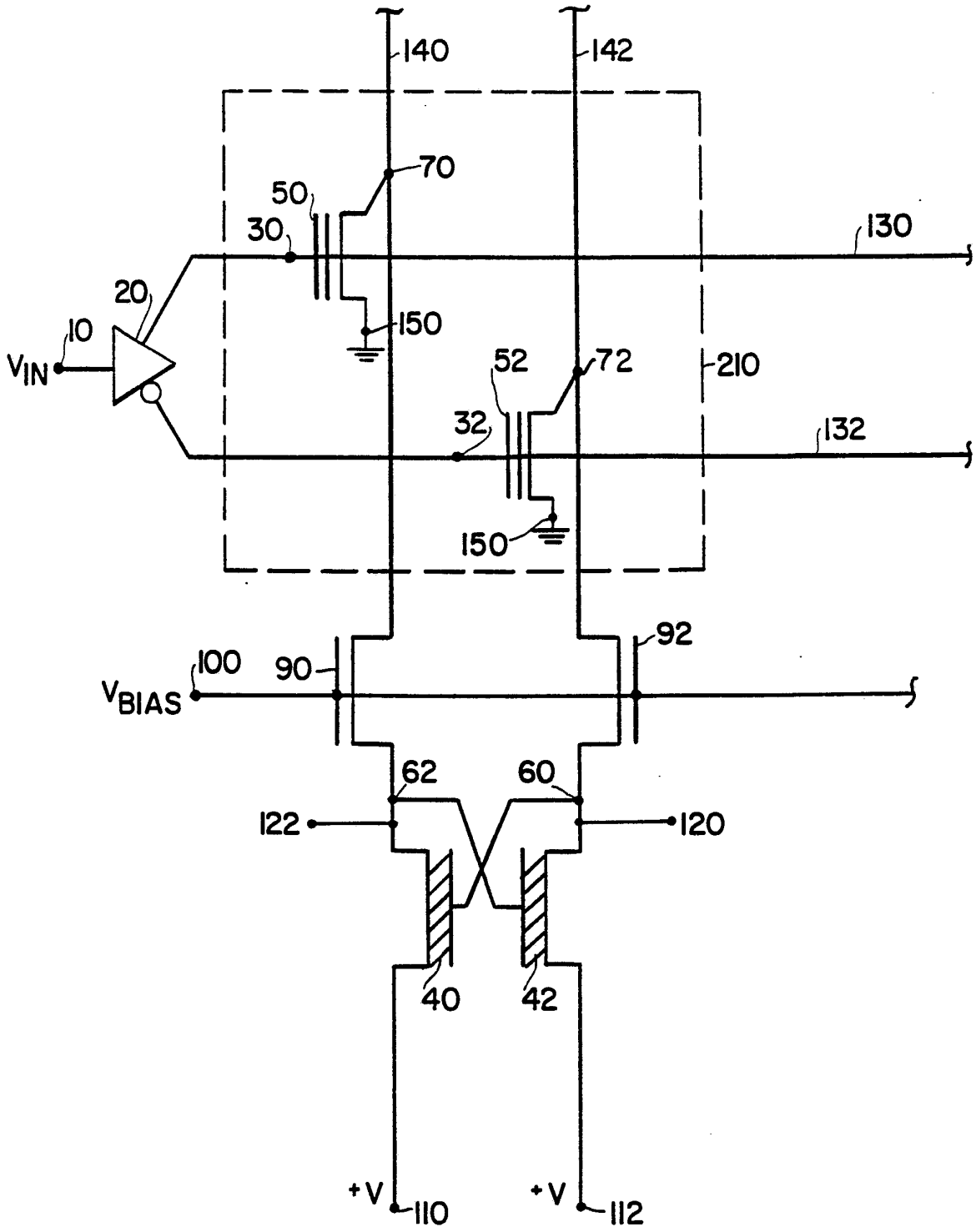
140
142
70
50
30
130
20
10
150
V_{IN}
52
72
210
32
132
150
92
100
90
V_{BIAS}
62
60
122
120
40
42
+V
110
+V
112

FIG. 1

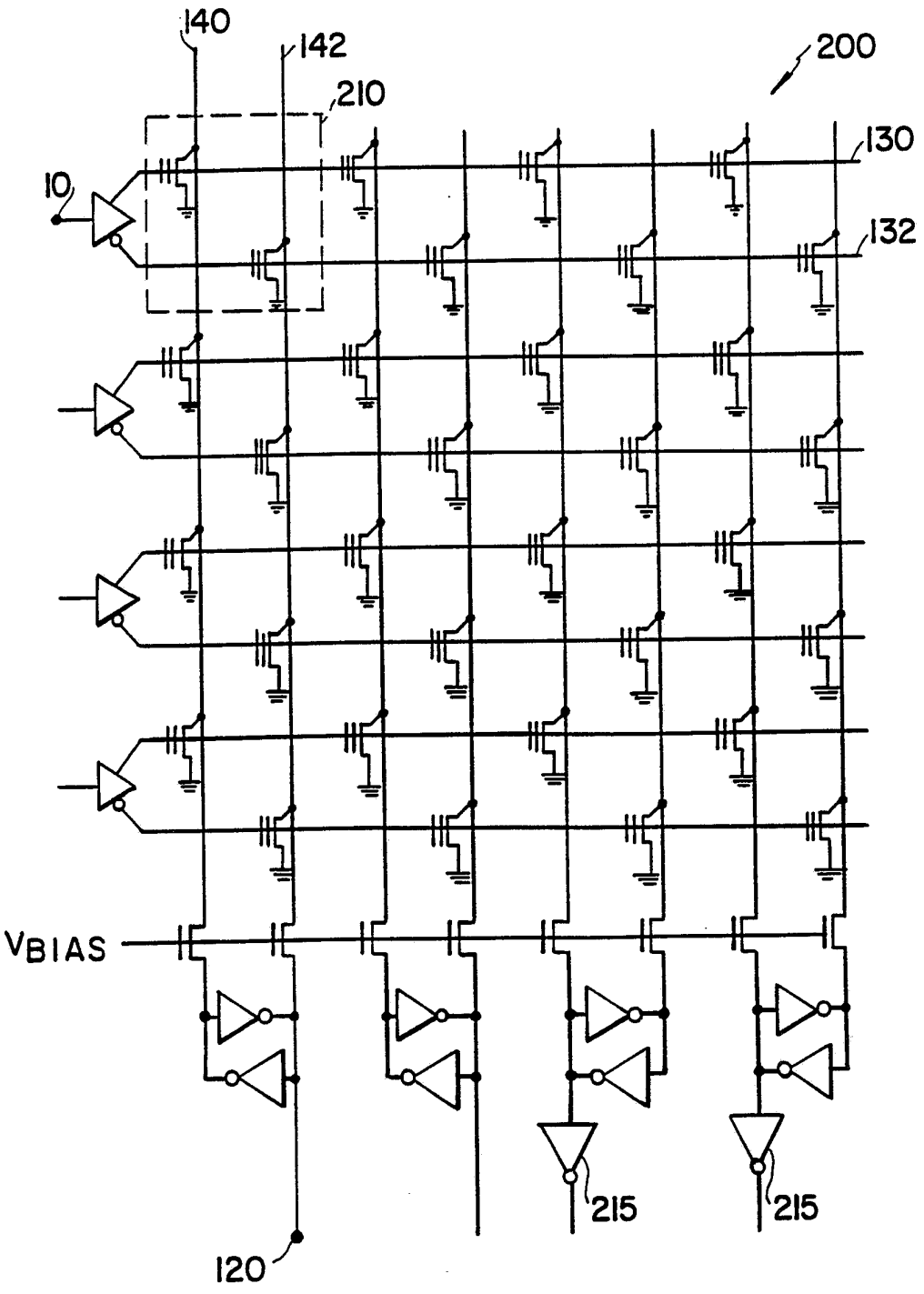

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04Q 1/00, 3/00; H03K 19/177
US CL :340/825.83,825.9,825.91,825.93,825.89.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/825.79,825.85,825.86,825.87,825.88;307/468-469.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US,A, 4,853,562 (Yamada) 01 August 1989 See Fig. 6 and Fig. 8; and col. 5, line 25 to Col. 8, line 60.	1-5,10-12, 17-18 6-9,13-16,19-23
A	US,A, 4,897,645 (Hofmann) 30 January 1990 See Figure 1 to Figure 5.	1-23
P,Y	US,A, 5,128,565 (McClintock et al) 07 July 1992 See Fig. 2 and Fig. 5; and col. 3, line 50 to col. 4, line 37 and col. 5, line 8 to col. 6, line 40.	6-9,13-16, 19-23
A	US,A, 4,317,110 (Hsu) 23 February 1982 See Figure 1 and Figure 4.	1-23

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,779,010 (Moss) 18 October 1988 See Fig. 3, Fig. 6, Fig. 7 and Fig. 8.	1-23
A	US,A, 4,899,070 (Ou et al.) 06 February 1990 See Fig. 1.	1-23