United States Patent

Peronneau

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[54] **SYSTEM FOR THE DISPLAY OF SYNTHESIZED GRAPHIC SYMBOLS**

[72] Inventor: **Georges Peronneau**, La Celle Saint Cloud, France

[73] Assignee: **Thomson-CSF Visualisation Et Traitement Des Informations (T-V.T.)**, Paris, France

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[51] **Int. Cl.**.....**G06f 3/14**
[58] **Field of Search**.....340/324 A; 235/198, 197

[56] **References Cited**

UNITED STATES PATENTS

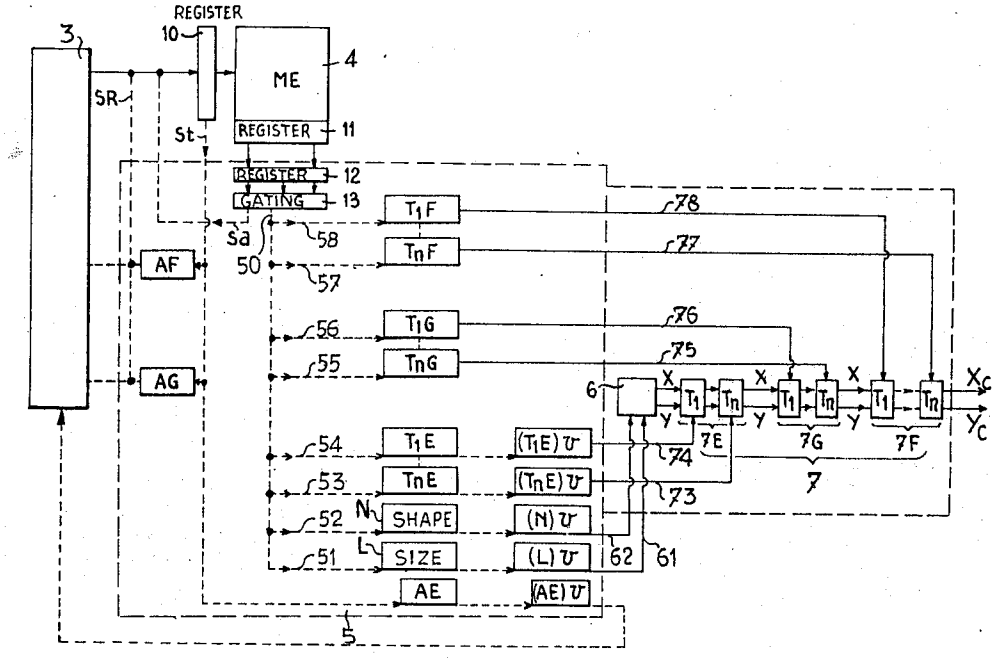
3,335,315	8/1967	Moore	340/324 A
3,364,382	1/1968	Harrison	340/324 A
3,476,974	11/1969	Turnage, Jr. et al.	340/324 A
3,520,994	7/1970	McAfee et al.	340/324 A
3,603,964	9/1971	Harrison	340/324 A
3,394,367	7/1968	Dye	340/324
3,309,692	3/1967	Wilhelmsen	340/324
3,417,281	12/1968	Stauffer	340/324
3,497,613	2/1970	Botjer et al.	340/324
3,444,319	5/1969	Artzt et al	340/324
3,466,645	9/1969	Granberg et al	340/324
3,422,419	1/1969	Mathews et al	340/324

Primary Examiner—John W. Caldwell
Assistant Examiner—Marhsall M. Curtis
Attorney—Karl F. Ross

[57] **ABSTRACT**

A variety of graphic symbols, to be displayed on the screen of a cathode-ray tube under the control of a computer, are synthesized from a store of basic elements which can be selectively combined into groups, the latter in turn being assembled into figures. Digital instructions regarding the nature, size, orientation and location of any selected configuration in each of these three denominations (element, group, figure) are transmitted by the computer, via a memory containing the necessary data, to an analog processor which includes a function generator and several function modifiers in the sweep circuit of the cathode-ray tube to project successively the several elements defining a group, the several groups forming a figure, and the several figures constituting the display, with individual treatment of each higher-order configuration as to overall positioning and size. A function generator capable of producing different conic sections includes two cross-connected integrating amplifiers in the signal paths for the control of the horizontal and the vertical scan. A coincidence circuit may be activated to detect the traverse of the boundaries of a selected rectangular screen area by any elemental trace for instructing the computer to suppress all parts of the display outside that area for the purpose of distinctive visualization of the framed portion.

15 Claims, 8 Drawing Figures



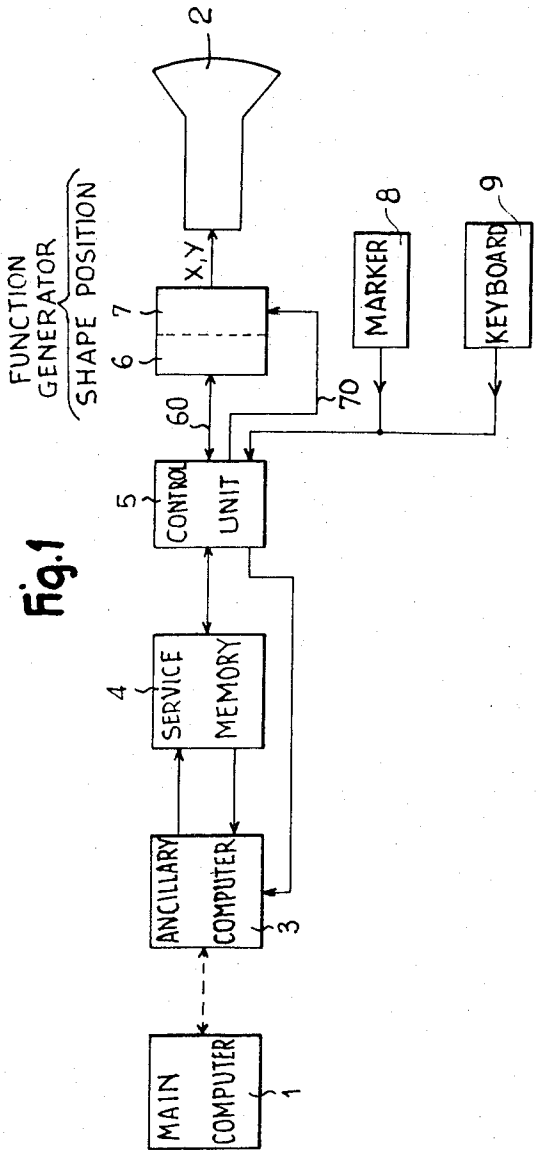


Fig.1

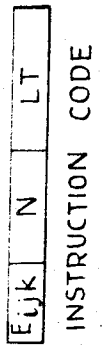
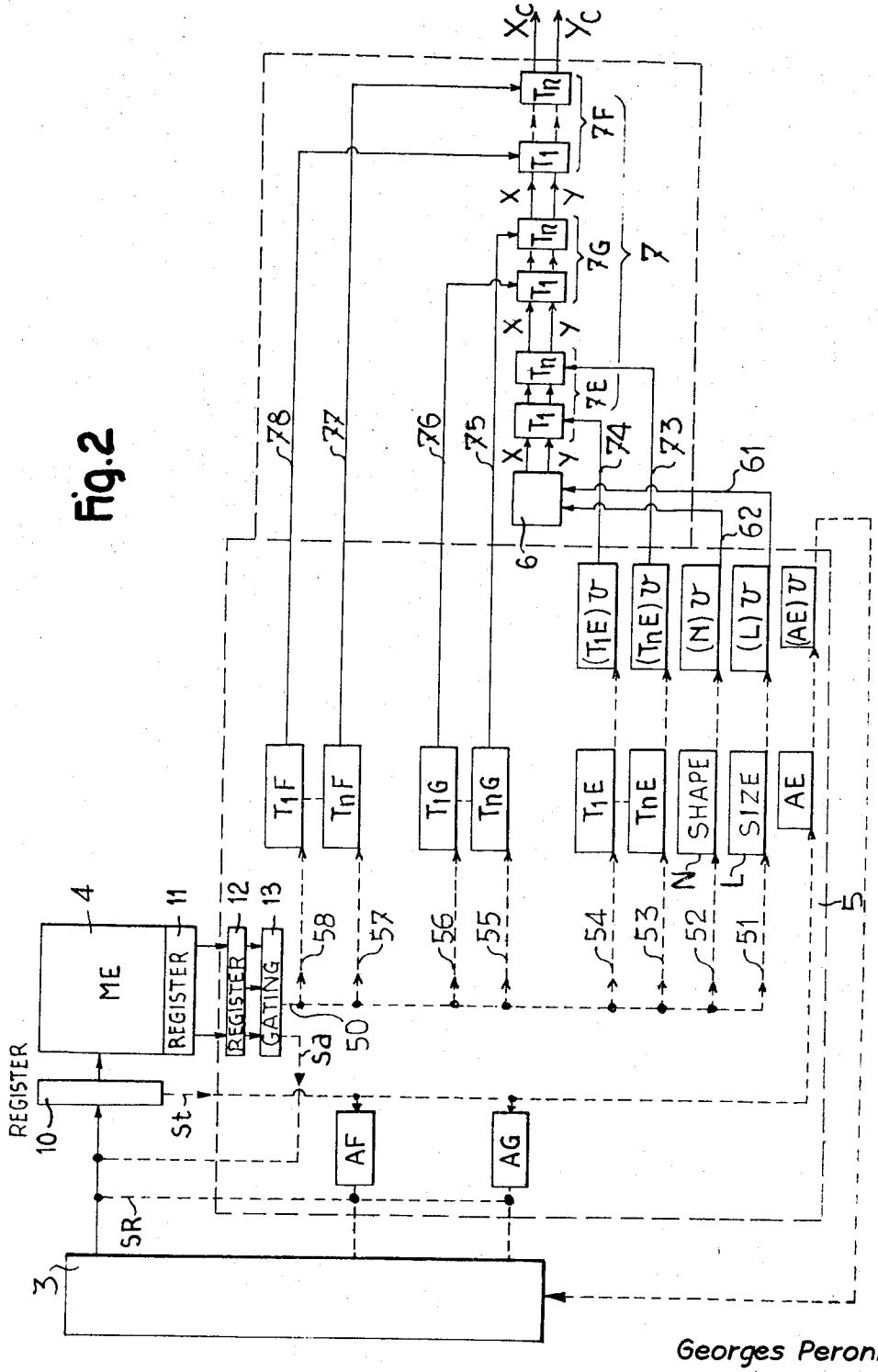


Fig.3

Georges Peronneau
Inventor.

By Karl F. Ross
Attorney

Fig.2



Georges Peronneau
Inventor.

By

Karl F. Ross
Attorney

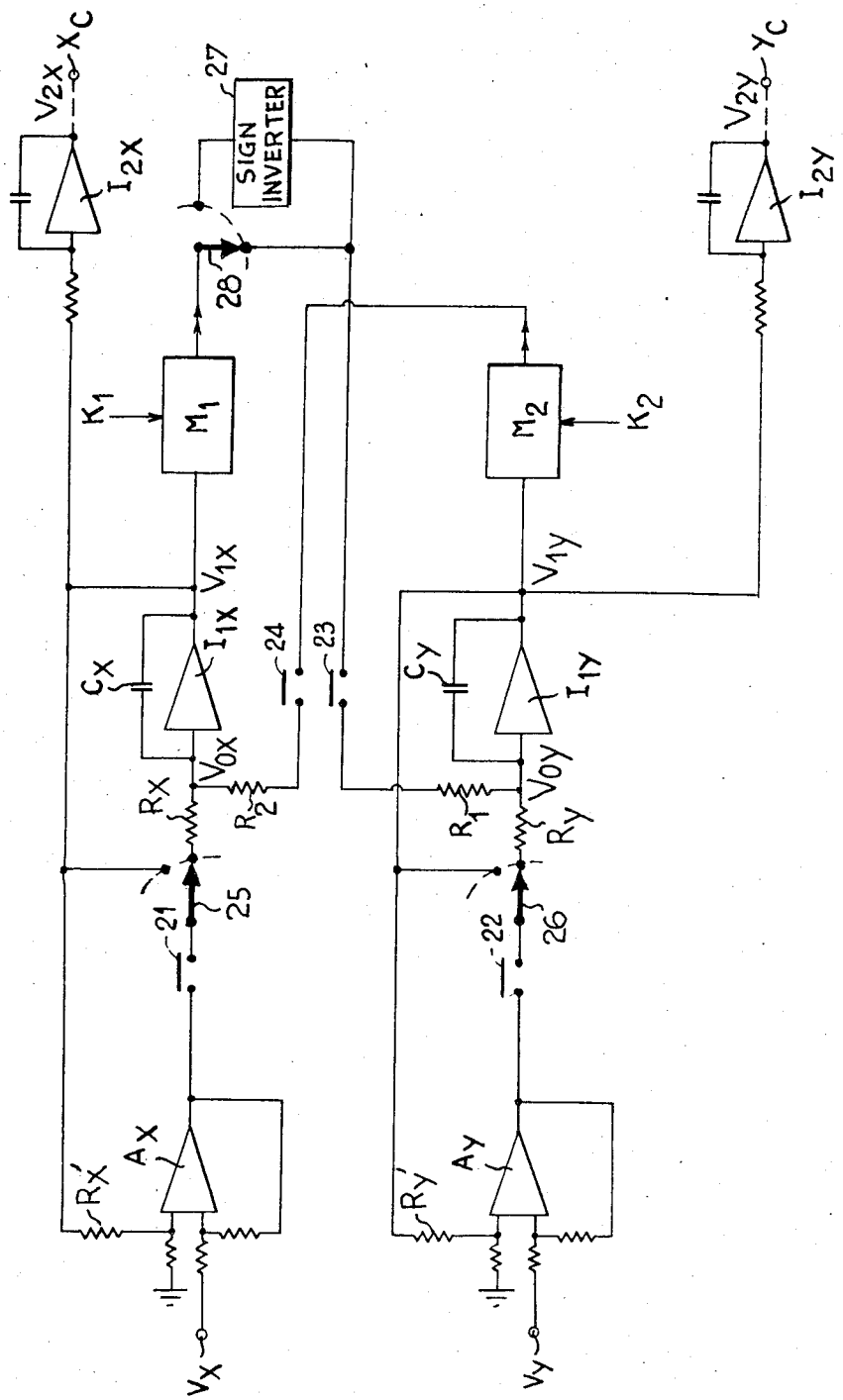
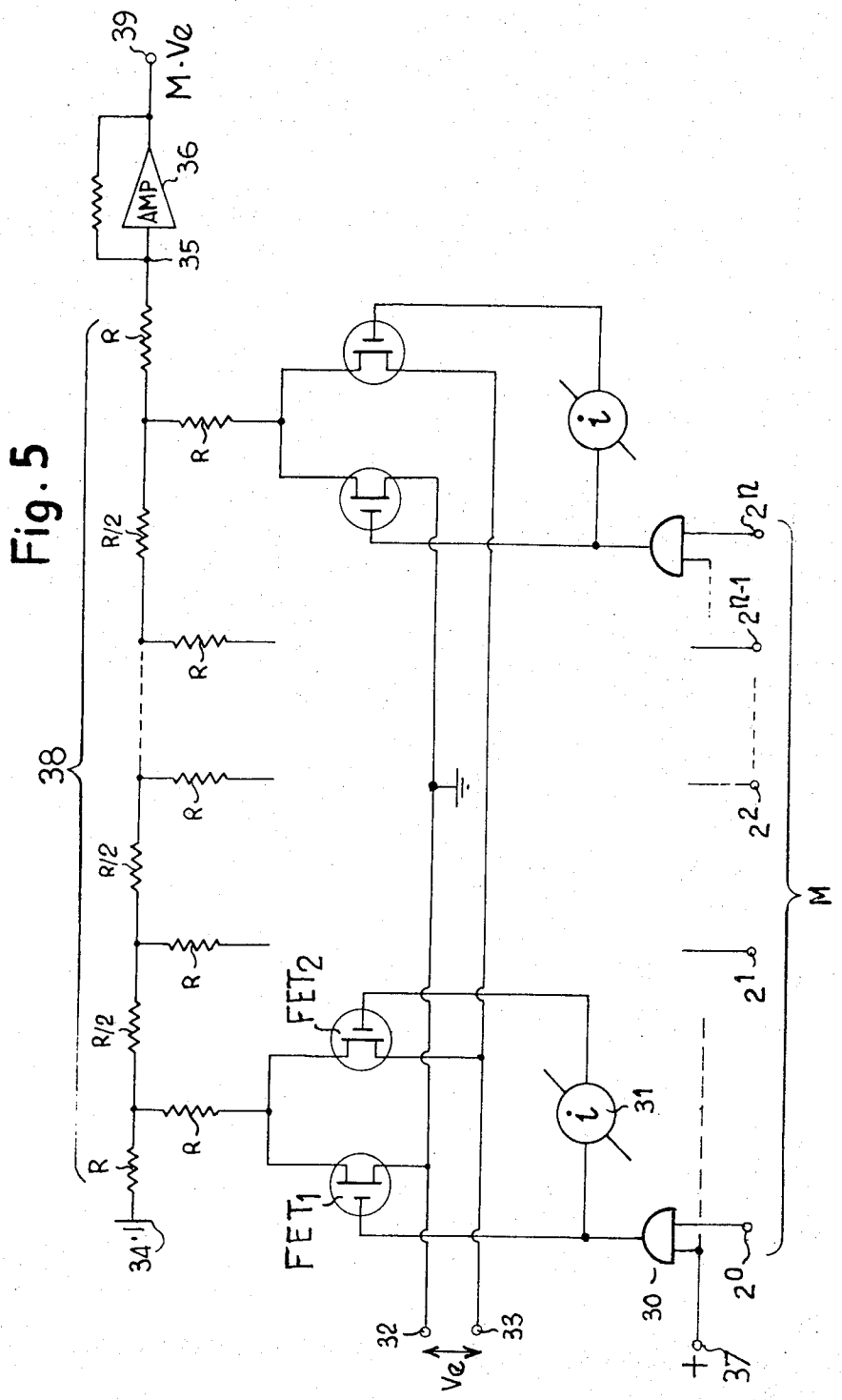


Fig. 4

Georges Peronneau
Inventor.

By Karl F. Ross
Attorney

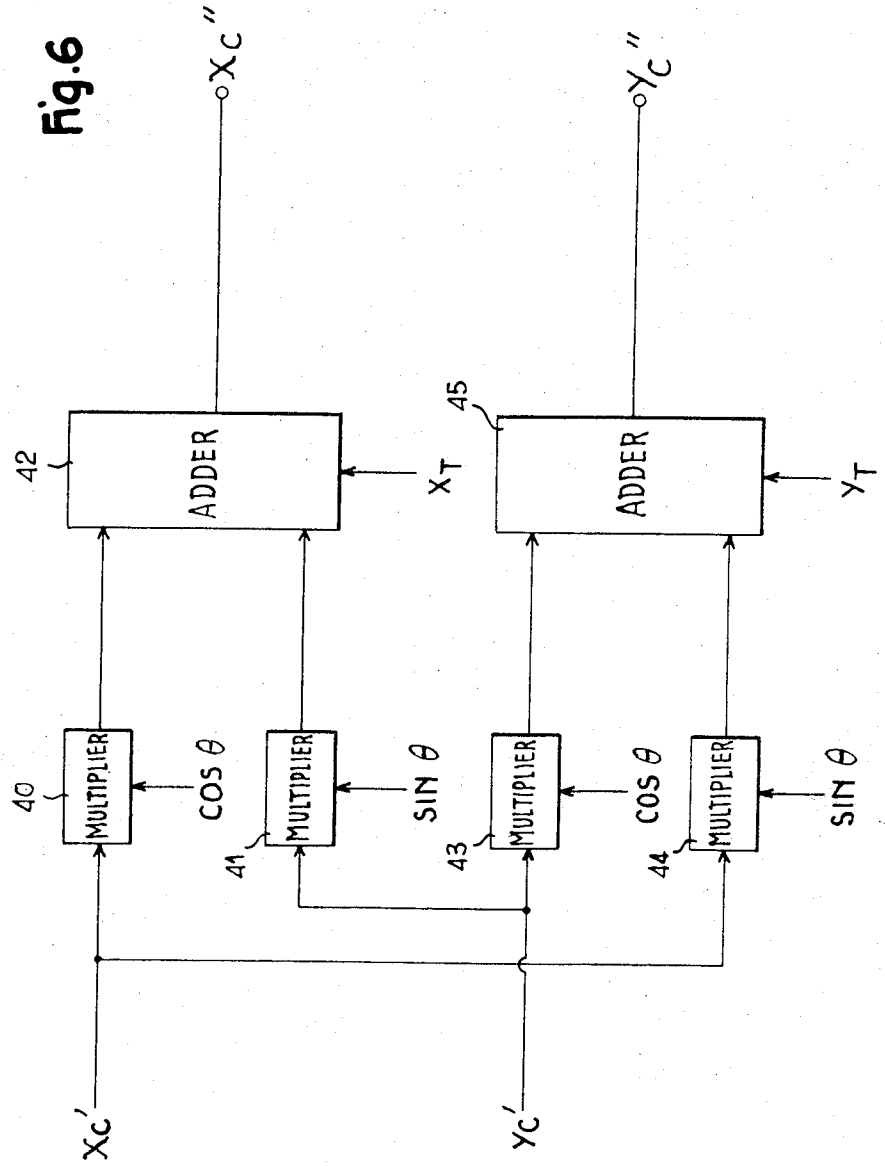
Fig. 5



Georges Peronneau
Inventor.

By Karl F. Ross
Attorney

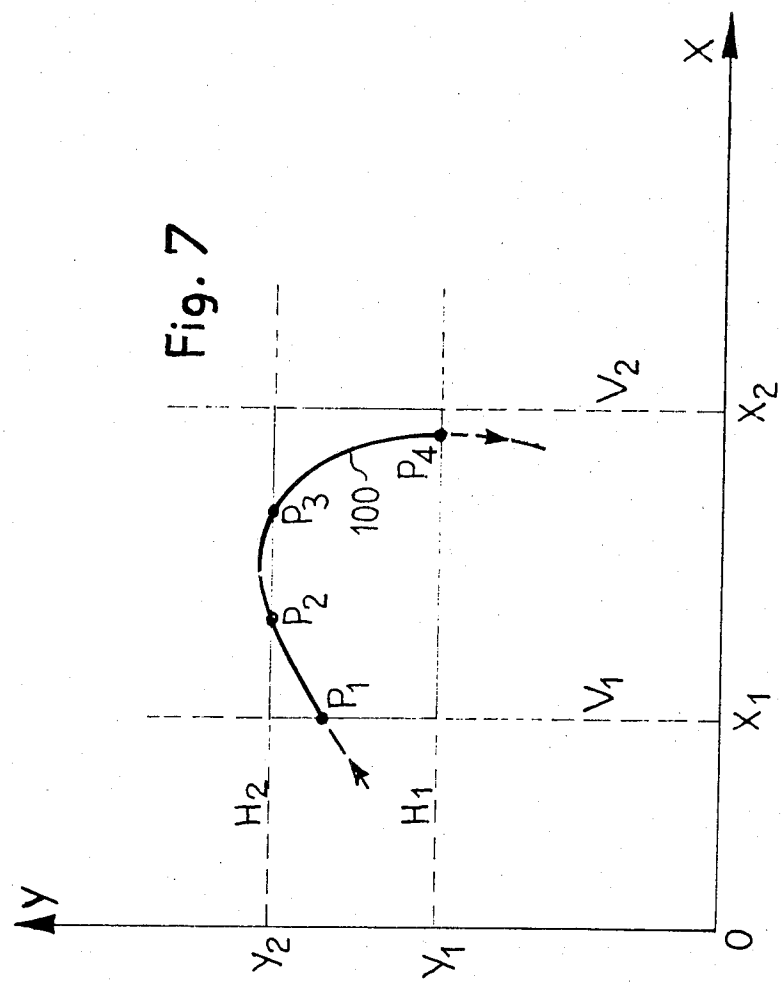
Fig.6



Georges Peronneau
Inventor.

By
Karl F. Ross
Attorney

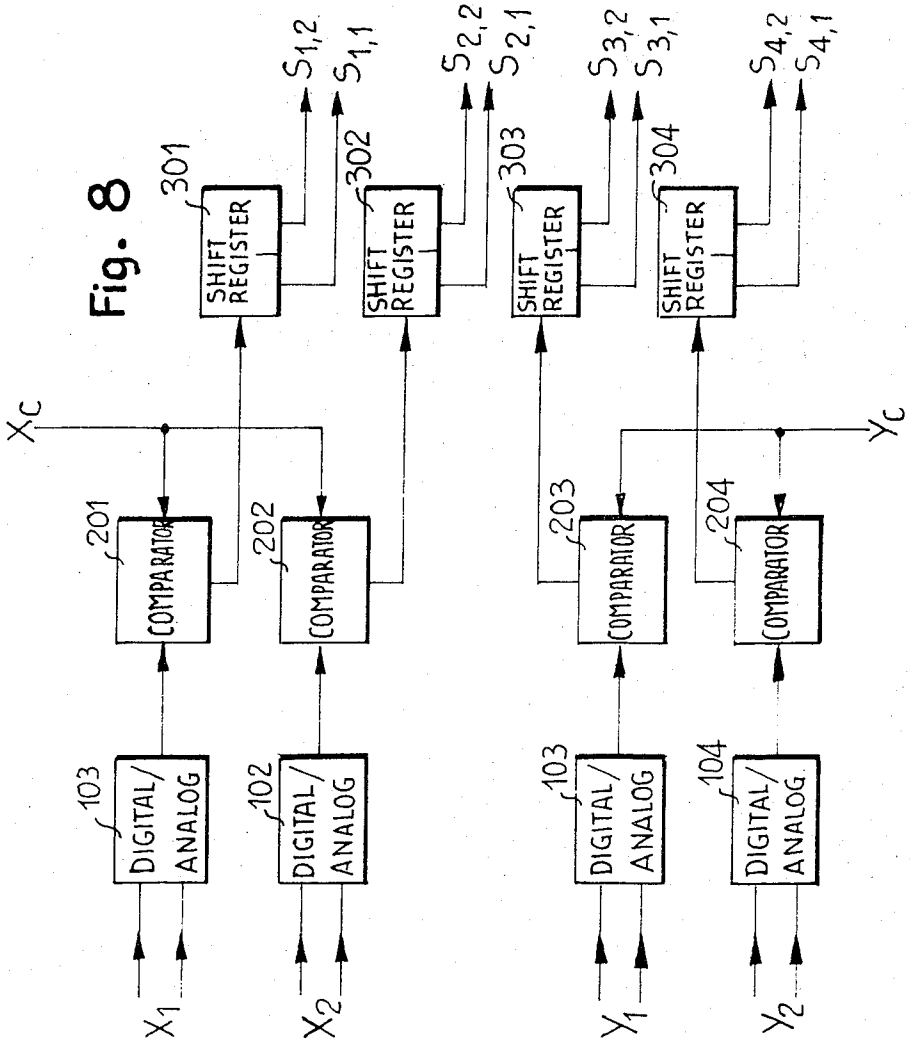
Fig. 7



Georges Peronneau
Inventor.

By Karl F. Ross
Attorney

Fig. 8



Georges Peronneau
Inventor.

By Karl F. Ross
Attorney

SYSTEM FOR THE DISPLAY OF SYNTHESIZED GRAPHIC SYMBOLS

The present invention relates to a system for displaying graphic symbols on the screen of a cathode-ray tube under the control of a computer.

Modern computers are capable of converting stored or instantly generated input data into scan-control signals for the sweep circuits of a cathode-ray tube whose beam thereupon traces a more or less complex figure visualizing the information received. The analog voltages or currents used to deflect the beam are derived from the digital output of a calculating section which may form part of the principal computer or constitute an ancillary unit. The binary words delivered by this calculating section must be stored in a buffer memory to enable the tracing of different shapes, in response to corresponding sets of instructions from the computer, to be generated repeatedly and in rapid succession so as to create a visual impression of a unitary picture.

With increasing complexity of the symbols to be so displayed, the computer must be capable of performing a large number of calculations in a short period of time. Moreover, though in many instances these symbols consist but of a relatively small number of different basic elements varying only as to size, relative position and orientation with reference to a given co-ordinate system, the computer must individually recalculate the law of each basic element in a time-consuming severely severly taxing the available facilities.

It is, therefore, the general object of my present invention to provide a display system of the character set forth which avoids the aforestated disadvantages and greatly accelerates the visual synthesis of complex shapes, to be traced on a CRT screen, from a limited number of basic elements.

A more particular object is to provide a system of this type which can be used, if desired, for direct communication between the machine and a human operator, i.e. for the creation or modification of a display by the actuation of a keyboard, a stylus or similar manual input means.

Still more specifically, my invention aims at providing a relatively simple yet highly versatile electronic function generator and associated circuitry for shifting, rotating and homothetically modifying (enlarging or reducing) any shape representating a function of the first or the second order, i.e. straight lines and conic sections (the former, of course, representing a limiting case of the latter).

To realize the general object stated above, a system according to my invention essentially comprises an analog processor including one or more function generators for the control of a CRT beam in response to characterization and modification commands from a service memory in which the information delivered to it by the computer is stored in digital form, the computer having access to the memory for calling out any word stored therein to specify both the shape (e.g. line, ellipse, hyperbola) and the parameters (size, position, orientation) of a basic element to be traced.

According to another advantageous feature of the invention, several such elements traced in sufficiently rapid succession to give the impression of a higher-order configuration are modified (displaced or changed in size) as a group, in response to special

group-instruction words called out from the service memory by the computer, so that only the relative positions and orientations of the several elements within a given group need be taken into account in the individual processing of each element. The same principle can be extended to additional classes of higher-order groupings, e.g. "figures" formed from "groups" composed of "elements."

In this manner, it is possible to synthesize even an involved symbol from various combinations of only a few basic elements and, in turn, to bodily modify such symbol with the aid of only a few additional instructions called out from the service memory. This characteristic can be utilized, pursuant to a further feature of the invention, for isolating and distinctively visualizing — e.g. magnifying — a selected portion of an overall display. This can be done, as more fully described hereinafter, by establishing two limiting values for each of a pair of signal voltages issuing from the processor for the control of the two mutually orthogonal sweep circuits of the cathode-ray tube (conventionally referred to as "horizontal" and "vertical", respectively) and, upon either of these signal voltages reaching one of the limiting values chosen for it, transmitting to the computer a marker pulse indicating that the element being traced on instructions from the computer touches or intersects one of the boundaries of a rectangular frame defined by these limiting values. The computer, by evaluating this information in light of the programmed position, size and shape of the element, can then give rise to special command d signals (not necessarily relayed through the service memory), to be stored for an indefinite number of cycles, which cause the suppression of the trace outside the selected frame area, the visible remainder of the trace being then subject to the same modifications as any original element or combination of elements regarding size and position. Thus, the operator may preselect the boundaries of that area by the setting of two potentiometers or the like and, by depressing a special "cropping" key of an associated keyboard may cut off all the external portions of the picture, thereafter manipulating his size, location and orientation controls to register the remaining details in a desired manner.

A function generator especially adapted to produce sweep voltages for the selective tracing of a variety of conic sections includes, in accordance with another feature of this invention, a pair of integrating amplifiers connected in a pair of parallel branches in the output of the processor, these amplifiers being provided with cross-connections for generating conjugate complex functions of time. Given a zero input voltage in one branch and a finite input voltage in the other branch, such a pair of amplifiers will generate trigonometric (sine and cosine) functions if the two cross-connections are of relatively inverted sign, i.e. if one is positive while the other is negative, and will produce hyperbolic functions (sinh and cosh) if the signs are equal. Without cross-connections, the resulting function will be linear after integration in a first amplifier stage and parabolic after similar integration in a second stage.

The above and other features of the invention will be described in detail hereinafter with reference to the accompanying drawing in which:

FIG. 1 is a block diagram of the principal components of a visualization system embodying the invention;

FIG. 2 is a more detailed circuit diagram of some of the components shown in Fig. 1;

FIG. 3 is a schematic representation of a composite instruction code delivered to a service memory shown in Fig. 2;

FIG. 4 is a circuit diagram of an analog function generator included in the system;

FIG. 5 is a somewhat simplified circuit diagram of a hybrid multiplier forming part of a processor included in the system;

FIG. 6 is a block diagram of another part of the processor;

FIG. 7 is a graph showing a selected frame area of a CRT screen for the cropping of a picture displayed by the system; and

FIG. 8 is a block diagram of a comparison circuit serving to determine the intersections of a trace with the boundaries of the frame area shown in Fig. 7.

In Fig. 1 I have shown a main computer 1 exchanging information with an ancillary computer 3, the latter cooperating with a service memory 4 storing data for a digital control unit 5. This controller, which also has input connections from a marker 8 and a keyboard 9, coacts with an analog processor comprising two sections 6, 7. Section 6 establishes the fundamental shape of a basic element to be traced by the beam of a cathode-ray tube 2 whose horizontal and vertical sweep circuits receive respective input voltages from section 7 which specifies the variable parameters defining the position of the trace with reference to the sweep axes. The size of the trace, included among several variables transmitted in digital form to the analog processor 6, 7 from the control unit 5, is communicated to generator section 6 via a channel 60 also carrying the signals which determine the algorithm of such shape (e.g. linear, elliptical or hyperbolic). Another channel 70, whose individual leads are partly illustrated in Fig. 2 described below, conveys the positioning signals to several subsections of section 7 shown in Fig. 2 at 7E (for the basic elements), 7G (for the groups) and 7F (for the figures).

Thus, a typical code word delivered in binary form from ancillary computer 3 to memory 4 may be divided into three parts as illustrated in Fig. 3, i.e. a classification part E_{ijk} denoting the i^{th} element of the i^{th} group of the k^{th} figure, a characterization part N identifying the geometrical shape, and a modification part LT giving original size (L) as well as transformation (T) including commands for translational and/or rotational displacement with reference to the origin as well as possible enlargement or reduction.

Calculating unit 3, which generates the code word of Fig. 3, may be physically separated from the main computer 1 and could, in fact, be linked to it (or to some other source of binary data) via a transmission line or radio channel.

The construction of units 5–7 will now be described in greater detail with reference to Fig. 2.

Fig. 2 shows an input register 10 and an output register 11 associated with memory 4, together with a transfer register 12 in unit 5 receiving the instructions called out from the memory and distributing them through a gating network 13 pursuant to the directions contained in the classification part of the code work shown in Fig. 3. (It should be noted in this connection that instructions relating to groups and figures, rather than to basic elements, lack the second part N and the portion L of the third part of the code.) The timing and programming of the readout of memory 4 is controlled by conventional circuits not further illustrated.

The output of memory 4, as emitted by gating network 13, is channeled over a multiplicity of leads collectively designated 50 delivering the binary information L, N (Fig. 3) to correspondingly designated registers via respective leads 51, 52 and to elemental, group and figure transformation registers T_1E ... T_nE, T_1G ... T_nG, T_1F ... T_nF by way of leads 53–58. Registers L, N and T_1... T_nE are duplicated at $(L)\nu$, $(N)\nu$,$(T_1.\nu$ ... $(T_nE)\nu$ to provide for the storage of a new set of elemental instructions while digital commands for the tracing of a previously selected element are transmitted to analog processor 6, 7 by way of corresponding output leads 61, 62, 73, 74. The output leads of registers T_1G ... T_nG and T_1F ... T_nF, also carrying digital commands, have been designated 75–78.

Unit 5 further comprises three address registers AE (element), AG (group) and AF (figure), the first of these being again duplicated at (AE) for dealing with consecutively called-out elements. These address registers receive their information from input register 10 over leads collectively designated St and feed it back to calculator 3 and also, via a signal path SR, to register 10 for conditioning same to switch to the next group or figure after all the constituents of such higher-order grouping have been processed; lead SR does not serve the register AE.

The several registers shown in Fig. 2 may be conventionally provided with ferrite cores or the like for the storage of the individual bits of each message or word received. Registers 10 and 11 may be included in the associated memory 4. This memory may also store various commands for controlling the intensity of the beam of tube 2 (Fig. 1) and performing other ancillary functions, under the control of computer 3 and/or an associated programmer not shown, in a manner only peripherally relevant to the present improvement.

All the data relating to a given display, received from computer 3, may be stored in register 10 for an indefinite period to facilitate repetitive reproduction of the same image at rates fast enough to create the impression of a persistent image. This image may be subject to modification with the aid of, for example, the manually operable units 8, 9 of Fig. 1 as more fully described hereinafter. Unit 8 may comprise a conventional tracker ball or any other means for marking a selected part of the display in order to make the computer 3 receptive to new information (e.g. fed in via keyboard 9) concerning this part. Reference may be made in this connection to two copending U.S. Pat. applications filed by me jointly with others; i.e. Ser. No. 692,026, dated 20Jan. 1967 and Ser. No. 20,369 dated 17 Mar. 1970. The first of these two applications, now Pat. No. 3,559,182, disclosed an electronic stylus or pointer with photoelectric means for picking up the luminous spot of a CRT beam on the screen of the tube to give a signal at the precise instant when that beam traverses a selected location; the second application

describes the generation of voltages corresponding to the cotordinates of a selected point by an electric transducer responsive to mechanical pressure locally applied to the screen.

I shall now describe the operation of the system to the extent that it is performed automatically, without the intervention of a local operator, under the control of calculator **3** receiving its digital input from main computer **1** (Fig. **1**) either directly or after storage on a tape or the like.

Thus, at the instant when the programmer signals the beginning of a display cycle, memory **4** may contain in its register **10** a number of code words F_kT_{fk} indicating one or more transformations to which each figure of the display is to be individually subjected; a number of code words $G_{jk}T_{gjk}$ specifying the transformations to be undergone by any group G_j of any figure F_k ; and a number of composite code words of the type shown in Fig. **3**, relating to all the elements E_i of each group G_j of any figure F_k . Advantageously, this memory is programmed to read out first the instructions F_1T_{f1} , $F_1T_{f1'}$, $_{F1}T_{f1''}$ pertaining to the first figure; when all these instructions are decoded by gating network **13** and routed to the proper buffer registers T_1F ... T_nF in the "figures" set, register **10** generates an identification signal on multiple St to enter in register AF the address (here "**1**") of the figure being processed. Register AF , via multiple SR , reports this address to register **10** while gating network **13**, upon decoding a switchover command issuing from memory **4** at that point, energizes a lead *Sa* to cause a shift within register **10** from figure processing to group processing with readout of the instructions $G_{11}T_{g11}$, $G_{11}T_{g11'}$,etc. relating to the first group of the first figure. It should be noted that all instructions concerning a particular configuration (element, group or figure) are transferred in parallel from memory **4** via buffer registers **11**, **12** to network **13**.

In a manner analogous to that described above with reference to the processing of figures, the completion of the loading of any register or combination or register in "group" set T_1G ... T_nG causes entry of the address of this group in register AG with feedback to register **10**. In response to another switchover command, network **13** again energizes the lead *Sa* to initiate a shift to element treatment with readout of the corresponding instructions. The "N" part of the code word shown in Fig. **3** is merely a progressively increasing numerical value that steps the "element" section of memory **10** , essentially a binary counter, to call forth the several elements of the group in a predetermined sequence from a roster stored in a section of memory **4**. Thus, for example, *N*=1 may signify a straight line, *N*=2may be a circle, *N*=3 may designate a parabola, whereas two multiplicities of values of *N* may be assigned to ellipses and hyperbolas with different axial ratios.

Again, the identity of each element read out is stored on address register AE as soon as registers L, N, T_1E – T_nE have been loaded. During the time slot immediately following the one in which the first element was read out (the number of such time slots in a display cycle or frame varying according to the complexity of the picture); the second element of the first group of the first figure is called forth; to make room for the corresponding information, the data heretofore stored in registers T_1E ... T_nE, N, L and AE are transferred at this point to the respective companion registers $(T_1E)v$, ... $T_nE)v$, $(N)v$, (L)vand (AE)*v* for the control of processor stages **6** and **7E** as well as the reporting to calculator **3** of the identity of the element being traced. This duplication of registers, therefore, considerably accelerates the translation of coded instructions into a visual display.

When the entire roster of elemental shapes has been scanned in the synthesis of the first group of the first figure, network **13** responds to another (reverse) switchover command to instruct register **10** to shift back to group selection but to read out the data pertaining to the group immediately following the group just processed, i.e. the one whose address (here "**2**") is greater by 1than the address now stored in register AG. That second group is then treated in the same manner as the group preceding it, and the completed processing of all the groups of the first figure gives rise to another "reverse" switchover command for restarting the same sequence of operations on the groups and elements of the next figure, i.e. the second one of the display as determined from the address stored in register AF. When all the figures have been thus displayed, the system starts a new frame by shifting back to the first figure.

If an operator wishes to alter or replace any element of the display, he may identify it to the computer by his marker **8** with the aid of the information available to calculator **3** from address registers AF , AG and (AE)*v*. To change the geometric law of the trace, for example, he may depress a modification key and one or more alphanumerical keys on keyboard **9** (Fig. **1**) so as to substitute another "N" value for the original one, that new value being then read out by the register **10** in its proper numerical place but with the same position-indicating parameters to make it appear at the location previously occupied by the former shape. The modified data then remain stored in register **10** until a new modification occurs or the entire display is canceled.

Processor section **6** may include, ahead of a function generator proper, a digital/analog converter operating on the binary codes transmitted via the multiple represented by lead **61**. Multiple **62** may control a variety of switches as described hereinafter with reference to Fig. **4**. Modification sections **7E**, **7G**, **7F** may include hybrid multipliers, advantageously of the type described below in connection with Fig. **5**, to form the product between the analog values (i.e. voltages) issuing from section **6** and the digital magnitudes transmitted by way of leads **73** – **78**.

The sweep x_c Xc and y_c appearing in the outputs of the two signal channels X and Y of Fig. **2** are fed to the horizontal and vertical scanning circuits, respectively, of cathode-ray tube **2** (Fig. **1**). Though the final magnitudes of these output voltages are determined by the cascaded modifiers **7E**, **7G** and **7F** following the processor section **6**, their law of variation (within a time slot allotted to the tracing of a graphic element) is established by the function generator or generators in that section which could be selectively switched in and out under the control of register N(*v*) and multiple **62**. In accordance with an important feature of the invention, however, it is preferable to use for this purpose a single amplifier unit adapted to generate all the functions discussed above, i.e. straight lines and conic sec-

tions. Such a universal function generator, shown in Fig. 4, has two parallel branches designed to convert a pair of fixed input voltages v_x and v_y into the desired output voltages x_c and y_c. Voltages v_x and v_y are the analog equivalents of the digitized values transmitted from register (L)v over multiple **61** (Fig. 2).

The "x" branch of the function generator comprises an operational amplifier A_x of the feedback-stabilized type, a first integrating amplifier I_{1x} with a differentiating feedback circuit including a capacitor C_x and a resistor R_x, and a similarly designed second integrating amplifier I_{2x}; amplifier A_x feeds amplifier I_{1x} through an electronic switch **21** and is connected to the output of the latter through a feedback loop including a resistor R'_x. Another electronic switch **25** enables selective energization of the second-stage integrator I_{2x} from either the first integrating stage I_{1x} or amplifier A_x. All the switches shown in Fig. **4** are controlled by commands transmitted via multiple **62** (Fig. 2).

The "y" branch of the function generator of Fig. **4** is identical with the "x" branch and comprises an operational amplifier A_y, two integrating amplifiers T_{1y}, I_{2y}, a feedback capacitor C_y, resistors R_y, R'_y, and switches **22, 26**. The two branches are connected by a first path, extending from the output of amplifier I_{1x} through a multiplier M_1 and a resistor R_1 to the input of amplifier I_{1y}, and a second path, analogously extending from the output of amplifier I_{1y} through a multiplier M_2 and a resistor R_2 to the input of amplifier I_{x1} . The two cross-connecting circuits may be broken with the aid of switches **23, 24**. Multipliers M_1 and M_2, which are advantageously of the hybrid type described hereinafter, receive respective factors K_1 and K_2 o from unit **5** via lead **62** (Fig. 2).

Switches **21**, **22** open and close periodically, in response to clock pulses from a timer feeding the lead **50** of Fig. **2**, to allow for the establishment of the selected starting conditions in the outputs of amplifiers A_x and A_y before the function generator is made operational for the remainder of the corresponding time slot. Generally, the following choices are possible:

(a) Generation of straight line. Switches **25** and **26** are reversed to cut out the first integrating stages I_{1x} and I_{1y}; the output voltages of stages I_{2x} and I_{2y} are linear functions of time t given by

$$\text{ti } x_c = p_x t + q$$

$$x_y = p_y t + q_y$$

with the parameters p_x, p_y determined by the applied voltages v_x, v_y and with the constants q_x, q_y additively (or subtractively) superimposed in the outputs of amplifiers I_{2x}, I_{2y}. Circuit breakers **23** and **24** remain open.

(b) Generation of parabolic segment. Circuit breakers **23** and **24** are still open whereas one of the two switches **25**, **26** is in its illustrated position, with cascading of the corresponding integrating stages. If, for example, switch **26** is in that normal position, output voltage x_x has the value given above whereas voltage v_y follows the law

$$v_y = p_y t^2 + q_y t + r_y$$

where, again, the parameters p_y, q_y and r_y are independently determined.

(c) Generation of hyperbolic segment. The time the circuit breakers **23, 24** are closed and the switches **25, 26** are in their illustrated normal position. A sinh (or cosh) function appearing in the output of either integrator I_{1x}, I_{1y} returns to its input as the conjugate of that function while a like conjugate is added thereto over the cross-connection from the companion stage. So long as the amplifiers do not become overloaded within the allotted time slot, the system in this and the preceding cases may be regarded as stable (i.e. nonoscillatory).

(d) Generation of ellipse or segment thereof. The stable system of the preceding paragraph is modified by relatively inverting the signs of the cross-fed voltages. For this purpose, a sign inverter **27** has been diagrammatically illustrated in Fig. **4** together with a switch **28** adapted to insert it in the circuit leading from amplifier I_{1x} to amplifier I_{2y}. This causes oscillations at a frequency determined by the fixed circuit parameters and by the selected input voltages, v_x, v_y as well as magnification factors K_1, K_2. The immediate output voltages of integrator stages I_{2x}, I_{2y} are conjugate trigonometric functions (sine and cosine or vice versa) of ωt (ωbeing the pulsatance of the oscillation) of equal amplitudes, thus defining a circle as a special case of an ellipse. Further multipliers (not shown) in the outputs of integrating amplifiers I_{2x} and I_{2y} may then individually modify these amplitudes in order to provide an ellipse of desired axial ratio; in the same manner the hyperbolic function referred to in the preceding paragraph may be altered.

The postulated generation of circular and hyperbolic traces under the conditions described above may be verified by the following considerations:

If amplifiers I_{1x} and I_{1y} have identical forward gains and feedback factors of absolute magnitudes α and β, respectively, and if (with inverter **27** disconnected by switch **28**) the input voltages v_{ox}, v_{oy} of stages I_{1x}, I_{1y} are considered to satisfy the relationships $v_{ox} = A \sinh zt$ and $v_{oy} = A \cosh zt$, then amplifier I_{1x} has an output $v_{1x} = A/z\ \alpha \cosh zt$ whereas amplifier I_{1y} supplies an output voltage $v_{1y} = A/z\ \alpha \sinh zt$. Input voltage v_{ox} must equal the sum of its own feedback voltage, applied through condenser C_x, and the cross-fed voltage $K_2 v_{1y}$ from the output of multiplier M_2. Similarly, input voltage must equal the sum of its own feedback voltage from condenser C_y and the cross-feed voltage $K_1 v_{1x}$ from multiplier M_1. We therefore obtain the relationships

$$A \sinh zt = A\,\alpha\,\beta \sinh zt + A/z(K2)\,\alpha \sinh zt \quad (1).$$

and

$$A\,A \cosh zt = A\,\alpha\,\beta \cosh zt + A/z(K1)\,\alpha \cosh zt \quad (2).$$

whence

$$z = K_2\,\alpha/(1-\alpha\beta) = K_1\,\alpha/(1-\alpha\beta) \quad 3.$$

so that the system is in equilibrium if $K_1 = K_2 = K$ and

$$z = K\,\alpha/(1-\alpha\beta). \quad 4.$$

At $t = 0$,i.e. upon closure of switches **21** and **22**, v_{ox} must be zero if the sinh function is to develop in the "x" branch. The initial magnitude A of voltage v_{oy} then represents the half-axis of an equilateral hyperbola. The double integration in stages I_{1x} and I_{1y} preserves

the sinh function in the output x_c so that, in the absence of subsequent shifting or rotation, the vertex of the hyperbola comes to lie on the vertical axis of the screen.

Let us now assume that the input voltages of amplifiers I_{1x} and I_{1y} satisfy the relationships $v_{ox} = A\alpha \sin \omega t$ and $v_{oy} = A\alpha \cos \omega t$. The corresponding output voltages then have the form $v_{1x} = -(A)/(\omega)\alpha \cos \omega t$ and $v_{1y} = (A)/(\omega)\alpha \sin \omega t$, respectively.

The foregoing equations now become

$$A \sin \omega t = A\alpha\beta \sin \omega t + (A/\omega)(K_2)\alpha \sin \omega t \quad 1'.$$

and

$$A \cos \omega t = A\alpha\beta \cos \omega t - A/\omega (K_1)\alpha \cos \omega t \quad 2'.$$

whence

$$\omega = K_2\alpha/(1-\alpha\beta) = -K_1\alpha/(1-\alpha\beta) \quad 3'.$$

so that the system is in equilibrium if $K_1 = -K_2$ or $K_2 = K$, $K_1 = -K$ with

$$\omega = K\alpha/(1-\alpha\beta). \quad 4'.$$

The insertion of inverter **27** (or an equivalent modification of multiplier M_1 therefore creates the requisite conditions for such oscillatory operation.

As before, the amplitudes of the two conjugate functions in the outputs of the two-stage integrators will be the same so that the trace, if not modified in the signal paths beyond stages I_{2x} and I_{2y}, will be a circle. The sine function develops in the branch having the starting voltage *0* applied to it, the magnitude *A* of the other input voltage representing the radius of the circle.

It is desirable to make the peripheral tracing speed independent of radius, in order to simply the task of the computer in measuring a desired length of arc. Since, in a circle, this tracing speed equals the radius times the angular velocity ω, *K*,since the latter varies directly with the multiplication factor K , this constancy can be achieved by making the amplitude *A* inversely proportional to *K* so that the finite input voltage, e.g. v_y , is increased with decreasing multiplication factors and vice versa. Since the second integration at I_{2x} , I_{2y} again introduces the magnitude of ω and therefore of *K* into the denominator of the voltage function v_{2x} , v_{2y} generated by the system of Fig. **4**, the final radius still depends on the choice of *K*. Similar considerations apply to the tracing of ellipses and hyperbolae. On the CRT screen itself, of course, the tracing speed will depend on the chosen parameters, yet the computer need only take into consideration the magnifications or reductions, if any, occurring beyond stages I_{1x} , I_{1y} .

Other exponential functions may be established, for example, by operating the system of Fig. **4** with equal starting voltages v_x , v_y and with inverter **27** disconnected, there being no finite values of *t* for which the cosh and sinh functions are identical.

In Fig. **5** I show a hybrid multiplier suitable for use in the function generator of Fig. **4** as well as in any of the modifying subsections **7E**, **7G**, **7F** of processor section **7**. A ladder-type resistance network **38** is connected between a terminal **34** of fixed reference potential (here ground) and the input **35** of an operational amplifier **36** having an output **39**. Network **38** has two terminal sections of magnitude *R* separated by a multiplicity of series arms of half that magnitude, the junctions of these series arms with one another and with the two terminal sections being connected to respective shunt arms also of magnitude *R* . Each shunt arm is connected to a pair of input terminals **32**, **33**, by way of respective gating elements here shown as field-effect transistors FET_1 , FET_2 , the gates of these transistors being tied to the output of an associated AND gate **30** with interposition of an inverter **31** in the case of transistor FET_2. All the AND gates **30** have one terminal tied to a source of blocking potential (here positive) represented by a terminal **37**. The other input of each AND gate is tied to an individual conductor of a multiple carrying a multidigit binary value *M*, such as the multiples illustrated as leads **73**– **78** in Fig. **2**. These conductors have been labeled 2^0 , 2^1, 2^2 , ... 2^{n-1} , 2^n , according to their denominational ranks in the binary code.

Input terminal **32** is assumed to be held at a fixed potential equal to that of terminal **34** (ground) so that an input voltage applied to network **38** at any point between amplifier **36** and one of the network junctions is reduced in a predetermined ratio, consistent with the digital position of the corresponding shunt arm, when the respective AND gate **30** is nonconductive whereby field-effect transistor FET_1 is saturated and represents a negligible resistance. An analog voltage V_e to be multiplied by the magnitude of number *M* appears on terminal **33** but cannot pass the companion transistor FET_2 under these conditions, that transistor being cut off by the inversion of the AND gate output at circuit **31**. Conversely, if the second input of any AND gate **30** is energized, the associated transistor FET_1 is blocked while the companion transistor FET_2 is saturated so as to give passage to voltage V_e . With only the lowest-order conductor 2^0 energized, for example, the magnification factor is unity; thus, the gain of amplifier **36** should be so chosen that the potential of terminal **39** equals that of terminal **33** under these conditions. With other digital inputs energized, the output voltage at terminal **39** is then a multiple $M{:}V_e$ of the analog input voltage V_e .

The network of Fig. **5** can be easily adapted for use with complementary binary codes (i.e. with designation of a bit by the absence rather than presence of voltage on the correspondingly conductor 2^0– 2^n by the simple expedient of reversing the input connections by grounding the terminal **33** and applying the potential V_e to terminal **32**.

Moreover, if a voltage of unity value is applied to the live terminal **33** (or **32**), this system will operate as a digital/analog converter. As such it may be used, for example, in processor section **6** ahead of the function generator described with reference to Fig. **4**.

As compared with conventional voltage-dividing networks using weighted resistances, the circuit arrangement of Fig. **5** offers the additional advantages of simplified manufacture (requiring only two calibrated resistance values R and R/2), operativeness with resistors of relatively low magnitudes, and a constant input resistance as seen from voltage source V_e.

Fig. **6** shows a circuit, adapted to be used in any of the processor subsections **7E**, **7G**, **7F**, for selectively displacing a generated trace by translation and/or rotation. This circuit includes four multipliers **40**, **41**, **43**, **44**, each preferably of the hybrid type just described, and two conventional adders **42**, **45**. An analog voltage

x'_c from a preceding stage is applied to the analog inputs (**32**, **33** in Fig. **5**) of multipliers **40** and **44** in parallel, a companion voltage y'_C being similarly applied to multiplier **41** and **43**. If the trace is to be rotated through an angle θ, multipliers **40** and **44** receive at their binary inputs (M, Fig. **5**) the digitized magnitudes of cos θ while the other two multipliers similarly receive the magnitude of sin θ. Adders **42** and **45**, respectively receiving the outputs of multipliers **40**, **41** and multipliers **43**, **44** perform the operations

$$x''_c = x'_c \cos\theta - y'_c \sin\theta$$

$$y''_c = x'_c \sin\theta + y'_c \cos\theta$$

which represents the desired inclination of the co-ordinate system by the angle θ. A translational shift, such as those needed to add a constant in the above-discussed formulas for straight lines and conic sections, may be carried out with the aid of further voltages x_T and y_T applied to additional inputs of adders **42** and **45**, respectively. A simple shift occurs with $\theta = 0$, i.e. zero voltages at the binary inputs of multipliers **41** and **44** along with unit voltages at the corresponding inputs of the other two multipliers.

The circuitry of Fig. **6** allows for the original plotting of straight lines along one or the other co-ordinate axis, followed by a suitable rotation, which further simplifies the task of the calculator.

Fig. **7** illustrates part of the screen of a cathode-ray tube on which an elemental trace **100** is being displayed. By depressing special keys on the keyboard **9** of Fig. **1**, and by the use of some numerical keys thereof in selected combinations, the operator has chosen two pairs of constant potentials X_1, X_2, Y_1 and Y_2 (Fig. **8**) corresponding to specific values of the deflecting voltages for the sweep circuits of the tube, thereby establishing two imaginary vertical lines V_1, V_2 with abscissae x_1, x_2 and horizontal lines H_1, H_2 with ordinates y_1, y_2 as measured along axes x and y. The part of trace **100** within the area framed by these four lines is to be explored in detail, the remaining portions being of no interest.

Points P_1, P_2, P_3, P_4 mark the intersections of the trace with the boundaries of the desired area. It will be seen that, in this example, trace **100** cuts the line V_1 once (at P_1) from without, the line H_1 once (at P_4) from within, the line H_2 twice (at P_2, P_3) and the line V_2 not at all.

As shown in Fig. **8**, the selected potentials X_1, X_2, Y_1, Y_2 are fed to respective digital/analog converters, such as that described with reference to Fig. **5**, respectively designated **101**, **102**, **103**, **104** and working into associated comparators **201**, **202**, **203**, **204**. The first two comparators also receive the sweep voltage x_c from the channel X (Fig. **2**) while the two other comparators receive the companion voltage y_c. The output of each comparator is transmitted to a two-stage shift register **301**, **302**, **303**, **304**, this number of stages being sufficient inasmuch as no second-order curve can intersect a given line more than twice.

When the sweep voltage y_c matches the analog equivalent of the limiting voltage X_1 or X_2, comparator **201** or **202** responds and trips the associated shift register **301** or **302**. Similarly, a coincidence of voltage y_c with either limiting voltage Y_1, Y_2 actuates the comparator **203** or **204** to step the corresponding shift register **303** or **304**. In the outputs of these shift registers there are thus generated up to eight possible signal pulses $S_{1,1}$, $S_{1,2}$, $S_{2,1}$, $S_{2,2}$, $S_{3,1}$, $S_{3,2}$, $S_{4,1}$, $S_{4,2}$ which mark the intersections between the trace **100** and the frame in Fig. **7**. Thus, point P_1 gives rise to a marker pulse $S_{1,1}$ from register **301**, points P_2 and P_3 trigger the register **304** to generate marker pulses $S_{4,1}$ and $S_{4,2}$, and point P_4 causes the emission of a marker pulse $S_{3,1}$ by register **303**. All these registers are, of course, automatically reset at the end of each time slot so that similar information can be obtained on other elements crossing or touching the boundaries of the frame.

In this manner, the calculator **3** receiving the marker pulses can ascertain from the contents of address registers (AE)v, AG, AF the identity of such an element; having available all the data relating to the nature and position of that element, it may then compute the extent to which it falls within the selected frame area and give instructions to memory **4** (Fig. **2**) for the suppression of the remainder in subsequent cycles. The cropped picture within that area may then be magnified (and shifted, if necessary) by the aforedescribed modification circuits without extensive recalculation.

The system of Fig. **8** is illustrative of a variety of means enabling an operator to communicate with the computer, through the intermediary of the control unit **5**, in producing or changing a display. Such communication is also possible with the aid of various marking implements, e.g. the photoelectric stylus of U.S. Pat. No. 3,559,182 enabling the free-hand tracing of pictures on a conventionally illuminated screen with transformation of the data into digital information by the main computer **1**.

Of course, the invention is not limited to the embodiments described and shown which has been given solely by way of example.

I claim:

1. A system for the visualization of graphic symbols on the screen of a cathode-ray tube provided with scanning means for controlling the position of its beam, said symbols being composed of groupings of basic elements, comprising:

memory means for storing a variety of instructions for said scanning means in digital form;

a first set of registers connected to said memory means for receiving therefrom instructions relating to said basic elements;

a second set of registers connected to said memory means for receiving therefrom instructions relating to said groupings;

an analog processor interposed between said memory means and said scanning means, said processor including function-generating means controllable by the contents of said first set of registers and function-modifying means in cascade with said function-generating means having a first section operating on the output of said function-generating means in response to the contents of said first set of registers, said function modifying means having a second section operating on the output of said first section in response to the contents of said second set of registers;

first address means for successively calling forth instructions relating to different basic elements of a

grouping from said memory means for temporary storage in said first set of registers to control said first section of said function modifying means;

second address means for successively calling forth instructions relating to different groupings from said memory means for temporary storage in said second set of registers to control said second section of said function-modifying means; and

computer means for programming said first and second address means to read out to said first set of registers the instructions relating to all the elements of one grouping identified by said second address means before shifting to the instructions relating to all the elements of the next grouping so identified.

2. A system as defined in claim **1** wherein said first set of registers are duplicated for preserving instructions relating to one element during readout of instructions relating to the next element.

3. A system as defined in claim **1** wherein said function-generating means include size and shape generators, said function-modifying means including transformation generators.

4. A system as defined in claim **3** wherein said function-generating means includes other transformation generators controllable by certain of said first set of registers.

5. A system for the visualization of graphic symbols on the screen of a cathode-ray tube provided with scanning means including a pair of orthogonally related sweep circuits for controlling the position of its beam, comprising:

memory means for storing a variety of digital instructions for controlling the operation of said scanning means;

a control unit connected to said scanning means;

an analog processor interposed between said control unit and said scanning means, said processor including function-generating means responsive to certain of said instructions and function-modifying means responsive to other of said instructions, said processor having output connections to said scanning means for applying analog sweep voltages thereto according to parameters established by said function-generating and function-modifying means, said control unit receiving such instructions from said memory means and distributing same between said function-generating means and said function-modifying means;

and computer means having access to said memory means for calling out any of said instructions to said control unit;

said function-generating means including first operational amplifier means with two cascaded integrating stages in a first channel connected to generate a signal voltage for one of said sweep circuits and second operational amplifier means with two cascaded integrating stages in a second channel connected to generate a signal voltage for the other of said sweep circuits;

said function-modifying means including switch means for selectively establishing cross-connections from a first-stage output of either of said operational amplifier means to a first-stage input of the other operational amplifier means and independently settable multiplication networks in said cross-connections for generating complex conjugate functions of time.

6. A system as defined in claim **5** wherein said switch means includes sign-inverting means in at least one of said cross-connections for the selective generation of trigonometric and hyperbolic functions.

7. A system as defined in claim **5** wherein said function-modifying means includes bypass switches for selectively cutting out the first integrating stage of either of said amplifier means.

8. A system as defined in claim **5** wherein said multiplication networks are hybrid networks with a multiplicand input for analog voltages and a multiplier input for digital signals.

9. A system as defined in claim **8** wherein each of said hybrid networks comprises a ladder-type resistance network with a plurality of shunt branches connected in parallel to said multiplicand input and individual gates between said multiplicand input and said shunt branches having control leads connected to said multiplier input.

10. A system as defined in claim **9** wherein said shunt branches are resistors of identical magnitude and are separated by series resistors of half said magnitude bracketed between two terminal resistors of said magnitude.

11. A system as defined in claim **5** wherein one set of said instructions relates to basic elements of a symbol to be displayed whereas another set of said instructions relates to groups of such basic elements arrayed in selected combinations, said function-modifying means including circuitry divided into a first subsection for the processing of individual elements and at least one other subsection for the processing of higher-order groupings.

12. A system as defined in claim **11** wherein said control unit comprises a first set of registers for the control of said function-generating means and said first subsection, and a second set of registers for the control of said other subsection, said first set of registers being duplicated for controlling said processor to trace an element to be visualized and for simultaneously registering information relating to a subsequent element.

13. A system as defined in claim **11** wherein said control unit includes respective address registers for the temporary identification of the element and the group represented by the last instructions read out from said memory means, said address registers being provided with feedback connections to said memory means for enabling same to deliver instructions for successive elements in consecutive groups in a predetermined order.

14. A system as defined in claim **5**, further comprising selector means for establishing two limiting values for each signal voltage and comparison means connected to said channels and to said selector means for transmitting a marker pulse to said computer means upon coincidence of either of said signal voltages with either of the two limiting values established therefor.

15. A system as defined in claim **14** wherein said comparison means comprises two pairs of coincidence circuits and two pairs of shift registers respectively connected to said coincidence circuits for emitting a marker pulse any time a trace of said beam, produced under the control of said processor, reaches the outline of a rectangular area defined by said limiting values.

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