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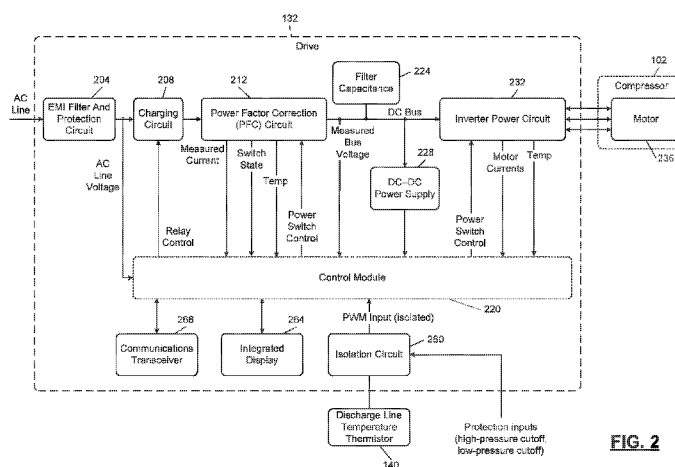


FIG. 2

(57) Abstract: A converter circuit is provided and includes: a first EMI filter connected to AC lines and includes one or more across-the-line capacitors; a charging circuit that receives power from the first EMI filter and limits an amount of current passing from the first EMI filter to a DC bus; and a PFC circuit of a compressor drive that provides PFC between an output of the charging circuit and a generated first DC voltage. The PFC circuit includes: a rectification circuit that rectifies the power from the AC lines or a charging circuit output; and a second EMI filter connected downstream from the rectification circuit and including a DC bus rated capacitor. The second EMI filter outputs a filtered DC signal based on a rectification circuit output. The PFC circuit, based on the second EMI filter output, outputs the first DC voltage to the DC bus to power the compressor drive.

CHOKES AND EMI FILTER CIRCUITS FOR POWER FACTOR CORRECTION CIRCUITS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a PCT International Application of U.S. Application No.

5 15/487,201, filed on April 13, 2017. This application claims the benefit of the earlier filing date and right of priority to U.S. Provisional Application No. 62/323,607, filed on April 15, 2016, and U.S. Provisional Application No. 62/398,668, filed on September 23, 2016. The entire disclosures of the applications referenced above are incorporated herein by reference.

FIELD

10 **[0002]** The present disclosure relates to source EMI filters, protection circuits, and power factor correction circuits including AC-to-DC converters with active switch control.

BACKGROUND

[0003] The background description provided herein is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent the work is
15 described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] Compressors are used in a wide variety of industrial and residential applications including, but not limited to, heating, ventilating, and air conditioning (HVAC) systems. Electric
20 motors are used to power and/or actuate elements of the compressors. A control system for controlling operation of an electric motor of a compressor can include a drive. The drive can include a power factor correction (PFC) circuit for providing power factor correction between an inputted alternating current (AC) and a generated direct current (DC).

[0005] A power factor is an indicator of a relationship between current and voltage in a circuit,
25 or how effectively a circuit uses actual electrical power as compared to reactive power, which is stored and returned to a power source. A power factor can be expressed as a value between zero and one. A power factor can be equal to a ratio of actual electrical power dissipated by a circuit relative to a product of root mean squared (RMS) values of current and voltage for the circuit. The power factor approaches 1 as this ratio increases. The PFC circuit can be implemented to
30 increase a power factor of a drive, thereby increasing an amount of actual electrical power used

by the circuit as compared with an amount of reactive power the circuit stores and returns to the power source.

SUMMARY

- [0006]** A converter circuit is provided and includes a first electromagnetic interference filter, a charging circuit, and a power factor correction circuit of a compressor drive. The first electromagnetic interference filter is connected to AC lines and includes one or more across-the-line capacitors. The charging circuit is configured to (i) receive power from the first electromagnetic interference filter, and (ii) limit an amount of current passing from the first electromagnetic interference filter to a DC bus. The power factor correction circuit is configured to provide power factor correction between an output of the charging circuit and a generated first DC voltage. The power factor correction circuit includes: a rectification circuit configured to rectify the power from the AC lines or an output of the charging circuit depending on whether the rectification circuit is upstream or downstream from the charging circuit; and a second electromagnetic interference filter connected downstream from the rectification circuit and including one or more DC bus rated capacitors. The second electromagnetic interference filter is configured to output a filtered DC signal based on an output of the rectification circuit. The power factor correction circuit is configured to, based on the output of the second electromagnetic interference filter, output the first DC voltage to the DC bus to power the compressor drive.
- [0007]** In other features, a converter circuit is provided and includes a charging circuit and a power factor correction circuit of a compressor drive. The charging circuit is configured to (i) receive power based on power from AC lines, and (ii) limit an amount of current passing to a DC bus. The power factor correction circuit is configured to provide power factor correction between an output of the charging circuit and a generated first DC voltage. The power factor correction circuit includes a rectification circuit and a first electromagnetic interference filter. The rectification circuit is configured to rectify the power from the AC lines or an output of the charging circuit depending on whether the rectification circuit is upstream or downstream from the charging circuit. The first electromagnetic interference filter includes one or more DC bus rated capacitors, where the first electromagnetic interference filter is configured to output a filtered DC signal based on an output of the rectification circuit. At least one of the following exists: the converter circuit is void of an across-the-line capacitor upstream from the power factor correction circuit; capacitance of each of the one or more DC bus rated capacitances is less than or equal to a capacitance of each across-the-line capacitor connected upstream from the charging circuit or the rectification circuit; or the converter circuit is void of across-the-line

capacitors. The power factor correction circuit is configured to, based on an output of the first electromagnetic interference filter, output the first DC voltage to the DC bus to power the compressor drive.

- 5 [0008] In other features, a converter circuit is provided and includes a charging circuit and a power factor correction circuit of a compressor drive. The charging circuit is configured to (i) receive power based on power from AC lines, and (ii) limit an amount of current passing to a DC bus. The power factor correction circuit is configured to provide power factor correction between an output of the charging circuit and a generated DC voltage. The power factor correction circuit includes: a rectification circuit configured to rectify the power from the AC
- 10 lines or an output of the charging circuit depending on whether the rectification circuit is upstream or downstream from the charging circuit; and at least one of a common mode choke or a grounded electromagnetic interference filter. The common mode choke or the grounded electromagnetic interference filter is configured to, based on an output of the rectification circuit, output the DC voltage for the DC bus to power the compressor drive.
- 15 [0009] Further areas of applicability of the present disclosure will become apparent from the detailed description, the claims and the drawings. The detailed description and specific examples are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF DRAWINGS

- 20 [0010] FIG. 1 is a functional block diagram of an example refrigeration system.
- [0011] FIG. 2 is a block diagram of an example implementation of the compressor motor drive of FIG. 1.
- [0012] FIG. 3A is a block diagram of an example implementation of the power factor correction (PFC) circuit of FIG. 2.
- 25 [0013] FIG. 3B is a block diagram of another example implementation of the PFC circuit of FIG. 2.
- [0014] FIG. 4 is a schematic diagram of an example of a portion of a PFC circuit of the drive of FIG. 2 including a boost converter in accordance with an embodiment of the present disclosure.
- 30 [0015] FIG. 5 is an example plot of a rectified AC signal, a predetermined DC voltage and operational switch periods in accordance with an embodiment of the present disclosure.

[0016] FIG. 6 is an example plot of sensed current in the drive of FIG. 2 in accordance with an embodiment of the present disclosure.

[0017] FIG. 7 is a schematic diagram of an example electromagnetic interference (EMI) filter in accordance with an embodiment of the present disclosure.

5 [0018] FIG. 8 is a functional block diagram of an example of a PFC switch control module in accordance with an embodiment of the present disclosure.

[0019] FIG. 9 is a flow diagram illustrating an example method of operating a drive with a PFC circuit having a boost converter in accordance with an embodiment of the present disclosure.

10 [0020] FIG. 10 is a schematic diagram of an example of a portion of a PFC circuit of a drive including a buck converter in accordance with an embodiment of the present disclosure.

[0021] FIG. 11 is a flow diagram illustrating an example method of operating a drive with a PFC circuit having a buck converter in accordance with an embodiment of the present disclosure.

15 [0022] FIG. 12 is a flow diagram illustrating an example method of operating a drive with a PFC circuit having a power converter in accordance with an embodiment of the present disclosure.

[0023] FIG. 13 is a functional block diagram of an example of a single phase converter circuit including a non-line non-grounded EMI filter in a PFC circuit in accordance with an
20 embodiment of the present disclosure.

[0024] FIG. 14 is a functional block diagram of another example of a single phase converter circuit including a common mode choke, a protection circuit, and a grounded EMI filter in a PFC circuit in accordance with an embodiment of the present disclosure.

[0025] FIG. 15 is a functional block diagram of another example of a single phase converter
25 circuit including multiple EMI filters in a PFC circuit in accordance with an embodiment of the present disclosure.

[0026] FIG. 16 is a functional block diagram of an example of a 3-phase converter circuit including a non-line non-grounded EMI filter in a PFC circuit in accordance with an embodiment of the present disclosure.

30 [0027] FIG. 17 is a functional block diagram of another example of a 3-phase converter circuit including a common mode choke, a protection circuit, and a grounded EMI filter in a PFC circuit in accordance with an embodiment of the present disclosure.

[0028] FIG. 18 is a functional block diagram of another example of a 3-phase converter circuit including multiple EMI filters in a PFC circuit in accordance with an embodiment of the present disclosure.

5 [0029] FIG. 19 is a functional block and schematic diagram of an example of the converter circuit of FIG. 13.

[0030] FIG. 20 is a functional block and schematic diagram of an example of the converter circuit of FIG. 14.

[0031] FIG. 21 is a functional block and schematic diagram of an example of the converter circuit of FIG. 16.

10 [0032] FIG. 22 is a functional block and schematic diagram of an example of the converter circuit of FIG. 17.

[0033] FIG. 23 is a schematic diagram of an example of the portion of the PFC circuit of FIG. 4 including a common mode choke, a protection circuit, and EMI filters in accordance with an embodiment of the present disclosure.

15 [0034] FIG. 24 is a schematic diagram of an example of the portion of the PFC circuit of FIG. 10 including a common mode choke, a protection circuit, and EMI filters in accordance with an embodiment of the present disclosure.

[0035] FIG. 25 is a functional block diagram of another example of a 3-phase converter circuit including multiple EMI filters and a charging circuit in a PFC circuit in accordance with an
20 embodiment of the present disclosure.

[0036] FIG. 26 is a schematic diagram of an example of a portion of a PFC circuit of the drive of FIG. 2 including a boost converter for a 3-phase implementation in accordance with an embodiment of the present disclosure.

25 [0037] FIG. 27 is a schematic diagram of another example of a portion of a PFC circuit of the drive of FIG. 2 including an inverter and a boost converter for a 3-phase implementation in accordance with an embodiment of the present disclosure.

[0038] In the drawings, reference numbers may be reused to identify similar and/or identical elements.

DESCRIPTION

30 [0039] FIG. 1 is a functional block diagram of an example refrigeration system 100 including a compressor 102, a condenser 104, an expansion valve 106, and an evaporator 108. According to

the principles of the present disclosure, the refrigeration system 100 may include additional and/or alternative components, such as a reversing valve or a filter-drier. In addition, the present disclosure is applicable to other types of refrigeration systems including, but not limited to, heating, ventilating, and air conditioning (HVAC), heat pump, refrigeration, and chiller systems.

5 **[0040]** The compressor 102 receives refrigerant in vapor form and compresses the refrigerant. The compressor 102 provides pressurized refrigerant in vapor form to the condenser 104. The compressor 102 includes an electric motor that drives a pump. For example only, the pump of the compressor 102 may include a scroll compressor and/or a reciprocating compressor.

10 **[0041]** All or a portion of the pressurized refrigerant is converted into liquid form within the condenser 104. The condenser 104 transfers heat away from the refrigerant, thereby cooling the refrigerant. When the refrigerant vapor is cooled to a temperature that is less than a saturation temperature, the refrigerant transforms into a liquid (or liquefied) refrigerant. The condenser 104 may include an electric fan that increases the rate of heat transfer away from the refrigerant.

15 **[0042]** The condenser 104 provides the refrigerant to the evaporator 108 via the expansion valve 106. The expansion valve 106 controls the flow rate at which the refrigerant is supplied to the evaporator 108. The expansion valve 106 may include a thermostatic expansion valve or may be controlled electronically by, for example, a system controller 130. A pressure drop caused by the expansion valve 106 may cause a portion of the liquefied refrigerant to transform back into the vapor form. In this manner, the evaporator 108 may receive a mixture of
20 refrigerant vapor and liquefied refrigerant.

[0043] The refrigerant absorbs heat in the evaporator 108. Liquid refrigerant transitions into vapor form when warmed to a temperature that is greater than the saturation temperature of the refrigerant. The evaporator 108 may include an electric fan that increases the rate of heat transfer to the refrigerant.

25 **[0044]** A utility 120 provides power to the refrigeration system 100. For example only, the utility 120 may provide single-phase alternating current (AC) power at approximately 230 Volts root mean squared (V_{RMS}). In other implementations, the utility 120 may provide three-phase AC power at approximately 400 V_{RMS} , 480 V_{RMS} , or 600 V_{RMS} at a line frequency of, for example, 50 or 60 Hz. When the three-phase AC power is nominally 600 V_{RMS} , the actual
30 available voltage of the power may be 575 V_{RMS} .

[0045] The utility 120 may provide the AC power to the system controller 130 via an AC line, which includes two or more conductors. The AC power may also be provided to a drive 132 via the AC line. The system controller 130 controls the refrigeration system 100. For example only,

the system controller 130 may control the refrigeration system 100 based on user inputs and/or parameters measured by various sensors (not shown). The sensors may include pressure sensors, temperature sensors, current sensors, voltage sensors, etc. The sensors may also include feedback information from the drive control, such as motor currents or torque, over a serial data bus or other suitable data buses.

[0046] A user interface 134 provides user inputs to the system controller 130. The user interface 134 may additionally or alternatively provide the user inputs directly to the drive 132. The user inputs may include, for example, a desired temperature, requests regarding operation of a fan (e.g., a request for continuous operation of the evaporator fan), and/or other suitable inputs. The user interface 134 may take the form of a thermostat, and some or all functions of the system controller (including, for example, actuating a heat source) may be incorporated into the thermostat.

[0047] The system controller 130 may control operation of the fan of the condenser 104, the fan of the evaporator 108, and the expansion valve 106. The drive 132 may control the compressor 102 based on commands from the system controller 130. For example only, the system controller 130 may instruct the drive 132 to operate the motor of the compressor 102 at a certain speed or to operate the compressor 102 at a certain capacity. In various implementations, the drive 132 may also control the condenser fan.

[0048] A thermistor 140 is thermally coupled to the refrigerant line exiting the compressor 102 that conveys refrigerant vapor to the condenser 104. The variable resistance of the thermistor 140 therefore varies with the discharge line temperature (DLT) of the compressor 102. As described in more detail, the drive 132 monitors the resistance of the thermistor 140 to determine the temperature of the refrigerant exiting the compressor 102.

[0049] The DLT may be used to control the compressor 102, such as by varying capacity of the compressor 102, and may also be used to detect a fault. For example, if the DLT exceeds the threshold, the drive 132 may power down the compressor 102 to prevent damage to the compressor 102.

[0050] In FIG. 2, an example implementation of the drive 132 includes an electromagnetic interference (EMI) filter and protection circuit 204, which receives power from an AC line. The EMI filter and protection circuit 204 reduces EMI that might otherwise be injected back onto the AC line from the drive 132. The EMI filter and protection circuit 204 may also remove or reduce EMI arriving from the AC line. Further, the EMI filter and protection circuit 204 protects against

power surges, such as may be caused by lightening, and/or other other types of power surges and sags.

[0051] A charging circuit 208 controls power supplied from the EMI filter and protection circuit 204 to a power factor correction (PFC) circuit 212. For example, when the drive 132 initially powers up, the charging circuit 208 may place a resistance in series between the EMI filter and protection circuit 204 and the PFC circuit 212 to reduce the amount of current inrush. These current or power spikes may cause various components to prematurely fail.

[0052] After initial charging is completed, the charging circuit 208 may close a relay that bypasses the current-limiting resistor. For example, a control module 220 may provide a relay control signal to the relay within the charging circuit 208. In various implementations, the control module 220 may assert the relay control signal to bypass the current-limiting resistor after a predetermined period of time following start up, or based on closed loop feedback indicating that charging is near completion.

[0053] The PFC circuit 212 converts incoming AC power to DC power. The PFC circuit 212 may not be limited to PFC functionality, for example, the PFC circuit 212 may also perform voltage conversion functions, such as acting as a boost circuit and/or a buck circuit. In some implementations, the PFC circuit 212 may be replaced by a non-PFC voltage converter. The DC power may have voltage ripples, which are reduced by filter capacitance 224. Filter capacitance 224 may include one or more capacitors arranged in parallel and connected to the DC bus. The PFC circuit 212 may attempt to draw current from the AC line in a sinusoidal pattern that matches the sinusoidal pattern of the incoming voltage. As the sinusoids align, the power factor approaches one, which represents the greatest efficiency and the least demanding load on the AC line.

[0054] The PFC circuit 212 includes one or more switches that are controlled by the control module 220 using one or more signals labeled as power switch control. The control module 220 determines the power switch control signals based on a measured voltage of the DC bus, measured current in the PFC circuit 212, AC line voltages, temperature or temperatures of the PFC circuit 212, and the measured state of a power switch in the PFC circuit 212. While the example of use of measured values is provided, the control module 220 may determine the power switch control signals based on an estimated voltage of the DC bus, estimated current in the PFC circuit 212, estimated AC line voltages, estimated temperature or temperatures of the PFC circuit 212, and/or the estimated or expected state of a power switch in the PFC circuit 212. In various implementations, the AC line voltages are measured or estimated subsequent to the EMI filter and protection circuit 204 but prior to the charging circuit 208. The control module

220 is powered by a DC–DC power supply 228, which provides a voltage suitable for logic of the control module 220, such as 3.3 Volts, 2.5 Volts, etc. The DC–DC power supply 228 may also provide DC power for operating switches of the PFC circuit 212 and an inverter power circuit 232. For example only, this voltage may be a higher voltage than for digital logic, with 15 Volts being one example.

[0055] The control module 220 is powered by a DC–DC power supply 228, which provides a voltage suitable for logic of the control module 220, such as 3.3 Volts, 2.5 Volts, etc. The DC–DC power supply 228 may also provide DC power for operating switches of the PFC circuit 212 and an inverter power circuit 232. For example only, this voltage may be a higher voltage than for digital logic, with 15 Volts being one example.

[0056] The inverter power circuit 232 also receives power switch control signals from the control module 220. In response to the power switch control signals, switches within the inverter power circuit 232 cause current to flow in respective windings of a motor 236 of the compressor 102. The control module 220 may receive a measurement or estimate of motor current for each winding of the motor 236 or each leg of the inverter power circuit 232. The control module 220 may also receive a temperature indication from the inverter power circuit 232.

[0057] For example only, the temperature received from the inverter power circuit 232 and the temperature received from the PFC circuit 212 are used only for fault purposes. In other words, once the temperature exceeds a predetermined threshold, a fault is declared and the drive 132 is either powered down or operated at a reduced capacity. For example, the drive 132 may be operated at a reduced capacity and if the temperature does not decrease at a predetermined rate, the drive 132 transitions to a shutdown state.

[0058] The control module 220 may also receive an indication of the discharge line temperature from the compressor 102 using the thermistor 140. An isolation circuit 260 may provide a pulse-width-modulated representation of the resistance of the thermistor 140 to the control module 220. The isolation circuit 260 may include galvanic isolation so that there is no electrical connection between the thermistor 140 and the control module 220.

[0059] The isolation circuit 260 may further receive protection inputs indicating faults, such as a high pressure cutoff or a low pressure cutoff, where pressure refers to refrigerant pressure. If any of the protection inputs indicate a fault and, in some implementations, if any of the protection inputs become disconnected from the isolation circuit 260, the isolation circuit 260 ceases sending the PWM temperature signal to the control module 220. Therefore, the control

module 220 may infer that a protection input has been received from an absence from the PWM signal. The control module 220 may, in response, shut down the drive 132.

[0060] The control module 220 controls an integrated display 264, which may include a grid of LEDs and/or a single LED package, which may be a tri-color LED. The control module 220 can provide status information, such as firmware versions, as well as error information using the integrated display 264. The control module 220 communicates with external devices, such as the system controller 130 in FIG. 1, using a communications transceiver 268. For example only, the communications transceiver 268 may conform to the RS-485 or RS-232 serial bus standards or to the Controller Area Network (CAN) bus standard.

[0061] In FIG. 3A, a PFC circuit 300 is one implementation of the PFC circuit 212 of FIG. 2. The PFC circuit 300 includes a rectifier 304 that converts incoming AC into pulsating DC. In various implementations, the rectifier 304 includes a full-wave diode bridge. The DC output of the rectifier 304 is across first and second terminals. The first terminal is connected to an inductor 308, while the second terminal is connected to a current sensor 312. An opposite end of the inductor 308 is connected to a node that is common to the inductor 308, an anode of a diode 316, and a first terminal of a switch 320.

[0062] The PFC circuit 300 generates a DC bus, where a first terminal of the DC bus is connected to a cathode of the diode 316 while a second terminal of the DC bus is connected to the second output terminal of the rectifier 304 via the current sensor 312. The current sensor 312 can therefore sense the current within the switch 320 as well as the current in the DC bus and current in the inductor 308. The second terminal of the DC bus is also connected to a second terminal of the switch 320.

[0063] A driver 324 receives the power switch control signal from the control module 220 of FIG. 2 and rapidly charges or discharges a control terminal of the switch 320. For example, the switch 320 may be a field effect transistor with a gate terminal as the control terminal.

[0064] More specifically, the switch 320 may be a power metal-oxide-semiconductor field-effect transistor (MOSFET), such as the STW38N65M5 power MOSFET from STMicroelectronics. The driver 324, in response to the power switch control signal, charges or discharges the capacitance at the gate of the field effect transistor.

[0065] A switch monitor circuit 328 measures whether the switch is on or off. This closed loop control enables the control module 220 to determine whether the switch 320 has reacted to a command provided by the power switch control signal and may also be used to determine how long it takes the switch 320 to respond to that control signal. The measured switch state is output

from the switch monitor circuit 328 back to the control module 220. The control module 220 may update its control of the power switch control signal to compensate for delays in turning on and/or turning off the switch 320.

[0066] In FIG. 3A, the inductor, the switch 320, and the diode 316 are arranged in a boost configuration. In brief, the switch 320 closes, causing current through the inductor 308 to increase. Then the switch 320 is opened, but the current through the inductor 308 cannot change instantaneously because the voltage across an inductor is proportional to the derivative of the current. The voltage across the inductor 308 becomes negative, meaning that the end of the inductor 308 connected to the anode of the diode 316 experiences a voltage increase above the voltage output from the rectifier 304.

[0067] Once the voltage at the anode of the diode 316 increases above the turn on voltage of the diode 316, the current through the inductor 308 can be fed through the diode 316 to the DC bus. The current through the inductor 308 decreases and then the switch 320 is closed once more, causing the current and the inductor 308 to increase.

[0068] In various implementations, the switch 320 may be turned on until the current sensor 312 determines that a predetermined threshold of current has been exceeded. At that time, a switch 320 is turned off for a specified period of time. This specified period may be adaptive, changing along with the voltage of the DC bus as well as the voltage of the AC input change. However, the off time (when the switch 320 is open) is a specified value. Once a time equal to the specified value has elapsed, the switch 320 is turned back on again and the process repeats. The off time can be fixed or variable. In the case of the off time being variable, the off time can be limited to at least a predetermined minimum off time.

[0069] To reduce the physical size and parts cost of the PFC circuit 300, the inductance of the inductor 308 (which may be the largest contributor to the physical size of the PFC circuit 300) may be lowered. However, with a lower inductance, the inductor 308 will saturate more quickly. Therefore, the switch 320 will have to operate more quickly. While more quickly and smaller are relative terms, present power switching control operates in the range of 10 kilohertz to 20 kilohertz switching frequencies. In the present application, the switching frequency of the switch 320 may be increased to more than 50 kilohertz, more than 100 kilohertz, or more than 200 kilohertz. For example, the switching frequency of the switch may be controlled to be approximately 200 kilohertz.

[0070] The switch 320 is therefore chosen to allow for faster switching as well as to have low switching losses. With faster switching, the inductance of the inductor 308 can be smaller. In

addition, the diode 316 may need to be faster. Silicon carbide diodes may have fast response times. For example, the diode 316 may be a STPSC2006CW Silicon Carbide dual diode package from STMicroelectronics.

[0071] In order to accurately drive the switch 320 when operating at higher speeds, the control strategy must similarly be accelerated. For example only, the control module 220 may include multiple devices, such as a microcontroller configured to perform more involved calculations and an FPGA (field programmable gate array) or PLD (programmable logic device) configured to monitor and respond to inputs in near real time. In this context, near real time means that the time resolution of measurement and time delay in responding to inputs of the FPGA or PLD is negligible compared to the physical time scale of interest. For faster switching speeds, the near real time response of the FPGA/PLD may introduce non-negligible delays. In such cases, the delay of the FPGA/PLD and driving circuitry may be measured and compensated for. For example, if the turn-off of a switch occurs later than needed because of a delay, the turn-off can be instructed earlier to compensate for the delay.

[0072] A bypass rectifier 340 is connected in parallel with the rectifier 304 at the AC line input. A second output terminal of the bypass rectifier 340 is connected to the second terminal rectifier 304. However, a first output terminal of the bypass rectifier 340 is connected to the cathode of the diode 316.

[0073] As a result, when the PFC circuit 300 is not operating to boost the DC bus voltage, the bypass rectifier 340 will be active when the line-to-line voltage of the AC input exceeds the voltage across the DC bus. The bypass rectifier 340, in these situations, diverts current from passing through the diode 316. Because the inductor 308 is small, and the switch 320 switches rapidly, the diode 316 is selected to also selected to exhibit fast switching times. The diode 316 may, therefore, be less tolerant to high currents, and so current is selectively shunted around the diode 316 by the bypass rectifier 340.

[0074] In addition, the current path through the rectifier 304 and the diode 316 experiences three diode voltage drops or two diode voltage drops and the switch voltage drop, while the path through the bypass rectifier 340 experiences only two diode voltage drops. While the single phase AC input in FIG. 3A is associated with a boost converter topology, the present disclosure also encompasses a buck converter topology or a buck-boost converter topology.

[0075] In FIG. 3B, a buck converter topology is shown with a three-phase AC input signal. Note that the principles of the present disclosure also apply to a boost converter or buck-boost

converter topology used with a three-phase AC input. A PFC circuit 350 represents another implementation of the PFC circuit 212 of FIG. 2.

[0076] A three-phase rectifier 354 receives three-phase AC and generates pulsating DC across first and second terminals. A switch 358 is connected to the first terminal of the three-phase
5 rectifier 354 by a current sensor 362. The switch 358 is connected to an inductor 366 at a common node. The common node is also connected to a cathode of a power diode 370.

[0077] An anode of the power diode 370 is connected to a second terminal of the three-phase rectifier 354. An opposite terminal of the inductor 366 establishes one terminal of the DC bus, while the second output of the three-phase rectifier 354 establishes the other terminal of the DC
10 bus. In the configuration shown in FIG. 3B, the switch 358, the inductor 366, and the diode 370 are configured in a buck topology.

[0078] A current sensor 362 is connected in series between the anode of the diode 370 and the DC bus. In other implementations, the current sensor 362 may be located in series with the inductor 366. In other implementations, the current sensor 362 may be located in series with the
15 switch 358. In other implementations, the current sensor 362 may be located in series between the anode of the diode 370 and the second output of the three-phase rectifier 354. The current sensor 362 measures current through the inductor 366 as well as current through the DC bus and provides a current signal indicative of the amount of the current.

[0079] A driver 374 drives a control terminal of the switch 358 based on a power switch
20 control signal from the control module 220 in FIG. 2. A switch monitor circuit 378 detects whether the switch 358 has opened or closed and reports the switch state to the control module 220. With the location of the current sensor 362, the current sensor 362 will measure approximately zero current when the switch 358 is open.

[0080] FIG. 4 shows a portion 400 of the PFC circuit 212 of the drive 132 of FIG. 2 including
25 a boost converter 401. The portion 400 includes a rectification circuit 402, an inductor 404, a diode 406, an EMI filter 407, a switch 408, a driver 410 and one or more current sensors 412a, 412b (collectively current sensors 412). The rectification circuit 402 includes a primary (or first) bridge rectifier 414 and a secondary (or second) bridge rectifier 416. The secondary bridge rectifier 416 may be referred to as a bypass rectifier and allows for current to bypass the primary
30 bridge rectifier 414 and the boost converter 401. Each of the bridge rectifiers 414, 416 may include four diodes, as shown.

[0081] Each of the bridge rectifiers 414, 416 includes AC inputs, a return input and an output. The AC inputs of each of the bridge rectifiers 414, 416 are connected to a differential AC input

420 that receives an AC voltage V_{AC} from the EMI filter 202. The return inputs are connected to a same output 418 of the second current sensor 412b. The output of the primary bridge rectifier 414 is connected to an input of the first current sensor 412a or the inductor 404. The output of the secondary bridge rectifier 416 is connected to a DC output 422 of the PFC circuit 212. The output voltages of the bridge rectifiers 414, 416 may be referred to as main voltages. Although current sensors 412a and 412b are shown, other current sensors may be alternatively or additionally incorporated into the portion 400. For example, a current sensor may be connected in series with one or more of the diode 406, the switch 408, and the capacitor 430. This current sensor may detect current passing through the diode 406, the switch 408 and/or the capacitor 430. In one embodiment, the current sensor is connected between the inductor 404 and the switch 408. In another embodiment, the current sensor is connected between the switch 408 and the reference terminal 426. Also, any or all of the disclosed current sensors may be utilized. Any of the signals and/or parameters derived from the signals of the disclosed current sensors may be utilized in the below described circuits and methods.

[0082] The EMI filter 407 may be connected to the output of the primary bridge rectifier 714 or an output of the first current sensor 412a. The EMI filter 407 filters an output of the primary bridge rectifier 414. The EMI filter 407 decouples the boost converter 401 from the primary bridge rectifier 414 to minimize noise generated by the boost converter 401 from being seen at the primary bridge rectifier 414. The DC output 422 may be connected to the DC bus, which is connected between the PFC circuit 212 and the inverter power circuit 208 of FIG. 2.

[0083] The inductor 404, diode 406, switch 408 and driver 410 provide the boost converter 401, which increases a DC output voltage V_{DCOUT} and/or a DC bus voltage of the DC bus to a commanded (or predetermined) DC voltage V_{DCCOM} . The boost converter 401 is a power converter. The commanded DC voltage V_{DCCOM} may be determined by the control module 250 and is set to be less than a peak (or maximum) output voltage of the bridge rectifiers 414, 416. The inductor 404 is connected in series with the diode 406 between (i) the output of the primary bridge rectifier 414 and/or the first current sensor 412a and (ii) the DC output 422. The inductor 404 is connected (i) at a first end, to the output of the primary bridge rectifier 414 or the output of the first current sensor 412, and (ii) at a second end, to an anode of the diode 406 and a first terminal of the switch 408. The inductor 404 may be small (e.g., 80 micro-Henry (μH)) and operates as a choke. The diode 406 may be formed of, for example, silicon carbide SiC for quick switching frequencies and no reverse recovery time. The diode 406 may include multiple diodes connected in parallel.

[0084] The switch 408 may be a transistor, such as a super-junction field effect transistor (FET), a power metal oxide semiconductor field-effect transistor (MOSFET), and/or a super-junction MOSFET. The switch 408 may be configured to be oscillated between ON (e.g., closed) and OFF (e.g., open) states at a high frequency (e.g., greater than or equal to 200 kilohertz (kHz)). The first terminal of the switch 408 is connected to the inductor 404 and the anode of the diode 406. A second terminal of the switch 408 is connected to an input 425 of the second current sensor 412b and a reference terminal 426 (e.g., a 0 voltage bus or other voltage reference or return terminal). A control terminal of the switch 408 receives a control signal SW_{CTRL} from the driver 410. The driver 410 generates the control signal SW_{CTRL} based on an output signal PFC_{OUT} of the control module 250. The control module 250 generates the output signal PFC_{OUT} based on: one or more current sense signals PFC_{INC1} , PFC_{INC2} from the current sensors 412a, 412b; an AC signal PFC_{ACREP} representative of the AC voltage V_{AC} ; and a DC signal PFC_{DCREP} that is representative of the DC output voltage V_{DCOUT} of the PFC circuit 212. The current sense signal PFC_{INC1} may be equal to and/or indicative of an amount of current (i) passing through the inductor 404, and/or (ii) passing through the PFC circuit 212. The current sense signal PFC_{INC2} may be equal to and/or indicative of an amount of current (i) returning from the DC output 422 to the second current sensor 412b, and/or (ii) passing through the PFC circuit 212. The AC signal PFC_{ACREP} may be equal to and/or indicative of the AC voltage V_{AC} . The DC signal PFC_{DCREP} may be equal to and/or indicative of the DC output voltage V_{DCOUT} .

[0085] A capacitor 430 may be connected between the DC output 422 and the reference terminal 426. The capacitor 430 may be connected (i) at a first end, to a cathode of the diode 406 and to the DC output 422, and (ii) at a second end, to the reference terminal 426 and the input 425 of the second current sensor 412b.

[0086] During operation, the boost converter may be ON when the DC bus voltage is greater than the AC voltage V_{AC} . Current does not pass from the secondary rectifier 416 to the DC bus when the DC bus voltage is greater than the AC voltage V_{AC} . When the DC bus voltage is less than the AC voltage V_{AC} , then the boost circuit 401 may be active and storing energy in the inductor 404 and releasing energy from the inductor 404 onto the DC bus to boost voltage of the DC bus. The energy may be stored when the switch 408 is closed and released when the switch 408 is opened.

[0087] FIG. 5 shows a plot of a rectified AC signal 450. The rectified AC signal 450 may represent an output of the primary bridge rectifier 414 and/or an output of the secondary bridge rectifier 416 of FIG. 4. The rectified AC signal 450 may be offset from zero, such that a minimum voltage of the rectified AC signal 450 is at an offset voltage V_{Offset} .

[0088] The control module 250 may control operation of the driver 410 to control a state of the switch 408, such that the DC output voltage V_{DCOUT} is equal to or within a predetermined range of the commanded DC voltage V_{DCCOM} . The control module 250 controls operation of the driver 410, such that the switch 408 is oscillated between open and closed states at a predetermined frequency during active periods 452 and is maintained in an OFF (or open) state during inactive periods 454.

[0089] During operation, an output of the diode 406 is provided to the DC output 422 while the switch 408 is in an open state and the DC output voltage V_{DCOUT} is less than an output voltage of the primary bridge rectifier 414. This may occur during the active periods 452.

During the active periods, voltages of the rectified AC signal 450 are increased (i.e. boosted) to match the commanded DC voltage V_{DCCOM} . An amount of time that the switch 408 is maintained in the OFF (or open) state affects how much a voltage of the rectified AC signal 450 is boosted to match the commanded DC voltage V_{DCCOM} . The boost converter 401 is ON during the active periods 452. Conversely, the boost converter 401 is OFF during the inactive periods.

When the boost converter 401 is OFF, current does not pass through the inductor 404 and diode 406 to the DC bus. This may be because the diode 406 is in a reversed bias state. Pure rectification through the secondary bridge rectifier 416 may be provided when the boost converter 401 is OFF.

[0090] The ON time and the OFF time of the switch 408 per AC cycle and thus the duty cycle of the switch 408 is controlled by the control module 250. The control module 250 and/or the driver 410 may adjust the duty cycle of the switch 408 including adjusting the OFF time and/or the ON time of each pulse of the control signal SW_{CTRL} . Operational control of the switch 408 is further described below.

[0091] An output of the secondary bridge rectifier 416 is provided to the DC output 422 when the DC output voltage V_{DCOUT} is less than an output voltage of the primary bridge rectifier 416, which may occur during (i) the active periods 452 when the switch 408 is being oscillated, and (ii) inactive periods 454 when the switch 408 is not being oscillated. During the inactive periods the switch 408 may be in an open state and the DC output voltage V_{DCOUT} changes based on an output of the secondary bridge rectifier 416. The diode 406 is bypassed while the switch 408 is in the closed state. The DC output voltage V_{DCOUT} may increase from a voltage less than or equal to the commanded DC voltage V_{DCCOM} to a voltage greater than or equal to the commanded DC voltage V_{DCCOM} . The amount of increase may depend on durations of the active periods and/or the inactive periods.

[0092] In FIG. 5, start times s1-s6 and end times e1-e6 of active operation of the switch 408 are shown. The switch 408 is oscillated between ON and OFF states during the active periods 452. The switch 408 is not oscillated between ON and OFF states during the inactive periods 454. Although start times s1-s6 and end times e1-e6 are shown at certain angles (or phases) of the rectified AC signal 450, the start times s1-s6 and end times e1-e6 may be adjusted in time relative to the rectified AC signal 450. As shown, the end times e1-e6 correspond to moments in time when a voltage of the rectified AC signal 450 is increasing and matches the commanded DC voltage V_{DCCOM} at a first (increasing) cross-over point. As shown, the start times s1-s6 correspond to moments in time when a voltage of the rectified AC signal 450 is decreasing and matches the commanded DC voltage V_{DCCOM} at a second (decreasing) cross-over point.

[0093] Various implementations are described below with respect phase angles of V_{AC} and/or outputs of the bridge rectifiers 414, 416. The implementations and corresponding conditions and task may be determined and/or performed, as described below, based on V_{AC} , voltages of outputs of the bridge rectifiers 414, 416 and/or voltages of an output of a corresponding power converter. The voltages may be monitored and used as an alternative to or in addition to the phase angles when performing the below described tasks.

[0094] As an example, the end times e1-e6 may be adjusted to occur earlier in time and at phase angles of the rectified AC signal 450 prior to respective increasing cross-over points with the commanded DC voltage V_{DCCOM} . As another example, the start times s1-s6 may be advanced to occur earlier in time and at phase angles of the rectified AC signal 450 prior to respective decreasing cross-over points with the commanded DC voltage V_{DCCOM} and/or closer in time to the corresponding end times e1-e6. These adjustments may minimize how much the DC output voltage V_{DCOUT} exceeds the commanded DC voltage V_{DCCOM} and/or minimize peak current during the inactive periods. By having the start times s1-s6 closer in time to the end times e1-e6, the inactive periods are reduced in length, which decreases the amount of time that the output of the secondary bridge 416 is solely provided to the DC output 422 and/or decreases durations of the inactive periods.

[0095] During the active periods and due to the oscillated operation of the switch 408, the current within the inductor 404 ramps up and down. When the current ramps down, the secondary bridge rectifier 416 protects the diode 406 from transient spikes in voltage out of the inductor 404 by allowing current to pass from the secondary bridge rectifier 416 directly to the DC output 422. The secondary bridge rectifier 416 minimizes the number of components between the differential AC input 420 and the DC output 422. When current is passing through the secondary bridge rectifier 416 to the DC output 422, the current passes through a single

diode of the secondary bridge rectifier 416 instead of passing through a diode of the primary bridge rectifier 414, the inductor 404, and the diode 406. This reduces the number of components from 3 to 1, which reduces voltage and power losses.

[0096] In an alternative embodiment, the frequency of oscillated operation of the switch 408 is decreased rather than deactivated. The frequency may be decreased to less than, for example, 200 kHz during low activity periods (or low activity mode). Timing of the low activity periods may be the same or similar to that of the previously described inactive periods. As an example, the frequency during the low activity periods may be an order of magnitude less than during the active periods (or active mode). As such, operation of the switch 408 may be transitioned between low activity modes and high activity modes rather than between inactive modes and active modes. The switch 408 may be operated in the low activity mode during periods between the end points e1-e6 and the successive start points s1-s6. The ON time (or closed periods) of the switch 408 may be decreased for operation in the low activity mode and increased for operation in the high activity mode.

[0097] Although the start times s1-s6 are described with respect to start times of the active or high activity mode, the start times s1-s6 also refer to end times of an inactive mode or low activity mode. Also, although the end times e1-e6 are described with respect to end times of the active or high activity mode, the end times e1-e6 also refer to start times of the inactive mode or low activity mode.

[0098] Although FIG. 4 shows conversion and rectification of a single phase, the circuit of FIG. 4 may be modified to convert and rectify three-phases of current. This may include replacing the bridge rectifiers 414, 416 with three-phase bridge rectifiers that each provide a single DC output.

[0099] FIG. 6 shows an example of changes in an amount of current sensed by the second current sensor 412b of FIG. 4 due to the activation and deactivation of oscillated operation of the switch 408. The oscillated operation of the switch 408 is enabled at start times s1-s6 and disabled at end times e1-e6, which correspond with the start times s1-s6 and end times e1-e6 of FIG. 5. Lengths of increasing current periods 460 and decreasing current periods 462 may be adjusted to change peaks of current 464 by altering the start times s1-s6 and end times e1-e6, as described above. The peaks of current 464 may be adjusted relative to a base peak current level I_{base} .

[0100] The above-described dual bridge circuit configurations of the bridge rectification circuit 402 of FIG. 4 are able to handle an increased maximum allowable forward surge current

(IFSM). The secondary bridge circuit 416 is able to handle increased current over a single bypass diode arrangement, where the secondary bridge circuit 416 is replaced with two diodes instead of a full bridge. Arrangement provides higher efficiency if active PFC is not running. As an alternative, a single diode may be used to replace the secondary bridge 416 by (i) connecting the anode of the single diode to the cathodes of the two diodes connected to the first current sensor 412a, and (ii) a cathode of the diode to the output terminal 422. The dual bridge circuit configurations also provide the conduction path for partial PFC operation when the peak of the input line voltage V_{AC} is greater than V_{DCOUT} .

[0101] FIG. 7 shows an example of the EMI filter 407. The EMI filter 407 may include one or more capacitors 470. If more than one capacitor is included, the capacitors are connected in parallel between a first bus 472 and a second bus 474. The first bus is connected between the output of the bridge rectifier 414 and the inductor 404. The second bus 474 is connected between the second current sensor 412b and the reference terminal 426. By having multiple (e.g., 3) capacitors connected in parallel, parasitic inductance associated with the EMI filter 407 is reduced.

[0102] FIG. 8 shows the control module 250 that includes a load module 502, an AC voltage module 504, a DC voltage module 506, a current module 508, an output module 510 and a memory 512. Although the modules 502, 504, 506, 508, 510 and the memory 512 are shown as part of the control module 250, one or more of the modules 502, 504, 506, 508, 510 and the memory 512 may be part of or also included in the system control module 270. The information (data, parameters, and signals) received and/or generated by the module 502, 504, 506, 508, 510 may be shared between the modules 502, 504, 506, 508, 510. The output module 510 may include a timing module 513, a reference generation module 514, timers 515 and/or a peak detector 517. The memory 512 may include one or more tables 516. Operation of the modules 502, 504, 506, 508, 510 and memory 512 are described below with respect to the methods of FIGs. 9 and 11-12.

[0103] The output module 510 may operate in the active mode, the inactive mode, the low activity mode, the high activity mode, a full PFC mode, and a partial PFC mode. The full PFC mode may refer to when the boosting converter 401 is continuously in an active or high activity mode to boost the DC bus voltage to match the commanded DC voltage V_{DCCOM} . This may occur when the commanded DC voltage V_{DCCOM} is greater than or equal to a peak voltage of the AC voltage V_{AC} and/or outputs of the bridge rectifiers 414, 416. The partial PFC mode refers to switching between operating in (i) an active or high activity mode and (ii) an inactive or low activity mode.

[0104] In one embodiment, the timing module 510 switches from operating in the full PFC mode to operating in the partial PFC mode. The partial PFC mode reduces power losses by operating at reduced DC voltages and provides improved operating efficiency. The timing module 510 may, for example, operate in the partial PFC mode during light compressor loading conditions (e.g., load on compressor less than a predetermined load) and operate in the full PFC mode during heavy compressor loading conditions (e.g., load on compressor greater than or equal to the predetermined load).

[0105] Referring to FIGs. 6 and 8, although during the inactive periods the current is permitted to increase above a current threshold level corresponding to a transition end time as shown, the amount of increase can be controlled and/or minimized. Also, although the current increases that occur during the inactive periods can negatively affect a power factor of the PFC circuit, the improved efficiency provided during the partial PFC mode outweighs the small negative affect on the power factor. The efficiency may refer to a ratio between output power and input power of the boost converter 401, the PFC circuit 212 and/or the drive 132, which may be less than or equal to 1%.

[0106] For further defined structure of the modules of FIGs. 2-4 see below provided method of FIGs. 9 and 12 and below provided definition for the term “module”.

[0107] The systems disclosed herein may be operated using numerous methods, example methods are illustrated in FIGs. 9 and 11-12. In FIG. 9, a method of operating a drive (e.g., the drive 132 of FIG. 2) with a boost converter (e.g., the boost converter 401 of FIG. 4) and a PFC circuit (e.g., the PFC circuit 212 of FIG. 2) is shown. Although the following tasks are primarily described with respect to the implementations of FIGs. 4-8, the tasks may be easily modified to apply to other implementations of the present disclosure. The tasks may be iteratively performed. Tasks 602-614 may be performed while tasks 616-628 are performed.

[0108] The method may begin at 600. At 602, the load module 502 may receive various signals and parameters from (i) the PFC circuit 212 of FIG. 2 including signals and parameters from the portion 400 of FIG. 4, and (ii) the inverter power circuit 208 of FIG. 2. The signals and parameters may include a voltage $DC_{V_{Bus}}$ of the DC bus between the PFC circuit 212 and the inverter power circuit 208. At least some of the signals and parameters are disclosed in and described with respect to FIG. 2. The signals and parameters may include DC signals and/or measured DC voltages corresponding to DC voltages on the DC bus, amounts of current supplied to the compressor 102, voltages of power supplied to the compressor 102, sensor input data, commanded and/or manually entered parameters, and/or other shared data and parameters. The load module 502 may generate a load signal LD that is indicative of a load on the

compressor 102 based on the stated signals and parameters. The load signal LD may be generated based on a load algorithm, one or more maps, one or more equations, one or more tables (e.g., one or more of the tables 516), predetermined (or historical) data, and/or predicted (or estimated) future data. The load algorithm, maps, equations and/or tables may relate the signals and parameters to provide a calculated load and/or value indicative of the load on the compressor.

[0109] At 604, the AC voltage module 504 may receive or generate the AC signal PFC_{ACREP} . The AC voltage module 504 may detect voltages at the outputs of the bridge rectifiers 414, 416. The AC signal PFC_{ACREP} may be set equal to and/or be representative of one or more of the outputs of the bridge rectifiers 414, 416.

[0110] At 606, the DC voltage module 506 may receive or generate the DC signal PFC_{DCREP} . The DC voltage module 506 may (i) detect the voltage DC_{VBus} at the DC bus between the PFC circuit 212 and the inverter power circuit 208, and/or (ii) receive a DC bus voltage indication signal from a sensor and/or module external to the control module 250 and/or the DC voltage module 506.

[0111] At 608, the current module 508 may determine an amount of current: supplied to the compressor 102 and/or passing through one or more of the current sensors 412. This may be based on the current sense signals PFC_{INC1} , PFC_{INC2} .

[0112] At 610, the reference generation module 514 may generate a reference sinusoidal signal and/or a reference rectified sinusoidal signal. The reference signals may be generated based on the AC input signal V_{AC} , the outputs of the bridge rectifiers 414, 416, and/or an output of the EMI filter 407. In one embodiment, the reference signals are generated based on the output of the EMI filter 407. This may include estimating the phase of the output of the EMI filter 407. The AC input signal V_{AC} , the outputs of the bridge rectifiers 414, 416 and/or the output of the EMI filter 407 may have noise or irregular activity as not to be a perfect sinusoidal and/or rectified sinusoidal waves. The reference generation module 514 generates the reference signals to be pure sinusoidal and/or rectified sinusoidal reference signals having the same phase as the AC input signal V_{AC} , the outputs of the bridge rectifiers 414, 416 and/or the output of the EMI filter 407. This synchronizes the reference signals to the AC input signal V_{AC} , the outputs of the bridge rectifiers 414, 416 and/or the output of the EMI filter 407. The reference generation module 514 may output reference data signals including phase, frequency, period, and/or other time-varying derivative (or gradient) of the reference data signals. The reference data may include scaled versions of the reference data signals.

[0113] At 612, the timing module 510 generates the commanded DC voltage V_{DCCOM} to be less than a peak (or maximum) AC input voltage V_{AC} and/or a peak (or maximum) output voltage of the bridge rectifiers 414, 416. This is unlike traditional PFC circuits, which always have the commanded DC voltages above a peak AC input voltage. The commanded DC voltage V_{DCCOM} may be set to be within a predetermined range of the peak output voltage of one or more of the bridge rectifiers 414, 416. As an example, as the load on the compressor 102 increases, the commanded DC voltage V_{DCCOM} may be decreased. By lowering the commanded DC voltage V_{DCCOM} , the amount of time between end times and successive start times (or times between active modes and following inactive modes) of oscillated switch control operation increases. This allows the DC output voltage V_{DCOUT} and current to increase during inactive periods to a higher peak voltage and higher peak current. Mode transition points refer to transitions between (i) the active (and/or high activity) mode (oscillated switch operation enabled) and (ii) the inactive mode (oscillated switch operation disabled) or low activity mode. Examples of mode transition points are shown as cross-over points in FIG. 5, however the mode transition points may not match corresponding cross-over points depending on the start times and end times (i.e. phase angles and/or corresponding voltages) of the mode transition points. As another example, by increasing the commanded DC voltage V_{DCCOM} relative to the peak voltage of V_{AC} and/or outputs of the bridge rectifiers 414, 416, periods when oscillated operation of the switch 408 are decreased in length. A small change in the commanded DC voltage V_{DCCOM} can make a large difference in peak current supplied.

[0114] At 614, the timing module 510 may adjust (i) next start times and/or end times of the oscillated operation of the switch 408, (ii) duty cycle of the oscillated operation of the switch 408, and/or (iii) frequency of the oscillated operation of the switch 408. This may include adjusting times of rising and/or falling edges of the control signal SW_{CTRL} . The stated adjustment(s) may be based on the load of the compressor determined at 602, the AC voltage received and/or generated at 604, the DC voltage received and/or generated at 606, one or more of the current levels detected at 608, and/or one or more of the reference signals generated at 610. The adjustments may also be based on capacitance of the DC bus, torque commanded of the compressor 102, predicted voltages of the outputs of the bridge rectifiers 414, 416, and/or other parameters associated with operation of the portion 400. The adjustments may advance or delay the transition start times and/or the transition end times. The adjustments may be determined based on equations, algorithms, maps, and/or tables relating the stated parameters, which may be stored in the memory 512 and accessed by the timing module 510. The adjustments may also be based on previous (historical) values and/or results, which may be stored in and accessed from the memory 512. For example, if a last peak DC bus voltage or peak

detected current (current detected by one of the current sensors 412a, 412b) was above a predetermined threshold, then the next transition end time or transition start time may be advanced to reduce the peak DC bus voltage or peak detected current.

[0115] At 616, the timing module 510 determines whether the phase angle of the output of one or more of the bridge rectifiers 414, 416 matches a predetermined start time of an active period. In addition or alternatively, voltages of the outputs of the bridge rectifiers 414, 416 (or input of the inductor 404) and/or the output of the boost converter 401 (or output of the diode 406) may be compared to predetermined voltages for the predetermined start time to determine whether the stated condition exists. If there is a match, task 618 is performed, otherwise task 620 is performed.

[0116] At 618, the timing module 510 transitions to the active (or high activity) mode. This includes oscillated operation of the switch 408 at a first (or high) frequency. The duty cycle of the switch 408, including durations of ON times and OFF times, may correspond to duty cycle information determined at 614. Task 602 may be performed subsequent to task 618.

[0117] At 620, the timing module 510 may determine whether the DC bus voltage is less than or equal to the commanded DC voltage V_{DCCOM} and/or whether a next transition phase angle (next phase angle at which point a transition between operating modes occurs) is an end time (e.g., one of the end times e1-e6 of FIGs. 5-6) for an active mode and/or high activity mode. In addition or alternatively, voltages of the outputs of the bridge rectifiers 414, 416 and/or the boost converter 401 may be compared to predetermined voltages for the end time to determine whether one or more of the stated conditions exist. The timing module 510 may also or alternatively determine whether the current transition phase angle is within a predetermined phase angle range (e.g., between a last start time and a subsequent end time) of a current active mode and/or high activity mode. In addition or alternatively, voltages of the outputs of the bridge rectifiers 414, 416 and/or the boost converter 401 may be compared to a predetermined voltage ranges corresponding to the predetermined phase angle range to determine whether the stated condition exists. At the end time, the timing module 510 transitions from an active and/or high activity mode to an inactive or low activity mode. If the DC bus voltage is less than or equal to the commanded DC voltage V_{DCCOM} and/or the next transition phase angle is at an end time for an active mode and/or high activity mode, then task 622 is performed, otherwise task 624 is performed.

[0118] At 622, the timing module 510 operates in the active mode and/or high activity mode. Task 602 may be performed subsequent to task 622. At 624, the timing module 510 determines whether the phase angle is an end time of an active mode and/or a high activity mode. In

addition or alternatively, voltages of the outputs of the bridge rectifiers 414, 416 and/or the boost converter 401 may be compared to predetermined voltages for the end time to determine whether the stated condition exists. If the phase angle is an end time, task 626 is performed, otherwise task 628 is performed. At 626, the timing module 510 transitions to the inactive mode or low activity mode. If the timing module 510 transitions to the inactive mode, then the boost converter 401 is transitioned to an OFF state and the switch 408 is switched to a closed state. This allows for pure rectification via the secondary bridge rectifier 416. The output of the secondary bridge rectifier 416 is provided to the DC output 422 without receiving current from the primary bridge rectifier 414, the inductor 404 and the diode 406. The pure rectification reduces voltage and power losses. If the timing module 510 transitions to the low activity mode, then oscillated operation of the switch 408 continues, but at a reduced frequency and/or at an increased duty cycle, such that OFF times of the switch 408 are increased and/or the ON times of the switch 408 are decreased. Task 602 may be performed subsequent to task 626. At 628, the timing module 510 remains in the inactive mode or operating in the low activity mode. Task 602 may be performed subsequent to task 628.

[0119] Although the above tasks 616-628 are provided in a particular order, tasks 616-628 may be performed in a different order. As an example, task 624, 626, 628 may be performed prior to tasks 616, 618, 620 and 622. If task 624, 626, 628 are performed prior to tasks 616, 618, 620 and 622, then task 620 may be modified to determine whether the DC bus voltage is greater than or equal to the commanded voltage, the next transition phase angle is a start time of an inactive mode or low activity mode, and/or the current phase angle is within a predetermined range (e.g., between an end time of an active mode and/or high activity mode and a subsequent start time of the active mode and/or high activity mode). This may include comparing voltages of the outputs of the bridge rectifiers 414, 416 and/or the boost converter 401 to corresponding predetermined voltages and ranges to effectively determine if the next transition phase angle is a start time of an inactive mode or low activity mode, and/or the current phase angle is within a predetermined range.

[0120] Although the portion 400 of FIG. 4 includes a boost converter 401 and is configured for reception of a single phase AC signal, the portion may be implemented multiple times; once for each phase of a 3-phase input signal. As another example implementation, the portion 400 may be modified for a 3-phase input signal and may include a different converter. For example, the portion 400 may include a buck converter or other suitable converter. An example of a 3-phase implementation including a buck converter is shown in FIG. 10.

[0121] FIG. 10 is a schematic diagram of a portion 700 of a PFC circuit (e.g., the PFC circuit 212 of FIG. 2) of a drive (e.g., the drive 132 of FIG. 1) including a buck converter 701. The portion 700 includes a rectification circuit 702, an inductor 704, a diode 706, an EMI filter 707, a switch 708, a driver 710 and one or more current sensors 712a, 712b. The rectification circuit 702 includes a bridge rectifier 714. The bridge rectifier 714 may include six diodes, as shown. The bridge rectifier 714 includes AC inputs, a return input and an output. The AC inputs of the bridge rectifier 714 receive a 3-phase AC voltage V_{AC} from a 3-phase AC input 720. The return inputs are connected to a same output 718 of the second current sensor 712b. The output of the bridge rectifier 714 is connected to the switch 708. An output voltage of the bridge rectifier 714 may be referred to as a main voltage.

[0122] The EMI filter 707 may be connected to the output of the bridge rectifier 714 or an output of the first current sensor 712a. The EMI filter 707 filters output of the bridge rectifier 714. The EMI filter 707 decouples the buck converter 701 from the bridge rectifier 714 to minimize noise generated by the buck converter 701 from being seen at the bridge rectifier 714. An example EMI filter that may replace the EMI filter 707 is shown in FIG. 7. The DC output 722 may be connected to an input of the DC bus, which is connected between the PFC circuit 212 and the inverter power circuit 208 of FIG. 2.

[0123] The inductor 704, diode 706, switch 708 and driver 710 provide the buck converter 701. The buck converter 701 operates as a power converter. The buck converter 701, instead of boosting voltage as does the boost converter 401 of FIG. 4, steps down voltage while stepping up current. The buck converter 701 may be (i) OFF (operating in an inactive mode and switch 708 is held in an open state) or ON and switching the switch 708 between ON and OFF states at a low frequency for rising and falling portions of rectified AC signal out of the bridge rectifier 714, or (ii) ON and switching the switch 708 between ON and OFF states at a high frequency near peaks of the rectified AC signal out of the bridge rectifier 714. This is the opposite of the boost converter 401 of FIG. 4, which is (i) ON and switching the switch 408 between ON and OFF states at a high frequency during rising and falling portions of a rectified AC signals out of the bridge rectifiers 414, 416, and (ii) OFF (switch 408 is held open) or ON and switching the switch 408 between ON and OFF states at a low frequency near peaks of the rectified AC signals out of the bridge rectifiers 414, 416. The operation of the buck converter 701 limits the DC output voltage V_{DCOUT} at the DC output terminal 722 while reducing power losses of the buck converter 701.

[0124] The timing module 513 of FIG. 8 may command a DC output voltage V_{DCOUT} and/or DC bus voltage (first predetermined voltage) that are greater than a peak voltage of the input

voltage V_{AC} , the output of the bridge rectifier 714, and/or during rising and falling portions of the rectified AC signal out of the bridge rectifier 714. The timing module 513 may command a DC output voltage V_{DCOUT} and/or a DC bus voltage (second predetermined voltage) that are less than the peak voltage of the input voltage V_{AC} and/or the output of the bridge rectifier 714 during a period when the DC output voltage V_{DCOUT} and/or the DC bus voltage are within a predetermined range. The predetermined range may be centered on the peak voltage of the input voltage V_{AC} and/or the output of the bridge rectifier 714. The commanded voltages may be determined by the control module 250.

[0125] The inductor 704 is connected (i) at a first end, to the switch and a cathode of the diode 706, and (ii) at a second end, to the DC output terminal 722 and a capacitor 723. The inductor 704 operates as a choke and may be small (e.g., 80 micro-Henry (μH)). The diode 706 may be formed of, for example, silicon carbide SiC. The anode of the diode 706 is connected to an input 724 of the second current sensor 712b and a reference terminal 726 (e.g., a ground reference). The switch 708 is connected in series with the inductor 704 between (i) the output of the primary bridge rectifier 714 and/or the first current sensor 712a and (ii) the inductor 704.

[0126] The switch 708 may be a transistor, such as a super-junction field effect transistor (FET), a power metal oxide semiconductor field-effect transistor (MOSFET), and/or a super-junction MOSFET. The switch 708 may be configured to be oscillated between ON (e.g., closed) and OFF (e.g., open) states at a high frequency (e.g., greater than or equal to 200 kilohertz (kHz)). A first terminal of the switch 708 is connected to the output of the primary bridge rectifier 714 or an output of the first current sensor 712a. A second terminal of the switch 708 is connected to the inductor 704 and a cathode of the diode 706.

[0127] A control terminal of the switch 708 receives a control signal SW_{CTRL} from the switch driving (or control) circuit 710. The driver 710 generates the control signal SW_{CTRL} based on an output signal PFC_{OUT} of the control module 250. The control module 250 generates the output signal PFC_{OUT} based on: one or more current sense signal PFC_{INC1} , PFC_{INC2} from the current sensors 712; an AC signal PFC_{ACREP} representative of the AC voltage V_{AC} ; and a DC signal PFC_{DCREP} that is representative of the DC output voltage V_{DCOUT} of the PFC circuit 212. The current sense signal PFC_{INC1} may be equal to and/or indicative of an amount of current (i) passing through the inductor 704, and/or (ii) passing through the PFC circuit 212. The current sense signal PFC_{INC2} may be equal to and/or indicative of an amount of current (i) returning from the DC output 722 to the second current sensor 712b, and/or (ii) passing through the PFC circuit 212. The AC signal PFC_{ACREP} may be equal to and/or indicative of the AC voltage V_{AC} . The DC signal PFC_{DCREP} may be equal to and/or indicative of the DC output voltage V_{DCOUT} .

[0128] The capacitor 723 may be connected between the DC output 722 and the reference terminal 726. The capacitor 723 may be connected (i) at a first end, to the inductor 704 and the DC output terminal 722, and (ii) at a second end, to the input 724 of the second current sensor 712b and the reference terminal 726.

- 5 **[0129]** The buck converter 701 may be turned OFF (i.e. the switch 708 is closed) and maintained in the ON state, such that there is no switching losses. This may occur during light load conditions. For further defined structure of the modules of FIGs. 2-4 and 10 see below provided methods of FIGs. 11-12 and below provided definition for the term “module”.

[0130] In FIG. 11, shows a method of operating a drive (e.g., the drive 132 of FIG. 2) with a buck converter (e.g., the buck converter 701) and a PFC circuit (e.g., the PFC circuit 212 of FIG. 2) is shown. Although the following tasks are primarily described with respect to the implementations of FIGs. 8 and 10, the tasks may be easily modified to apply to other implementations of the present disclosure. The tasks may be iteratively performed. Tasks 802-814 may be performed while tasks 816-828 are performed.

- 15 **[0131]** The method may begin at 800. At 802, the load module 502 may receive various signals and parameters from (i) the PFC circuit 212 of FIG. 2 including signals and parameters from the portion 700 of FIG. 10, and (ii) the inverter power circuit 208 of FIG. 2. The signals and parameters may include a voltage $DC_{V_{Bus}}$ of the DC bus between the PFC circuit 212 and the inverter power circuit 208. At least some of the signals and parameters are disclosed in and described with respect to FIG. 2. The signals and parameters may include DC signals and/or measured DC voltages corresponding to DC voltages on the DC bus, amounts of current supplied to the compressor 102, voltages of power supplied to the compressor 102, sensor input data, commanded and/or manually entered parameters, and/or other shared data and parameters. The load module 502 may generate a load signal LD that is indicative of a load on the compressor 102 based on the stated signals and parameters. The load signal LD may be generated based on a load algorithm, one or more maps, one or more equations, one or more tables (e.g., one or more of the tables 516), predetermined (or historical) data, and/or predicted (or estimated) future data. The load algorithm, maps, equations and/or tables may relate the signals and parameters to provide a calculated load and/or value indicative of the load on the compressor.

[0132] At 804, the AC voltage module 504 may receive or generate the AC signal PFC_{ACREP} . The AC voltage module 504 may detect voltages at the output of the bridge rectifier 714. The AC signal PFC_{ACREP} may be set equal to and/or be representative of one or more of the output of the bridge rectifier 714.

[0133] At 806, the DC voltage module 506 may receive or generate the DC signal PFC_{DCREP} . The DC voltage module 506 may (i) detect the voltage $DC_{V_{Bus}}$ at the DC bus between the PFC circuit 212 and the inverter power circuit 208, and/or (ii) receive a DC bus voltage indication signal from a sensor and/or module external to the control module 250 and/or the DC voltage module 506.

[0134] At 808, the current module 508 may determine an amount of current: supplied to the compressor 102 and/or passing through one or more of the current sensors 712. This may be based on the current sense signals PFC_{INC1} , PFC_{INC2} .

[0135] At 810, the reference generation module 514 may generate a reference sinusoidal signal and/or a reference rectified sinusoidal signal. The reference signals may be generated based on the AC input signal V_{AC} , the output of the bridge rectifier 714, and/or an output of the EMI filter 707. In one embodiment, the reference signals are generated based on the output of the EMI filter 707. This may include estimating the phase of the output of the EMI filter 707. The AC input signal V_{AC} , the output of the bridge rectifier 714 and/or the output of the EMI filter 707 may have noise or irregular activity as not to be perfect sinusoidal and/or rectified sinusoidal waves. The reference generation module 514 generates the reference signals to be pure sinusoidal and/or rectified sinusoidal reference signals having the same phase as the AC input signal V_{AC} , the output of the bridge rectifier 714 and/or the output of the EMI filter 707. This synchronizes the reference signals to the AC input signal V_{AC} , the output of the bridge rectifier 714 and/or the output of the EMI filter 707. The reference generation module 514 may output reference data including phase, frequency, period, and/or other time-varying derivative (or gradient) of the reference signals. The reference data may include scaled versions of the reference signals.

[0136] At 812, the timing module 513 generates the commanded DC voltage V_{DCCOM} to be less than a peak (or maximum) AC input voltage V_{AC} and/or a peak (or maximum) output voltage of the bridge rectifier 714. This is unlike traditional PFC circuits, which always have the commanded DC voltages above a peak AC input voltage. The commanded DC voltage V_{DCCOM} may be set to be within a predetermined range of the peak output voltage of the bridge rectifier 714. As an example, as the load on the compressor 102 increases, the commanded DC voltage V_{DCCOM} may be decreased. By lowering the commanded DC voltage V_{DCCOM} , the amount of time between end times and successive start times (or times between active modes and following inactive modes) of oscillated switch control operation increases. This allows the DC output voltage V_{DCOUT} to increase during inactive periods to a higher peak voltage. Mode transition points refer to transitions between (i) the active (and/or high activity) mode (oscillated switch

operation enabled) and (ii) the inactive mode (oscillated switch operation disabled) or low activity mode. Examples of mode transition points are shown as cross-over points in FIG. 5, however the mode transition points may not match corresponding cross-over points depending on the start times and end times (i.e. phase angles) of the mode transition points. As another example, by increasing the commanded DC voltage V_{DCCOM} relative to the peak voltage of V_{AC} and/or output of the bridge rectifier 714, periods when oscillated operation of the switch 708 are decreased in length. A small change in the commanded DC voltage V_{DCCOM} can make a large difference in peak current supplied.

[0137] At 814, the timing module 513 may adjust (i) next start times and/or end times of the oscillated operation of the switch 708, (ii) duty cycle of the oscillated operation of the switch 708, and/or (iii) frequency of the oscillated operation of the switch 708. This may include adjusting times of rising and/or falling edges of the control signal SW_{CTRL} . The stated adjustment(s) may be based on the load of the compressor determined at 802, the AC voltage received and/or generated at 804, the DC voltage received and/or generated at 606, one or more of the current levels detected at 808, and/or one or more of the reference signals generated at 810. The adjustments may also be based on capacitance of the DC bus, torque commanded of the compressor 102, predicted voltages of the output of the bridge rectifier 714, and/or other parameters associated with operation of the portion 700. The adjustments may advance or delay the transition start times and/or the transition end times. The adjustments may be determined based on equations, algorithms, maps, and/or tables relating the stated parameters, which may be stored in the memory 512 and accessed by the timing module 513. The adjustments may also be based on previous (historical) values and/or results, which may also be stored in and accessed from the memory 512. For example, if a last peak DC bus voltage or peak detected current (current detected by one of the current sensors 712a, 712b) was above a predetermined threshold, then the next transition end time or transition start time may be advanced to reduce the peak DC bus voltage and/or peak detected current.

[0138] At 816, the timing module 513 determines whether the phase angle of the output of the bridge rectifier 714 matches a predetermined start time of an active period. In addition or alternatively, voltages of the output of the bridge rectifier 714 (or input to switch 708) and/or the output of the buck converter 701 (or output of the inductor 704) may be compared to predetermined voltages for the predetermined start time to determine whether the stated condition exists. If there is a match, task 818 is performed, otherwise task 620 is performed.

[0139] At 818, the timing module 513 transitions to the inactive mode or low activity mode. If the timing module 513 transitions to the inactive mode, then the buck converter 701 is

transitioned to an OFF state and the switch 408 is switched to an open state. If the timing module 513 transitions to the low activity mode, then oscillated operation of the switch 708 continues, but at a reduced frequency and/or at a reduced duty cycle, such that OFF times of the switch 708 are increased and/or ON times of the switch 708 are decreased. Task 802 may be performed subsequent to task 818.

[0140] At 820, the timing module 513 may determine whether the DC bus voltage is less than or equal to the commanded DC voltage V_{DCCOM} and/or whether a next transition phase angle (next phase angle at which point a transition between operating modes occurs) is an end time (e.g., one of the end times e1-e6 of FIGs. 5-6) for an inactive mode and/or low activity mode. In addition or alternatively, voltages of the output of the bridge rectifier 714 and/or the buck converter 701 may be compared to predetermined voltages for the predetermined end time to determine whether one or more of the stated conditions exist. The timing module 513 may also or alternatively determine whether the current transition phase angle is within a predetermined range (e.g., between a last start time and a subsequent end time) of a current inactive mode or low activity mode. In addition or alternatively, voltages of the output of the bridge rectifier 714 and/or the buck converter 701 may be compared to predetermined voltages for the predetermined range to determine whether the stated condition exists. At the end time, the timing module 513 transitions from an inactive mode or low activity mode to an active and/or high activity mode. If the DC bus voltage is less than or equal to the commanded DC voltage V_{DCCOM} and/or the next transition phase angle is at an end time for an inactive mode or low activity mode, then task 822 is performed, otherwise task 821 is performed.

[0141] At 821, the timing module 513 determines whether (i) a light load condition exists, (ii) V_{AC} is less than a “high-line” voltage (is at or near a maximum operating voltage) and/or voltage out of the bridge 714 (or V_{bridge}) is less than a predetermined maximum voltage, and/or (iii) if temperature of the inverter power circuit 232 is inbound (i.e. within a predetermined temperature range). By checking if V_{AC} is less than the “high-line” voltage and/or output of the bridge 714 V_{bridge} is less than the predetermined maximum voltage, the system prevents stress on the inverter power circuit 232 of FIG. 2. If a light load condition exists, V_{AC} is less than a “high-line” voltage, V_{bridge} is less than a predetermined maximum voltage, and/or the temperature of the inverter power circuit 232 is inbound, then task 830 is performed, otherwise task 824 is performed. In one embodiment, when (i) a light load condition exists, (ii) V_{AC} is less than a “high-line” voltage and/or V_{bridge} is less than a predetermined maximum voltage, and (iii) the temperature of the inverter power circuit 232 is inbound, task 830 is performed, otherwise task 824 is performed.

[0142] At 822, the timing module 513 remains in the inactive mode or operating in the low activity mode. Task 802 may be performed subsequent to task 822. At 824, the timing module 513 determines whether the phase angle is an end time of an active mode and/or a high activity mode. In addition or alternatively, a voltage of the output of the bridge rectifier 714 and/or the buck converter 701 may be compared to predetermined voltages for the end time to determine whether the stated condition exists. If the phase angle is an end time, task 826 is performed, otherwise task 828 is performed.

[0143] At 826, the timing module 513 transitions to the active (or high activity) mode. This includes oscillated operation of the switch 708 at a first (or high) frequency. The duty cycle of the switch 808, including durations of ON times and OFF times, may correspond to duty cycle information determined at 814. Task 802 may be performed subsequent to task 826. At 828, the timing module 513 operates in the active mode or high activity mode. Task 802 may be performed subsequent to task 828.

[0144] At 830, the switch 708 is held in a closed (or ON) state and is not switched between states. When the switch is ON, the portion 700 performs as a 3-phase rectifier with a DC choke. Thus, no switching occurs when V_{AC} is at a nominal or low-line voltage. Task 802 may be performed subsequent to task 830.

[0145] When V_{AC} is too high, switching of the switch 708 (or bucking) occurs to decrease the bus voltage V_{DCOUT} . As the load increases, the bus voltage V_{DCOUT} is decreased, the amount of current through the inductor 704 increases and the control module 250 begins bucking by pulse width modulating the switch 708 to lower the bus voltage V_{DCOUT} (e.g., at tasks 826, 828) to a selected command voltage. The control module 250 may shape the current by adjusting the duty cycle of SW_{CTRL} during this period for PFC operation. This may include providing a flat (or constant) amount of current through the choke or a profiled current shape. The ability to buck during certain conditions and not to buck during other conditions is referred to as "partial buck" operation.

[0146] During the light load condition, the switch 708 is left ON since the amount of current through the inductor 704 is low. As the current through the inductor 704 increases for increased load, the switch may be pulse width modulated to decrease the bus voltage. This prevents overheating the inverter power circuit 232 of FIG. 2 during heavy load conditions.

[0147] Although the above tasks 816-830 are provided in a particular order, tasks 816-830 may be performed in a different order. As an example, task 821, 824, 826, 828 may be performed prior to tasks 816, 818, 820 and 822. If task 821, 824, 826, 828 are performed prior to tasks 816,

818, 820 and 822, then task 820 may be modified to determine whether the DC bus voltage is greater than or equal to the commanded voltage, the next transition phase angle is a start time of an active mode and/or high activity mode, and/or the current phase angle is within a predetermined range (e.g., between an end time of an inactive mode or a low activity mode and a subsequent start time of the inactive mode or low activity mode). This may include comparing a voltage of the outputs of the bridge rectifier 714 and/or the buck converter 701 to corresponding predetermined voltages and ranges to effectively determine if the next transition phase angle is a start time of an active mode and/or high activity mode, and/or the current phase angle is within a predetermined range.

10 **[0148]** The above-described tasks of FIGs. 9 and 11 are meant to be illustrative examples; the tasks may be performed sequentially, synchronously, simultaneously, continuously, during overlapping time periods or in a different order depending upon the application. Also, any of the tasks may not be performed or skipped depending on the implementation and/or sequence of events.

15 **[0149]** The above-described examples provide high bandwidth peak mode control that allow for precise control of turn ON and OFF points of the boost converter 401 and buck converter 701. Peak mode control refers to operating mode transition control near peak DC bus voltages and controls peak voltages of the DC bus voltages. This is because of high speed switch control and transitioning between operating modes based on transition phase angles. The transitioning phase angles are determined based on a generated reference sinusoidal signal. Thus, the transition phase angles are not determined based only on an AC input and/or an output of a bridge rectifier, but rather are determined based on both (i) an AC input and/or the output of the bridge rectifier, and (ii) the reference sinusoidal signal. This high speed control is provided with feedback control based on various parameters feedback to the control module 250, as described above.

25 **[0150]** Although the above described tasks of FIGs. 9 and 11 are primarily described with respect to adjusting phase angles at which start times and end times of operating modes occur, voltage thresholds and/or current thresholds may be adjusted, monitored and/or used as a basis for transitioning between operating modes. For example, the voltage $DC_{V_{Bus}}$ of the DC bus may be monitored and when the voltage $DC_{V_{Bus}}$ exceeds or drops below voltage thresholds, the timing module 513 of FIG. 8 may transition between (i) the active mode and/or high activity mode and (ii) the inactive or low activity mode. The voltage thresholds may correspond to the transition phase angles of the rectified AC signals out of one or more of the bridge rectifiers of the PFC circuit 212.

[0151] Instead of monitoring the phase and/or voltages of the AC input voltage V_{AC} and/or outputs of the bridge rectifiers 414, 416 of FIG. 4, the method of FIG. 12 may be performed to adjust transition timing between operating modes (the active mode, the high activity mode, the inactive mode, and/or the low activity mode). The method of FIG. 12 may be performed to maintain current levels detected by the current sensors 412 between predetermined operating ranges. The method of FIG. 12 may also be performed to adjust the DC bus voltage to be within a predetermined range for partial PFC operation.

[0152] In FIG. 12, a method of operating a drive (e.g., the drive 132 of FIG. 2) with a power converter (e.g., the boost converter 401 of FIG. 4) and a PFC circuit (e.g., the PFC circuit 212 of FIG. 2) is shown. Although the following tasks are primarily described with respect to the implementations of FIGs. 4 and 8, the tasks may be easily modified to apply to other implementations of the present disclosure. The tasks may be modified to apply to the buck converter 701 of FIG. 10. The tasks may be iteratively performed. Tasks 908-920 may be performed while tasks 922-940 are performed.

[0153] The method may begin at 900, which may include resetting the timers 515 of FIG. 8. At 902, the modules 502, 504, 506, 508 may receive and/or determine various signals and/or parameters, such as the signals received and determined during tasks 602-608 of FIG. 9. In one embodiment, the parameters include a measured DC bus voltage, a speed of a compressor, an amount of load, and/or an amount of current drawn by the compressor and/or detected by one or more of the current sensors 412.

[0154] At 908, the output module 510 may determine whether a first timer (one of timers 515) is indicative that a first predetermined period has been reached (e.g., 100 ms). The first predetermined period may be set to provide stability. If the first predetermined period (or amount of time) has passed, task 912 is performed, otherwise task 910 may be performed. At 910, the first timer may be incremented, if implemented as a counter. Task 902 may be performed subsequent to tasks 908 and/or 910. At 912, the first timer may be reset.

[0155] At 914, the output module 510 determines whether a peak current I_{peak} and/or measured current level is greater than a first predetermined maximum current level $I_{predmax1}$ (e.g., 20A). Task 914 may be performed to determine if partial PFC has been performed too long, such that the peak current I_{peak} is high and should be decreased to be within a predetermined range (e.g., between 15A and 20A). The peak current I_{peak} may be, for example, current detected by the second current sensor 412b or indicated by PFC_{INC2} . If the peak current I_{peak} is greater than the first predetermined maximum current level $I_{predmax1}$, then task 916 is performed, otherwise task 918 is performed.

[0156] At 916, the output module 510 sets an adjustment variable Adjust equal to Adjust minus a predetermined amount (e.g., 2V). The adjustment variable Adjust is used to adjust a commanded DC voltage V_{DCCOM} at 940. For example, if commanded DC voltage V_{DCCOM} is increased, then less partial PFC operation. If commanded DC voltage V_{DCCOM} is decreased, then more (or longer) partial PFC operation is performed. Task 902 may be performed after task 916.

[0157] At 918, the output module 510 determines whether I_{peak} and/or measured current level is less than a predetermined minimum current level $I_{predmin}$ (e.g., 15A). Task 918 may be performed to determine if I_{peak} is low and partial PFC operation can be performed longer to increase I_{peak} to be within the predetermined range. When initially starting the drive 132, the current detected by the current sensors 412 may be low and gradually increase. As an example, the current detected by the current sensor 412b may gradually increase to be between $I_{predmin}$ and $I_{predmax1}$. If I_{peak} and/or measured current level is less than $I_{predmin}$, then task 920 is performed, otherwise task 902 is performed. At 920, Adjust is set equal to Adjust plus a predetermined amount (e.g., 2V).

[0158] At 922, the output module 510 determines whether a second timer (another one of the timers 515) is indicative of a second predetermined period (e.g., 1ms) being reached. The second predetermined period may be less than the first predetermined period and may be set to allow detection of quick changes in current and/or voltage. If the second predetermined period (or amount of time) has passed, task 924 is performed, otherwise task 923 may be performed. At 923, the second timer may be incremented, if implemented as a counter. Task 902 may be performed subsequent to tasks 922 and/or 923. At 924, the second timer may be reset.

[0159] At 925, the control module 250 determines whether power factor correction is disabled. If power factor correction is disabled, task 926 is performed, otherwise task 927 is performed. At 926, the output module 510 sets Adjust equal to 0 and V_{DCCOM} equal to 0.

[0160] At 927, the output module 510 may (i) determine initial values for a requested voltage V_{req} (e.g., 280V) and a temporary voltage V_{tmp} if the corresponding drive 132 is powered up, or (ii) adjust and/or maintain current values of V_{req} and V_{tmp} if performing an additional iteration of the method of FIG. 12. The requested voltage V_{req} may refer to a minimum voltage requested for operation of the compressor 102. The temporary voltage V_{tmp} may be set equal to a peak voltage V_{peak} (e.g., 325V) plus an offset voltage (e.g., 10V). V_{tmp} may be initially set high, such that there are not any current peaks, such as peaks 464 of FIG. 6, and the current peak is I_{base} . The peak voltage V_{peak} is a peak AC V_{AC} input voltage or peak voltage out of the bridge rectifiers 414, 416. The requested voltage V_{req} may be determined based on the signals and/or parameters received, generated and/or determined during task 902. The requested voltage

V_{req} may be based on a speed of a motor of the compressor 102 and/or other operating conditions (e.g., load on the compressor 102). The requested voltage V_{req} may be determined based on an algorithm, a map, a table, and/or equations. As an example, the table may relate speeds of the motor of the compressor 102 to requested voltages.

- 5 **[0161]** At 928, the output module 510 determines whether V_{req} is greater than or equal to V_{tmp}. If V_{req} is greater than or equal to V_{tmp}, then task 930 is performed, otherwise task 932 is performed. If V_{req} is greater than or equal to V_{tmp} and the power converter is a boost converter, then the boost converter may be operated to continuously boost the DC bus voltage. At 930, the output module 510 sets Adjust equal to 0 and V_{DCCOM} equal to V_{req}.
- 10 **[0162]** At 932, the output module 510 determines whether (i) I_{peak} and/or measured current level is greater than a second predetermined maximum current level I_{predmax2} (e.g., 25A), and/or (ii) Adjust is less than 0. I_{predmax2} is greater than I_{predmax1}. This task determines whether the current detected by one of the current sensors 412 is too high, which may occur when load on the compressor 102 increases. If I_{peak} and/or measured current level is greater
- 15 than I_{predmax 2} and/or Adjust is less than 0, then task 934 is performed, otherwise task 936 is performed. Performance of tasks 932 and 934 allows the control module 250 executing the PFC algorithm to quickly adjust and prevent tripping of a power shut off procedure. If a trip occurs, power to the compressor is shut off. The control module 250 instead of gradually reducing the current, performs task 934 to quickly reduce the current, such that the control module is
- 20 operating in the full PFC mode rather than the partial PFC mode. This is unlike when performing, for example, tasks 914-920 when the control module 250 may be operating in the partial PFC mode. Task 934 may also be performed when Adjust is a negative value. This prevents voltage from being adjusted in an upward direction. At 934, the output module sets (i) Adjust equal to 0, and (ii) V_{DCCOM} equal to V_{tmp}. This resets Adjust and V_{DCCOM} to initial
- 25 values.
- [0163]** At 936, the output module 510 determines whether Adjust is greater than V_{tmp} minus V_{req}. This task prevents V_{DCCOM} from dropping below V_{req}. If Adjust is greater than V_{tmp}-V_{req}, then task 938 is performed, otherwise task 940 is performed. At 938, the output module 510 sets (i) Adjust equal to V_{tmp} minus V_{req}, and (ii) V_{DCCOM} equal to V_{req}.
- 30 **[0164]** At 940, the output module 510 sets the commanded DC voltage V_{DCCOM} equal to V_{tmp} minus Adjust. Task 902 may be performed subsequent to tasks 930, 934, 938 and 940.
- [0165]** During the above-described tasks, V_{peak} and I_{peak} may be detected via the peak detector 517. The peak detector 517 may detect peak voltages and/or current levels of the power

converter and/or the DC bus. The peak detector 517 may store and update the peak voltages and/or current levels. The peak detector 517 may update increasing peak levels quicker than decreasing peak levels. The peak detector 517 may thus perform as a filter for peak levels that are decreasing and may not perform as a filter for peak levels that are increasing. The peak
 5 detector 517 may track peak levels over each cycle of the AC input voltage V_{AC} and/or outputs of the bridge rectifiers 414, 416. The tracking and updating of the peak voltages and current levels may be performed as described in U.S. Patent No. 8,508,166, which is incorporated herein by reference.

[0166] The above-described tasks of FIG. 12 may be performed for single phase, 3-phase,
 10 and/or multi-phase operation. The above-described tasks of FIG. 12 may be applied to a circuit having a single rectifier converting a 3-phase input to a single rectified (or DC) output. The above-described tasks of FIG. 12 may also be applied to a circuit receiving multiple independent phases of current and having multiple rectifiers receiving a respective one of the independent phases and outputting a respective rectified (or DC) output. The above-described tasks of FIG.
 15 12 are meant to be illustrative examples; the tasks may be performed sequentially, synchronously, simultaneously, continuously, during overlapping time periods or in a different order depending upon the application. Also, any of the tasks may not be performed or skipped depending on the implementation and/or sequence of events.

[0167] Although the above-described tasks 908-920 are described with respect to peak mode
 20 control, average mode control may be used as an alternative. This includes changing the decisions of tasks 914 and 918 to be based on average current rather than peak current.

[0168] The method of FIG. 12 may be modified for the buck converter 701 of FIG. 10. During a buck converter implementation, the bus current may be adjusted in an upward direction rather than in a downward direction as in a boost converter implementation. The above-described tasks
 25 908-920 are associated with an inner current control loop. The above-described tasks 922-940 are associated with an outer voltage control loop. In one buck converter embodiment, the voltage control loop is used and not the current control loop, where the bus voltage is equal to a product of (i) the voltage out of the rectification circuit 702 or V_{bridge} , and (ii) a duty cycle of SW_{CTRL} . In one embodiment, the outer voltage loop associated with tasks 922-940 is the same for buck
 30 converter operation. In another embodiment, the inner current control loop and the outer voltage control loop are utilized. For buck operation, the inductance of the inductor 704 may be smaller for peak current mode control than for average current mode control.

[0169] FIG. 13 shows a single phase converter circuit 1000 that includes a first line protection circuit 1002, a first line EMI filter 1004, a common mode choke 1006, a second protection

circuit 1008, a grounded EMI filter 1010, a second line EMI filter 1012, a charging circuit 1014, and a PFC circuit 1016. The PFC circuit 1016 includes a rectification circuit 1018, one or more non-line non-grounded EMI filters 1020 and a driver circuit 1022. The rectification circuit 1018 and the driver circuit 1022 may be implemented similarly to and/or the same as any of the
5 rectification circuits and driver circuits disclosed herein. The converter circuit 1000 converts a single phase AC input voltage to a DC voltage, which is provided on a DC bus (e.g., the DC bus shown in FIG. 2). The first line protection circuit 1002 provides line surge protection to limit current, including at startup, provided from AC inputs (may be referred to as “mains”) of the first line protection circuit 1002 to circuits (e.g., the common mode choke 1006, the charging
10 circuit 1014, and the PFC circuit 1016) downstream from the first line protection circuit 1002. The first line protection circuit 1002 may include fuses and metal oxide varistors (MOVs).

[0170] The first line EMI filter 1004 filters an output of the first line protection circuit 1002 and decouples circuits downstream from the first line EMI filter 1004 from the AC inputs of the first line protection circuit 1002. The first line EMI filter 1004 may include one or more across-
15 the-line capacitors (e.g., X-rated capacitors) connected in parallel across the outputs of the first line protection circuit 1002.

[0171] The common mode choke 1006 provides high impedance to a common mode signal to provide EMI filtering and filters an output of the first line EMI filter 1004. The common mode choke 1006 decouples circuits downstream from the common mode choke 1006 from circuits
20 upstream from the common mode choke 1006.

[0172] The second protection circuit 1008 provides line to ground surge protection and may include MOVs and a gas discharge tube (GDT). The grounded EMI filter 1010 provides EMI filtering and may include line-to-ground capacitors (e.g., Y-rated capacitors). The second protection circuit 1008 and the line-to-ground capacitors may be connected to ground 1009 (e.g.,
25 earth ground). One or both of the protection circuits 1002, 1008 may be included. Use of both protection circuits provides increased protection.

[0173] The charging circuit 1014 limits, including at startup, an amount of current that flows from the AC inputs of the first line protection circuit 1002 to the DC bus. Impedance between the mains and capacitors downstream from the rectification circuit 1018 may be small. For this
30 reason, the charging circuit 1014 limits the amount of current to prevent damage to circuit components downstream from the charging circuit 1014. The charging circuit 1014 may include a relay, variable resistors, and other circuit components. The other circuit components may include capacitors if the charging circuit 1014 is, for example, on a line side of the rectification circuit 1018. The charging circuit 1014 can also be placed on a load side of the rectification

circuit 1018 if one or more current limiting elements of the charging circuit 1014 conducts DC. As an example, current limiting elements are shown in FIG. 22 and may include resistors, thermistors (e.g., negative thermal coefficient thermistors or positive thermal coefficient thermistors), or other current limiting elements.

5 **[0174]** The PFC circuit 1016 may be replaced by, include and/or be configured similarly to one of the other single phase input PFC circuits disclosed herein (e.g., the PFC circuit 400 of FIG. 4). The rectification circuit 1018 may include one or more rectifiers. The non-line non-grounded EMI filter(s) 1020 filter an output of the rectification circuit 1018 and decouples a converter (e.g., boost converter 401 of FIG. 4) or the driver circuit 1022 from a bridge rectifier
10 (e.g., the primary bridge rectifier 414 of FIG. 4) to minimize noise generated by the converter from being seen at the bridge rectifier. The rectification circuit 1018 may be configured similarly to the rectification circuit 402 of FIG. 4. In one embodiment, the rectification circuit 1018 does not include the rectifier 416.

[0175] The non-line non-grounded EMI filter(s) 1020 may include one or more capacitors
15 connected in parallel. An example of the non-line non-grounded EMI filter(s) 1020 is shown in FIGs. 7, 19 and 20 and is provided to reduce and/or eliminate the need for the second line EMI filter 1012. The capacitances of the capacitors in the second EMI filter 1012 depend on the capacitance(s) of the one or more capacitors in the non-line non-grounded EMI filter(s) 1020. The larger the capacitance(s) of the non-line non-grounded EMI filter(s) 1020, the smaller the
20 capacitances of the second EMI filter 1012. The number of capacitors in the non-line non-grounded EMI filter(s) 1020 may be less than the number of capacitors in the second EMI filter 1012. In one embodiment, the non-line non-grounded EMI filter(s) 1020 includes only a single capacitor. This reduces the number, costs and sizes of the capacitors associated with the converter circuit 1000, which reduces an envelope of the converter circuit 1000 and size of a
25 corresponding printed circuit board (PCB) and heat sink (an example PCB and heat sink are shown in FIG. 20).

[0176] In addition, the capacitors of the EMI filters 1004 and 1012 are X-capacitors because the capacitors are rated for high voltage and are connected across mains (or AC lines). The capacitors of the grounded EMI filter 1010 are line-to-ground capacitors (Y-capacitors) because
30 the capacitors are rated for a high voltage and are connected from the AC lines to ground 1009. In contrast, the capacitors of the non-line non-grounded EMI filter(s) 1020 are connected between a DC voltage line and reference terminal 1023 and the DC voltage of the DC voltage line and see less AC voltage and are not directly across the AC mains. Thus, the capacitors of the non-line non-grounded EMI filter(s) 1020 do not need to satisfy power and safety

requirements associated with the use of X-capacitors and/or Y-capacitors and can be much smaller in size and constructed differently than X-capacitors and Y-capacitors. In addition, each X-capacitor and Y-capacitor transitions to an open state in an event of a failure of the X-capacitor or Y-capacitor. Each of the capacitors (referred to as a DC bus rated capacitor) of the non-line non-grounded EMI filter(s) 1020 are rated for the DC bus and may be in an open state or a shorted (i.e. providing a low resistive connection) state in an event of a failure of the DC bus rated capacitor.

[0177] The DC bus rated capacitors have a higher resonance frequency than the X-capacitors and the Y-capacitors due to the reduced size and different construction of the DC bus rated capacitors. The higher the resonance frequency, the more effective the capacitor is against high frequency EMI. The higher the resonance frequency of a capacitor, the larger the range of high frequencies for which signals are prevented from passing through the capacitor. In addition, by having the DC bus rated capacitors downstream from the rectification circuit 1018 rather than X-capacitors upstream from the rectification circuit, the effective overall capacitance of the rectification circuit and the DC bus rated capacitors is increased, thereby providing a lower cutoff frequency and thus increased filtering (i.e. filtering out an increased number of frequencies).

[0178] The non-line non-grounded EMI filter(s) 1020 may have multiple capacitors connected in parallel as shown in FIG. 7. The smaller in size and the more capacitors that are connected in parallel, the better the high frequency characteristics of the non-line non-grounded EMI filter(s) 1020. For example, 3 small capacitors (having small capacitances) connected in parallel downstream from the rectification circuit 1018 have better high frequency characteristics than a single larger capacitor (having a large capacitance) connected upstream from the rectification circuit 1018. The 3 small capacitors have a higher resonance frequency than the single large capacitor. Each capacitor has parasitic equivalent series resistance (ESR) and parasitic equivalent series inductance (ESL), which can be undesirable characteristics. Connecting in parallel 3 small capacitors can significantly reduce the effects of the parasitic ESR and parasitic ESL as compared to using a single larger capacitor.

[0179] Examples of the protection circuits 1002, 1008, the EMI filters 1004, 1010, 1020, and the common mode choke 1006 are shown in FIGs. 19-20. Examples of the PFC circuit 1016 are shown in FIGs. 4, 23. The driver circuit 1022 may include a boost converter, a buck converter, or other driver circuit and provides a DC output on the DC bus. The driver circuit 1022 also has a reference output terminal 1023 (e.g., 0 voltage terminal or other reference voltage and/or return terminal).

[0180] FIG. 14 shows a single phase converter circuit 1050 that includes the first line protection circuit 1002, the first line EMI filter 1004, the charging circuit 1014, and a PFC circuit 1052. The PFC circuit 1052 includes the rectification circuit 1018, a common mode choke 1053, a second protection circuit 1054, a grounded EMI filter 1056, one or more non-line non-grounded EMI filters 1058 and the driver circuit 1022. By including the common mode choke 1053, the second protection circuit 1054, the grounded EMI filter 1056, and the one or more non-line non-grounded EMI filters 1058 downstream from the rectification circuit 1018, envelope of the convert circuit 1050 is minimized and may be smaller than the envelope of the converter circuit 1000 of FIG. 13. By including the first line protection circuit 1002 and the first line EMI filter 1004 upstream from the rectification circuit 1018, surge protection is provided for the rectification circuit 1018. The benefit is larger in 3-phase circuits than in single phase circuits because three capacitors connected from each line to each other line are reduced to one capacitor across the DC bus.

[0181] Although the common mode choke 1053, second protection circuit 1054, and grounded EMI filter 1056 are shown downstream from the rectification circuit 1018, one or more of the common mode choke 1053, the second protection circuit 1054, the grounded EMI filter 1056, the non-line non-grounded EMI filters 1058 may not be included. If the common mode choke 1053, the second protection circuit 1054, the grounded EMI filter 1056, and/or the non-line non-grounded EMI filters 1058 are not included, then the common mode choke 1006, the second protection circuit 1008, the grounded EMI filter 1010, and/or the second line EMI filter 1012 may be included upstream from the rectification circuit 1018, as shown in FIG. 13. For example, if the common mode choke 1053 is not included, then the common mode choke 1006 is included.

[0182] FIG. 15 shows a single phase converter circuit 1100 that includes the first line protection circuit 1002, a charging circuit 1014 and a PFC circuit 1102. The PFC circuit 1102 includes the rectification circuit 1018, a first line EMI filter 1104, the common mode choke 1053, the second protection circuit 1054, the grounded EMI filter 1056, the one or more non-line non-grounded EMI filters 1058 and the driver circuit 1022. By including the first line protection circuit 1002 upstream from the charging circuit 1014, surge protection is provided for the rectification circuit 1018. The first line EMI filter 1104 may include one or more DC bus rated capacitors that are connected in parallel across the outputs of the rectification circuit 1018. In one embodiment, the second protection circuit 1054 is not included because insulation of the corresponding system with respect to ground is adequate enough that additional protection is not needed. In other embodiments, the second protection circuit 1054 is included.

[0183] FIG. 16 shows a 3-phase converter circuit 1150 that includes a first line protection circuit 1152, a first line EMI filter 1154, a common mode choke 1156, a second protection circuit 1158, a grounded EMI filter 1160, a second line EMI filter 1162, a charging circuit 1164, and a PFC circuit 1166. The PFC circuit 1166 includes a rectification circuit 1168, one or more non-line non-grounded EMI filter(s) 1170 and a driver circuit 1172. The rectification circuit 1168 and the driver circuit 1172 may be implemented similarly to and/or the same as any of the rectification circuits and driver circuits disclosed herein. The converter circuit 1150 converts 3-phase AC input voltages (e.g., 480 V AC or 600V AC) to a DC voltage, which is provided on a DC bus (e.g., the DC bus shown in FIG. 2). The first line protection circuit 1152 provides line surge protection to limit current, including at startup, provided from AC inputs (may be referred to as “mains”) of the first line protection circuit 1152 to circuits (e.g., the common mode choke 1156, the charging circuit 1164, and the PFC circuit 1166) downstream from the first line protection circuit 1152. The first line protection circuit 1152 may include fuses and MOVs.

[0184] The first line EMI filter 1154 filters an output of the first line protection circuit 1152 and decouples circuits downstream from the first line EMI filter 1154 from the AC inputs of the first line protection circuit 1152. The first line EMI filter 1154 may include one or more across-the-line capacitors (e.g., X-rated capacitors) connected across the outputs of the first line protection circuit 1152.

[0185] The common mode choke 1156 provides high impedance to a common mode signal to provide EMI filtering and filters an output of the first line EMI filter 1154. The common mode choke 1156 decouples circuits downstream from the common mode choke 1156 from circuits upstream from the common mode choke 1156.

[0186] The second protection circuit 1158 provides line to ground surge protection and may include MOVs and a GDT. The grounded EMI filter 1160 provides EMI filtering and may include line-to-ground capacitors (e.g., Y-rated capacitors). The second protection circuit 1158 and the line-to-ground capacitors may be connected to ground 1159 (e.g., earth ground).

[0187] The charging circuit 1164 limits, including at startup, an amount of current that flows from the AC inputs of the first line protection circuit 1152 to the DC bus. Impedance between the mains and capacitors downstream from the rectification circuit 1168 may be small. For this reason, the charging circuit 1164 limits the amount of current to prevent damage to circuit components downstream from the charging circuit 1164. The charging circuit 1164 may include a relay, variable resistors, and other circuit components.

[0188] Although the charging circuit is shown upstream from the PFC circuit 1450 and the rectification circuit 1168, the charging circuit 1164 may be included as part of the PFC circuit 1450 and/or be downstream of rectification circuit 1168. An example of this is shown in FIG. 25. Although a charging circuit is only shown as being downstream of a rectification circuit in FIG. 25, charging circuits corresponding to the embodiments of FIGs. 13-24 may be located downstream of the corresponding rectification circuits. If the charging circuit 1164 is located downstream of the rectification circuit 1168, then the charging circuit 1164 may include only a single pole relay for the DC output line of the rectification circuit 1168. An amount of current passing through the single pole relay may be higher than an amount of current passing through each of the one or more relays of the charging circuit 1164 when the charging circuit 1164 is located upstream of the rectification circuit 1168.

[0189] The PFC circuit 1166 may be replaced by, include and/or be configured similarly to one of the other 3-phase input PFC circuits disclosed herein (e.g., the PFC circuit 700 of FIG. 10). The rectification circuit 1168 may include one or more rectifiers. The non-line non-grounded EMI filter(s) 1170 filter an output of the rectification circuit 1168 and decouples a converter (e.g., buck converter 701 of FIG. 10) or the driver circuit 1172 from a bridge rectifier (e.g., the primary bridge rectifier 714 of FIG. 10) to minimize noise generated by the converter from being seen at the bridge rectifier. The rectification circuit 1168 may be configured similarly to the rectification circuit 702 of FIG. 10.

[0190] The non-line non-grounded EMI filter(s) 1170 may include one or more capacitors connected in parallel. An example of the non-line non-grounded EMI filter(s) 1170 is shown in FIGs. 7, 21 and 22 and is provided to reduce and/or eliminate the need for the second line EMI filter 1162. The capacitances of the capacitors in the second EMI filter 1162 depend on the capacitance(s) of the one or more capacitors in the non-line non-grounded EMI filter(s) 1170. The larger the capacitance(s) of the non-line non-grounded EMI filter(s) 1170, the smaller the capacitances of the second EMI filter 1162. The number of capacitors in the non-line non-grounded EMI filter 1170 may be less than the number of capacitors in the second EMI filter 1162. This reduces the number, costs and sizes of the capacitors associated with the converter circuit 1150, which reduces an envelope of the converter circuit 1150 and size of a corresponding PCB and heat sink (an example PCB and heat sink are shown in FIG. 22). The second line EMI filter 1162 may not be included if the non-line non-grounded EMI filter(s) 1170 have include circuit components (e.g., capacitors) that provide appropriate filtering (e.g., permitting passage of frequencies within a predetermined frequency range). One capacitor in non-line non-grounded EMI filter(s) 1170 can provide the same protection as 3 capacitors in

second EMI filter 1162. The type of capacitor used in non-line non-grounded EMI filter(s) 1170 may not be a X-rated capacitor as are the capacitors in the second EMI filter 1162, which leads to smaller more cost effective EMI filtering.

[0191] In addition, the capacitors of the EMI filters 1154 and 1162 are X-capacitors because the capacitors rated for high voltage and are connected across mains (or AC lines). The capacitors of the grounded EMI filter 1160 are line-to-ground capacitors because the capacitors are rated for a high voltage and are connected from the AC lines to ground 1159. In contrast, the capacitors of the non-line non-grounded EMI filter(s) 1170 are connected between a DC voltage line and a reference terminal 1173 and the DC voltage of the DC voltage line is less than the AC voltages across the mains. Thus, the capacitors of the non-line non-grounded EMI filter(s) 1170 do not need to satisfy power and safety requirements as associated with the use of X-capacitors and/or Y-capacitors and can be much smaller in size and constructed differently than X-capacitors and Y-capacitors. In addition, each X-capacitor and Y-capacitor transitions to an open state in an event of a failure of the X-capacitor or Y-capacitor. Each of the capacitors (referred to as a DC bus rated capacitor) of the non-line non-grounded EMI filter(s) 1170 are rated for the DC bus and may be in an open state or a shorted (i.e. providing a low resistive connection) state in an event of a failure of the DC bus rated capacitor.

[0192] The DC bus rated capacitors have a higher resonance frequency than the X-capacitors and the Y-capacitors due to the reduced size and different construction of the DC bus rated capacitors. In addition, by having the DC bus rated capacitors downstream from the rectification circuit 1018 rather than X-capacitors upstream from the rectification circuit, the effective overall capacitance of the rectification circuit and the DC bus rated capacitors is increased, thereby providing a lower cutoff frequency and thus increased filtering (i.e. filtering out an increased number of frequencies).

[0193] Examples of the protection circuits 1152, 1158, the EMI filters 1154, 1160, 1170, and the common mode choke 1156 are shown in FIGs. 21-22. Examples of the PFC circuit 1166 are shown in FIGs. 10, 24. The driver circuit 1172 may include a boost converter, a buck converter or other driver circuit and provides a DC output on the DC bus. The driver circuit 1172 has an output reference terminal 1173.

[0194] FIG. 17 shows a 3-phase converter circuit 1200 that includes the first line protection circuit 1152, the first line EMI filter 1154, the charging circuit 1164, and a PFC circuit 1202. The PFC circuit 1202 includes the rectification circuit 1168, a common mode choke 1203, a second protection circuit 1204, a grounded EMI filter 1206, one or more non-line non-grounded EMI filters 1208 and the driver circuit 1172. By including the common mode choke 1203, the

second protection circuit 1204, the grounded EMI filter 1206, and the one or more non-line non-grounded EMI filters 1208 downstream from the rectification circuit 1168, envelope of the convert circuit 1200 is minimized and may be smaller than the envelope of the converter circuit 1150 of FIG. 16.

- 5 **[0195]** Although the common mode choke 1203, second protection circuit 1204, and grounded EMI filter 1206 are shown downstream from the rectification circuit 1168, one or more of the common mode choke 1203, the second protection circuit 1204, the grounded EMI filter 1206, and the non-line non-grounded EMI filters 1208 may not be included. If the common mode choke 1203, the second protection circuit 1204, the grounded EMI filter 1206, and/or the non-
- 10 line non-grounded EMI filters 1208 are not included, then the common mode choke 1156, the second protection circuit 1158, the grounded EMI filter 1160, and/or the second line EMI filter 1162 may be included upstream from the rectification circuit 1168, as shown in FIG. 17. For example, if the common mode choke 1203 is not included, then the common mode choke 1156 is included.
- 15 **[0196]** By having the common mode choke 1203 downstream from the rectification circuit 1168 rather than the common mode choke 1156 upstream from the rectification circuit 1168; a smaller common mode choke is included. For example, the common mode choke 1156 may include three coils, whereas the common mode choke 1203 may have two coils. This reduces the number of inductors (or windings), total number of turns per inductor, and the size of the
- 20 common mode choke included. As an example, the common mode choke 1156 may have $3/2$ as many windings and/or turns as the common mode choke 1203. Since the inductance of a common mode choke is a function of the number of turns squared, the inductance of the common mode choke 1203 is greater than the inductance of the common mode choke 1156. In addition, by having the common mode choke 1203 downstream from (or on a right-hand side of)
- 25 the rectification circuit 1168, a frequency cutoff of the filter is lowered. Also, with a same number of turns per inductor between the common mode chokes 1156, 1203 and since the common mode choke 1203 has one less winding than the common mode choke 1156, the common mode choke 1203 has $(3/2)^2$ more inductance than the common mode choke 1156. Two coils are connected in parallel instead of three coils, which increases inductance further by
- 30 another factor of $3/2$ (or a total of $(3/2)^3$ more inductance).

[0197] By having the one or more non-line non-grounded EMI filters 1208 downstream from the rectification circuit 1168 rather than having corresponding EMI filters upstream from the rectification circuit 1168, overall effective capacitance of the EMI filters is increased and as a result the corresponding cutoff frequency is reduced. This holds true if capacitors of the non-line

non-grounded EMI filters 1208 have a same capacitance as the capacitors of the upstream EMI filters. The reduced cutoff frequency corresponds to increased filtering. Overall effective capacitance of the converter circuit 1150 due to the inclusion of the non-line non-grounded EMI filters 1208 and not the inclusion of the second line EMI filter 1162 may be $\sqrt{3}$ more effective capacitance than inclusion of the second line EMI filter 1162 and not inclusion of the non-line non-grounded EMI filters 1208.

[0198] FIG. 18 shows a 3-phase converter circuit 1250 that includes the first line protection circuit 1152, a charging circuit 1164 and a PFC circuit 1252. The PFC circuit 1252 includes the rectification circuit 1018, a first line EMI filter 1254, the common mode choke 1203, the second protection circuit 1204, the grounded EMI filter 1206, the one or more non-line non-grounded EMI filters 1208 and the driver circuit 1172. The first line EMI filter 1254 may include one or more DC bus rated capacitors that are connected in parallel across the outputs of the rectification circuit 1168.

[0199] FIG. 19 shows an example of the 3-phase converter circuit 1000 of FIG. 13. FIG. 19 shows a 3-phase converter circuit 1000' that includes a first line protection circuit 1002', a first line EMI filter 1004', a common mode choke 1006', a second protection circuit 1008', a grounded EMI filter 1010', a second line EMI filter 1012', a charging circuit 1014, and a PFC circuit 1016'. The PFC circuit 1016' includes a rectification circuit 1018, a non-line non-grounded EMI filter 1020' and a driver circuit 1022.

[0200] The first line protection circuit 1002' includes fuses 1300 and a MOV 1302. The fuses 1300 are connected in series between (i) inputs of the 3-phase converter circuit 1000' and the mains, and (ii) inputs of the first EMI filter 1004'. The MOV 1302 is connected across the outputs of the fuses 1300.

[0201] The first line EMI filter 1004' may include one or more across-the-line capacitors, X-rated capacitors, and/or other UL (USA) regulation safety rated capacitors (a single capacitor 1304 is shown) having V_{DD} construction for being applied across mains of an AC source. The capacitor 1304 is connected across the outputs of the first line protection circuit 1002'.

[0202] The common mode choke 1006' includes inductors 1306 wound around a common core 1307. The inductors 1306 are connected in series between respective outputs of the first line EMI filter 1004' and inputs of the second protection circuit 1008'.

[0203] The second protection circuit 1008' includes MOVs 1308 and a GDT 1310. First ends of the MOVs 1302 are connected to respect outputs of the common mode choke 1006'. Second

ends of the MOVs 1308 are connected to a first end of the GDT 1310. A second end of the GDT 1310 is connected to the ground 1009.

[0204] The grounded EMI filter 1010' includes pairs of capacitors 1312, 1314. The capacitors in the first pair of capacitors 1312 are connected in series between a first output (or first line) of the second protection circuit 1008' and the ground 1009. The capacitors in the second pair of capacitors 1314 are connected in series between a second output (or second line) of the second protection circuit 1008' and the ground 1009. Although multiple capacitors are connected in series between the lines and the ground 1009, a single capacitor may be connected between each of the lines and the ground 1009. Multiple capacitors may be connected in series as shown for high voltage (e.g., 600V) applications.

[0205] The second line EMI filter 1012' includes one or more capacitors (one capacitor 1316 is shown) connected across the outputs (or lines) of the grounded EMI filter 1010'. The size of the capacitor 1316 may be small (e.g., 0.01 μ F-0.1 μ F), since another EMI filter 1020' (referred to as the non-line non-grounded EMI filter 1020') is connected between a DC line and ground downstream from the rectification circuit 1018.

[0206] The non-line non-grounded EMI filter 1020' may include one or more capacitors connected across outputs of the rectification circuit 1018. This is different than the second line EMI filter 1012' including multiple large capacitors and the non-line non-grounded EMI filter 1020' not being included in the PFC circuit 1016', which would result in using larger capacitors having higher capacitances, a larger PCB and a larger heat sink. As shown, the non-line non-grounded EMI filter 1020' may include a single capacitor 1310. In one embodiment, the non-line non-grounded EMI filter 1020' includes a single capacitor (e.g., 0.33 μ F) and the second line EMI filter 1012' includes a capacitor connected across the AC lines, as shown. As an example, each of the capacitors of the second line EMI filter 1012' may be a 0.01-0.1 μ F capacitor. In one embodiment, the capacitance of the capacitor 1316 is an order of magnitude or more less than the capacitance of the capacitor 1320.

[0207] FIG. 20 shows an example of the converter circuit 1050 of FIG. 14. FIG. 20 shows a 3-phase converter circuit 1050' that includes a first line protection circuit 1002', a first line EMI filter 1004', the charging circuit 1014, and a PFC circuit 1052'. The circuits 1002', 1004', 1014, 1052' may be mounted on a PCB 1330, which may include a heat sink 1332. The heat sink 1332 dissipates heat generated by circuit components mounted on the PCB 1330. The PFC circuit 1052' includes the rectification circuit 1018, a common mode choke 1053', a second protection circuit 1054', a grounded EMI filter 1056', one or more non-line non-grounded EMI filters 1058' and the driver circuit 1022. By including the common mode choke 1053', the second

protection circuit 1054', the grounded EMI filter 1056', and the one or more non-line non-grounded EMI filters 1058' downstream from the rectification circuit 1018, an envelope of the convert circuit 1050' is minimized and may be smaller than an envelope of the converter circuit 1000' of FIG. 19. By including the first line protection circuit 1002' and the first line EMI filter 1004' upstream from the rectification circuit 1018, surge protection is provided for the rectification circuit 1018.

[0208] Although the common mode choke 1053', second protection circuit 1054', and grounded EMI filter 1056' are shown downstream from the rectification circuit 1018, one or more of the common mode choke 1053', the second protection circuit 1054' and the grounded EMI filter 1056' may not be included. If the common mode choke 1053', the second protection circuit 1054' and/or the grounded EMI filter 1056' are not included, then the common mode choke 1006', the second protection circuit 1008' and/or the grounded EMI filter 1010' may be included upstream from the rectification circuit 1018, as shown in FIG. 13. For example, if the common mode choke 1053' is not included, then the common mode choke 1006' is included.

[0209] The common mode choke 1053' includes inductors 1340 and a core 1342. The inductors 1340 are connected in series between respective outputs of the rectification circuit 1016 and inputs of the second protection circuit 1054'.

[0210] The second protection circuit 1054' includes MOVs 1344 and a GDT 1346. First ends of the MOVs 1344 are connected to respect outputs of the common mode choke 1053'. Second ends of the MOVs 1344 are connected to a first end of the GDT 1346. A second end of the GDT 1346 is connected to the ground 1009.

[0211] The grounded EMI filter 1056' includes pairs of capacitors 1350, 1352. The capacitors in the first pair of capacitors 1350 are connected in series between a first output (or first line) of the second protection circuit 1054' and the ground 1009. The capacitors in the second pair of capacitors 1352 are connected in series between a second output (or second line) of the second protection circuit 1054' and the ground 1009. Although multiple capacitors are connected in series between the lines and the ground 1009, a single capacitor may be connected between each of the lines and the ground 1009. Multiple capacitors may be connected in series as shown for high voltage (e.g., 600V) applications.

[0212] The one or more non-line non-grounded EMI filters 1058' may include one or more capacitors connected in parallel between the DC line 1360 and a return (or low voltage) line 1362. The one or more capacitors are DC bus rated capacitors (e.g., capacitor 1320 and/or capacitor 1364). In one embodiment, a single capacitor is included.

[0213] FIG. 21 shows an example of the converter circuit 1150 of FIG. 16. FIG. 21 shows a 3-phase converter circuit 1150' that includes a first line protection circuit 1152', a first line EMI filter 1154', a common mode choke 1156', a second protection circuit 1158', a grounded EMI filter 1160', a second line EMI filter 1162', the charging circuit 1164, and a PFC circuit 1166'.

5 The PFC circuit 1166' includes the rectification circuit 1168, a non-line non-grounded EMI filter 1170' and the driver circuit 1172. The converter circuit 1150' converts 3-phase AC input voltages (e.g., 480 V AC or 600V AC) to a DC voltage, which is provided on a DC bus (e.g., the DC bus shown in FIG. 2). The first line protection circuit 1152' provides line surge protection to limit current, including at startup, provided from AC inputs (may be referred to as "mains") of
10 the first line protection circuit 1152' to circuits (e.g., the common mode choke 1156', the charging circuit 1164, and the PFC circuit 1166') downstream from the first line protection circuit 1152'. The first line protection circuit 1152' may include fuses 1400 and MOVs 1402.

[0214] The first line EMI filter 1154' filters an output of the first line protection circuit 1152' and decouples circuits downstream from the first line EMI filter 1154' from the AC inputs of the
15 first line protection circuit 1152'. The first line EMI filter 1154' may include one or more across-the-line capacitors 1404 (e.g., X-rated capacitors) connected across the outputs of the first line protection circuit 1152'.

[0215] The common mode choke 1156' provides high impedance to a common mode signal to provide EMI filtering and filters an output of the first line EMI filter 1154'. The common mode
20 choke 1156' decouples circuits downstream from the common mode choke 1156' from circuits upstream from the common mode choke 1156'. The common mode choke includes inductors 1406 (one for each phase) and cores 1408.

[0216] The second protection circuit 1158' provides line to ground surge protection and may include MOVs 1410 (one for each phase) and a GDT 1412. The grounded EMI filter 1160'
25 provides EMI filtering and may include line-to-ground capacitors 1414, 1416, 1418 (e.g., Y-rated capacitors). The second protection circuit 1158' and the line-to-ground capacitors 1414, 1416, and 1418 may be connected to ground 1159 (e.g., earth ground). The line-to-ground capacitors 1414, 1416, and 1418 may include three pairs of capacitors (one pair for each phase) as shown or a different number of capacitors depending on the voltage and/or number of phases.

30 **[0217]** The second line EMI filter 1162' may include across-the-line capacitors 1420, which are connected across respective pairs of the AC lines 1422. The size and capacitance of the capacitors 1420 are small due to the inclusion of the non-line non-grounded EMI filter 1170'. In one embodiment, the second line EMI filter 1162' is not included.

[0218] The non-line non-grounded EMI filter 1170' filters an output of the rectification circuit 1168 and decouples a converter (e.g., buck converter 701 of FIG. 10) or the driver circuit 1172 from a bridge rectifier (e.g., the primary bridge rectifier 714 of FIG. 10) to minimize noise generated by the converter from being seen at the bridge rectifier. The non-line non-grounded EMI filter 1170' may include one or more DC bus rated capacitors (one capacitor 1430 is shown). In one embodiment, the non-line non-grounded EMI filter 1170' includes a single DC bus rated capacitor 1430 as shown and the second line EMI filter 1162' is not included. As a result, the number, size and cost of the capacitors are reduced. The single capacitor 1430 replaces the three capacitors 1420 and may be smaller in size and have a smaller capacitance than each capacitor of the second line EMI filter 1162'. For example, if the non-line non-grounded EMI filter 1170' is not included, then the capacitors 1420 may each be large (e.g., 0.47 μ F). If the non-line non-grounded EMI filter 1170' is included, capacitance of each of the capacitors 1420 may be substantially reduced (0.01-0.1 μ F) or the second line EMI filter 1162' may not be included. As an example, capacitance of each of the capacitors 1420 and 1430 may be 0.33 μ F. In one embodiment, each of the capacitors of the non-line non-grounded EMI filter 1170 is less than or equal to capacitance of each of the across-the-line capacitors upstream from the charging circuit 1164 and/or the rectification circuit 1168.

[0219] FIG. 22 shows an example of the converter circuit 1200 of FIG. 17. FIG. 22 shows a 3-phase converter circuit 1200' that includes the first line protection circuit 1152', the first line EMI filter 1154', the charging circuit 1164, and a PFC circuit 1450. The circuits 1152', 1154', 1164, 1450 may be mounted on a PCB 1451, which may include a heat sink 1453. The heat sink 1453 dissipates heat generated by circuit components mounted on the PCB 1451. The PFC circuit 1450 includes the rectification circuit 1168, a common mode choke 1203', a second protection circuit 1204', a grounded EMI filter 1206', one or more non-line non-grounded EMI filters 1208' and the driver circuit 1172. By including the a common mode choke 1203', the second protection circuit 1204', the grounded EMI filter 1206', and the one or more non-line non-grounded EMI filters 1208' downstream from the rectification circuit 1168, envelope of the convert circuit 1200' is minimized and may be smaller than the envelope of the converter circuit 1150' of FIG. 21.

[0220] Although the common mode choke 1203', second protection circuit 1204', and grounded EMI filter 1206' are shown downstream from the rectification circuit 1168, one or more of the common mode choke 1203', the second protection circuit 1204' and the grounded EMI filter 1206' may not be included. If the common mode choke 1203', the second protection circuit 1204' and/or the grounded EMI filter 1206' are not included, then the common mode

choke 1156', the second protection circuit 1158' and/or the grounded EMI filter 1160' may be included upstream from the rectification circuit 1168, as shown in FIG. 21. For example, if the common mode choke 1203' is not included, then the common mode choke 1156' is included.

[0221] By having the common mode choke 1203' downstream from the rectification circuit 1168 rather than the common mode choke 1156' upstream from the rectification circuit 1168, a smaller common mode choke is included. For example, the common mode choke 1156' may include three coils, whereas the common mode choke 1203' may have two coils 1452 and a single core 1454. This reduces the number of inductors (or windings), total number of turns, and the size of the common mode choke included. As an example, the common mode choke 1156' may have 3/2 as many windings and/or turns as the common mode choke 1203'. Since the inductance of a common mode choke is a function of the number of turns squared, the inductance of the common mode choke 1203' may be greater than the inductance of the common mode choke 1156'. In addition, by having the common mode choke 1203' downstream from (or on a right-hand side of) the rectification circuit 1168, a frequency cutoff of the EMI filter is lowered. Also, with a same number of turns per winding in each of the common mode chokes 1156', 1203' and since the common mode choke 1203' has one less winding than the common mode choke 1156', the common mode choke 1203' may have 50% more inductance than the common mode choke 1156' because there are two coils in parallel instead of three in the common mode for more effective inductance and high impedance.

[0222] By having the one or more non-line non-grounded EMI filters 1208' downstream from the rectification circuit 1168 rather than having corresponding EMI filters upstream from the rectification circuit 1168, overall capacitance of the EMI filters is reduced and as a result the corresponding cutoff frequency is reduced. This holds true if capacitors of the non-line non-grounded EMI filters 1208' have a same capacitance as the capacitors of the upstream EMI filters. The reduced cutoff frequency corresponds to increased filtering. Overall effective capacitance of the converter circuit 1200' due to the inclusion of the non-line non-grounded EMI filters 1208' and not the inclusion of X-capacitors, such as capacitor 1316 of FIG. 19, may be more effective capacitance than inclusion of the X-capacitors and not inclusion of the non-line non-grounded EMI filters 1208'. In 3-phase implementation of FIG. 21, more capacitance is provided than when X-capacitors 1420 are included.

[0223] The second protection circuit 1204' includes MOVs 1460 and a GDT 1462. First ends of the MOVs 1460 are connected to respect outputs of the common mode choke 1203'. Second ends of the MOVs 1460 are connected to a first end of the GDT 1462. A second end of the GDT 1462 is connected to the ground 1159.

[0224] The grounded EMI filter 1206' includes pairs of capacitors 1466, 1468. Capacitors in the first pair of capacitors 1466 are connected in series between a first output (or first line) of the second protection circuit 1204' and the ground 1159. Capacitors in the second pair of capacitors 1468 are connected in series between a second output (or second line) of the second protection circuit 1204' and the ground 1159. Although multiple capacitors are connected in series between the lines and the ground 1159, a single capacitor may be connected between each of the lines and the ground 1159. Multiple capacitors may be connected in series as shown for high voltage (e.g., 600V) applications.

[0225] The one or more non-line non-grounded EMI filters 1208' may include one or more capacitors connected in parallel between the DC line 1470 and a return (or low voltage) line 1472. The one or more capacitors are DC bus rated capacitors (e.g., capacitor 1430 and/or capacitor 1474). In one embodiment, a single capacitor is included.

[0226] The charging circuit 1164 may include one or more relays 1480, a relay drive circuit 1482, and current limiting elements (CLEs) 1484. The CLEs 1484 may include resistors, thermistors, or other current limiting elements. The relay drive circuit 1480 controls operation of the relays 1482. This control may be based on a control signal received from the control module 250 of FIG. 8. The CLEs 1484 are connected across one of the relays 1482. The CLEs 1484 are connected to a first line input and a first line output of the one of the relays. The one of the relays 1482 may be opened during an initial power-up period, effectively incorporating the CLEs 1484 in the path between the first line input and the first line output of the one of the relays. Only two phases of the three phase input are connected during power up, for example, with the CLE's in this current path. Two sets of CLE's may be used is all 3 phases are connected during power up. The one of the relays 1482 is closed after the initial power-up period.

[0227] FIG. 23 shows another example portion 1500 of the PFC circuit 212 of FIG. 4 including a common mode choke 1501, a protection (or second protection) circuit 1502, a grounded EMI filter 1504, a first EMI filter 1503, and/or a second EMI filter 1506. The second protection circuit 1502 and the grounded EMI filter 1504 are connected to ground 1508 (e.g., earth ground). The first EMI filter 1503 may be included as shown downstream of the rectification circuit 402 or may be upstream of the rectification circuit 402, as represented by capacitor 1590.

[0228] The portion 1500 includes the boost converter 401, and the rectification circuit 402 having the bridge rectifiers 414, 416 with the differential AC input 420. The boost converter 401 (or driver circuit) includes the inductor 404, the diode 406, the switch 408, and the capacitor 430. The portion 1500 has output terminal 422 and reference terminal 426. Control module 250

may receive PFC_{ACREP} , PFC_{DCREP} , PFC_{INC1} (shown in FIG. 4), and/or PFC_{INC2} (shown in FIG. 4) and generate PFC_{OUT} , as described above. Although sensors 412 of FIG. 4 are not shown in FIG. 23, the sensors 412 may be included.

[0229] The common mode choke 1501, if included, is connected across the primary bridge rectifier 414. The common mode choke 1501 may be configured as the common mode choke 1053 of FIG. 20. The second protection circuit 1502 may be configured as the second protection circuit 1054' of FIG. 20. The grounded EMI filter 1504 may be configured as the grounded EMI filter 1056' of FIG. 20. The EMI filter 1506 may be configured as the EMI filter 407 of FIG. 7 or as the one or more non-line non-grounded EMI filters 1058' of FIG. 20.

[0230] FIG. 24 shows another example portion 1550 of the PFC circuit 700 of FIG. 10 including a common mode choke 1551, a protection (or second protection) circuit 1552, a grounded EMI filter 1554, a first EMI filter 1555, and/or a second EMI filter 1556. The first EMI filter 1555 may be included as shown downstream of the rectification circuit 702 or may be upstream of the rectification circuit 702, as represented by capacitors 1592, 1594, 1596. The second protection circuit 1552 and the grounded EMI filter 1554 are connected to ground 1558 (e.g., earth ground). The portion 1550 includes the buck converter 701, and the rectification circuit 702 having the bridge rectifier 714 with the AC input 720. The buck converter 701 (or driver circuit) includes the inductor 704, the diode 706, the switch 708, and the capacitor 723. The portion 1550 has output terminal 722 and reference terminal 726. Control module 250 may receive PFC_{ACREP} , PFC_{DCREP} , PFC_{INC1} (shown in FIG. 10), and/or PFC_{INC2} (shown in FIG. 10) and generate PFC_{OUT} , as described above. Although sensors 712 of FIG. 10 are not shown in FIG. 23, the sensors 712 may be included. A first non-grounded EMI filter (e.g., the first non-grounded EMI filter 1154' of FIG. 21) may be included upstream or downstream of the rectification circuit 702.

[0231] The common mode choke 1551, if included, is connected across the primary bridge rectifier 714. The common mode choke 1551 may be configured as the common mode choke 1203' of FIG. 22. The second protection circuit 1552 may be configured as the second protection circuit 1204' of FIG. 22. The grounded EMI filter 1554 may be configured as the grounded EMI filter 1206' of FIG. 22. The EMI filter 1556 may be configured as the EMI filter 407 of FIG. 7 or as the one or more non-line non-grounded EMI filters 1208' of FIG. 22.

[0232] The circuits 1500, 1550 may include another EMI filter with one or more across-the-line (or X-rated) capacitors located upstream of the rectification circuits 402, 702. Across-the-line capacitors 1590, 1592, 1594, 1596 are shown. In one embodiment, the across-the-line capacitors 1590, 1592, 1594, 1596 are not included. In one embodiment, the across-the-line

capacitors 1590, 1592, 1594, 1596 are included instead of including (i) across-the-line capacitors upstream of the AC input and/or (ii) across-the-line capacitors between (a) the rectification circuit and (b) the common mode choke 1501 and/or one of the inductors 404, 704.

[0233] FIG. 25 shows another 3-phase converter circuit 1600 that includes the first line protection circuit 1152 and a PFC circuit 1252'. The PFC circuit 1252' includes the rectification circuit 1018, a charging circuit 1164', a first line EMI filter 1254, 1254', or 1254'', the common mode choke 1203, the second protection circuit 1204, the grounded EMI filter 1206, the one or more non-line non-grounded EMI filters 1208 and the driver circuit 1172. The first line EMI filter 1254 may include one or more across-the-line capacitors; one or more X-rated capacitors if located upstream of the rectification circuit 1018 or one or more DC bus rated capacitors if located downstream of the rectification circuit 1018. Examples of the first line EMI filters 1254, 1254', 1254'' are the first line EMI filters 1304, 1404 of FIGs. 19-22. The across-the-line capacitors are connected in parallel across outputs of the first line EMI filter 1254, the charging circuit 1164', or the rectification circuit 1168. A 3-phase converter circuit 1600 is shown in FIG. 25, a 2-phase converter circuit may include a PFC circuit having a charging circuit downstream of a rectification circuit and a first line EMI filter located upstream or downstream of the rectification circuit as shown in FIG. 25.

[0234] FIG. 26 shows an example of a portion 1750 of a PFC circuit of the drive of FIG. 2 including a boost converter 1751 for a 3-phase implementation. The portion 1750 includes a rectification circuit 1752, an inductor 1754, a diode 406, the EMI filter 407, the switch 408, the driver 410 and one or more current sensors 1762a, 1762b, 1762c, 1762d (collectively current sensors 1762). Although not shown in FIG. 26, the portion 1750 may include the second protection circuit 1502, the grounded EMI filter 1504, and/or other protection circuits and/or EMI filters disclosed herein. The rectification circuit 1752 includes a primary (or first) bridge rectifier 1764 and a secondary (or second) bridge rectifier 1766. The secondary bridge rectifier 1766 may be referred to as a bypass rectifier and allows for current to bypass the primary bridge rectifier 1764 and the boost converter 1751. The primary bridge rectifier 1764 includes six diodes 1767 (or a diode pair for each input phase of V_{AC}). In one embodiment, the secondary bridge rectifier 1766 includes six diodes; three bypass 1768 and three optional diodes 1769. In another embodiment, the bypass diodes 1768 are included and the optional diodes 1769 are not included.

[0235] Each of the bridge rectifiers 1764, 1766 includes 3-phase AC inputs, a return input and an output. The 3-phase AC inputs of each of the bridge rectifiers 1764, 1766 are connected respectively to outputs of the current sensors 1762a, 1762b, 1762c. Inputs of the current sensors

1762a, 1762b, 1762c are connected to AC input terminals 1770, which receive phases of the 3-phase AC voltage V_{AC} from the EMI filter 407. The return inputs of the bridge rectifiers 1764, 1766 are connected to a same output 1772 of the fourth current sensor 1762d. The output of the bridge rectifier 1764 is connected to the inductor 1754. The output of the bridge rectifier 1766 is connected to an output terminal 1774, which is connected to the DC bus. In one embodiment, a current sensor is located in series with the inductor 1754 and upstream or downstream from the inductor. In another embodiment, a current sensor is located in series with and on either side of the switch 408 or the capacitor 1780. In another embodiment, a current sensor is located on the DC bus. Current sensors may be located anywhere in the portion 1750 and the corresponding sensor signals may be provided to the control module 250 and used to control a state of the switch 408.

[0236] The output voltages of the bridge rectifiers 1764, 1766 may be referred to as main voltages. Although current sensors 1762a, 1762b, 1762c, 1762d are shown, other current sensors may be alternatively or additionally incorporated into the portion 1750. For example, one or more current sensors may be connected in series with one or more of the diode 1756, the switch 408, and a capacitor 1780. The capacitor 1780 is connected between the output terminal 1774 and ground (or reference) terminal 1782. The capacitor 1780 may be connected (i) at a first end, to a cathode of the diode 1756 and to the output terminal 1774, and (ii) at a second end, to the reference terminal 1782 and the input 1784 of the fourth current sensor 412d. The other current sensors, connected in series with one or more of the diode 1756, the switch 408, and a capacitor 1780, may detect current passing through the diode 1756, the switch 408 and/or the capacitor 1780. A diode 1783 may be connected across the switch 408. In one embodiment, a current sensor is connected between the inductor 1754 and the switch 408. In another embodiment, the current sensor is connected between the switch 408 and the reference terminal 1782. Also, any or all of the disclosed current sensors may be utilized. Any of the signals and/or parameters derived from the signals of the disclosed current sensors may be utilized in the circuits and methods disclosed herein.

[0237] The EMI filter 407 may be connected to the output of the primary bridge rectifier 1764. The EMI filter 407 filters an output of the primary bridge rectifier 1764. The EMI filter 407 decouples the boost converter 1751 from the primary bridge rectifier 1754 to minimize noise generated by the boost converter 1751 from being seen at the primary bridge rectifier 1754. The output terminal 1774 may be connected to the DC bus, which is connected between the PFC circuit 212 and the inverter power circuit 208 of FIG. 2.

[0238] The inductor 1754, diode 1756, switch 408 and driver 410 provide the boost converter 1751, which increases a DC output voltage V_{DCOUT} and/or a DC bus voltage of the DC bus to a commanded (or predetermined) DC voltage V_{DCCOM} . The boost converter 1751 is a power converter. The commanded DC voltage V_{DCCOM} may be determined by the control module 250 and may be set to be less than a peak (or maximum) output voltage of the bridge rectifiers 1764, 1766. The inductor 1754 is connected in series with the diode 1756 between the output of the primary bridge rectifier 1764 and the output terminal 1774. The inductor 1754 is connected (i) at a first end, to the output of the primary bridge rectifier 1764, and (ii) at a second end, to an anode of the diode 1756 and a first terminal of the switch 408. The inductor 1754 may be small (e.g., 80 micro-Henry (μH)) and operates as a choke. The diode 1756 may be formed of, for example, silicon carbide SiC for quick switching frequencies and no reverse recovery time. The diode 1756 may include multiple diodes connected in parallel. The switch 408 may be replaced with multiple switches connected in parallel.

[0239] The switch 408 may be a transistor, such as a super-junction field effect transistor (FET), a power metal oxide semiconductor field-effect transistor (MOSFET), and/or a super-junction MOSFET. The switch 408 may be configured to be oscillated between ON (e.g., closed) and OFF (e.g., open) states at a high frequency (e.g., greater than or equal to 200 kilohertz (kHz)). The first terminal of the switch 408 is connected to the inductor 1754 and the anode of the diode 1756. A second terminal of the switch 408 is connected to an input 1784 of the fourth current sensor 412d and the reference terminal 1782. The switch may be a IGBT for lower switching frequencies.

[0240] A control terminal of the switch 408 receives a control signal SW_{CTRL} from the driver 410. The driver 410 generates the control signal SW_{CTRL} based on an output signal PFC_{OUT} of the control module 250. The control module 250 generates the output signal PFC_{OUT} based on: one or more current sense signals PFC_{INC1} , PFC_{INC2} , PFC_{INC3} , PFC_{INC4} from the current sensors 1762a, 1762b, 1762c, 1762d and/or other current sensors disclosed herein; an AC signal PFC_{ACREP} representative of the AC voltage V_{AC} ; and a DC signal PFC_{DCREP} that is representative of the DC output voltage V_{DCOUT} of the PFC circuit 212. The AC voltage V_{AC} may not be monitored if partial PFC operation is not being performed. The current sense signals PFC_{INC1} , PFC_{INC2} , PFC_{INC3} may be equal to and/or indicative of the amounts of current (i) provided from each phase of the input voltage V_{AC} , (ii) collectively equal to an amount of current passing through the inductor 1754, and/or passing through the PFC circuit 212. The current sense signal PFC_{INC4} may be equal to and/or indicative of an amount of current (i) returning from the output terminal 1774 to the fourth current sensor 412d, and/or (ii) passing through the PFC circuit 212.

The AC signal PFC_{ACREP} may be equal to and/or indicative of the AC voltage V_{AC} . The DC signal PFC_{DCREP} may be equal to and/or indicative of the DC output voltage V_{DCOUT} .

[0241] During operation, the boost converter 1751 may be ON when the DC bus voltage is greater than the AC voltage V_{AC} . Current does not pass from the secondary rectifier 1766 to the DC bus when the DC bus voltage is greater than the AC voltage V_{AC} . When the DC bus voltage is less than the AC voltage V_{AC} , then the boost circuit 1751 may be active and storing energy in the inductor 1754 and releasing energy from the inductor 1754 onto the DC bus to boost voltage of the DC bus. The energy may be stored when the switch 408 is closed and released when the switch 1758 is opened.

[0242] The control module 250 may control operation of the driver 410 to control a state of the switch 408, such that the DC output voltage V_{DCOUT} is equal to or within a predetermined range of the commanded DC voltage V_{DCCOM} . The control module 250 may control operation of the driver 410, such that the switch 408 is oscillated between open and closed states at a predetermined frequency during, for example, active periods 452 and is maintained in an OFF (or open) state during inactive periods 454 of FIG. 5.

[0243] The 3-phases are rectified by the primary bridge rectifier 1764 to provide 3-phase rectified output voltages. Partial PFC operation for the boost converter 1751 may be the same or similarly to partial PFC operation of the boost converter 401 of FIG. 4. The additional bridge connections provided by diodes 1768 for the 3-phases conduct when V_{AC} is greater than the bus voltage of the DC bus and/or V_{DCOUT} . This provides improved efficiency by reducing switching losses and reduced EMI. The 3-phase operation is similar to the single phase operation except the 3-phases are essentially 'ORed' together. If the bus voltage is controlled to be less than a peak voltage of V_{AC} , then the rectification circuit 1752 conducts current and the switch is OFF (i.e. no switching) when the bus voltage is less than the peak voltage of V_{AC} . Current shaping may be performed by the control module 250 and the driver 410 when V_{AC} is less than a peak of the bus voltage.

[0244] When the switch 408 is ON, the bus voltage is equal to the voltage received by the inductor (or choke) 1754. The switch 408 may be turned OFF during small adjustment windows for 3-phase operation similar as for single phase operation.

[0245] FIG. 27 shows another example of a portion 2000 of a PFC circuit of the drive of FIG. 2 for a 3-phase implementation. The portion 2000 includes a rectification circuit 2002 and a boost converter 2004 with a switched bridge circuit 2006 and a driver 2008. The rectification circuit 2002 includes a bridge 2010 rectifier with six diodes (a diode pair for each phase of V_{AC} .

The inputs of the bridge rectifier 2010 receive respective phases of V_{AC} and are respectively connected to (i) the current sensors 1762a, 1762b, 1762c, and (ii) inputs of inductors 2011, 2012, 2014. The output of the bridge rectifier 2010 is connected to the output terminal 1774 and/or the DC bus. The return input of the bridge rectifier 2010 is connected to the output 1772 of the fourth current sensor 1762d.

[0246] The switched bridge circuit 2006 includes three sets of diode pairs and switch pairs. Each set includes a diode pair (identified as diodes 2020, 2022, 2024) and a switch pair (identified as switches 2026, 2028, 2030). The diodes in each of the diode pairs are connected in series between (i) the output terminal 1774 and (ii) the reference terminal 1782. The switches in each of the switch pairs are connected in series between (i) the output terminal 1774 and (ii) the reference terminal 1782. Each of the diodes is connected across a respective one of the switches. In one embodiment, the switches 2026, 2028, 2030 of FIGs. 13-14 may be IGBTs or SiC FETs.

[0247] The portion 2000 may further include the EMI filter 407 and includes a control module 2032, which may be used instead of and operate similarly to the control module 250 of FIG. 4.

Although not shown in FIG. 27, the portion 2000 may include the second protection circuit 1502, the grounded EMI filter 1504, and/or other protection circuits and/or EMI filters disclosed herein. As an example, the second protection circuit 1502 and the grounded EMI filter 1504 may be located downstream of the fourth current sensor 1784 and upstream of the EM filter 407. The control module 2032 receives signals from the sensors 1762 and controls the driver 2008 based on the signals. The driver 2008 generates control signals (identified as $SW_{CTRL1-6}$) to control states of the switches 2026, 2028, 2030. Although current sensors 1762a, 1762b, 1762c, 1762d are shown, other current sensors may be alternatively or additionally incorporated into the portion 2000. For example, current sensors may be connected in series with one or more of the diodes 2020, 2022, 2024, the switches 2026, 2028, 2030, and a capacitor 2034. The capacitor 2034 is connected between the output terminal 1774 and the reference terminal 1782. The control module 2032 may control the driver 2008 based on signals from any of the current sensors. EMI filter components (e.g., X caps, Y caps, and/or a common mode choke) can all be connected upstream in the AC portion of the circuit (or portion 2000), such as upstream of the rectification circuit, or downstream in the DC portion of the circuit (or portion 2000) or any combination thereof.

[0248] The control module 2032 may control operation of the driver 2008 to control a state of the switches 2026, 2028, 2030, such that the DC output voltage V_{DCOUT} is equal to or within a predetermined range of the commanded DC voltage V_{DCCOM} . The control module 2032 may control operation of the driver 2008, such that the switch 408 is oscillated between open and

closed states at a predetermined frequency during, for example, active periods 452 and is maintained in an OFF (or open) state during inactive periods 454 of FIG. 5.

[0249] When V_{AC} is greater than the bus voltage, the diodes of the rectification circuit 2002 conducts and the switches 2026, 2028, 2030 are OFF (or OPEN), which provides different

5 voltages at inputs of inductors 2011, 2012 and 2014 than at the DC bus. This provides improved efficiency by reducing switching losses and reduced EMI. The bus voltage may be commanded to be slightly less (within a predetermined range of) a peak voltage of V_{AC} . If the bus voltage is controlled to be less than the peak voltage of V_{AC} and V_{AC} is greater than the bus voltage, then the rectification circuit 2002 conducts and the switches 2026, 2028, 2030 are OFF (or OPEN).

10 This occurs near the peak voltage of V_{AC} . Current shaping may be performed including pulse width modulating $SW_{CTRL1-6}$ and/or adjusting duty cycles of $SW_{CTRL1-6}$ when V_{AC} is less than the bus voltage. The portion 2000 of FIG. 14 provides more control than the portion 1750 of FIG.

13 due to the inclusion of the inductors 2011, 2012, 2014, the diodes 2020, 2022, 2024, and the switches 2026, 2028, 2030. In one embodiment, the control module 2032 independently controls

15 current through each of the inductors 2011, 2012, 2014 for each of the phases to shape current through the inductors 2011, 2012, 2014. The control module 2032 and the driver 2008 actuate the switches 2026, 2028, 2030 based on one or more of PFC_{INC1} , PFC_{INC2} , PFC_{INC3} , PFC_{INC4} , PFC_{ACREP} , PFC_{DCPREP} .

[0250] The foregoing description is merely illustrative in nature and is in no way intended to

20 limit the disclosure, its application, or uses. The broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification, and the following claims. It should be understood that one or more steps within a method may be executed in different order (or

25 concurrently) without altering the principles of the present disclosure. Further, although each of the embodiments is described above as having certain features, any one or more of those features described with respect to any embodiment of the disclosure can be implemented in and/or

combined with features of any of the other embodiments, even if that combination is not explicitly described. In other words, the described embodiments are not mutually exclusive, and

30 permutations of one or more embodiments with one another remain within the scope of this disclosure.

[0251] Spatial and functional relationships between elements (for example, between modules, circuit elements, semiconductor layers, etc.) are described using various terms, including

“connected,” “engaged,” “coupled,” “adjacent,” “next to,” “on top of,” “above,” “below,” and

“disposed.” Unless explicitly described as being “direct,” when a relationship between first and second elements is described in the above disclosure, that relationship can be a direct relationship where no other intervening elements are present between the first and second elements, but can also be an indirect relationship where one or more intervening elements are present (either spatially or functionally) between the first and second elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A OR B OR C), using a non-exclusive logical OR, and should not be construed to mean “at least one of A, at least one of B, and at least one of C.”

[0252] In the figures, the direction of an arrow, as indicated by the arrowhead, generally demonstrates the flow of information (such as data or instructions) that is of interest to the illustration. For example, when element A and element B exchange a variety of information but information transmitted from element A to element B is relevant to the illustration, the arrow may point from element A to element B. This unidirectional arrow does not imply that no other information is transmitted from element B to element A. Further, for information sent from element A to element B, element B may send requests for, or receipt acknowledgements of, the information to element A.

[0253] In this application, including the definitions below, the term “module” or the term “controller” may be replaced with the term “circuit.” The term “module” may refer to, be part of, or include: an Application Specific Integrated Circuit (ASIC); a digital, analog, or mixed analog/digital discrete circuit; a digital, analog, or mixed analog/digital integrated circuit; a combinational logic circuit; a field programmable gate array (FPGA); a processor circuit (shared, dedicated, or group) that executes code; a memory circuit (shared, dedicated, or group) that stores code executed by the processor circuit; other suitable hardware components that provide the described functionality; or a combination of some or all of the above, such as in a system-on-chip.

[0254] The module may include one or more interface circuits. In some examples, the interface circuits may include wired or wireless interfaces that are connected to a local area network (LAN), the Internet, a wide area network (WAN), or combinations thereof. The functionality of any given module of the present disclosure may be distributed among multiple modules that are connected via interface circuits. For example, multiple modules may allow load balancing. In a further example, a server (also known as remote, or cloud) module may accomplish some functionality on behalf of a client module.

[0255] Some or all hardware features of a module may be defined using a language for hardware description, such as IEEE Standard 1364-2005 (commonly called “Verilog”) and IEEE

Standard 1076-2008 (commonly called “VHDL”). The hardware description language may be used to manufacture and/or program a hardware circuit. In some implementations, some or all features of a module may be defined by a language, such as IEEE 1666-2005 (commonly called “SystemC”), that encompasses both code, as described below, and hardware description.

5 **[0256]** The term code, as used above, may include software, firmware, and/or microcode, and may refer to programs, routines, functions, classes, data structures, and/or objects. The term shared processor circuit encompasses a single processor circuit that executes some or all code from multiple modules. The term group processor circuit encompasses a processor circuit that, in combination with additional processor circuits, executes some or all code from one or more
10 modules. References to multiple processor circuits encompass multiple processor circuits on discrete dies, multiple processor circuits on a single die, multiple cores of a single processor circuit, multiple threads of a single processor circuit, or a combination of the above. The term shared memory circuit encompasses a single memory circuit that stores some or all code from multiple modules. The term group memory circuit encompasses a memory circuit that, in
15 combination with additional memories, stores some or all code from one or more modules.

[0257] The term memory circuit is a subset of the term computer-readable medium. The term computer-readable medium, as used herein, does not encompass transitory electrical or electromagnetic signals propagating through a medium (such as on a carrier wave); the term computer-readable medium may therefore be considered tangible and non-transitory. Non-
20 limiting examples of a non-transitory computer-readable medium are nonvolatile memory circuits (such as a flash memory circuit, an erasable programmable read-only memory circuit, or a mask read-only memory circuit), volatile memory circuits (such as a static random access memory circuit or a dynamic random access memory circuit), magnetic storage media (such as an analog or digital magnetic tape or a hard disk drive), and optical storage media (such as a CD,
25 a DVD, or a Blu-ray Disc).

[0258] The apparatuses and methods described in this application may be partially or fully implemented by a special purpose computer created by configuring a general purpose computer to execute one or more particular functions embodied in computer programs. The functional blocks and flowchart elements described above serve as software specifications, which can be
30 translated into the computer programs by the routine work of a skilled technician or programmer.

[0259] The computer programs include processor-executable instructions that are stored on at least one non-transitory computer-readable medium. The computer programs may also include or rely on stored data. The computer programs may encompass a basic input/output system

(BIOS) that interacts with hardware of the special purpose computer, device drivers that interact with particular devices of the special purpose computer, one or more operating systems, user applications, background services, background applications, etc.

[0260] The computer programs may include: (i) descriptive text to be parsed, such as HTML (hypertext markup language), XML (extensible markup language), or JSON (JavaScript Object Notation) (ii) assembly code, (iii) object code generated from source code by a compiler, (iv) source code for execution by an interpreter, (v) source code for compilation and execution by a just-in-time compiler, etc. As examples only, source code may be written using syntax from languages including C, C++, C#, Objective-C, Swift, Haskell, Go, SQL, R, Lisp, Java®, Fortran, Perl, Pascal, Curl, OCaml, Javascript®, HTML5 (Hypertext Markup Language 5th revision), Ada, ASP (Active Server Pages), PHP (PHP: Hypertext Preprocessor), Scala, Eiffel, Smalltalk, Erlang, Ruby, Flash®, Visual Basic®, Lua, MATLAB, SIMULINK, and Python®.

[0261] None of the elements recited in the claims are intended to be a means-plus-function element within the meaning of 35 U.S.C. §112(f) unless an element is expressly recited using the phrase “means for,” or in the case of a method claim using the phrases “operation for” or “step for.”

CLAIMS

What is claimed is:

1. A converter circuit comprising:
 - a first electromagnetic interference filter connected to alternating current (AC) lines and
 - 5 comprising one or more across-the-line capacitors;
 - a charging circuit configured to (i) receive power from the first electromagnetic interference filter, and (ii) limit an amount of current passing from the first electromagnetic interference filter to a direct current (DC) bus; and
 - a power factor correction circuit of a compressor drive, wherein the power factor
 - 10 correction circuit is configured to provide power factor correction between an output of the charging circuit and a generated first DC voltage, wherein the power factor correction circuit comprises
 - a rectification circuit configured to rectify the power from the AC lines or an
 - output of the charging circuit depending on whether the rectification circuit is upstream or
 - 15 downstream from the charging circuit, and
 - a second electromagnetic interference filter connected downstream from the rectification circuit and comprising one or more DC bus rated capacitors, wherein the second electromagnetic interference filter is configured to output a filtered DC signal based on an output
 - of the rectification circuit, and
 - 20 wherein the power factor correction circuit is configured to, based on the output of the second electromagnetic interference filter, output the first DC voltage to the DC bus to power the compressor drive.
2. The converter circuit of claim 1, wherein:
 - the first electromagnetic interference filter comprises an across-the-line capacitor for
 - 25 each phase of an AC input signal;
 - the second electromagnetic interference filter comprises only a single DC bus rated capacitor; and
 - a capacitance of each of the one or more across-the-line capacitors of the first electromagnetic interference filter is related to a capacitance of the single DC bus rated capacitor
 - 30 of the first electromagnetic interference filter, such that inclusion of the DC bus rated capacitor reduces capacitances of each of the one or more across-the-line capacitors.

3. The converter circuit of claim 1, wherein the second electromagnetic interference filter comprises a plurality of DC bus rated capacitors connected in parallel.
4. The converter circuit of claim 1, further comprising a third electromagnetic interference filter connected downstream from the first electromagnetic interference filter and comprising
5 one or more across-the-line capacitors, wherein a capacitance of each of the one or more DC bus rated capacitors is greater than a capacitance of each of the one or more across-the-line capacitors of the third electromagnetic interference filter.
5. The converter circuit of claim 4, wherein a capacitance of each of the one or more DC bus rated capacitors is an order of magnitude greater than a capacitance of each of the one or
10 more across-the-line capacitors of the third electromagnetic interference filter.
6. The converter circuit of claim 1, wherein the converter circuit is void of an across-the-line capacitor upstream from the rectification circuit.
7. The converter circuit of claim 1, further comprising a grounded electromagnetic interference filter comprising line-to-ground capacitors, wherein the grounded electromagnetic
15 interference filter is connected upstream or downstream from the rectification circuit.
8. The converter circuit of claim 7, wherein the power factor correction circuit comprises the grounded electromagnetic interference filter.
9. The converter circuit of claim 1, further comprising a first protection circuit configured to provide surge protection, wherein the protection circuit is connected upstream or downstream
20 from the rectification circuit and comprises at least one of a varistor or a gas discharge tube.
10. The converter circuit of claim 9, wherein the protection circuit is upstream from the rectification circuit to protect the rectification circuit from peak inverse voltage (PIV).
11. The converter circuit of claim 9, wherein:
the power factor correction circuit comprises the first protection circuit; and
25 the first protection circuit provides surge protection.

12. The converter circuit of claim 11, further comprising a second protection circuit connected upstream from the charging circuit, wherein the second protection circuit comprises surge protection.
13. The converter circuit of claim 1, further comprising a common mode choke, wherein the common mode choke is connected upstream or downstream from the rectification circuit.
14. The converter circuit of claim 13, wherein the power factor correction circuit comprises the common mode choke.
15. The converter circuit of claim 1, wherein the converter circuit is void of an across-the-line capacitor upstream from the rectification circuit.
16. The converter circuit of claim 1, wherein the converter circuit is void of a line-to-ground capacitor upstream from the rectification circuit.
17. The converter circuit of claim 1, wherein the rectification circuit comprises:
a first bridge rectifier configured to receive an AC voltage; and
a second bridge rectifier (i) receives the AC voltage, and (ii) bypasses at least one of the first bridge rectifier, a choke, and a diode of the power factor correction circuit to provide a rectified AC voltage out of the second bridge rectifier to the DC bus.
18. The converter circuit of claim 17, wherein the first bridge rectifier and the second bridge rectifier are each 3-phase bridge rectifiers.
19. The converter circuit of claim 17, wherein the power factor correction circuit comprises:
a power converter comprising a switch and configured to (i) receive an output of the first bridge rectifier, (ii) convert the output of the first bridge rectifier to a second DC voltage, and (iii) supply the second DC voltage to the DC bus; and
a control module configured to control operation of a driver to transition the switch between an open state and a closed state to adjust the first DC voltage on the DC bus, wherein the first DC voltage, depending on the AC voltage and the first DC voltage, is based on at least one of (i) the rectified AC voltage, and (ii) the second DC voltage.
20. The converter circuit of claim 1, further comprising a switched bridge circuit, wherein: the rectification circuit comprises a bridge rectifier configured to receive an AC voltage;

a switched bridge circuit comprising a plurality of switches;
a driver generating control signals to control states of the plurality of switches; and
a control module configured to control operation of the driver.

21. A converter circuit comprising:

5 a charging circuit configured to (i) receive power based on power from alternating current (AC) lines, and (ii) limit an amount of current passing to a direct current (DC) bus; and
a power factor correction circuit of a compressor drive, wherein the power factor correction circuit is configured to provide power factor correction between an output of the charging circuit and a generated first DC voltage, wherein the power factor correction circuit
10 comprises

a rectification circuit configured to rectify the power from the AC lines or an output of the charging circuit depending on whether the rectification circuit is upstream or downstream from the charging circuit, and

a first electromagnetic interference filter comprising one or more DC bus rated
15 capacitors, wherein the first electromagnetic interference filter is configured to output a filtered DC signal based on an output of the rectification circuit,

wherein at least one of

the converter circuit is void of an across-the-line capacitor upstream from the power factor correction circuit,

20 capacitance of each of the one or more DC bus rated capacitances is less than or equal to a capacitance of each across-the-line capacitor connected upstream from the charging circuit or the rectification circuit, or

the converter circuit is void of across-the-line capacitors, and

wherein the power factor correction circuit is configured to, based on an output of the
25 first electromagnetic interference filter, output the first DC voltage to the DC bus to power the compressor drive.

22. The converter circuit of claim 21, further comprising a first protection circuit configured to provide surge protection, wherein:

the charging circuit is configured to (i) receive the AC power based on an output of the
30 first protection circuit; and

the first protection circuit comprises at least one of a varistor and a gas discharge tube.

23. The converter circuit of claim 21, further comprising a first protection circuit configured to provide surge protection, wherein:

the charging circuit is configured to receive DC power from the rectification circuit;

the first protection circuit is upstream from the rectification circuit, connected between

5 the rectification circuit and the charging circuit, or downstream from the charging circuit; and

the first protection circuit comprises at least one of a varistor and a gas discharge tube.

24. The converter circuit of claim 21, further comprising a second protection circuit, (i) upstream from the rectification circuit, or (ii) included in the power factor correction circuit and downstream from the rectification circuit.

10 25. The converter circuit of claim 21, wherein the converter circuit is void of an across-the-line capacitor upstream from the power factor correction circuit.

26. The converter circuit of claim 21, wherein the capacitance of each of the one or more DC bus rated capacitances is less than or equal to the capacitance of each across-the-line capacitors connected upstream from the charging circuit or the rectification circuit.

15 27. The converter circuit of claim 21, wherein the converter circuit is void of a line-to-ground capacitor upstream from the power factor correction circuit.

28. The converter circuit of claim 21, further comprising a second electromagnetic interference filter connected upstream from the charging circuit, wherein the second electromagnetic interference filter comprises at least one of an across-the-line capacitor or a
20 line-to-ground capacitor.

29. The converter circuit if claim 28, wherein:

the second electromagnetic interference filter is upstream from the charging circuit and comprises an across-the-line capacitor; and

25 the converter circuit is void of an across-the-line capacitor downstream from the second electromagnetic interference filter and upstream from the rectification circuit.

30. The converter circuit of claim 21, wherein the rectification circuit comprises:
a first bridge rectifier configured to receive an AC voltage; and

a second bridge rectifier (i) receives the AC voltage, and (ii) bypasses at least one of the first bridge rectifier, a choke, and a diode of the power factor correction circuit to provide a rectified AC voltage out of the second bridge rectifier to the DC bus.

31. The converter circuit of claim 30, wherein the power factor correction circuit comprises:

5 a power converter comprising a switch and configured to (i) receive an output of the first bridge rectifier, (ii) convert the output of the first bridge rectifier to a second DC voltage, and (iii) supply the second DC voltage to the DC bus; and

a control module configured to control operation of a driver to transition the switch between an open state and a closed state to adjust the first DC voltage on the DC bus, wherein
10 the first DC voltage, depending on the AC voltage and the first DC voltage, is based on at least one of (i) the rectified AC voltage, and (ii) the second DC voltage.

32. The converter circuit of claim 21, further comprising a common mode choke, wherein the common mode choke is connected upstream or downstream from the rectification circuit.

33. A converter circuit comprising:

15 a charging circuit configured to (i) receive power based on power from alternating current (AC) lines, and (ii) limit an amount of current passing to a direct current (DC) bus; and

a power factor correction circuit of a compressor drive, wherein the power factor correction circuit is configured to provide power factor correction between an output of the charging circuit and a generated DC voltage, wherein the power factor correction circuit
20 comprises

a rectification circuit configured to rectify the power from the AC lines or an output of the charging circuit depending on whether the rectification circuit is upstream or downstream from the charging circuit, and

at least one of

25 a common mode choke, or

a grounded electromagnetic interference filter,

wherein the common mode choke or the grounded electromagnetic interference filter is configured to, based on an output of the rectification circuit, output the DC voltage for the DC bus to power the compressor drive.

34. The converter circuit of claim 33, further comprising a first electromagnetic interference filter comprising one or more DC bus rated capacitors, wherein:

the first electromagnetic interference filter is configured to output a filtered DC signal based on an output of the rectification circuit; and

5 the power factor correction circuit is configured to, based on the output of the first electromagnetic interference filter, output the DC voltage to the DC bus to power the compressor drive.

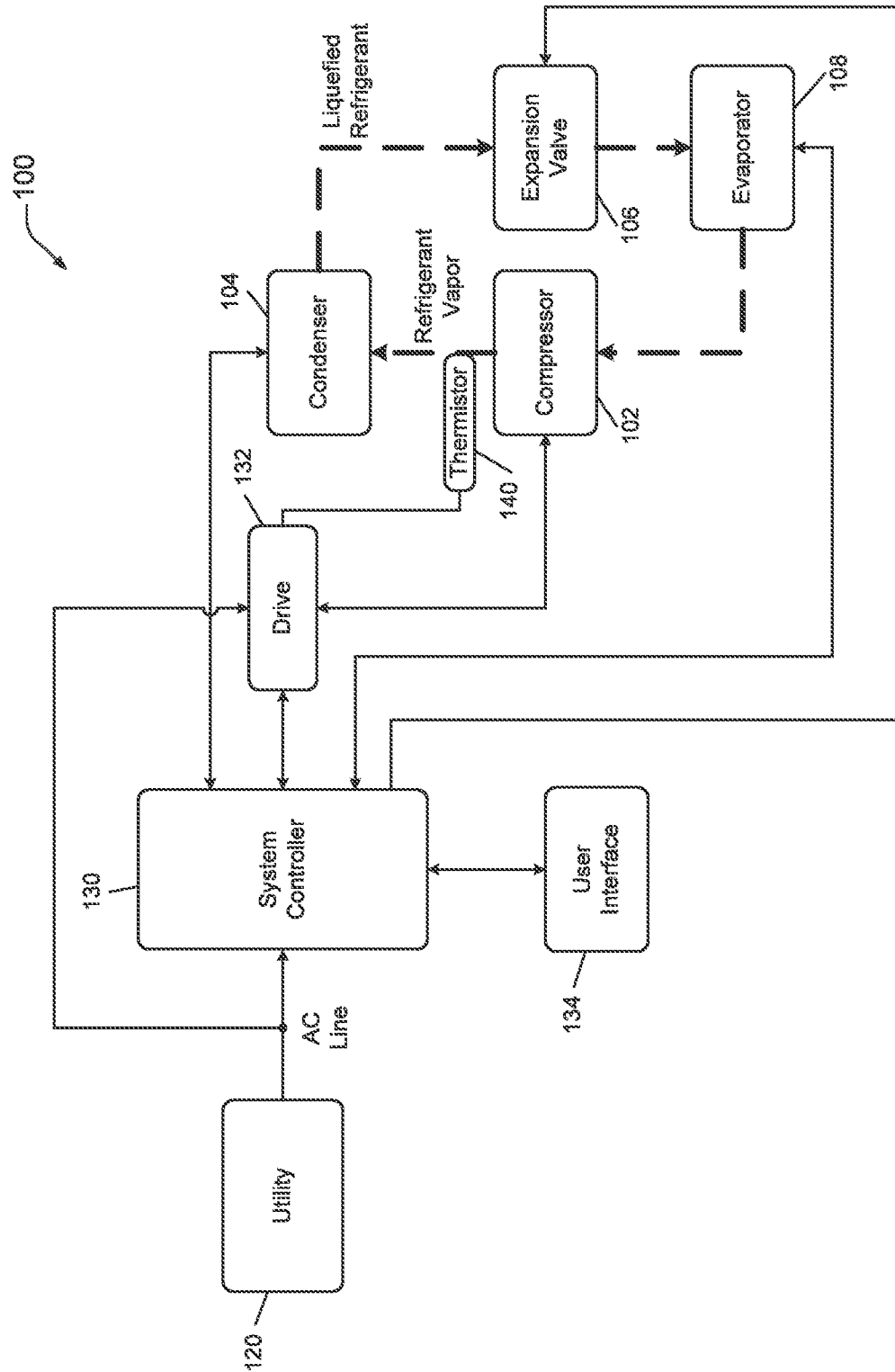
35. The converter circuit of claim 34, wherein the converter circuit is void of an across-the-line capacitor upstream from the power factor correction circuit.

10 36. The converter circuit of claim 34, wherein capacitance of each of the one or more DC bus rated capacitances is less than or equal to a capacitance of each across-the-line capacitor connected upstream from the charging circuit or the rectification circuit.

37. The converter circuit of claim 34, wherein the converter circuit is void of across-the-line capacitors.

15 38. The converter circuit of claim 33, further comprising a first protection circuit connected upstream from the charging circuit and configured to receive the AC power and provide surge protection.

39. The converter circuit of claim 38, wherein the first protection circuit comprises a metal oxide varistor.



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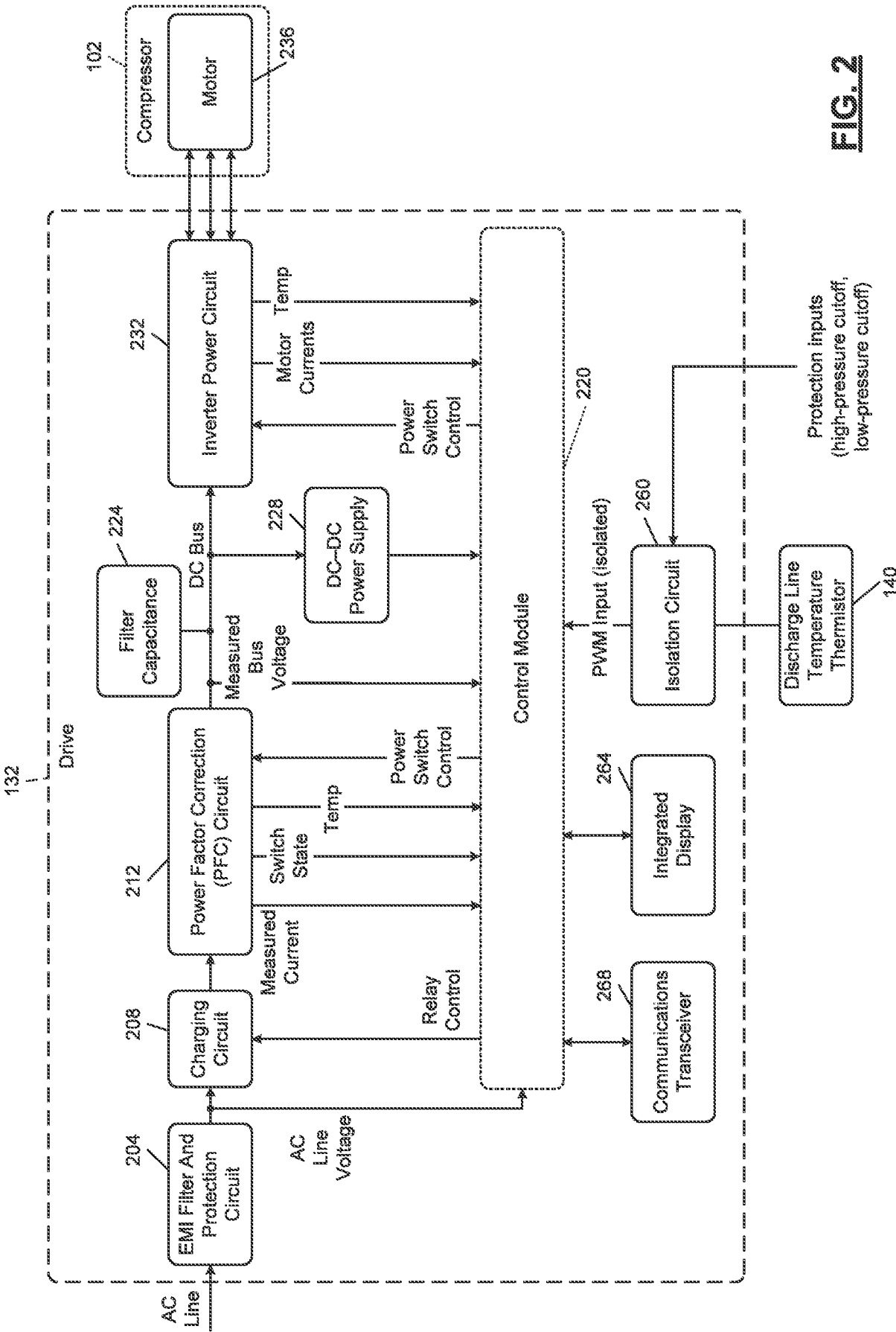


FIG. 2

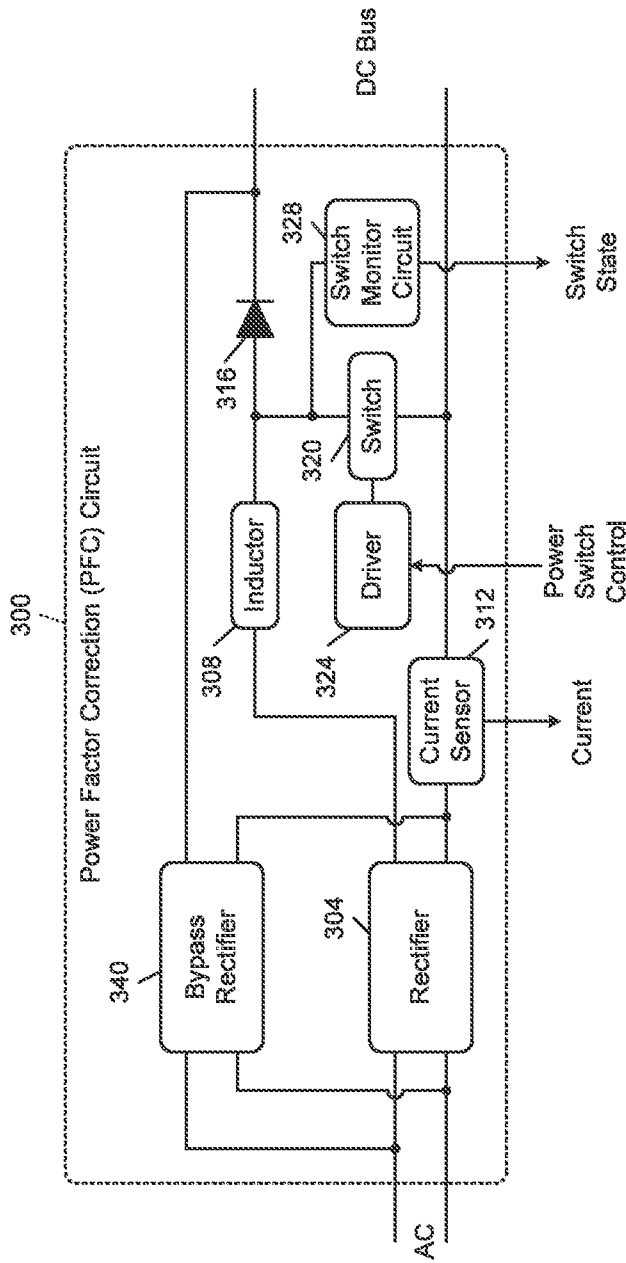


FIG. 3A

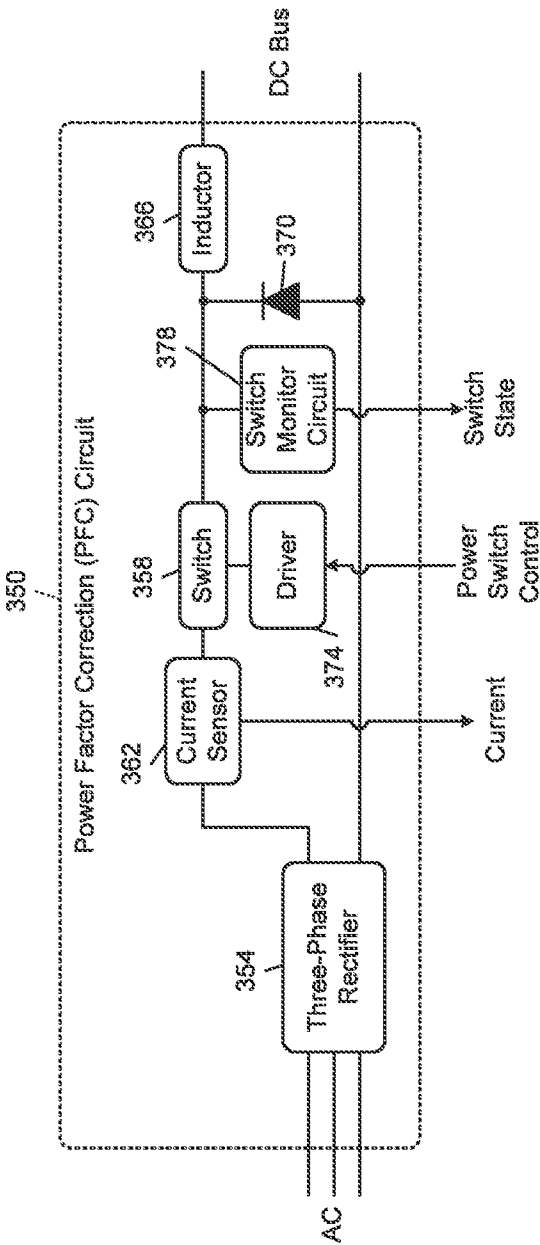


FIG. 3B

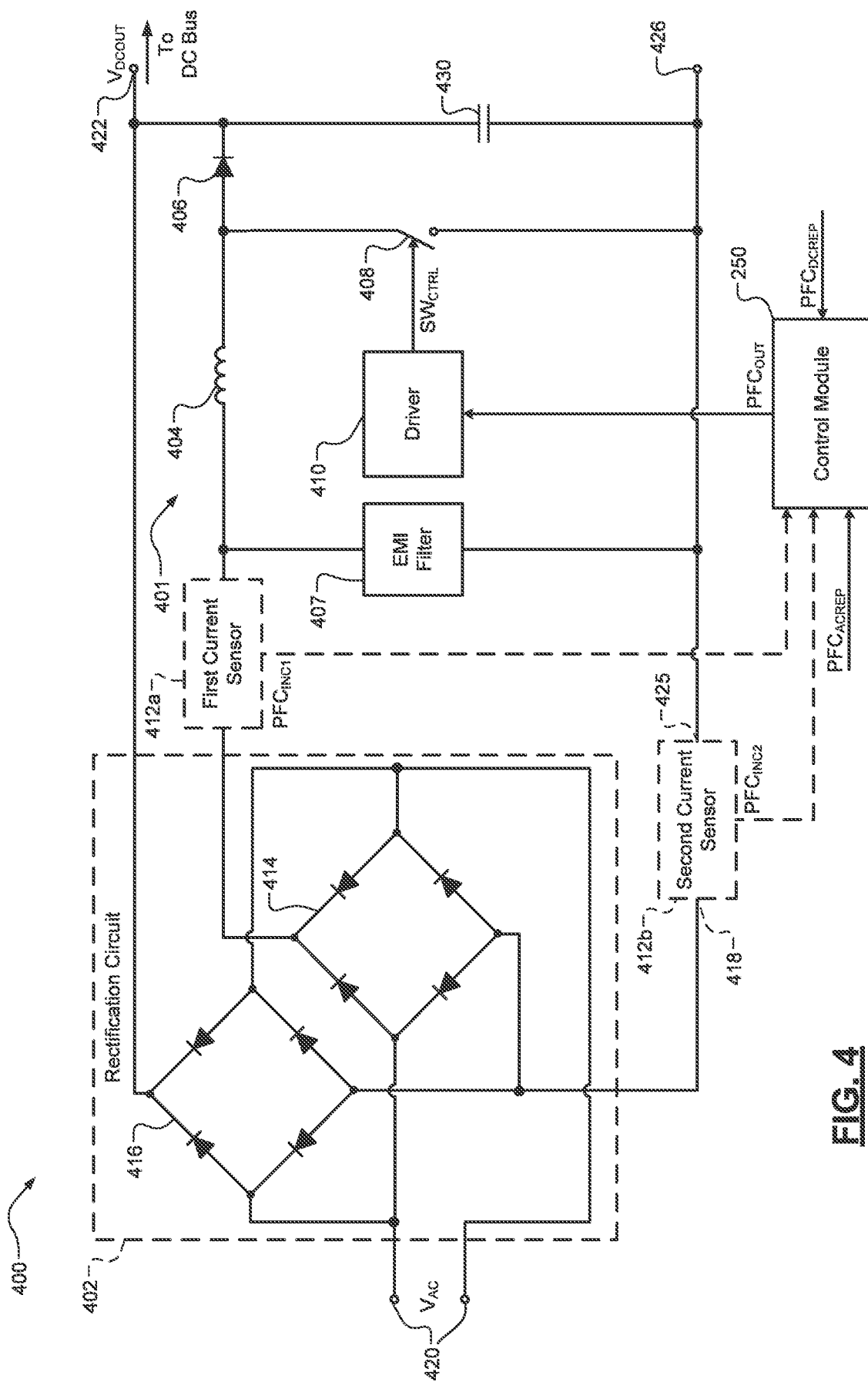


FIG. 4

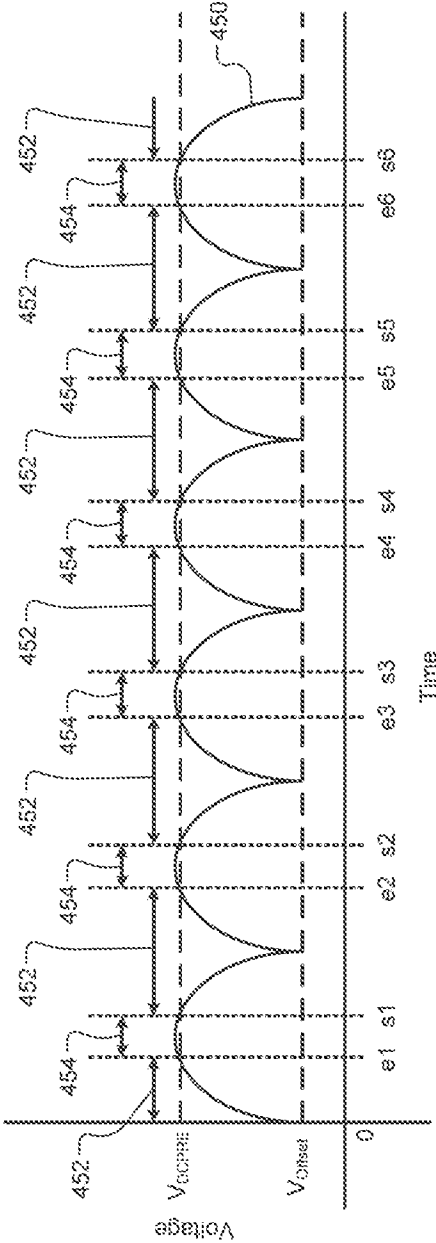


FIG. 5

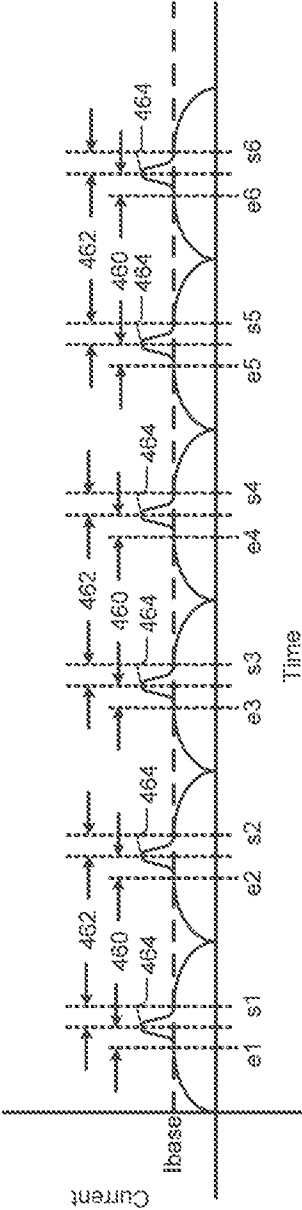


FIG. 6

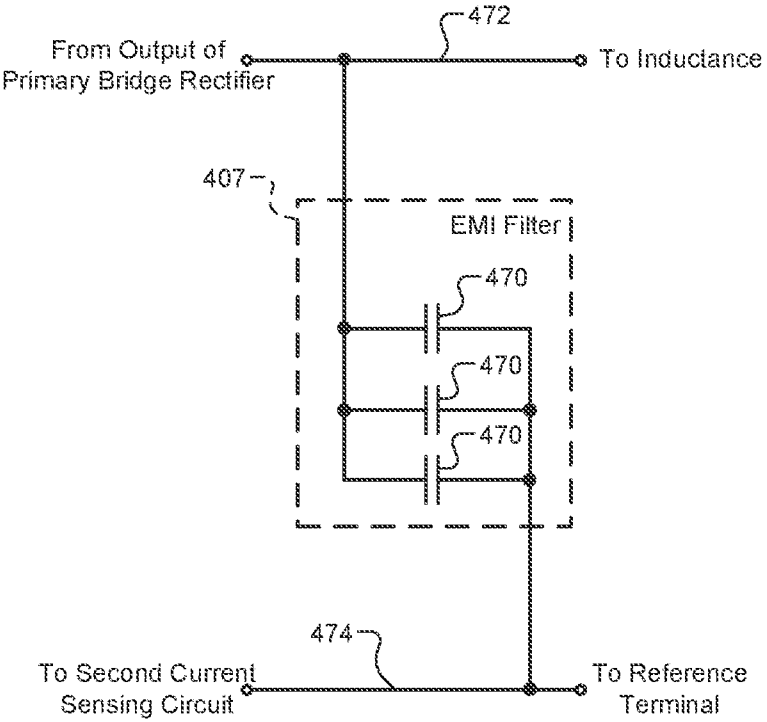


FIG. 7

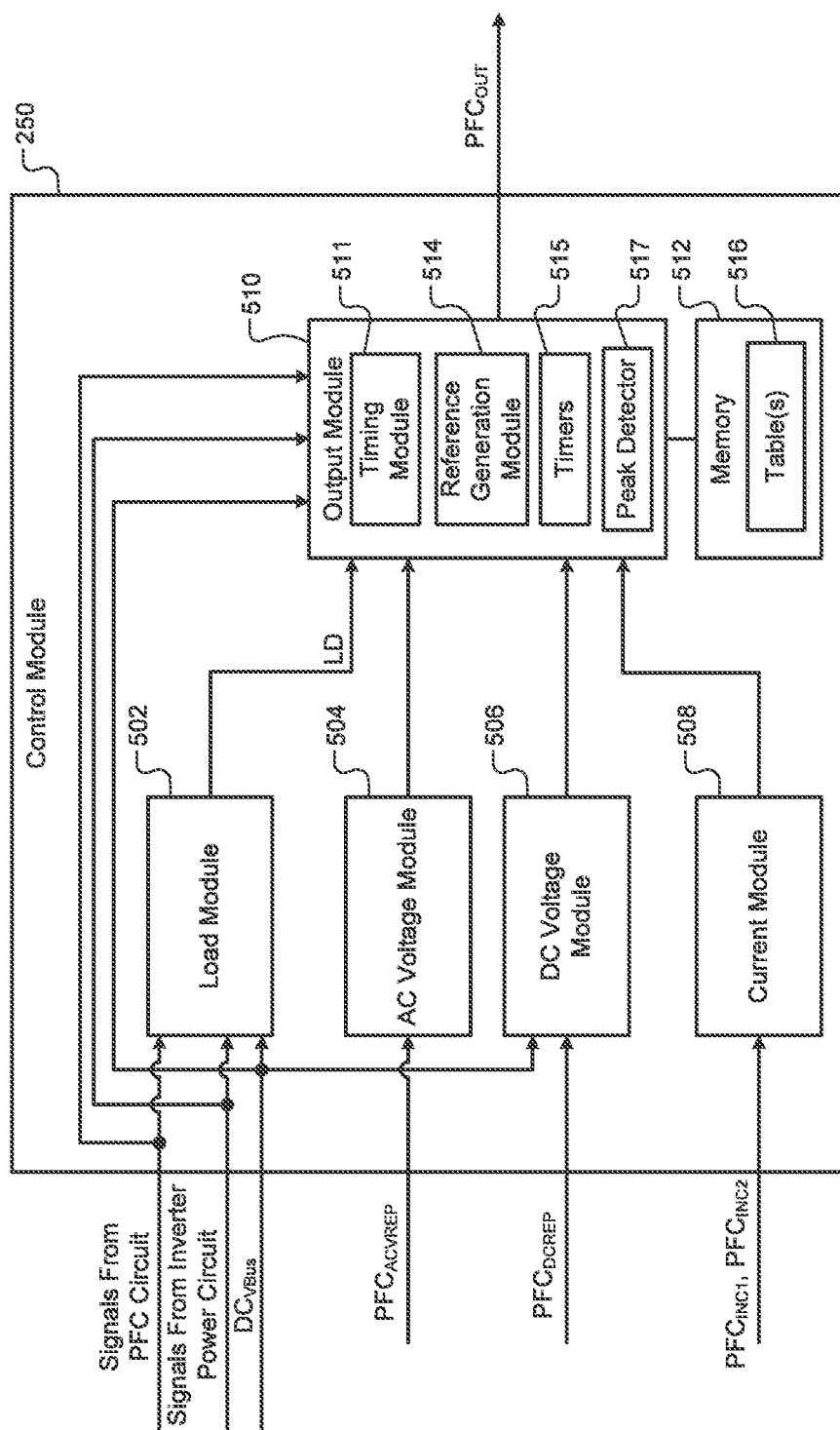
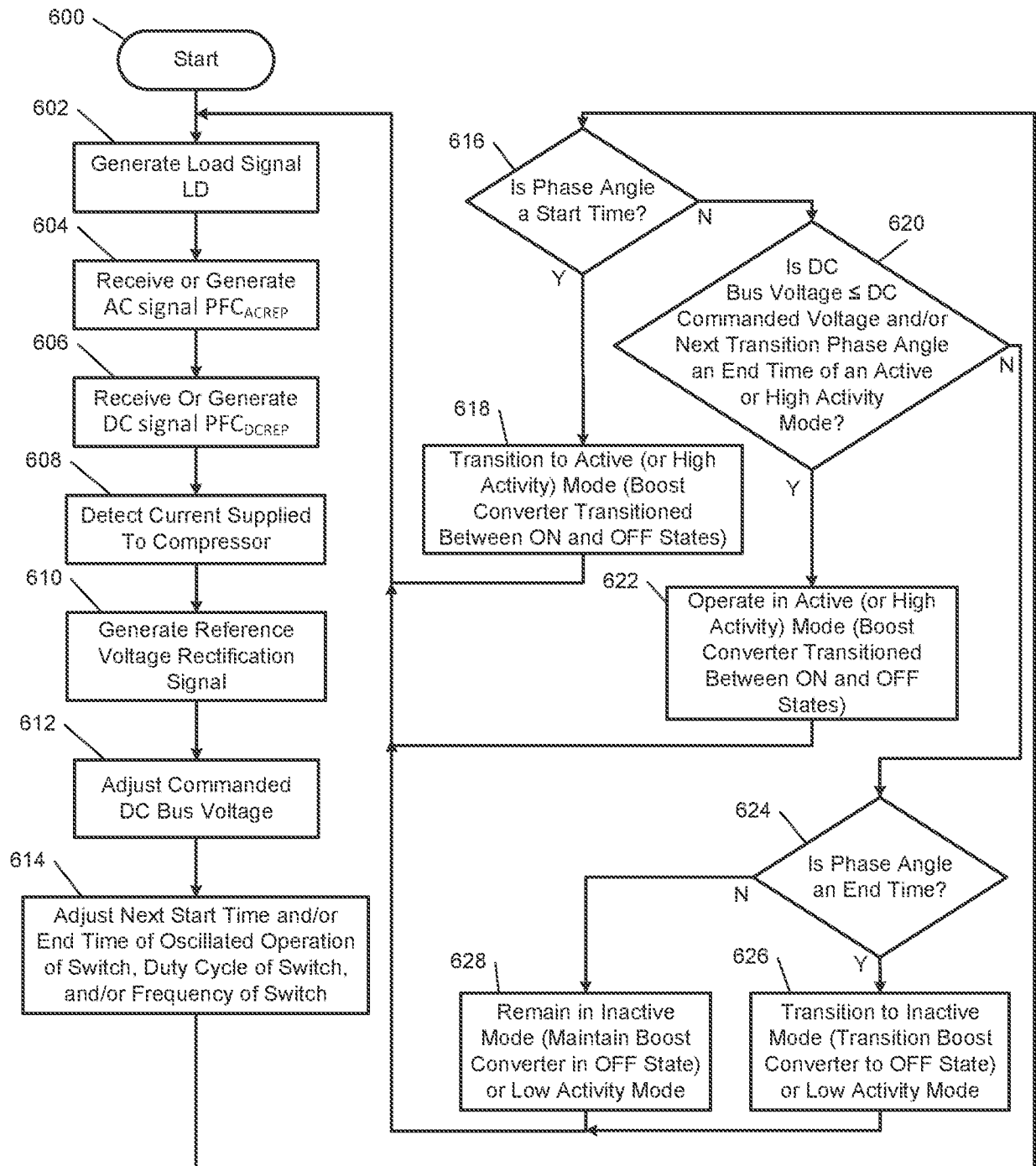
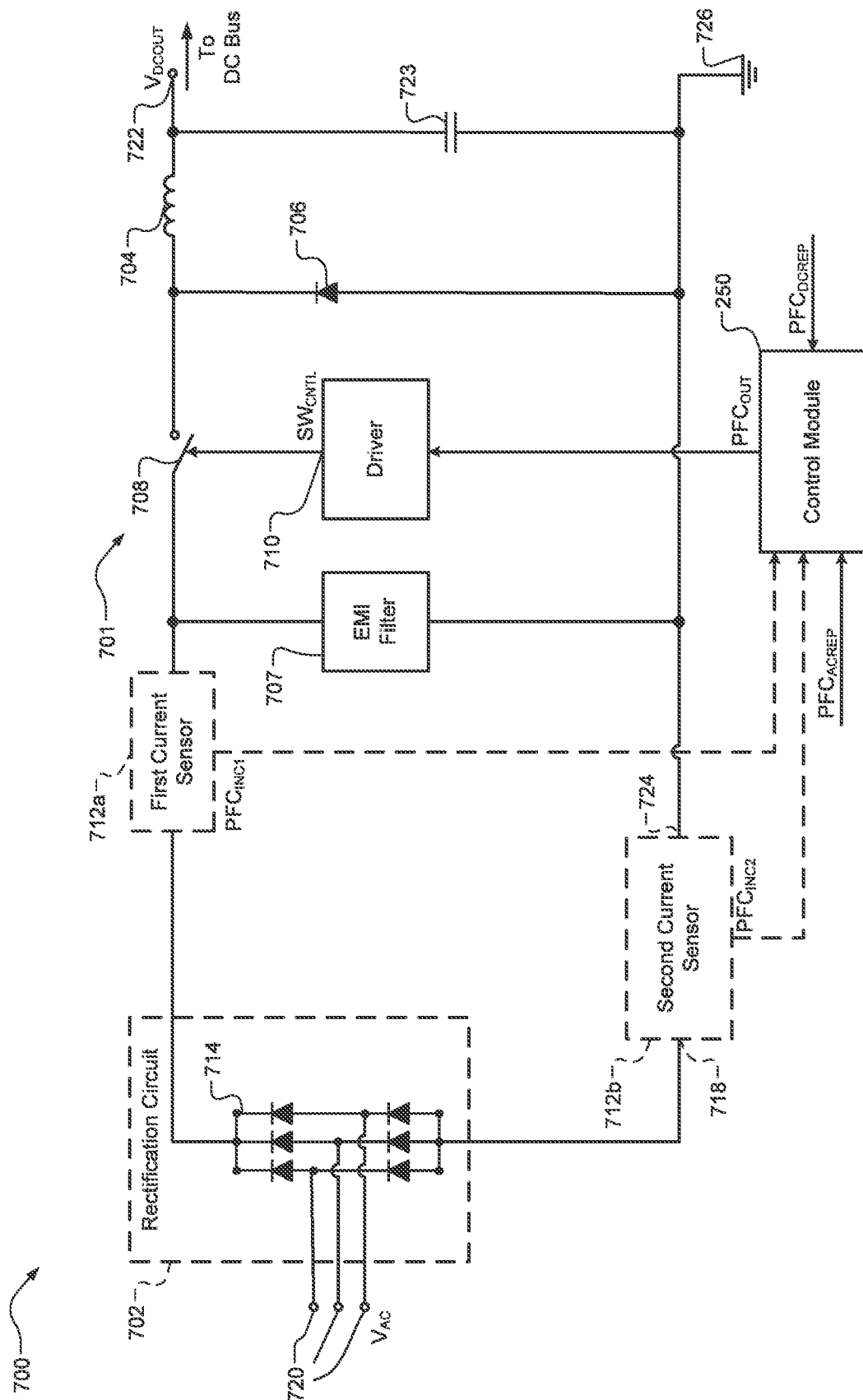
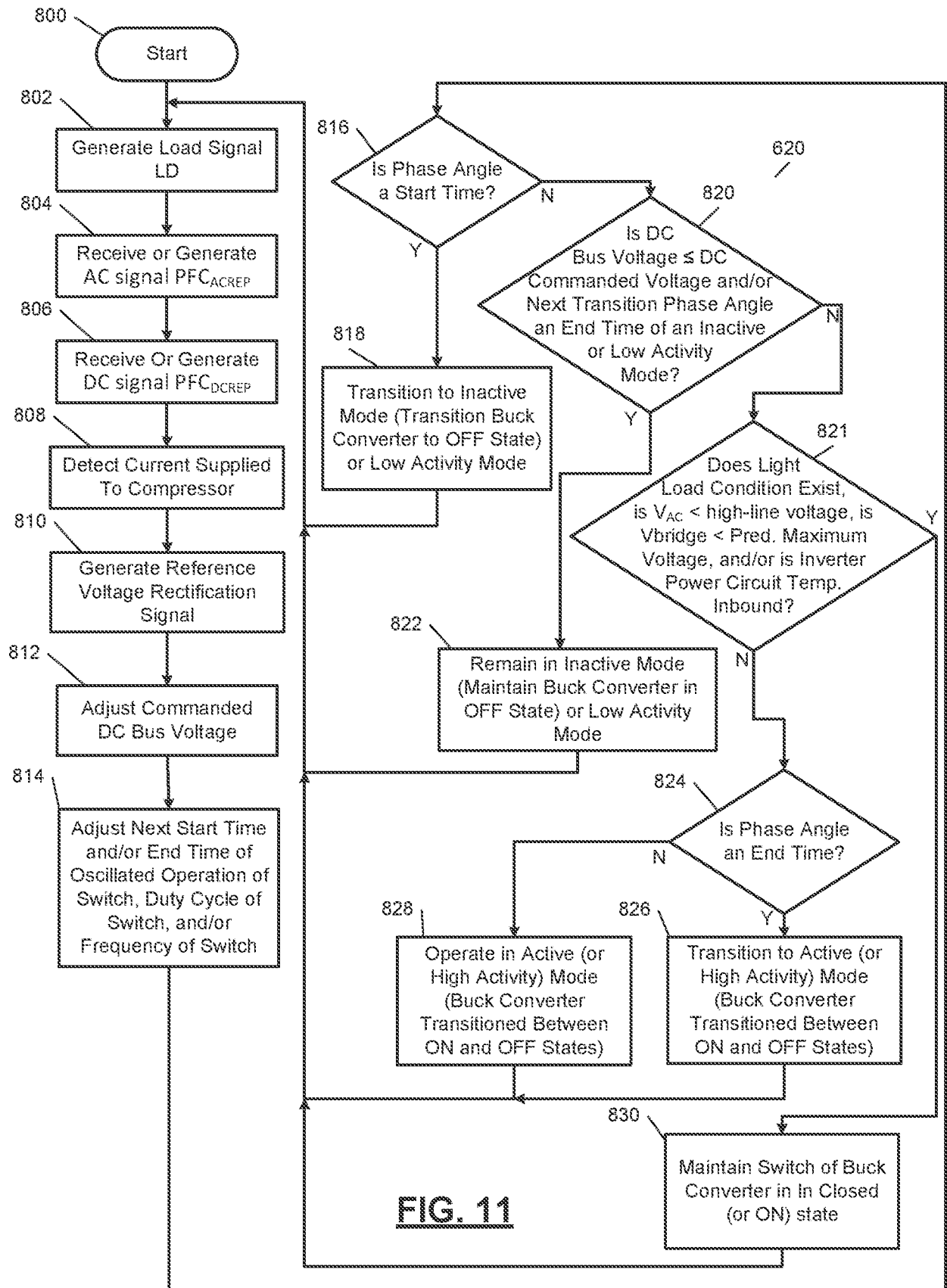


FIG. 8

**FIG. 9**



0101



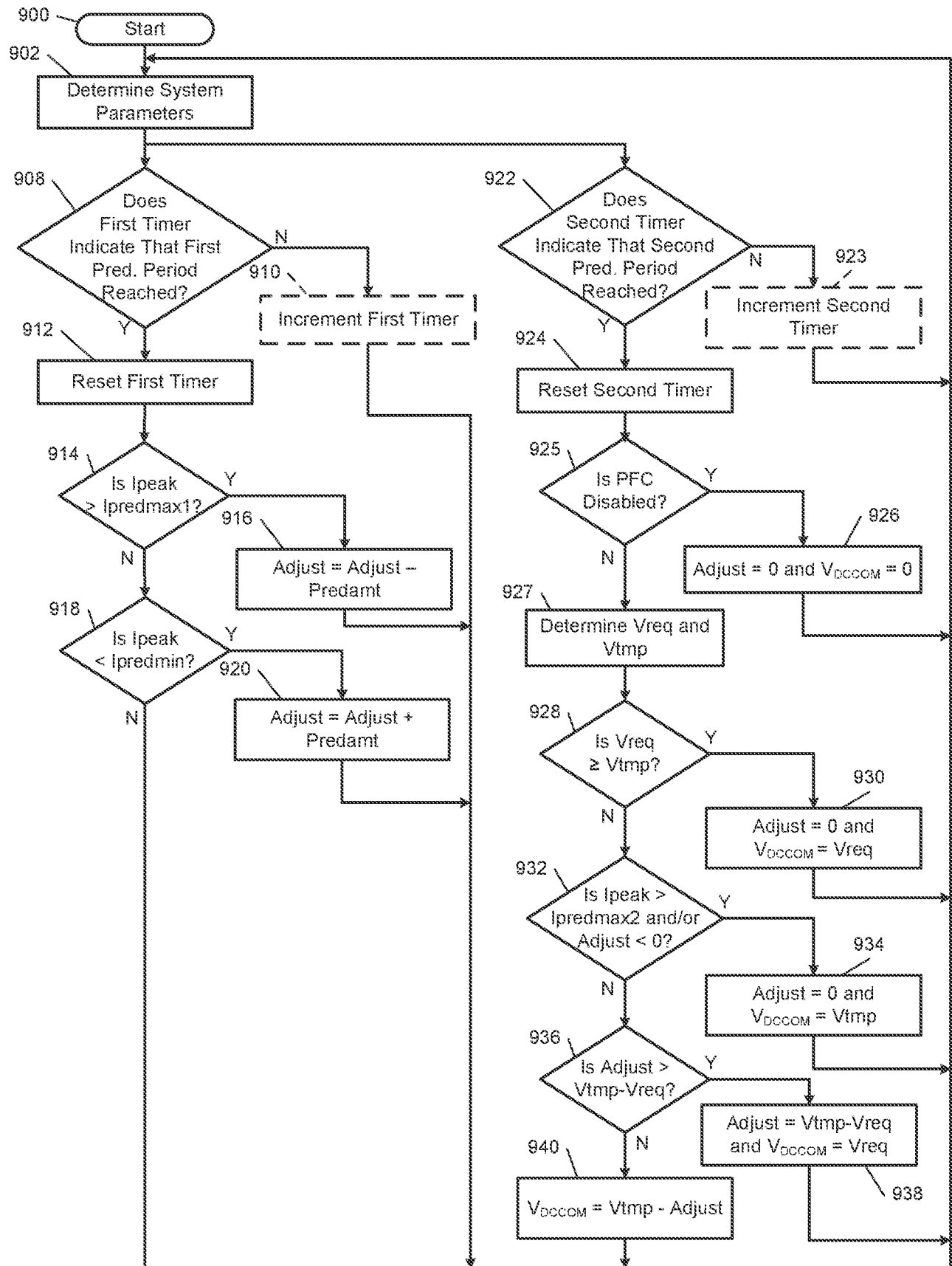


FIG. 12

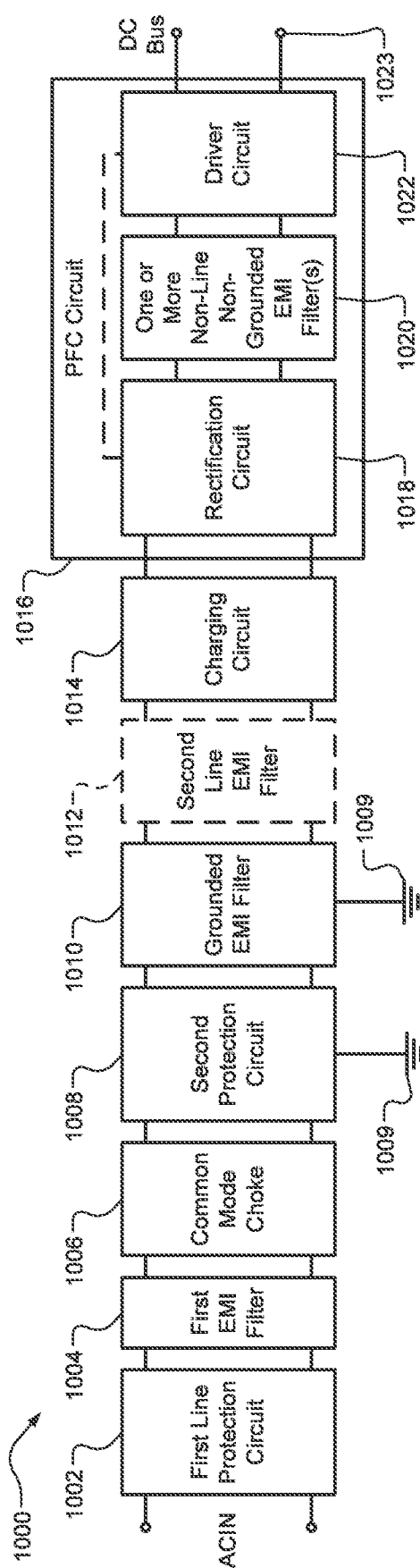


FIG. 13

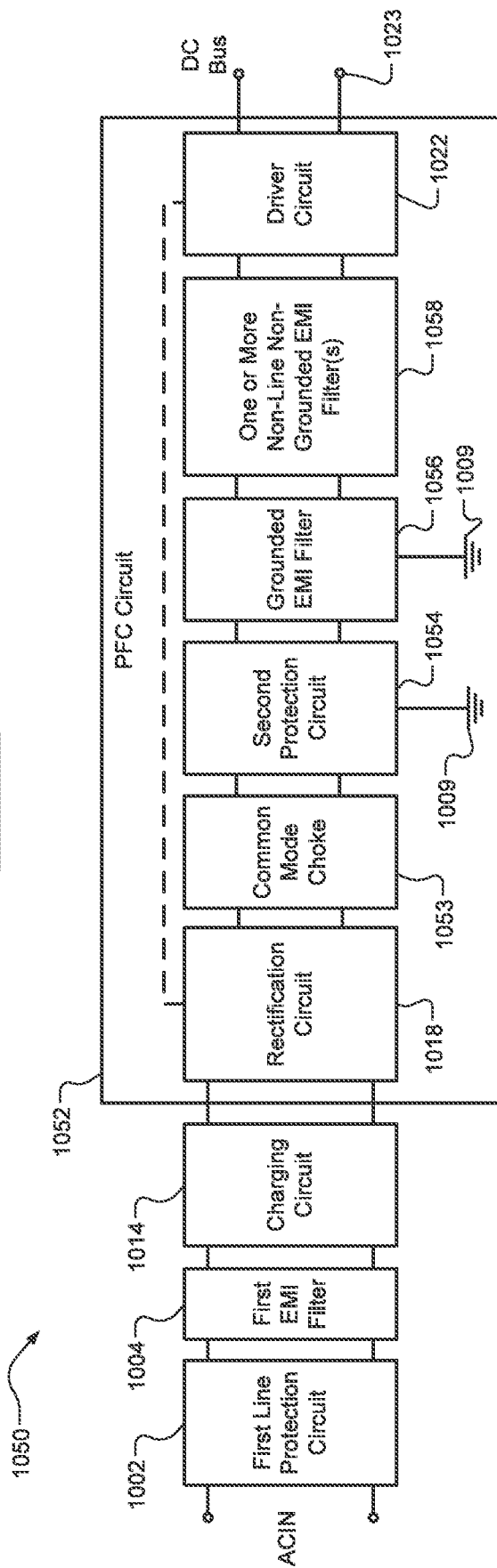


FIG. 14

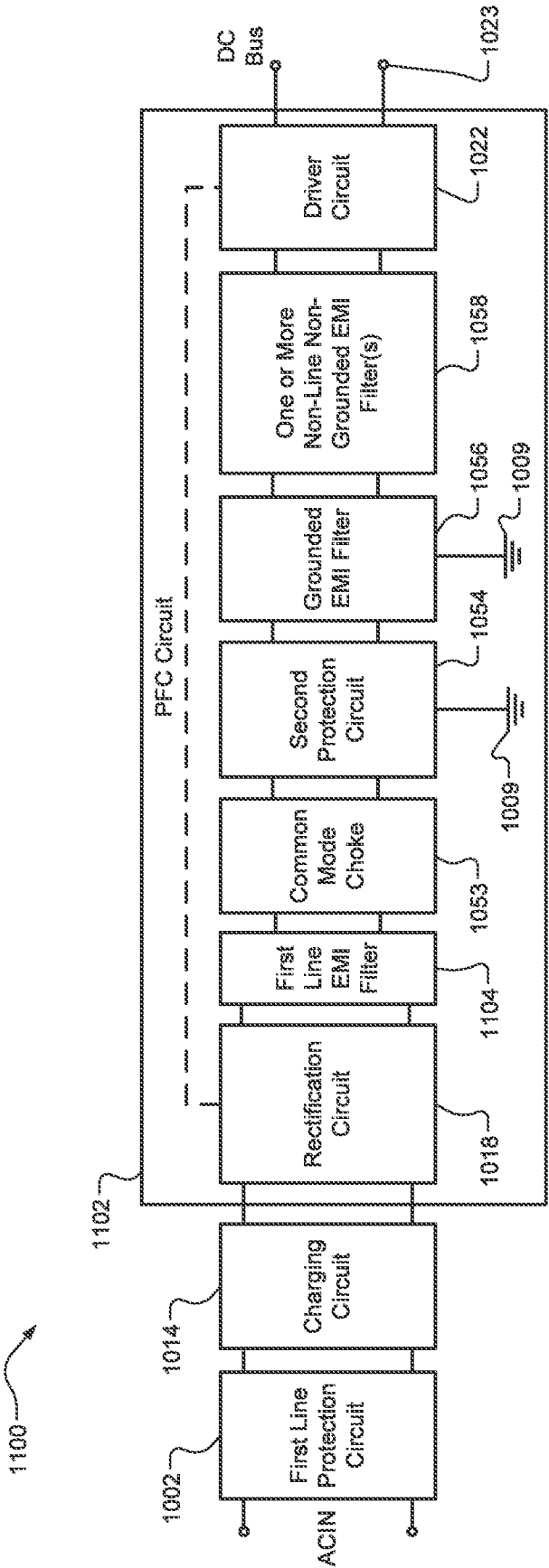


FIG. 15

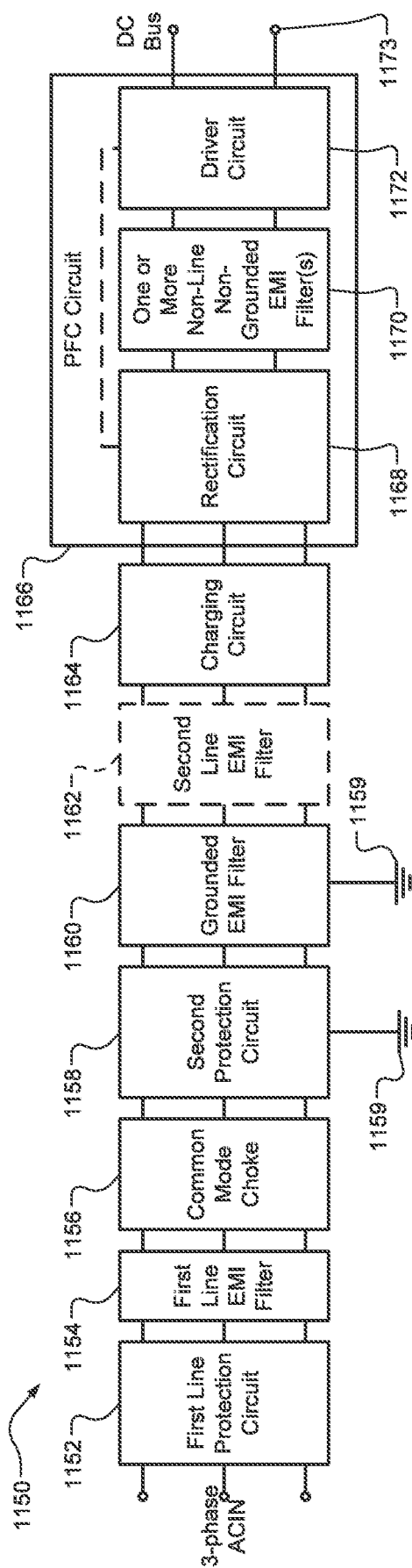


FIG. 16

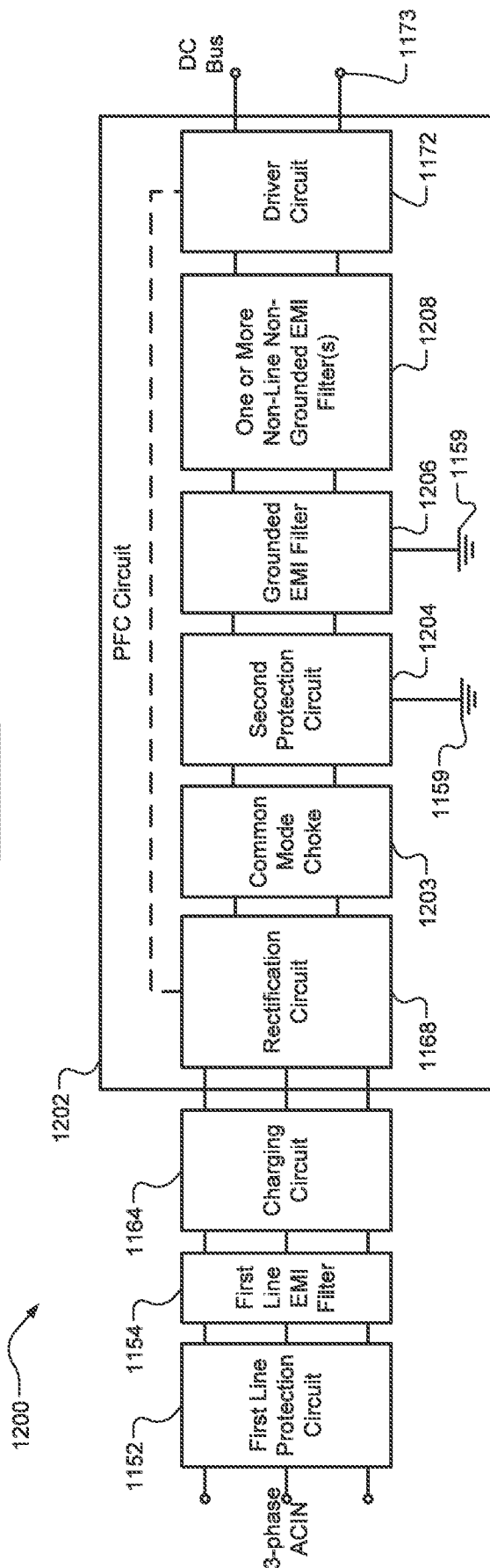


FIG. 17

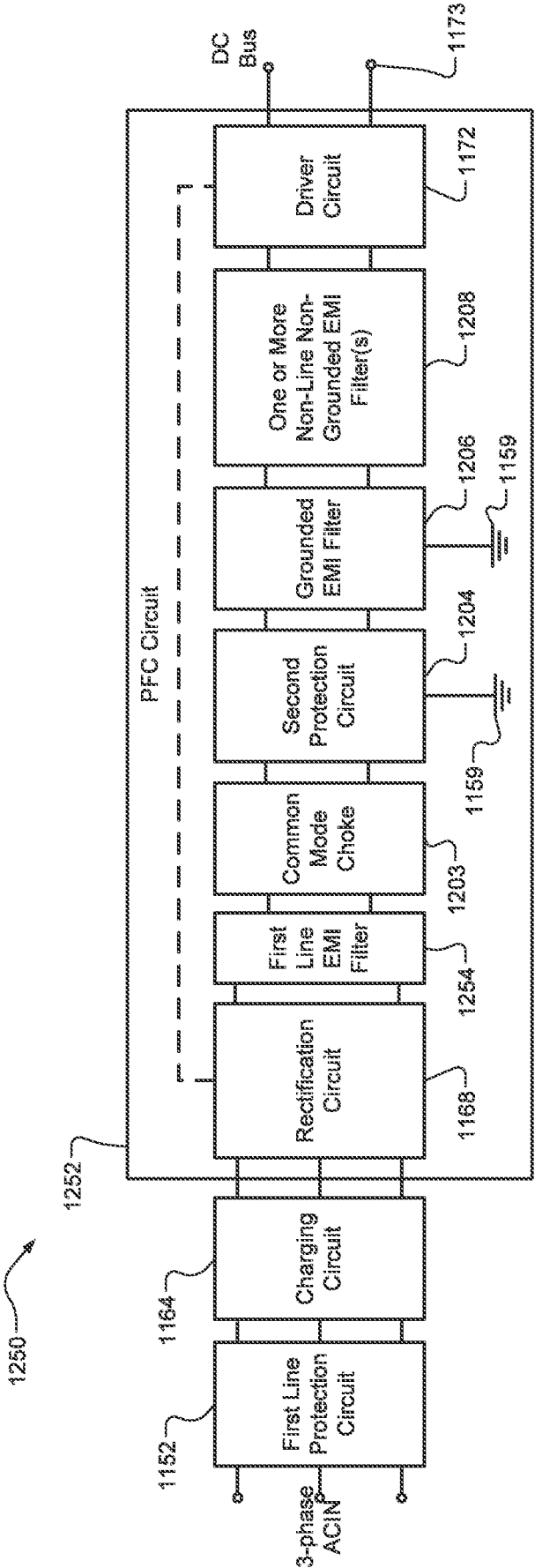


FIG. 18

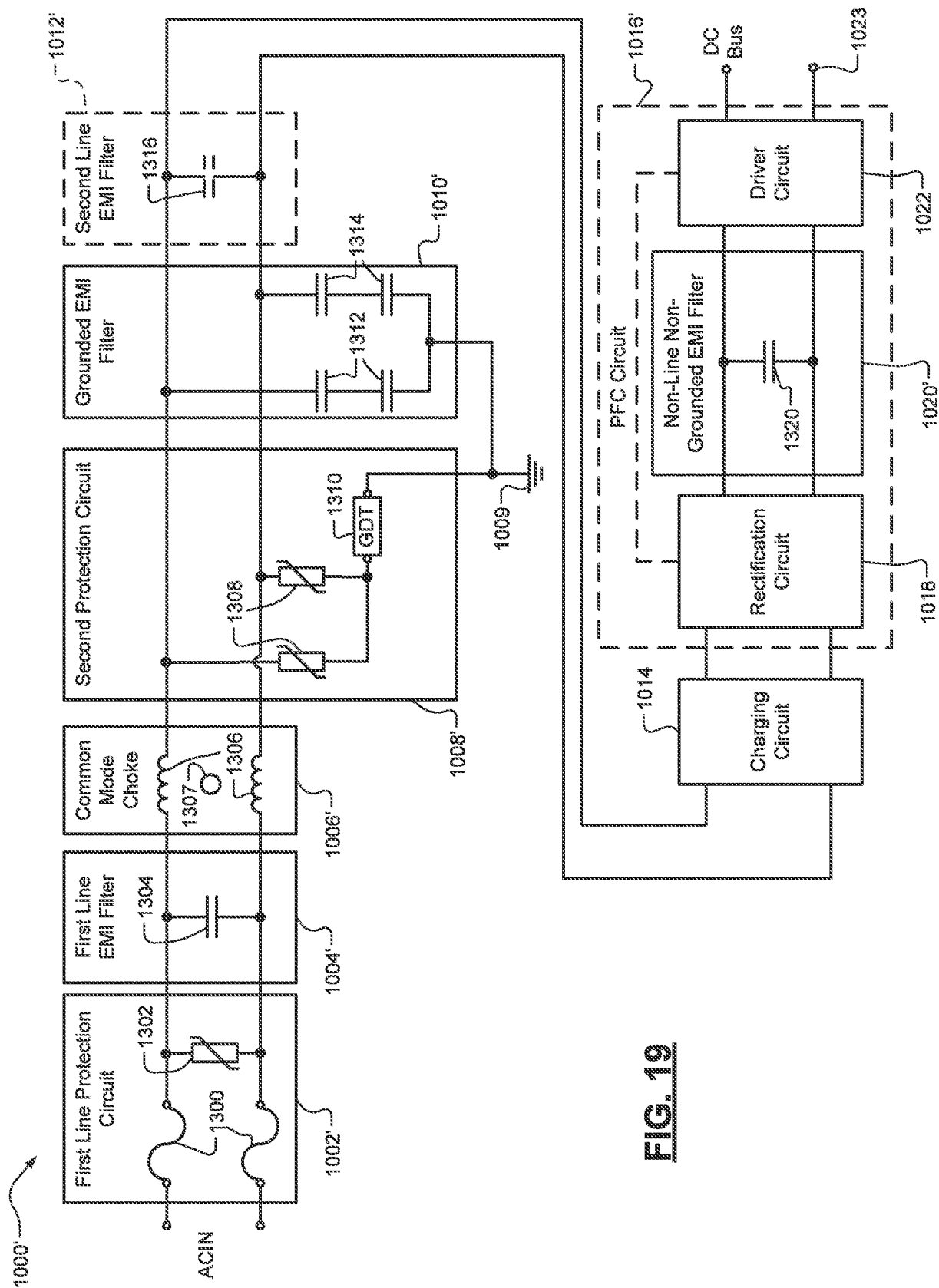


FIG. 19

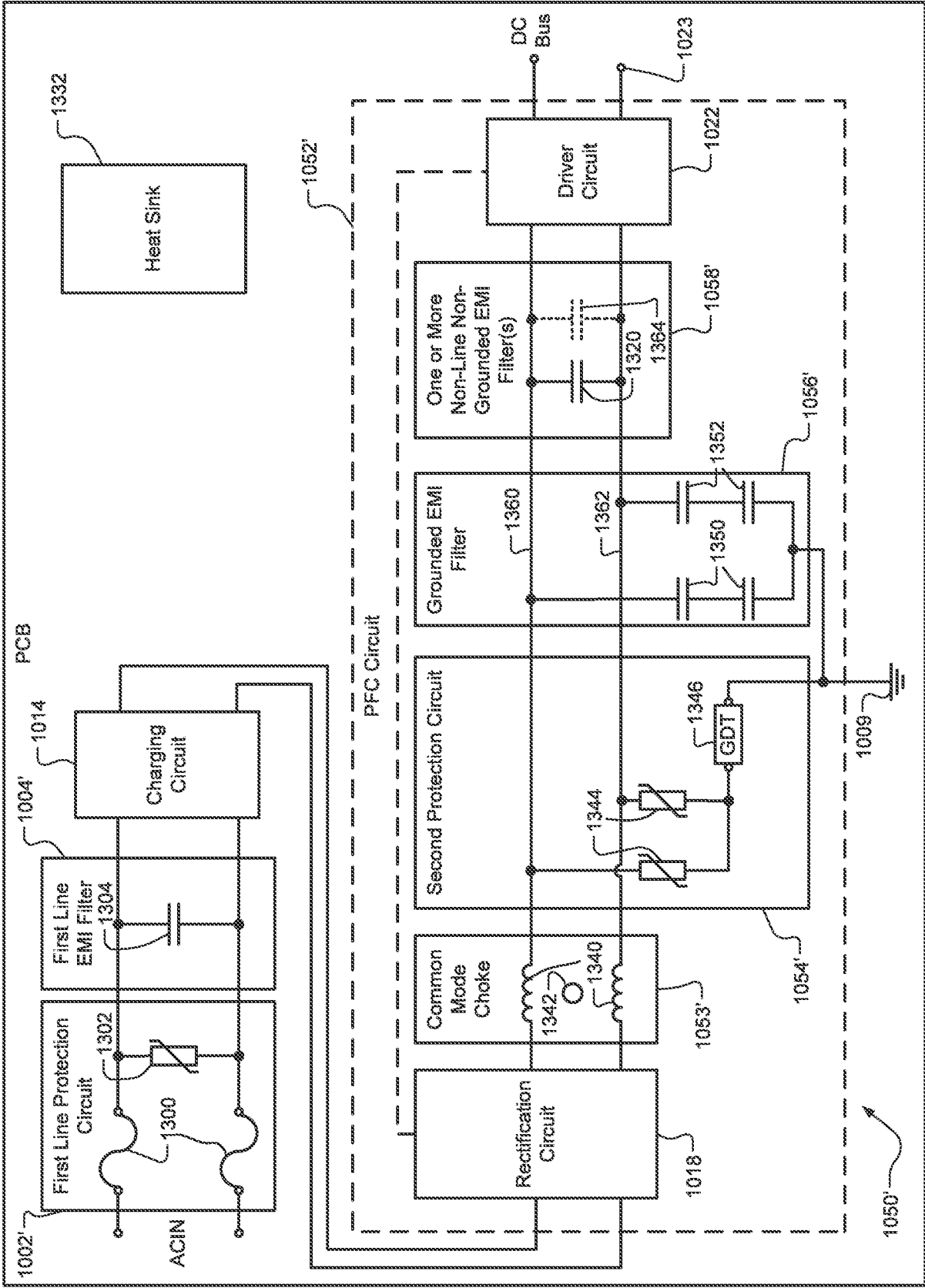


FIG. 20

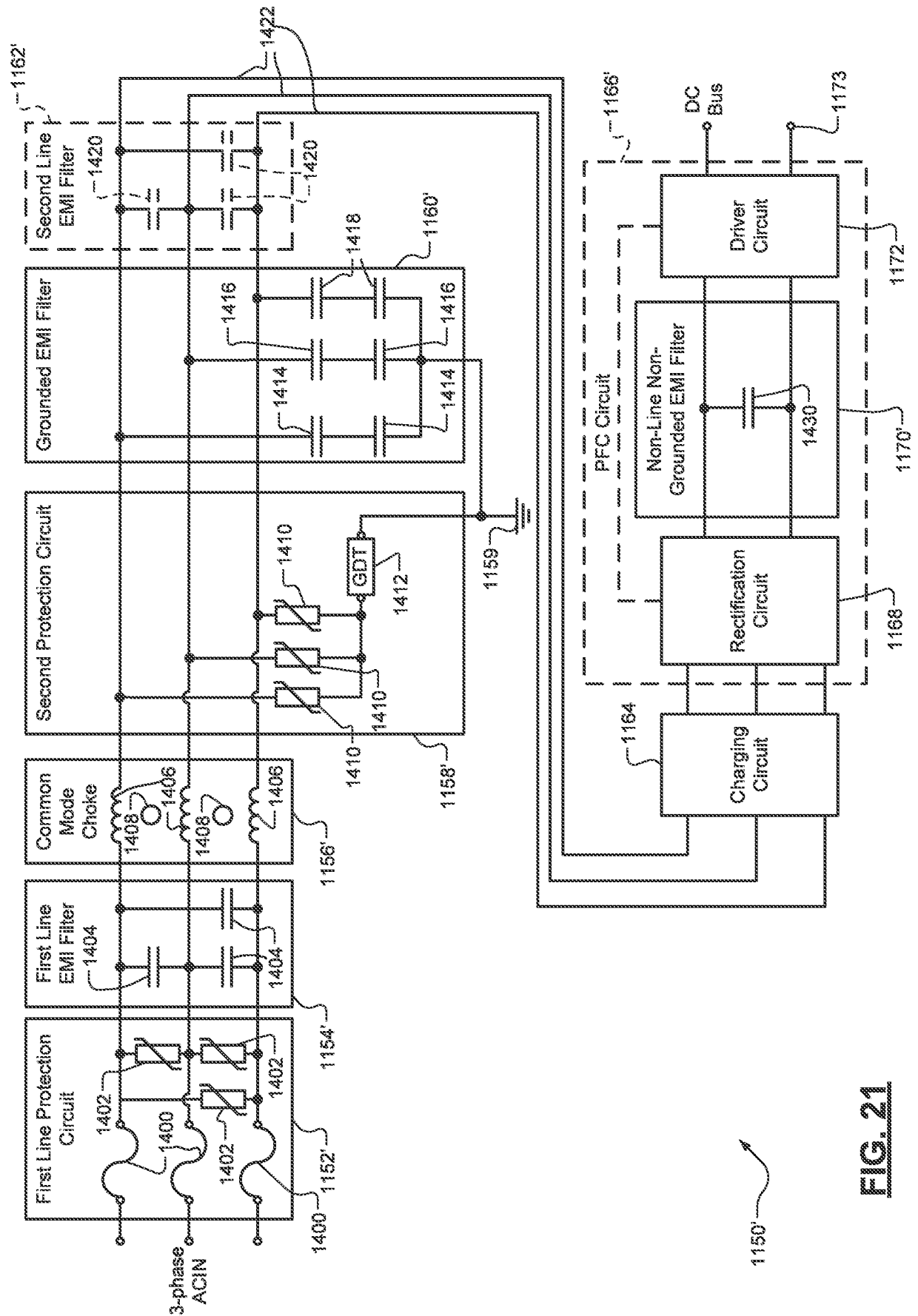


FIG. 21

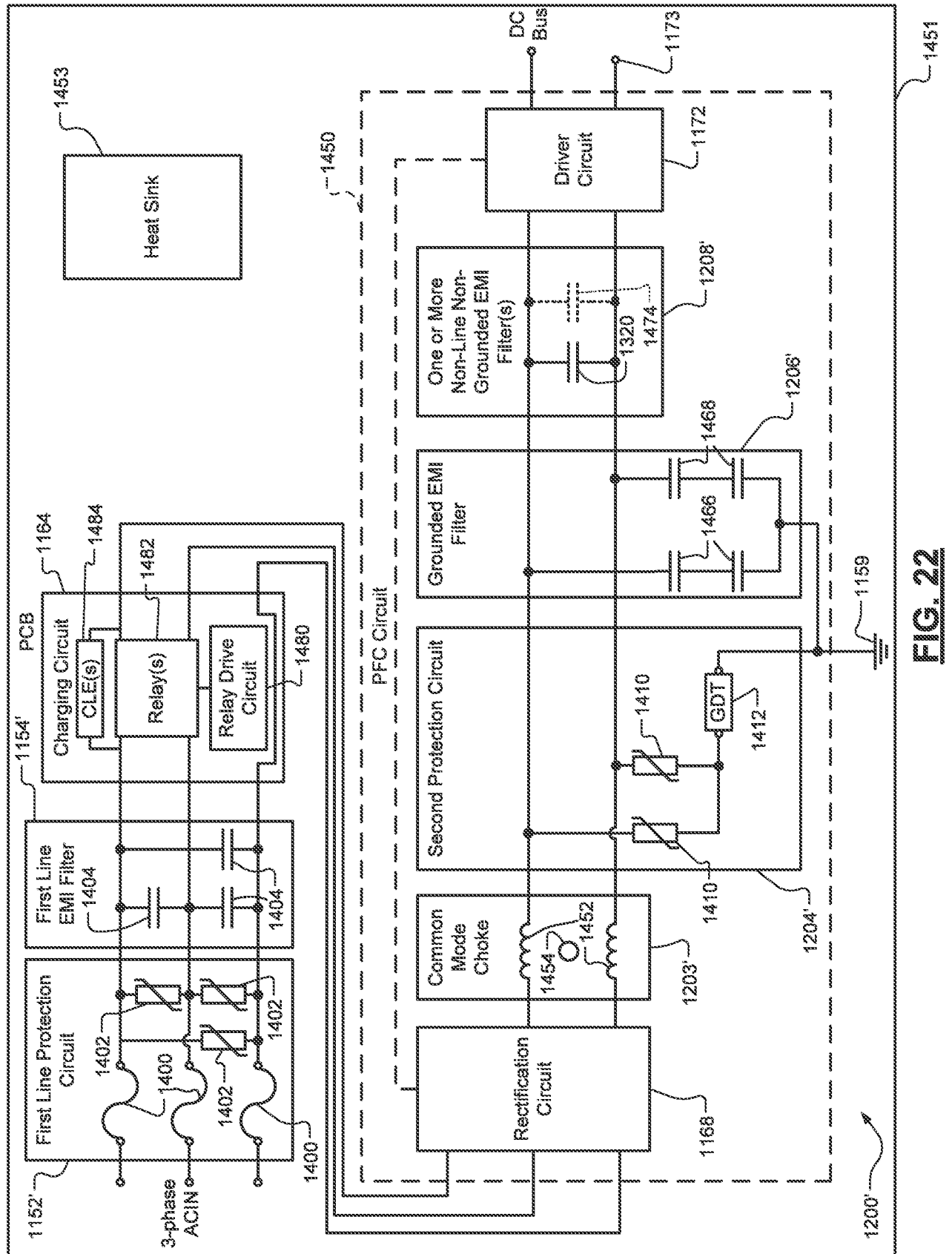


FIG. 22

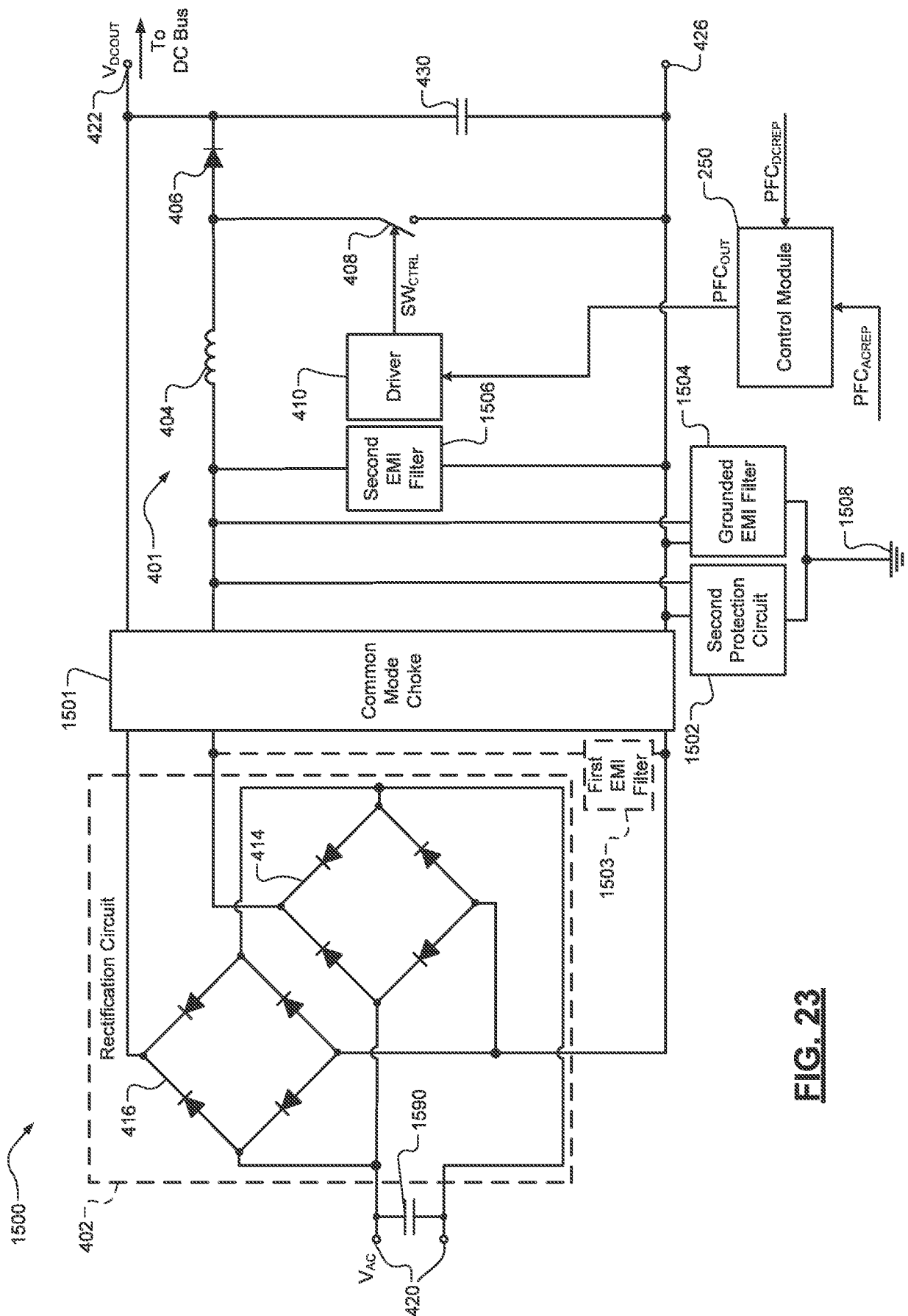


Fig. 23

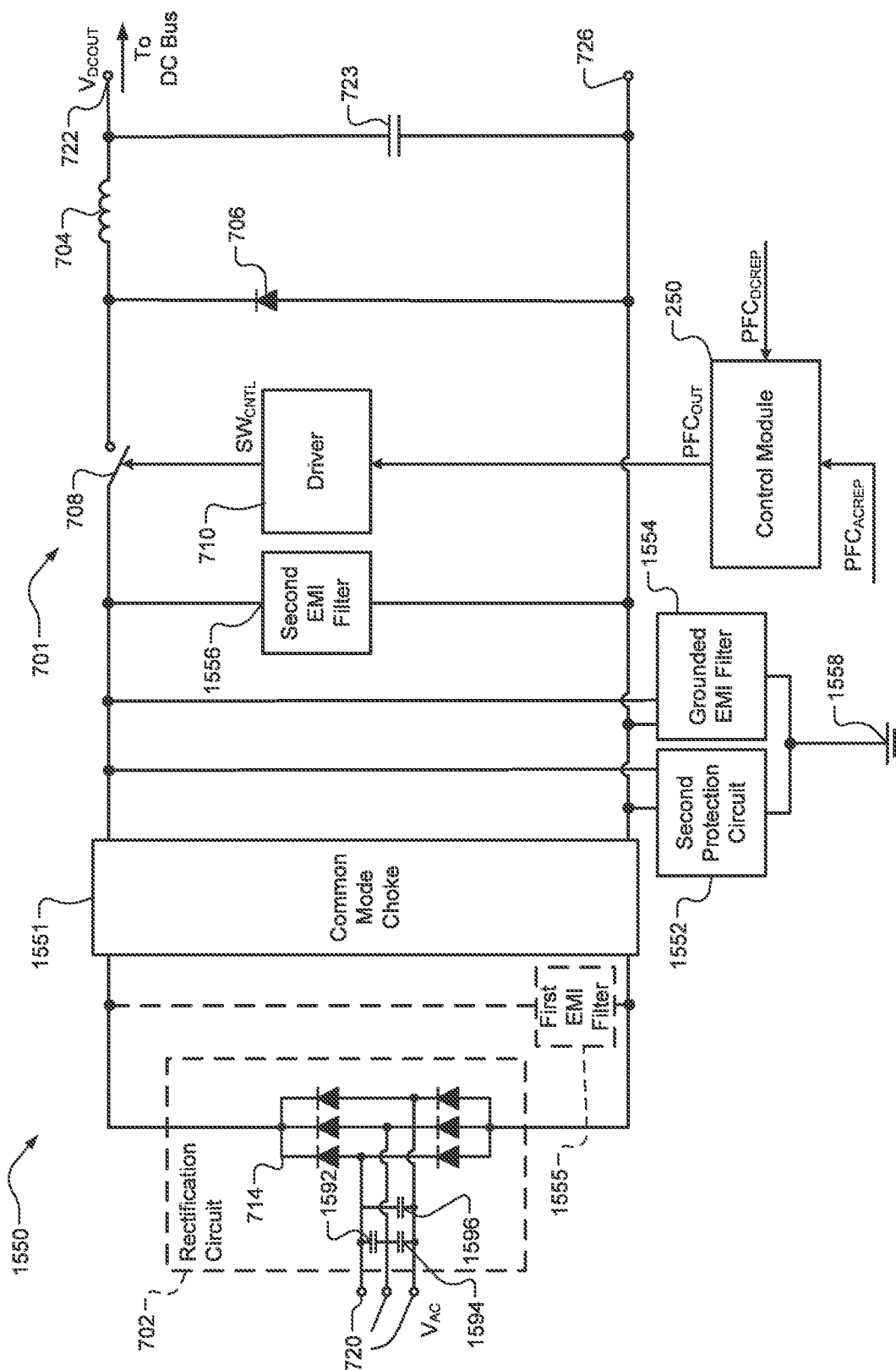


FIG. 24

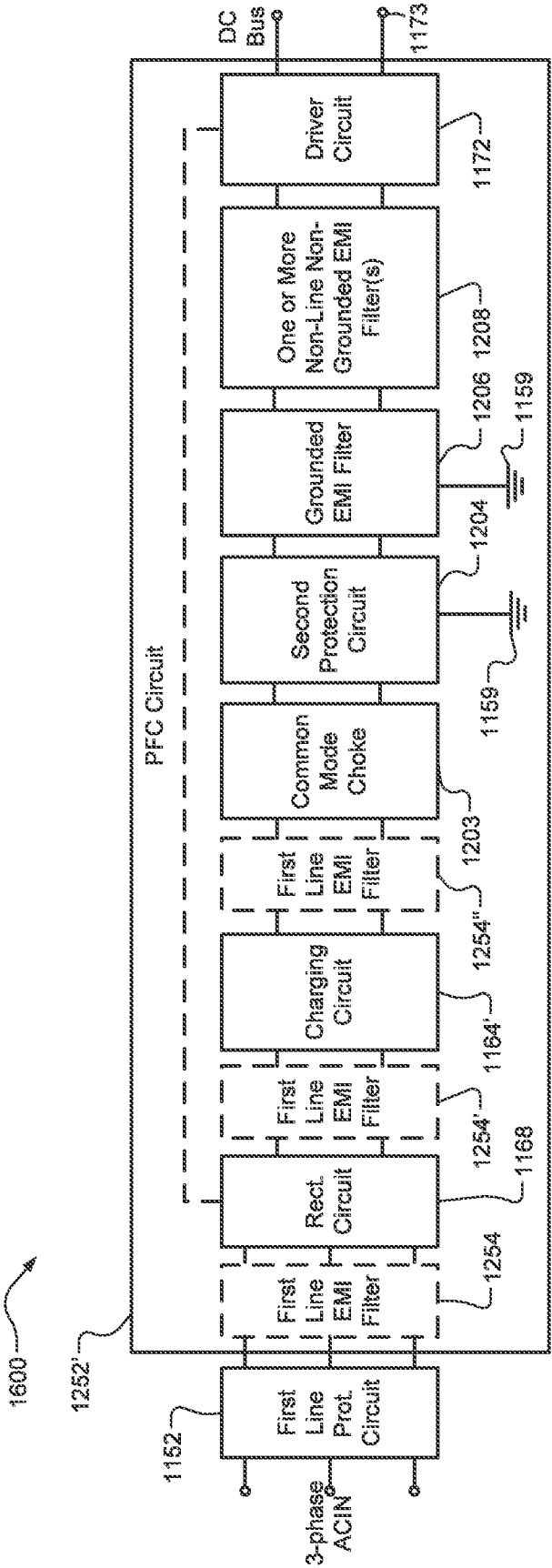


FIG. 25

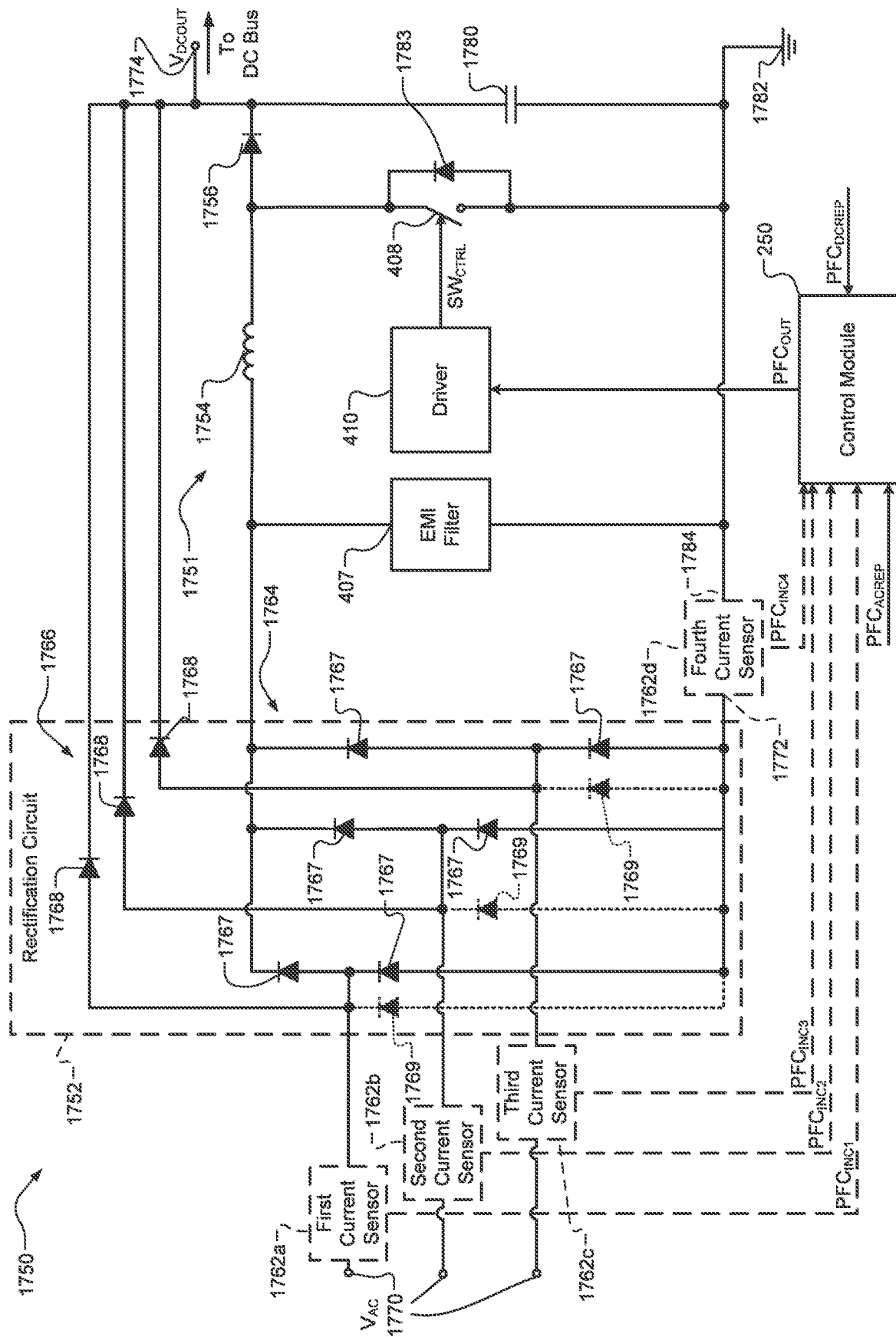


FIG. 26

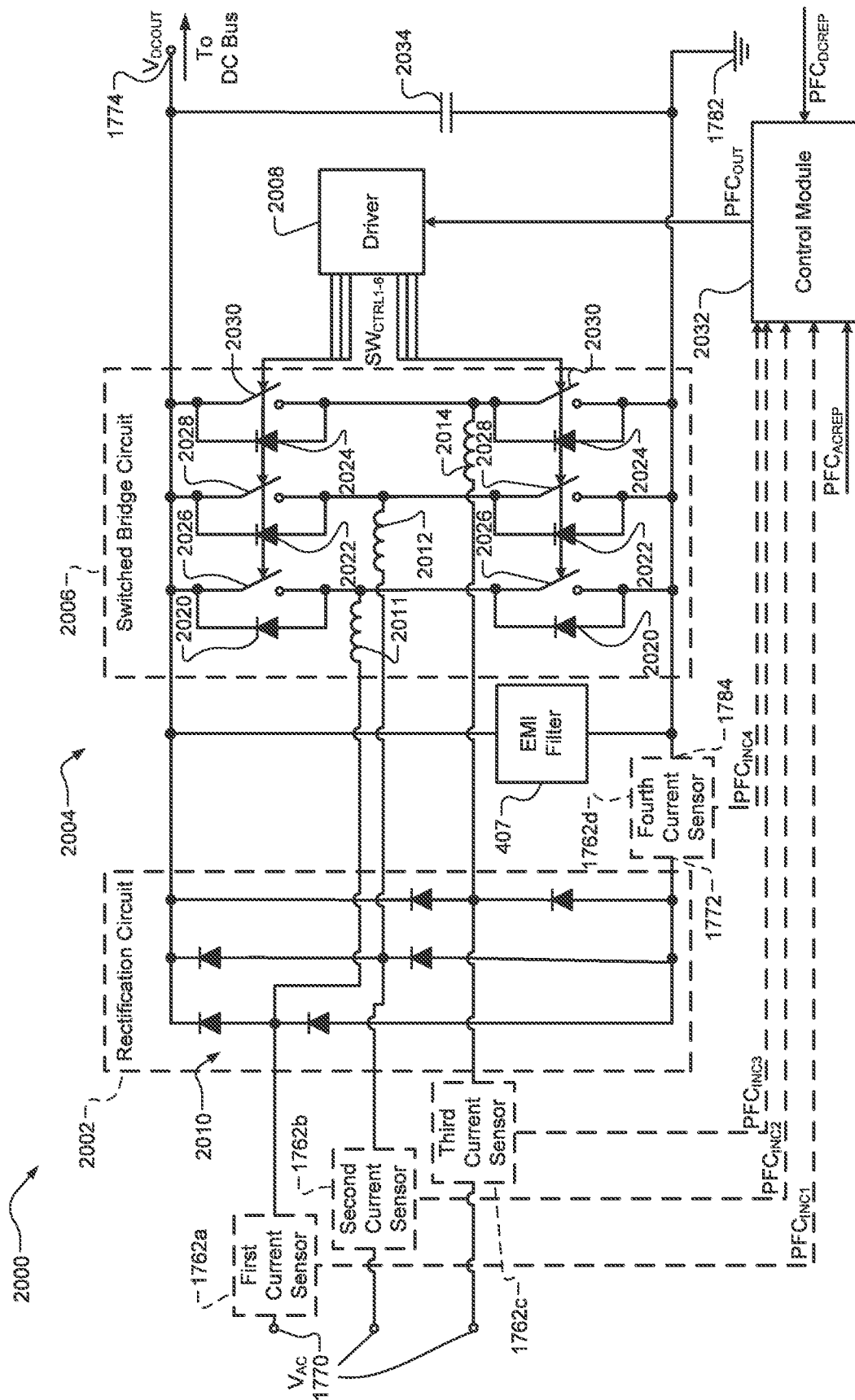


FIG. 27

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/027738**A. CLASSIFICATION OF SUBJECT MATTER****H02M 1/42(2007.01)i, H02M 1/44(2007.01)i, H02P 27/08(2006.01)i, F04B 49/03(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M 1/42; H02M 1/36; H02P 29/00; H02P 6/00; H02M 7/12; H02M 7/00; H02M 1/14; H02M 1/12; H02M 1/44; H02P 27/08; F04B 49/03

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: converter, power factor, filter, rectification, choke, charging circuit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0169046 A1 (CHICONY POWER TECHNOLOGY CO., LTD.) 19 June 2014 See paragraphs 16-19, and figure 1.	1-39
A	EP 0744816 A2 (AT&T IPM CORP.) 27 November 1996 See column 3, line 52 - column 4, line 7, claim 1, and figure 7.	1-39
A	US 9300241 B2 (REGAL BELOIT AMERICA, INC.) 29 March 2016 See the entire document.	1-39
A	JP 2010-541256 A (LSI INDUSTRIES, INC.) 24 December 2010 See the entire document.	1-39
A	US 7903441 B2 (FU-SUNG CHEN et al.) 08 March 2011 See the entire document.	1-39



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 August 2017 (18.08.2017)

Date of mailing of the international search report

18 August 2017 (18.08.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

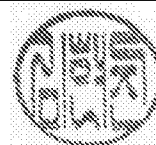


Facsimile No. +82-42-481-8578

Authorized officer

KIM HYEON JIN

Telephone No. +010-4310-7635



INTERNATIONAL SEARCH REPORT

Information on patent family members

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