1 578 174

PATENT SPECIFICATION

(11) 1 578 174

(21) Application No. 10902/78 (22) Filed 20 March 1978
(31) Convention Application No. 781261
(32) Filed 25 March 1977 in
(33) United States of America (US)
(44) Complete Specification published 5 Nov. 1980
(51) INT CL³ G01R 21/06
(52) Index at acceptance
G1U BE

(54) A DIGITAL PROCESSING AND CALCULATING AC ELECTRIC ENERGY METERING SYSTEM

(71) We, WESTINGHOUSE ELECTRIC CORPORATION of Westinghouse Building, Gateway Center, Pittsburgh, Pennsylvania, United States of America, a company organised and existing under the laws of the Commonwealth of Pennsylvania, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to electric energy measurements for electric utility systems, and more particularly such measurements utilizing digital processing with calculations by programmed control of solid state circuits.

In the field of electric utility power and energy measurements, electromechanical induction type watthour meters have been the most extensive type in commercial use. Although many electronic measuring circuits are known, improvements in their accuracy, ruggedness, reliability and cost is desired.

Analog system multiplying circuit techniques have been chiefly used in the electronic power and electric energy measuring circuits to compute the product of the voltage and current components of an electric energy quantity to be measured. Power consumption or the electric energy usage in kilowatt-hours and kilowatt demand is required for billing purposes by an electric utility company and a computed power quantity must be calculated by the measurement circuits by deriving the product of voltage and current. The power quantity must be integrated with respect to time to produce kilowatt-hour measurements. It is further desirable to have circuits with the capability of measuring additional electric energy parameters of a power line system, such as reactive kilovolt-ampere hours, volts-squared hours and ampere-squared hours for load studies.

In one solid state measuring circuit described in U.S. Patent No. 3,764,908 assigned to the assignee of this invention, voltage and current related signals are both applied to a semiconductor device having a logarithmic computing characteristic. Accordingly, an output signal is produced which is equal to the product of the input signals.

Another known analog multiplier technique includes time division multiplication. For example, a voltage signal is sampled to derive a pulse width modulated signal corresponding to the voltage amplitudes. The current signal is sampled at a rate controlled by the variable pulse width signal. An output is produced consisting of a series of pulses having a height proportional to the instantaneous current values and pulse width proportional to the instantaneous voltage values. The resultant signal is filtered to obtain an average value of the pulses which is, in turn, proportional to the instantaneous power. The average value signal is applied to a voltage-to-frequency converter utilizing integrating capacitors, for example. Variable frequency pulses of the converter are applied to a magnetic recorder or pulse totalizer formed by an electromechanical counter or electronic counting circuit. The accumulated pulses are representative of the electric energy kilowatt-hour consumption for billing or power analysis by an electric utility company. Electronic circuits for performing various measurements of electric energy are disclosed in U.S. Patents 3,864,631, and 3,778,794, both assigned to the assignee of this invention.

It has been found that the analog electronic circuit techniques are sometimes difficult to apply in order to obtain the desired accuracies. Accurate drift-free

analog multipliers are often expensive and it is further difficult to obtain square root computing circuits in the analog circuit field which are sometimes required for calculating electric power quantities. Also, analog integration circuits required in the analog electronic power measuring apparatus produce undesired drift and variations over long time intervals. In time division multiplication circuits it is known that frequency dependent sampling occurs at the multiplier with the associated digital integration also having similar dependency upon variations of integrating capacitors.

A more ideal approach to electric power measurements is to utilize digital processing techniques wherein voltage and current signals are sampled at very high rates, for example in the order of 1,000 times per cycle. The instantaneous sampled values would be quantized in high resolution analog-to-digital converters having a high order of bits provided in the binary representations of the digitizing outputs thereof. The time for the amplitude quantizations would be negligible and the speed of the digital processor circuitry would be sufficiently fast so that all of the calculations would keep up with the fast sampling rates.

The known advantages of an ideal digital approach, after the analog values have been converted to digital signals, is that there are no changes of accuracy occurring due to component drift and variations. Calculation of different electric power and energy parameters are more easily accomplished in digital circuits. The use of programmable read only memories permit flexibility in the measuring apparatus so that it is possible to accomplish many different functions without substantial changes in hardware.

The disadvantages of an ideal digital measuring apparatus include the use of analog-to-digital converters having very high speeds and high resolution which are rather expensive since these two characteristics are competing from a design standpoint due to the fact that more time is typically required to achieve higher resolutions in the quantizations. The higher resolution outputs of such converters produce higher order binary word lengths to represent the analog values so that associated circuits become more complex and expensive. Further, digital processing circuits capable of operating at varying fast speeds are substantially more complex, expensive and require higher operating power supplies.

Alternatively, a digital processing power measuring apparatus capable of operating at slower sampling speeds and digitizing the instantaneous signal values with less resolution retains the advantages of the digital techniques including stability and flexibility at substantially lower cost. The reduction in resolution permits handling of shorter binary words with less bits for producing the digitized binary representations of the analog signal amplitudes. Slower sampling speeds permit digital processing at lower speeds to simplify the digital processing circuit. However, the reduced sampling rates and lower digitizing resolution have a corresponding reduction in the accuracy of the digital representations of the sample amplitudes and a reduction in the true digital representation of each complete cycle of the input analog signals.

Examples of prior art patents generally disclosing the use of digital circuit techniques and digital calculations in power line and power measuring systems include U.S. Patent No. 3,758,763, disclosing a method of digitally processing AC signals utilizing a digital computer. Input AC power signal components are sampled and digitized at predetermined sampling times. A first sampled value is stored and then a second sampled value is obtained and the product of the two signals is derived to determine if the product has a negative sign, indicating that a zero crossing has occurred in the sampled signal. The disclosed system obtains frequencies, phase differences, powers and impedances of a power line network rather than measurement of electric energy parameters as in the present invention.

In U.S. Patent No. 3,569,785, a computer control system is disclosed for power system protective relaying, rather than for electric power measurement, in which the voltage and current components of an AC power line network are sampled and digitized and then applied to a computer for calculation of relaying control functions.

In measuring R.F. power, U.S. Patent No. 4,011,509 describes a digital measuring circuit that stores one digital power value and compares it to a measured power value to obtain a relative power value for expressing the measurement in decibels, not used in the subject invention.

Examples of electromechanical induction type watthour meter based metering packages having electric energy measurements produced that are closely related to the measurements produced in the present invention is the

magnetic tape metering package designated as types WRS, WRR and WRP. The aforementioned types of metering packages are available from the Westinghouse Electric Corporation, Meter and Instrument Transformer Division, Raleigh, North Carolina. The metering packages include a load survey type magnetic recorder, and a combination of a polyphase watthour meter, a Q-hour meter, and a V^2-hour or A^2-hour meter wherein each meter is equipped with an electronic pulse initiator for producing output pulses responsive to rotation of the meter movements. The metering packages are designed to monitor a variety of typical electric utility services for load research or billing applications. The electric energy parameters that can be obtained from the metering package data outputs include kilowatt-hours, kilowatt-demand, reactive KVA hours, volts-squared hours or ampere-squared hours to provide a complete analysis of the electric energy quantity measured and electric load profile for a given metering installation. The data can be used for load research or cost of service data, or for operational data relating to feeder loading, billing equipment sizing and other uses by an electric utility company.

Although the aforementioned metering packages are satisfactory in many applications, they are bulky, subject to limitations in the flexibility of the outputs and different energy measurements obtainable because of the use of a plurality of induction type meter devices.

The chief object of the present invention is to provide a digital processing and calculating AC electric energy measuring system to obviate the above problems with optimum use of digital circuit arrangements operating at optimum signal processing rates while obtaining desired reliability and accuracy.

With this object in view, the invention resides in a digital processing and calculating AC electric energy metering system for measuring an electric energy quantity occurring in an electric utility system, said metering system comprising: signal sample means including inputs and outputs, said inputs receiving input voltage and current signal components of said AC electric energy quantity, said output producing instantaneous values of the input voltage and current signals when said signal sample means is rendered to a sampling state; analog to digital converter means producing binary signal representations of each of the instantaneous signal values; sample timer means producing pulse signals at randomly varying intervals, said pulse signals initiating the sampling state of said signal sample means at randomly occurring sampling times; calculating means computing a quantity of the input signals from said binary signal representations thereof occurring at each sampling time; accumulator means receiving each quantity computed so as to store totalized values thereof, said totalized values being a time integral of the sums of each computed quantity received to produce measured values thereof; and output means responsive to the stored totalized values of said accumulator means to produce data output signals representing the measured values.

The invention will become more readily apparent from the following exemplary description, taken in connection with the accompanying drawings, wherein:

Figure 1 illustrates a block schematic diagram of the digital processing and calculating AC electric energy metering system of this invention;

Figures 2A and 2B illustrate an electrical circuit diagram of the system shown in Figure 1;

Figures 3A and 3B illustrate portions of a power supply circuit shown in Figure 1; and

Figure 4 is a pulse timing diagram illustrating control of the randomized signal sampling operation included in the system shown in Figures 2A and 2B.

The disclosure reveals a digital processing and calculating AC electric energy measuring system which includes a sequence controller and calculator subsystem for controlling the metering system operations in accordance with a predetermined stored program. An analog input of the system receives voltage and current signal components of an electric energy quantity supplied through an electric utility power line system to be measured by the metering system. Instantaneous sample values of the voltage and current signals are obtained at randomized sampling times to increase the accuracy of the metering system and to provide optimum utilization of the digital electronic circuits used. The instantaneous signal values are sequentially digitized at a single A/D converter. A readout display output produces numerical readings of a plurality of electric energy parameter measurements. A plurality of output pulse data signals

representing the measurements are produced to a pulse receiver device capable of transmitting the data pulses through a remote metering telemetry system or for being recorded in a magnetic recorder type of receiver device. Input and output (I/O) interfaces pass binary representations of the input signal samples, binary logic control and system monitoring system signals and data output signals between the system inputs and outputs and the sequence controller and calculator subsystem.

The system sequence controller and calculator subsystem includes a microprocessor subsystem having programmable read only memory (PROM) and random access memory (RAM). The programmed sequence of operation of the metering system and the system constants are stored in PROM. The stored system constants include limit values of the electric energy quantity to be measured so that upon the calculated values being incremented to the limit values, an output pulse data signal is produced representing a predetermined quantum of electric energy. RAM provides temporary storage of the system constants as well as temporary data and scratch pad or work space storage. A plurality of measurements of the electric energy quantity are calculated in a common calculation program subroutine digitally operating on the instantaneous signal values in binary representations. The system calculates Δ increments of kilowatt, Q and volts-squared. Incrementing each of these calculations produces the values of the time integral of the measured electric energy quantity. Demand interval pulses are received in the system to determine peak power usage or kilowatt demand by accumulating the maximum of the kilowatt-hour calculations occurring during demand intervals established between the demand interval pulses.

The accumulated values calculated are compared to the limit values, and when a limit value is reached, an output pulse data signal is initiated. The calculations are incremented in binary coded decimal (BCD) formats in BCD accumulator memory registers. The accumulated BCD binary signals are readily available for direct input to the readout display device to produce numerical readings, in real time, of the measured energy parameters. The BCD format of storage eleminates extra decoding circuitry required for binary to BCD code conversions for the display input.

A sample timer circuit utilizes the sequence controller and calculator subsystem clock source for producing sample interval timer (TIMR) pulses which initiate each randomized sampling interval. The TIMR pulses produce random time periods in the sampling intervals which vary about a predetermined average time period for the sampling intervals. TIMR pulses are sensed by the sequence controller and calculator subsystem. A random delay is produced between the beginning of each TIMR pulse and the time that a sample and hold circuit (HOLD) pulse is initiated at a sampling time whereupon an input signal amplitude is sampled and held for digitizing. A predetermined delay period is quantized in the programmed operation of the system controller and calculator subsystem, and the beginning of each TIMR pulse effects selection of one of a predetermined sequence of randomly occurring numbers which correspond in number to the predetermined number of delay period quanta. The randomized sampling intervals are produced so as to have the predetermined sampling interval average time after a substantial number of the random sampling intervals occur.

The metering system includes manual controls for selection of one of the measured parameters to be displayed, for resetting at the beginning of each kilowatt demand measuring period and for master resetting of the metering system.

A power supply for the metering system receives primary power from a conventional 120 VAC electric source to produce regulated DC voltages to the system solid state circuits. Monitoring of the regulated power supply output voltages and primary power outage detecting are provided in the power supply. Momentary power supply output carryover is provided so that when the sequence controller and calculator subsystem is of a microprocessor type, as in one preferred embodiment, the subsystem can be returned to a known position in the system program in preparation of an extended power outage condition. Battery carryover power is further provided so as to preserve RAM stored information including the system constants and the temporary data and scratch pad storage therein during an extended power outage condition.

Accordingly, it is a general feature of this invention to provide an electric energy metering system for producing binary representations of instantaneously

sampled values of input voltages and currents and to provide digital processing and calculating based on the binary representations to avoid undesired variations produced in analog signal processing measurement systems. A further general feature is to provide optimum utilization of digital processing and calculating circuits including randomized signal sampling to produce a desired accuracy in the measurements of different parameters of an AC electric energy quantity supplied through an electric utility system, and especially to provide measurements of the electric energy parameters for polyphase electric energy quantities.

Referring now to the drawings, and more particularly to Figure 1 there is shown a block schematic diagram of the digital processing and calculating AC electric energy metering system 20 made in accordance with the present invention. An analog input 22 receives input analog signals formed by the voltage components V_A, V_B, V_C and current components I_A, I_B, I_C included in three phases ØA, ØB, ØC of an AC electric energy supply network such as formed by a transmission or distribution network of an electric utility company. The analog inputs are assumed to be sinusoidal with a nominal power line frequency of sixty Hz. as typically supplied by a utility company. The component signals V_A B_B, V_C, I_A, I_B, and I_C are produced by conventional potential and current transformers, not shown, coupled to the transmission or distribution network, also not shown. The system 20 senses the voltage and current component signals and calculates a plurality of electric energy parameters of the polyphase electric energy quantity supplied to a customer's electrical loads and to be measured for billing, load survey and other analysis desired by an electric utility company.

A sequence controller and calculator subsystem 24 controls a programmed sequence of operation of the system 20 and includes a central processing unit (CPU) 26 of a microprocessor type described further hereinbelow. Address and data input and output lines of the CPU 26 are connected to read only memories (PROM) 27 and random access (read and write) memories (RAM) 28. A clock source 30 supplies clocking signals to both the CPU and to the system and also supplies a system logic control signal described further hereinbelow.

Input and output (I/O) interfaces 32 and 34, respectively, partially controlled by an associated address decoder 36, channel digital data and binary logic control signals into and out of the CPU 26 in response to addresses to the input and output interfaces 32 and 34 from the subsystem 24. An analog-to-digital (A/D) converter 38 supplies input digital data to the input interface 32 in the form of binary representations of instantaneous values of the six analog input signals. The analog input 22 simultaneously samples each of the six analog input signals and the instantaneous values are sequentially applied to the single A/D converter 38 for digitizing of all the signal samples. The sampling intervals are varied in a random fashion by control signal from the output interface 34. Upon completion of each digital conversion at the converter 38, the input interface 32 is addressed and applies the digitized data signals to the CPU 26.

Additional binary logic control inputs to the input interface 32 are applied from a manual control 40 including switch controls for selecting a desired one of the plural energy measurements to be displayed at a readout display 42. Numerals displayed at the readout display are produced by control signals from the output interface 34 for visually indicating the latest calculated value of the three phase electric energy quantity being measured. The system 20 measures three phase kilowatt-hours (KWH), kilowatt demand (KWD), Q-hour (QHR), and the volts-squared-hours (V^2H). The aforementioned electric energy measurements are typically used by electric utility companies for load research or cost of servicing data, operational information on feeder loading, billing equipment sizing and many other applications.

A demand interval control 44 is applied to the input interface 32 in the form of demand interval pulses which are understood by those skilled in the art as to be regular intervals of fifteen or thirty minutes, for example, used to determine the peak kilowatt demand during an established billing period. A sample timer 46 receives clock signals from the clock source 30 and includes a counter circuit arrangement described further hereinbelow for producing control signals to the input interface 32 used to establish the sampling times when the instantaneous values of the analog input signals are detected and held in the analog input 22. Signals from the output interface 34 are utilized to reset the sample timer 46 after

it has initiated a sampling interval. A further control signal from the sample timer 46 is applied to the clock 30 to indicate the failure of the sample timer to initiate another sampling interval and to restart the system by initially resetting the CPU 26 and causing the sequence controller and calculator subsystem 24 to re-initialize the system under the assumption that the correct program sequence has been lost and the system is required to recover by the failure to initiate a sampling interval.

A power supply 50 is connected to a primary source of 120 VAC at the input 52 of the power supply. The indicated plus and minus fifteen volts and plus five volts DC are produced to supply the required direct current voltages to the solid state circuit elements of the system 20. An indicator light 53 indicates that the input power is being received and the regulated direct current voltages are being supplied to the system 20. The system power light 53 is preferably mounted at a forward exposed location in a housing containing the system 20. The power supply 50 is heavily filtered to provide sufficient energy storage so that thirty to fifty milliseconds of carryover power supply output is furnished in case of a primary power input interruption before the power supply circuit will go out of regulation. As described further hereinbelow, the power supply circuit 50 supplies a signal to the input interface 32 indicating that there has been an interruption in the input power for longer than approximately twenty milliseconds. A battery 54 is included in the power supply circuit 50 and is normally charged by the input 52 and upon a power outage for longer than approximately twenty milliseconds, the battery 54 will supply plus five volts to RAM 28 to preserve the stored information therein during the power outage. The PROM 27 does not require the battery power carryover since they are of a permanently programmed type having permanent data and program storage. Upon loss of regulated power at the power supply circuit 50 and indication of such, a further signal is initiated at the output interface 34 and to the power supply 50. A control signal from the power supply to the clock source 30 resets the CPU 26 to stop system operation and carryover power is supplied from the battery 54 to the RAM 28.

Output signals 56 are produced from the output interface 34. A pulse output signal is produced for a predetermined quantum of a measured in parameter of an electric energy quantity. Accordingly, KWH, QHR and V^2H pulses are produced for reception at a pulse receiver 58. The output signals may be encoded for remote transmission or are capable of activating a three wire telemetry system, pulse totalizing devices, pulse recorders and the like. In the preferred embodiment of the system 20 the pulse receiver 58 includes a multichannel magnetic tape recorder which simultaneously records time pulses corresponding to the demand metering intervals. A test-pulse output 60 provides test pulses useful in calibration and testing of the system 20. Finally, the output interface 34 produces outputs to indicators 62, indicating the status of the system 20 in addition to the system power fail light 53 associated with the power supply circuit 50.

Description of Figures 2A and 2B

Referring now to Figures 2A and 2B wherein there is shown an electrical circuit diagram of the digital processing and calculating AC electric energy measuring system 20, the system 20 is shown in detail and corresponds to the general block diagram of Figure 1 described hereinabove in connection with the general description of this system. To aid in understanding of the Figures 2A and 2B, the binary logic control and data signals shown in Figure 2A are set forth in the following Tables I and II, describing the system interface inputs and system interface outputs, respectively. The program address, signal name and description are included in each of the tables to aid in the explanation and description of Figures 2A and 2B.

TABLE I

System Interface Inputs

Address	Name	Description
1E40	DB1	A/D Data Bit 1 (LSB)
2	DB2	A/D Data Bit 2
4	DB3	A/D Data Bit 3
6	DB4	A/D Data Bit 4
8	DB5	A/D Data Bit 5
A	DB6	A/D Data Bit 6
C	DB7	A/D Data Bit 7

TABLE I (contd.)
System Interface Inputs

Address	Name	Description
E	DB8	A/D Data Bit 8
1E50	DB9	A/D Data Bit 9
2	DB10	A/D Data Bit 10
4	DB11	A/D Data Bit 11
6	SIGN	A/D Sign Data Bit
8	STAT	A/D Status
A	PWRF	Primary Power OFF
C	$\overline{\text{DINT}}$	Demand Interval Pulse
E	$\overline{\text{RESET}}$	Master Reset Switch
1E60	$\overline{\text{DTST}}$	Display Test Switch
2	$\overline{\text{DVSQ}}$	Display Volts-Squared Hour Switch
4	$\overline{\text{DQHR}}$	Display Q-Hour Switch
6	$\overline{\text{DDEM}}$	Display KWH Demand Switch
8	$\overline{\text{RDEM}}$	Demand Reset Switch
A	$\overline{\text{RBEA}}$	Battery Carryover Error Reset Switch
C	$\overline{\text{DKWH}}$	Display KWH Switch
E	TIMR	Sample Interval Timer Pulse

TABLE II
System Interface Outputs

Address	Name	Description
E0 0	SCON	Start MUX Conversion
2	ADR0	MUX Address Bit
4	ADR1	MUX Address Bit
6	ADR2	MUX Address Bit
8	ZCONT	Current Amplitude Input Control
A	HOLD	Sample and Hold Control
C	———	
E	———	
E1 0	DSA	Digit Segment A
2	DSB	Digit Segment B
4	DSC	Digit Segment C
6	DSD	Digit Segment D
8	DSE	Digit Segment E
A	DSF	Digit Segment F
C	DSG	Digit Segment G
E	TLED	Test Pulse Ind. Output
E2 0	DS8	Digit Select 8
2	DS7	Digit Select 7
4	DS6	Digit Select 6
6	DS5	Digit Select 5
8	DS4	Digit Select 4
A	DS3	Digit Select 3
C	DS2	Digit Select 2
E	DS1	Digit Select 1
E3 0	RINT	Sample Timer Reset
2	KWHP	KWH Output Pulse
4	QHRP	QHR Output Pulse
6	VSQP	Volts-Squared Output Pulse
8	BCF	Battery Carryover Failure
A	STOP	Reset CPU
C	———	
E	$\overline{\text{TSTP}}$	Test-Pulse Pulse Output

The analog input 22 includes six sampled and hold (S&H) circuits 66, 67, 68 and 69, 70 and 71. Each of the circuits is a sample and hold circuit type AD 583 available from Analog Devices Inc., Norwood, MA 02062. The three phase voltage signal component V_A, V_B, and V_C of a power line network being monitored are applied to the analog signal inputs of the circuit 66, 67 and 68, respectively.

The S&H circuit output signal voltages all have a nominal ± five voltage range in one preferred embodiment. The HOLD binary logic control signal is applied to each of the sample and hold circuits 66, 67, 68, 69, 70 and 71. The logic one places the sample and hold circuits in the hold condition to maintain the sampled instantaneous value of the input signals at the outputs. The sampling time occurs at the time of the zero to one logic state transition of the HOLD signal. The logic zero of the HOLD signal permits the sample and hold circuit outputs to track or follow the circuit inputs. The three phase current signal components I_A, I_B and I_C are conditioned to have a zero to ten ampere range at the inputs of an analog multiplexer 73. The multiplexer is a triple 2 Channel Analog multiplexer type 14053 available from the CMOS Division, Motorola Semiconductor Products Inc. The current analog input signals pass through the analog multiplexer 73 when the ZCONT binary logic control signal has a logic one state to be applied to the analog inputs of the sample and hold circuits 69, 70 and 71. When ZCONT has a logic zero, the three input current values are held at the analog ground value or a zero reference level to calibrate and adjust for any drift or variations in the sensing of the sensed current values. Accordingly, the instantaneous values of the three current inputs are developed at the respective sample and hold circuit outputs, as described hereinabove for the voltage sample and hold circuits. It is to be understood that the signal values of signals V_A, V_B, V_C, I_A, I_B and I_C are developed with respect to the analog signal ground and have a predetermined proportional relationship to the voltage and current components of the three phase electric energy quantity to be measured.

The sample and hold circuits designated 66 through 71 include a 0.01 μf capacitor temporary storage circuit controlled by the HOLD input signals. These HOLD signals are produced in response to the sample timer 46 under control of the CPU 26, as described further hereinbelow to establish and define the sampling intervals at which time the instantaneous amplitudes of the analog input signals are detected for digitizing. The instananeous values of the analog signals at the time of the HOLD signal is held on the associated capacitor, not shown, while each sampled value is sequentially applied to the A/D converter 38.

An analog multiplexer (MUX) 76 receives each of the sample and hold circuit analog outputs and is provided by an eight Channel Analog Multiplexer type 14051 available from the aforementioned Motorola Semiconductor Products Inc. The instantaneous sampled signal values are each sequentially applied to the multiplexer output line 78 in response to a three bit binary address input applied by the MUX ADR address bus including the address signals ADR0, ADR1 and ADR2 from interface 34. The aforementioned MUX ADR address bits have a positive true state. Each of six different coded addresses connects a different one of the multiplexer inputs and therefore a different one of the sample and hold circuit outputs to the multiplexer output 78.

The A/D converter 38 is preferably formed by a 12-bit A to D Converter type 572 available from the aforementioned Analog Devices Inc. The converter 38 digitizes the instantaneous signal values applied to the converter input from the multiplexer output line 78. The binary coded A/D converter output is formed by the twelve data bits designated DB1 through DB11 plus SIGN bit shown in Table I. The converter is arranged so that eleven bit signals are representative of one of 2,048 quantizing bit levels of the analog input instantaneous values. The twelfth SIGN bit has a zero logic indicating positive data and a one logic state representing a negative data output to indicate the positive and negative phases at the analog input signals.

The converter 38 further includes a start conversion SCON control input and begins digitizing the level of the received input analog signal when SCON has a high true logic one level. The converter circuit begins digitizing and initiates a STAT signal having a logic one to logic zero transition indicating the completion of the digital conversion.

Operation of the analog multiplexer circuit 73 at the current inputs includes a signal drift compensation feature. Errors in the sensed levels of the analog current signals are capable of producing errors in the computation of the energy parameters in some applications of the system of this invention. As is known, the input current signal values will change with changes in the supplied electric load while the input voltage signals will remain relatively constant. Accordingly, when a ZCONT signal is present, all of the current signal inputs are tied to the analog reference zero level. These three current signals are sequentially passed through the MUX 76 to the converter 38 where the values are digitized. If the system

variations produce other than zero binary outputs at the data outputs of the converter 38, then it is known that the variations are producing errors in the digitized current signals. These variations from the zero reference establish an error offset value which is stored and used by the sequence controller and calculator subsystem 24 to correct the sensed current signals converted thereafter when the ZCONT releases the multiplexer 73.

The sequence controller and calculator subsystem 24 is now described before describing the remaining portions of the system 20 shown in Figures 2A and 2B. The subsystem 24 is formed by a microprocessor based system wherein the CPU 26 includes a type TMS 9900 sixteen bit microprocessor available from the Semiconductor Group, Texas Instruments Inc., Dallas, Texas 75222. The CPU 26, clock source 30 and PROM and RAM memories 27 and 28 form a TMS 9900 microprocessor subsystem described in the TMS 9900 Microprocessor Data Manual, 1976; the Minimum System Design TMS 9900 16-bit Microprocessor Application Report, Bulletin CA-184; and the Model 990 Computer/TMS 9900 Microprocessor Assembly Language Programmer's Guide, available from the aforementioned Texas Instruments Inc. The general architecture of the microprocessor CPU 26 is shown in Figure 2B as generally utilized in the present invention and will not be described herein since the aforementioned publications disclose the use and operation of the microprocessor subsystem as it is available for use in the system 20.

The subsystem 24 includes, besides the microprocessor CPU 26, a clock source 30 formed by a type SN74LS362 clock generator available from the Texas Instruments Inc. including a forty-eight MHz crystal controlled oscillator providing four phase clock signals, Ø1, Ø2, Ø3, and Ø4 clock signals to the CPU as shown in Figure 2B. As described in the aforementioned publications, the clock source 30 has associated therewith an RC network formed by the resistor 82 and capacitor 83. The junction 84 between the resistor and capacitor is connected to the D input of a Schmitt-triggered logic circuit in the clock source 30 with the other terminal of the capacitor connected to the system ground. The other end of the resistor 82 connected to positive five volts. When the clock D input is brought low, a power-on reset is applied to the CPU microprocessor pin six. The Q logic output at the clock source is labeled $\overline{\text{RESTART}}$ in Figure 2B which has a low true logic zero state effective to synchronize the CPU and to reset and initialize the CPU 26 at the power-turn reset. The line designated $\overline{\text{RESTART}}$ is the same as described as $\overline{\text{RESET}}$ in the aforementioned TMS 9900 Microprocessor pin functions to produce the CPU reset as described in the aforementioned publications.

The PROM 27 is formed by four separate type SN 745472 bipolar 512x8 bit PROMs, also available from the aforementioned Texas Instruments Inc., for permanent data and program storage. The four circuits in PROM 27 are designated by the numerals 27-1, 27-2, 27-3 and 27-4 in Figure 2B. The PROM 27 provides for up to 1,024x16 bit words of permanently stored programmable memory. The RAM 28 includes an array of type TMS 4042-CMOS RAM's designated by the numerals 28-1, 28-2, 28-3 and 28-4. The circuits in RAM are organized in a 256x16 bit pattern to provide temporary data storage and work space register areas.

The memory interface of the CPU 26 inlcudes an address bus 89 which outputs address bits A3 through A14 (LSB) in which the bits A6 to A14 are applied to the four PROM circuits 27-1 through 27-4 in parallel. The parallel address arrangement permits the selection of one of the five hundred twelve words in each PROM memory circuit to be accessed. The address bits A4 and A5 are decoded by the decoder logic including the NAND gates 91, 92 and 93 and the inverter gates 94 and 95 in which the NAND gate outputs are connected to the pair of PROM circuits 27-1, and 27-2, 27-3 and 27-4 and RAM circuits 28-1 and 28-2, and 28-3 and 28-4, as shown in Figure 2B. The address bits A4 and A5 are decoded by the memory select logic to simplify the addressing to the PROM 27 and RAM 28. A $\overline{\text{WE}}$ (write enable) is applied to each of the RAM circuits on line 97 and DBIN (CPU data bus in) is applied through an inverter circuit 99 in line 101 to provide a $\overline{\text{DBIN}}$ signal also to each of the RAM circuits 28-1 through 28-4.

The CPU 26 further includes a data bus 102 including the data bits D0 through D15 (LSB) which comprise a bidirectional three state data bus. The bus 102 transfers memory data to (when writing) and from (when reading) the PROM 27 and RAM 28. The data bits D8 through D15 are connected with the PROM memory circuits 27-1 and 27-3 and the remaining eight data bits D0 through D7 are connected with PROM circuits 27-2 and 27-4. Four data bits D12 through D15

are connected with RAM circuit 28-1, data bits D8 through D11 with RAM circuit 28-2, data bits D4 through D7 with RAM circuit 28-3 and the remaining four data bits D0 through D3 are connected with the RAM circuit 28-4.

Address bits are also applied from the CPU 26 externally of the subsystem 24 in address buses 105 and 106. The bus 105 includes address bits A7 through A11 and is outputted to the decoder 36. The bus 106 includes the three address bits A12, A13 and A14 and are applied through a bus driver 107 being of a type SN 8216. The address bus 106 from the bus driver 107 is applied to the input interface 32 and the output interface 34 in Figure 2A for purposes which will be described further hereinbelow.

The remaining outputs from the CPU 26 include the three microprocessor dedicated signals CRUCLK (CRU clock) provided on the line 110, the signal CRUOUT (CRU data out) provided on the line 112, and the signal CRUIN (CRU data in) provided on the line 114. Data is applied on the line 114 to the CPU 26 in a serial bit fashion and the CPU tests an input bit by placing the bit address on the address bus and then testing CRUIN to receive input data from the input interface 32. The CPU sets or resets an output bit by placing the bit address on the address bus, the output data bit on CRUOUT, and a clock pulse on CRUCLK. The data on the CRUOUT line 112 appears as serial data and is sampled by the output interface 34 when the CRUCLK signal is in a high or logic one state. The CRUOUT line 112 passes through the bus driver 107 and is applied to the output interface 34 and the CRUCLK line 110 passes through an inverter 116 to the output interface 34 to clock the data on line 112 into the output interface 34 as described more fully hereinbelow.

The sample timer circuit 46, shown in Figure 2B is now described since it is controlled by one of the TTL compatible clock pulses produced on line 116 at a 3.0 MHz. from the clock source 30. The sampler timer circuit 46 produces the TIMR signal on the timer output line 117 to control the randomized sampling intervals in the sample and hold (HOLD) signals applied to the analog input 22 as described in the description of Figure 4. A first $\overline{\text{SYSINT}}$ signal is produced on a second timer output line 118. The $\overline{\text{SYSINT}}$ signal has a true low logic condition as connected to the D logic input of the clock source 30 to initiate a $\overline{\text{RESTART}}$ from the clock source 30 when the normal time for the TIMR signal to occur has passed without its occurrence. The $\overline{\text{SYSINT}}$ signal is provided under the assumption that the correct program sequence has been lost since the TIMR signal did not occur and the subsystem 24 is required to recover.

The sample timer circuit 46 includes pulse counter arrangement including a divide-by-sixteen counter type SN. 74LS93, available from the aforementioned Texas Instruments Inc., designated by the numeral 121 receiving at a clock input the clock signals on line 116. The two outputs to pad connections 122 provide divide-by-four and divide-by-eight outputs and are brought out to the pad connections where they are selected by a jumper for applying alternative output pulse rates to a counter 124 formed by a fourteen stage binary counter type CD 4020 counter. The clock input of the counter 124 is divided by factors of 512, 1024 and 4096 at the three counter outputs 119-1, 119-2 and 119-3 and the first two outputs are made available at pad connections 126 having associated jumpers as shown. Selection of one or a combination of two of the available outputs of the counter 124 is made for input through the two inputs of NAND gate 127. A series of negative going TIMR pulses are produced on the line 117 at the output of the gate 127. The pulse periods can be varied from approximately 1.5 to 3.0 milliseconds by alternate connections at the pad connections 122 and 126. The TIMR pulse signal is applied through the interface 32 to the subsystem 24 to signal the beginning of a sampling interval. The alternate connections at the counters 121 and 124 provide for variations in the time period of the sampling intervals formed between consecutive sampling times.

A resetting control input to the sample timer 46 is connected to line 128 and includes a NOR gate 129 having both inputs connected to the $\overline{\text{RESTART}}$ line 128 so as to invert the logic of the line 128. A second NOR gate 131 receives one input from the gate 129 and a second input from the RINT signal line 133. The output of the gate 131 is applied through an inverter 134 to the reset inputs of the counters 121 and 124. When the subsystem 24 detects the beginning of a sampling interval, the RINT signal goes high at the output of the output interface 34 to reset the timer counter arrangement to zero. The lowest output of counter 124 is applied to both inputs of a NOR gate 136 having an output connected through the diode 137 to the line 118 to produce the $\overline{\text{SYSINT}}$ signal to the clock input. So long as the

counter is regularly reset by the RINT signal, the output of the NOR gate 136 will remain high. The period of the pulses applied to the gate 136 from the lowest output shown for the counter 124 is, as in one preferred embodiment, approximately twice the time between the periods of the TIMR pulses at the output of the NAND gate 127 so that if a TIMR signal is not produced for a time approximately twice that taken for normally providing the signal on line 117, the $\overline{\text{SYSINT}}$ is produced at the output of gate 136. This produces a $\overline{\text{RESTART}}$ signal which resets the CPU 26. Since the $\overline{\text{RESTART}}$ signal is applied to the NOR gate 128, the sample timer is also reset when the $\overline{\text{SYSINT}}$ is initiated by the gate 136, and in turn is released when the $\overline{\text{RESTART}}$ is applied to the sample timer 46.

The input and output interfaces 32 and 34 and the associated address decoder 36, providing an I/O interface chip addressing operation, is now described as shown in Figure 2A. The interface 32 includes three eight line to one line tri-state octal multiplexers designated by the numerals 140, 142 and 144. The octal multiplexers are of a type SN 74LS251, available from the aforementioned Texas Instruments Inc. The single output of the octal multiplexers 140, 142 and 144 are connected in parallel to the CPU data input line 114. Since the multiplexers each have eight inputs, the twenty four system input interface signals can be applied to the multiplexer inputs which define the input ports of the I/O interfaces 32 and 34 for input to the CPU input CRUIN. The CPU address bits A12, A13, and A14 are applied in parallel to the multiplexers 140, 142 and 144 from the bus 106. An enabling input of each of the multiplexers receives the chip select signals SEL4, SEL5 and SEL6, respectively, from the address decoder 36. One of the three circuit chips defining the multiplexers 140, 142 and 144 is enabled by one of the select signals SEL4, SEL5, and SEL6 so that the three bit address effects output of one of the eight system inputs to the data line 114.

The output interface 34 includes four addressable latches 146, 148, 150 and 152. The addressable latches are a type SN 74LS259 available from the aforementioned Texas Instruments, Inc. Three bit address inputs of the latches are connected in parallel to the bus 106 which applies the CPU address bits A12, A13 and A14 from the driver 107. The CPU data output line 112 applies the data out signals CRUOUT to the data inputs of the latches in the output interface 34. Reset inputs of the latches 146 through 152 are connected to the line 153 having the $\overline{\text{RESET}}$ signal which is developed when the system is manually reset, as described further hereinbelow. Enabling inputs of the latches 146, 148, 150 and 152 receive the chip select/clock signals SEL0, SEL1, SEL2 and SEL3 from the address decoder 36. The eight outputs from each of the four latches define output ports of the I/O interfaces 32 and 34 of the system 20 and provide the system output signals listed and described in the aforementioned Table II and shown at the outputs of the interface 34 in Figure 2A. When one of the SEL0, SEL1, SEL2 or SEL3 goes low or to a logic zero state, the corresponding addressable latch circuit chip is enabled and CPU data output of the line 112 passes into the selected latch and out of the output port designated by the three bit signal of the bus 106 when the latch select clock signals SEL0-3 are brought low in response to the CPU clock signals applied from the line 110 to the decoder 36. As noted hereinbelow, data at the CPU CRUOUT output should be sampled by the external interface logic when the CRUCLK goes high. The CRUCLK high logic state is inverted and appears as a corresponding low state at the SEL0 through 3 signals, as described further in connection with the decoder 36.

The address decoder 36 includes a decoder circuit 154 provided by a type SN 74LS138, available from the aforementioned Texas Instruments Inc. The decoder circuit 154 has eight outputs, seven of which are used and include the chip select signals SEL4, SEL5 and SEL6 applied to the octal multiplexers 140, 142 and 144, as described hereinabove. The decoder circuit further includes two NAND circuits 155 and 156 receiving address bits A3, A4, A5 and A6 from the bus 105 as shown in Figure 2A. The output of the NAND gates are applied to a NOR circuit 157 an output applied to the enable input of the decoder circuit 154. The address bits A7, A8, A9, A10 and A11 are applied to the circuit 154. Four of the outputs of the circuit 154 are applied to one input of the OR gates 158-1, 158-2, 158-3 and 158-4, respectively. An inverter is connected in series with the line 110 to apply the inverted CRUCLK signal to the second inputs of the OR gates 158-1 through 158-4. The decoder circuit 36 output associated with a latch circuit chip that is selected goes to the true low state so that the clock signals are applied by going to the low true state at the enable inputs of the latch circuits to properly clock the

data from the CPU 26 as noted hereinabove. The addresses A3 through A6 which are decoded and applied to the enabling input of the decoder circuit 154 assure that the addresses beginning with 1E0, 1E1, 1E2, and 1E3 must be present before the decoder circuit 154 is enabled since these are the most significant part of the system output addresses listed in Table II.

The input portion of the metering system 20 will now be described with regard to the inputs applied to the input interface 32. The A/D converter outputs include the data bits DB1 through DB8 being applied to the eight inputs of the octal multiplexer 140. The data bits DB9, DB10, and DB11 along with the twelfth converter output bit which is designated SIGN are applied to four of the inputs of the octal multiplexer 142. A/D data bits DB1 through DB11 and the SIGN are applied serially to the data input line 114 under control of the decoder 36 and addresses occurring on the address bus 106 to input the digitized signal values in binary representations.

The manual control 40 of Figure 1 includes a display selector 159, a demand reset switch 160, a power error lamp reset switch 161, and a master reset switch 162. The display selector 159 is a six position switch having a movable switch arm connecting the switch output terminals with the system ground. One of the calculated parameters of the electric energy quantity is displayed at the readout display 42 by positioning the switch arm of the switch selector 159. The output terminals of the selector 159 are designated KWH for displaying kilowatt-hours, KWD for displaying kilowatt demand, QH for displaying Q-hours and V^2H for displaying volts-squared-hours and TEST to display a test output at the readout display 42. Accordingly, the logic control signals $\overline{\text{DKWH}}$, $\overline{\text{DDEM}}$, $\overline{\text{DQHR}}$, $\overline{\text{DVSQ}}$ and $\overline{\text{DTST}}$ are applied from the corresponding switch outputs to six of the inputs of the octal multiplexer 144. The aforementioned display selector logic control signals have a true low logic state to signal the system the desired parameter value which is to be displayed at the readout display 42.

The switches 160, 161 and 162 are a single throw, single pole or pushbutton type having one terminal of each connected to the system ground as indicated in the Figure 2A. The demand reset switch 160 effects an $\overline{\text{REDEM}}$ signal to an input of the multiplexer 140 to reset the demand metering period of the metering system 20. This occurs generally at the end of a regular billing period such as once each month, corresponds to resetting to zero the maximum indicating pointer of an electrical mechanical demand meter. The switch 161 is effective to apply the control logic signal $\overline{\text{RBEA}}$ having a true low signal when the switch is closed to reset the power fail error lamp 163 described further hereinbelow. Finally, the master reset switch 162 produces a $\overline{\text{RESET}}$ to the multiplexer 142 when the switch is closed. The true low state of the $\overline{\text{RESET}}$ signal is effective as to reset the entire metering system 20 to zero including resetting of the addressable latches in the output interface 34 as described hereinabove.

The eighth input to the octal multiplexer 144 includes the TIMR signal on line 117 from the sample timer circuit 46 described hereinabove. The status output of the A/D converter 38 provides a STAT status input signal to the octal multiplexer 142. The logic one state of the STAT signal indicates data conversion is not complete and the transition to the logic zero state indicates that the data conversion has been completed and is ready for the A/D data outputs to be processed into the system. The DINT signal is developed in the pulse receiver 58 formed by a tape recorder as shown in Figure 2A. The demand interval pulse DINT has a low true logic state and is applied at regular demand intervals such as for example every 15 minutes. Finally, the multiplexer 142 receives the PWRF power failure control signal generated in the power supply 50 as described hereinbelow. A low true state of the PWRF signal indicates that the power supply input power at intervals 52 has been lost.

The output portion of the system 20 is now described initially referring to the system output ports formed by the outputs of the four latches 146, 148, 150 and 152 included in the output interface 34. The system output signals are listed in Table II and are generally included in the three output functions. The output functions include servicing of the eight digit numerical readouts of the readout display 42 and the display lights of the indicators section 62, and outputting the output signals corresponding to the measured parameters calculated by the system as well as a test-pulse signal output, and finally providing the system control signals produced in the sequence controller and calculator subsystem 24. Seven outputs of the latch 146 produce the digit segment select signals DSA, DSB,

DSC, DSD, DSE, DSF, and DSG through drivers 165 to the numerical readout display 42. The eight digits of display are each formed by seven segment light elements provided in the numerical readout display 42 which comprises two type DL-34M display units available from Litronix, Inc. The seven segments of each of the eight digits of the display are turned on by a logic zero state of the display segment select signals DSA—DSG. The eight outputs of the latch 148 provide the digit select signals DS1, DS2, DS3, DS4, DS5, DS6, DS7 and DS8 which are applied to circuit drivers 166 to the digit select inputs of the readout display 42.

The indicator section 62 includes the aforementioned power fail error status light 163 and a test pulse light 168 and both are formed by light emitting diodes (LEDs) having the anodes connected to a source of positive voltage as indicated. A TLED control signal from the eighth output of the latch 146 activates the light 168 through the circuit drivers 169 when the TLED has a logic one state. The logic signal BCF from the latch 150 activates the power fail error light 163 through the circuit drivers 169 when the BCF signal has a logic one state. The light 163 indicates the status that the system sensed a loss of memory in RAM 28, such loss being assumed to be caused by loss of battery carryover power applied from the power supply 50 and that the memory storage in the RAM 28 needed to be reloaded from PROM 27.

The system output measuring information signals are developed by the KWHP, QHRP and VSQP signals produced from the latch 150 and through circuit drivers 170 having outputs connected to the KWH, the QHR and V^2H output signal terminals shown in Figure 2A. The output terminals produce corresponding kilowatt-hour, Q-hours and volts-squared hours with the pulses having transitions between opposite voltage polarities so that the recording pulse currents pass in opposite directions through the recording heads H1, H2 and H3 of recorder type pulse receiver 58 connected to the aforementioned three output signal terminals. The magnetic recording heads provided in a magnetic recorder type pulse receiver 58 can be as disclosed in U.S. Patent Nos. 3,943,498; 2,470,470; 3,538,406; 3,913,129; and 3,913,130, and assigned to the assignee of this invention. As described in the aforementioned patents, a demand interval recording head, such as recording head H4 is provided in this type of recorder and is energized from a source of interval pulses 44 which may include regularly time spaced contact closures defining demand intervals which occur, for example, at fifteen minute intervals as noted hereinabove. Besides energizing the recording head H4, the source of interval pulses produces the DINT logic signal having a low true logic state, such as occurs for example with each of the aforementioned contact closures developing the demand interval pulses in the recorder type pulse receiver 58. Pulses are recorded on the recording tape medium 174 as described in the aforementioned patents. A test-pulse output jack 60 shown in Figure 2A produces test-pulses in response to a TSTP signal from the output of latch 150. The test-pulse output is monitored for checking and calibration of the metering system 20.

Referring now to the remaining system output signals, the RINT signal is produced from the latch 150 and is applied to the line 133 which is connected to the NOR gate 131 in the sample timer circuit 46 and the signal RINT has a logic one or high true reset state to reset the sample timer counter arrangement following a TIMR signal. A STOP signal is produced from an output of the latch 150 and drivers 169 and is applied to the power supply 50 to initiate a $\overline{\text{SYSINT}}$ to reset the CPU 26, as described further hereinbelow in connection with the description of the power supply 50.

The output interface latch 152 produces the SCON signal to the A/D converter 38 to start the data conversion process therein. The MUX ADR address bits ADR0, ADR1 and ADR2 of the MUX ADR bus are also provided at three outputs of the latch 152. The ZCONT is applied from latch 152 to the input current analog multiplexer 73. The logic one state of ZCONT allows the current input signals I_A, I_B and I_C to pass through to the sample and hold circuits 69, 70 and 71. The logic zero state of ZCONT grounds the current inputs of the sample and hold circuits 69, 70 and 71. The HOLD signal from the latch 152 is applied simultaneously to the six sample and hold circuits 66, 67, 68, 69, 70 and 71 to effect a sampling signal with the logic one of the signal forming the hold operation and the logic zero state allowing the sample and hold circuits to track or cause the analog outputs to follow the analog inputs directly.

Description of the Power Supply 50 and Figures 3A and 3B

Referring now to the power supply 50 generally shown in Figure 1 wherein is

shown the +5 VDC and ±15 VDC outputs that are generated using standard diode bridges and solid state regulators connected to the primary input 52 receiving the 120 VAC 60 Hz. primary power. Heavy filtering using conventional techniques, including capacitors provides for sufficient energy storage to provide a limit of between thirty to fifty milliseconds of carryover output power in case of a momentary primary power interruption at the input 52. Upon sustained loss of the primary power, the battery 54 is capable of furnishing the +5 VDC output which is used exclusively to supply the RAM section 28 and retain the memory storage therein during a power outage. Battery carryover circuit arrangements suitable for use in the power supply 50 are disclosed in the above-identified U.S. patents relating to a description of the magnetic recorder type pulse receiver 58.

In Figures 3A and 3B, two power supply status monitoring circuits are illustrated in the electrical schematic circuit diagrams therein. In Figure 3A, operational amplifier comparators 180 and 181 are provided, each forming one-half of a type SN 747. The three DC output voltages of the power supply 50 are summed and applied at both inverting inputs 182 and 183 of the OP AMPs and the outputs of the OP AMPs are applied through resistors 184 and 185 to the base biasing circuits of an NPN transistor 186 and a PNP transistor 187, respectively. The emitter-collector circuits of the transistors are connected in series with an LED forming the indicator light 53 also shown in Figure 1. The +5 output voltage is applied across a resistance voltage divider including the series of resistors 188 and 189. A second resistance voltage divider including a series of resistors 198 and 199 is connected across the +15 and −15 voltages. The commonly connected junctions of the voltage dividers produce a three volt reference voltage when the output voltages are properly regulated. +15 volts is applied across a resistance voltage divider including resistors 191, 192 and 193, the junction of the resistors 191 and 192 developing a +4 volt reference voltage at the non-inverting input 194 of the OP AMP 180. The junction between the resistors 192 and 193 applies a +2 volt reference voltage at the non-inverting input 195 of the OP AMP 181. The +3 reference voltage at the junction of the resistors 188 and 189 is applied through the equal valued resistors 196 and 197 and to the inverting inputs 182 and 183, respectively. The transistors 186 and 187 are held in a conductive state so long as the proper regulated DC voltage is being supplied from the power supply 50 so that the +3 reference voltage does not vary beyond the +2 and +4 comparator voltages. The indicator light 53 is illuminated while both transistors 186 and 187 are conducting.

Figure 3B shows the power supply monitoring circuit for monitoring the loss of the 120 VAC primary power to the power supply. The inputs 200 are connected to the 120 VAC input and the input voltage is rectified and conditioned by the diodes 201 and 202 and series resistor 203. The rectifier circuit is connected to an optical coupler of a type MCT-2 available from Monsanto Corporation and including an LED connected to the input half wave rectifier circuit. A photoresponsive transistor provides the output of the optical coupler 205 which is applied across a capacitor 206 connected in a serial connection with the resistor 207 and to a +5 volt reference. Resistor 207 charges capacitor 206 from the +5V source during the half cycle when the coupler 205 is not conducting. The capacitor 206 discharges through the coupler phototransistor when it is conducting during the other half cycle of the primary power. The capacitor voltage is applied through resistor 208 to an OP AMP comparator 209, being of a type SN 741. The resistor 208 is connected to the inverting input of the OP AMP comparator 209 and a +3 voltage source, available at the +3 volt reference in Figure 3A, is connected to a resistor 210 to the non-inverting input. The OP AMP circuit 209 is connected as shown including the resistor 211 and diode 212 connected between the output and the non-inverting input provides a comparator circuit operation. Rectified half cycles of 60 Hz. are applied to the optical coupler 205 and the charging and discharging voltages on the capacitor 206 remain below the +3 volt reference. When the primary 120 VAC is stopped or is interrupted, the voltage on the capacitor 206 will rise above the +3 value in approximately twenty milliseconds after the last half wave through the coupler 205. This causes the comparator 209 output to switch to a value below the logic ground or zero by the amount of the voltage drop across the diode 212.

The output of the OP AMP comparator 209 produces the PWRF signal and the output is also applied to the one input of a gate 214. A second input to the gate 214 is the STOP signal from the output interface 34. The PWRF logic signal from the comparator 209 is applied to the input interface 32. The PWRF signal has a

low true value occurring when the primary 120 VAC interruption occurs beyond twenty milliseconds. The system 20 senses the presence of the PWRF signal and in turn initiates the STOP signal at the interface 34 which has a high true value, as noted hereinabove. The low true logic zero state of PWRF and high true logic one state of STOP produce a gate 214 output having a low true logic state, producing the $\overline{\text{SYSINT}}$ signal which is applied to the D input of the clock source 30. This in turn initiates the $\overline{\text{RESTART}}$ signal to reset the CPU 26. The momentary carryover feature of at least 30 to 50 milliseconds due to the high output filtering of the power supply 50 assures that the CPU 26 has time to initiate its reset before the momentary power carryover is lost to the system 20 from the power supply 50. If primary power returns before the momentary power carryover expires, the $\overline{\text{SYSINT}}$ goes high to a logic one state and the $\overline{\text{RESTART}}$ is released so that the CPU 26 can return to operation. In brief summary, a primary power outage produces the PWRF signal to initiate the STOP signal and in turn the $\overline{\text{SYSINT}}$ and $\overline{\text{RESTART}}$ signals and bring the CPU 26 to the known reset condition which is followed by an IDLE routine. This enables a restart of the CPU 26 to go through its internally programmed initializing process and restart in synchronized operation. If power to the CPU 26 is lost without returning to the CPU reset condition, the system would not be able to start after a power outage since the routine sequence would be interrupted and out of order.

Description of the System Operation

The system 20 is operated in a predetermined programmed sequence of operation for measuring an electric energy quantity supplied or consumed in a polyphase power line network. The system performs asynchronous or randomized instantaneous sampling of the voltage and current signal components of the polyphase electric energy quantity, performs sequential digitizing of the instantaneous sampled values, performs real-time calculations of the electric energy quantity including kilowatt-hours, kilowatt demand, Q-hours and the volts-squared-hours, produces output pulse data signals representing the said calculations, continuously updates accumulated values in a BCD binary code format of the calculations for visual numerical display of the real time values, and monitors the sequence of the system operation and protects the system from erroneous operations in the event of loss of the system power supply. Since the sequence controller and calculator subsystem 24 is a microcomputer or microprocessor based subsystem, a programmed sequence of instructions is required for its operation. The aforementioned Texas Instruments Inc. publications directed to the TMS 9900M microprocessor are to be referred to for detailed explanations of the basic operating characteristics and program instructions for the internal microprocessor operation. The subsystem 24 has a configuration generally corresponding to the TMS 9900 system described in the aforementioned Application Report Bulletin CA-184, except for the details of the subsystem 24, described hereinabove.

The program of instructions for the system operation is permanently stored in the ROM 27. The known and prescribed instructions for the microprocessor based subsystem 24 are stored in the PROM 27 in accordance with the manufacturer's directions and instructions. The sequence of operation and program is not described herein for specific operations of the system 20 of this invention for purposes of simplifying this description and because detailed information is available, as noted hereinabove, for the microprocessor. While the PROM 27 is permanently programmed, the RAM 28 provides termporary read/write storage for thirty-eight system constants which are permanently stored in the PROM, for other data and for scratch pad and workspace use.

With reference to Fig. 4, as related to the system of Figs. 2A and 2B, the pulse timing diagram shows that after a TIMR signal is initiated by the system the HOLD signal is produced to initiate the sampling time instant. In the randomized or asynchronized sampling technique used herein, the time at which the HOLD signal is produced relative to the occurrence of the TIMR signal is randomly delayed. Randomized sampling is to be understood to mean the occurrence of sampling at unequal sampling intervals that are independent of the phase, frequency and harmonics of the input signals and therefore characterized as asynchronous.

Randomization of a delay routine following the TIMR signal is accomplished by utilizing a source of randomly occurring data within the sequence controller and calculator subsystem 24. For example, following each sampling time,

calculations of the electric energy quantities occur which produce random binary numbers. In the present technique, the four least significant bits from the contents of the KWH RAM accumulator register address are treated as three bit magnitude numbers and a sign bit so as to form a sequence of 16 four bit data having a zero mean value, represented by the 8th in the sequence of four bit data. By providing an address for each of fifteen consecutive no operation (referred to subsequently as NOP, as conventionally used to define time delay steps for a microprocessor) microprocessor instructions which is derived from the four bit data, the microprocessor CPU 26 can alter the time between the beginning of a TIMR signal and the time a HOLD signal is initiated. Thereby, the random binary numbers from the calculations are used to determine to which random point in the sequence of fifteen NOP instructions the microprocessor should jump and then execute the following remaining number of NOP instructions. In practice, this alters the sampling intervals by approximately ± twenty-one microseconds about a mean sampling interval time period since a NOP microprocessor instruction consumes ten clock cycles at 3.3 MHz. which is approximately three microseconds.

After the input variables have been sampled, digitized and stored for calculation, the three measurements of the electric energy quantity as produced by the outputs of the system 20 are calculated in a common calculation subroutine, since the same subroutine can be used with slight variations. Accordingly, it is only necessary to pass in the correct sequence through the subroutine which performs the computations.

Pulse data output signals are produced whose periods are proportional to the rate of change of the calculated quantities in accordance with the equations hereinbelow. The equations calculated in the system 20 are:

$$\Delta 3\emptyset KW=(VA_A^*\cdot I_A^*+V_B^*\cdot I_B^*+V_C^*\cdot I_C^*)/(\text{constant}=385)$$

$$\Delta 3\emptyset QHR=[(-V_C^*)\cdot I_A^*+(-V_A^*\cdot I_B^*)+(-V_B^*\cdot I_C^*)]/(\text{constant}=385)$$

$$\Delta VSQ=(V_A^*\cdot V_A^*)+(X\cdot X)+(Y\cdot Y)$$

where V* and I* quantities are the instantaneous sampled values of the input voltages and currents and X and Y are equal to zero.

It is seen in each of the above equations that the sum of three products is calculated and that there is a division by a constant which is determined by the levels of the input signals and the limits of 16 bit data against which the calculated values are compared. The Δ increments are the calculated instantaneous value of kilowatts, Q and volts-squared. The accumulations of the Δ increments calculated each sampling interval provides the integrals with respect to time for kilowatts, Q and volts-squared to produce the desired measurements of kilowatt-hours, Q-hours and volts-squared-hours. In the last equation, only the value of the square of the voltage of phase A is calculated, therefore, two product terms in the equation include X's and Y's that are set to zero in the process utilizing a common calculation subroutine. As is known in electric energy metering, instantaneous incremental quantities are derived and accumulated over a time interval to provide the time integration required to derive a measurement of an electric energy quantity. Accordingly, the instantaneous input signal values are sampled and used in the calculations of the above equations and these results are stored in the variable accumulator registers. When predetermined limits in the accumulators are reached, the pulse outputs are produced with the accumulators retaining the remainder in excess of the limit for addition to new accumulations. The output pulse circuits are made to change the direction of current or logic state upon reaching the limit of an associated accumulator register.

Referring again to Figure 4, there is shown the pulse timing chart of signals shown in Figure 2A to effect the randomized and asynchronous sampling of the input signals. The top pulses shown in Figure 4 are the TIMR sample interval timer pulses produced by the sample timer 46. When the signal goes low at time T0, the system would normally respond with the RINT signal without the randomized delay. The times shown in Figure 4 are to be understood to not be to scale so as to make more apparent the description of the operation of the random time delay to produce the randomized sample intervals. Accordingly, following time T0 in the occurrence of the falling edge of the TIMR signal, the source of

random numbers having a mean zero value as mentioned hereinabove, is obtained.

The longest delay of approximately forty-five microseconds may be effected to produce the rising TIMR pulse edge at time T1. The broken line T1′ indicates the minimum delay which may be effected, and the broken line corresponding to a time T1″ is the mean value of the delay which is the average which is produced by the randomized technique described hereinabove. It is to be noted that ending of the TIMR pulse at the earlier times of T′ and T″ would result in correspondingly earlier times for the RINT and HOLD and remaining signals shown in Figure 4 and such earlier times are not shown to simplify the Figure 4.

At the end of the time delay routine, the RINT signal is initiated and goes positive to reset the sample timer 46 and return the TIMR signal to the zero logic level. As a substantially constant fixed time T2 after the RINT signal, the HOLD signal is initiated to start the sampling interval one. The SCON signal is applied to the A/D converter 38 and at the end of the conversion of each of the sampled input signal values, the STAT signals are produced. The HOLD signal goes to the low logic state to release the sample and hold circuits at time T3. The system then waits for the timeout of the TIMR signal at time T4 to initiate the sampling interval two. At time T4, the sample timer 46 initiates another TIMR signal, going low, and the random delay subroutine is executed and initiates the RINT signal at T5 to reset the TIMR and initiate a HOLD signal at time T6 so that the time between T2 and T6 defines the sampling interval one. The randomized time delay in developing the randomized sampling intervals is the time between, for example, T0 and T1, the beginning of the TIMR signal, and the beginning of the RINT signal; another is at times T4 and T5. The other times shown being substantially constant in the operation of the system. The HOLD signal is initiated at time T6, followed by the start conversion SCON signal at T6 and the STAT signals follow. The release of the HOLD signal occurs at time T7 for the timeout of another TIMR signal at time T8 which ends at time T9 with the initiation of the RINT after the randomized delay to initiate a further HOLD signal at time T10, ending sampling interval two.

In the system disclosed hereinabove, the mean time value of the randomized sampling intervals between, for example, between times T2 and T6 and between T6 and T10 can be varied between one and one-half and three milliseconds with a mean sampling interval time of approximately 2.5 milliseconds having been employed in one preferred embodiment of this invention. Changes in the counter arrangement outputs at the pads 122 and 126 in the sample timer circuit 46 provide changes in the period of TIMR pulses following reset of the RINT signals. The random delay variations in the mean value occur approximately ± twenty-two milliseconds shorter or longer than the mean sampling value. The maximum variation between sampling intervals is approximately forty-five milliseconds or approximately one electrical degree at sixty Hz. This produces increased accuracy in the calculated values of the system 20 and avoids sensing the voltage and current signal components of the electric energy quantity being measured at the same sampled points in the sixty Hz. cycle, which frequency is also known to vary slightly in electric utility power line networks.

The randomized and asynchronous sampling provided herein is independent of the phase, fundamental frequency or harmonics of the fundamental frequency of the input signals. With limited numbers of sampling times occurring each cycle of the input signals, a given number of the binary representations of the randomly occurring instantaneous sampled signal values give more increased accuracy over the same number of sampled values that are synchronized with the input signals and have the same phase relationships with respect to the sampled signals. The random samples prevent erroneous results when the input signals are severely distorted from the ideal sinusoidal form. These distortions are known to be produced by some types of electrical loads such as those having solid state switching devices or having widely varying impedance characteristics. Also, if the sample times were known to be regular instead of randomized, it would afford an opportunity for those electric utility customers who are without scruples to vary their load characteristics to avoid true measurements at the regular samplings, and thus defeat the metering system if it were as heretofore known.

WHAT WE CLAIM IS:—

1. A digital processing and calculating AC electric energy metering system

for measuring an electric energy quantity occurring in an electric utility system, said metering system comprising:

signal sample means including inputs and outputs, said inputs receiving input voltage and current signal components of said AC electric energy quantity, said outputs producing instantaneous values of the input voltage and current signals when said signal sample means is rendered to a sampling state;

analog to digital converter means producing binary signal representations of each of the instantaneous signal values;

sample timer means producing pulse signals at randomly varying intervals, said pulse signals initiating the sampling state of said signal sample means at randomly occurring sampling times;

calculating means computing a quantity of the input signals from said binary signal representations thereof occurring at each sampling time;

accumulator means receiving each quantity computed so as to store totalized values thereof, said totalized values being a time integral of the sums of each computed incremental quantity received to produce measured values thereof; and

output means responsive to the stored totalized values of said accumulator means to produce data output signals representing the measured values.

2. The metering system as claimed in claim 1 wherein said input voltage and current signals are polyphase components of a polyphase electric energy quantity and wherein said data output signals represent the predetermined parameter of said polyphase electric energy quantity.

3. The metering system as claimed in claim 1 or 2 including a numerical readout display device responsive to the measured value and producing a corresponding numerical reading of the totalized values.

4. The metering system as claimed in claim 1 wherein said data output signals are pulse signals each representing a predetermined amount of the measurement.

5. The metering system as claimed in claim 4 wherein said accumulator means stores totalized values of the sums of each computed quantity to store real-time totalized values of the parameter to be measured, and wherein said metering system limits the stored totalized values in said accumulator means and wherein each of the pulse data output signals is produced when the limit of the totalized values is reached.

6. The system as claimed in claim 5 wherein each of the separate totalized values is a time integral of the sums of each of said plurality of computed quantities received to produce measured values for said electric energy quantity, and wherein said output means is responsive to the separately stored totalized values of said accumulator means to produce plural data output signals representing said measured values.

7. The metering system as claimed in any one of claims 1 to 6, said metering system including a display selector means for selectively displaying a readout corresponding to a separate one of said totalized values to thereby selectively display kilowatt hours, Q-hours, and volts-squared-hours.

8. The metering system as claimed in claim 7 including means for receiving demand interval pulse signals and wherein said accumulator means further includes stored measured values of peak kilowatt demand, said accumulator including first register means for storing each of the totalized values of kilowatt-hours occurring between consecutive demand interval pulses, and further including second register means for storing the highest totalized values of kilowatt-hours stored in said first storing means.

9. The metering system as claimed in claim 8 including a manual demand reset control means for resetting the first and second register means to zero.

10. The metering system as claimed in any one of claims 1 to 9 wherein said data output signals are a plurality of pulses having opposite binary states.

11. The metering system as claimed in claim 10 including a magnetic recorder having plural recording heads conducting current in opposite direction in response to the opposite binary states of the plural pulse data output signals to provide non-return to zero (NRZ) recordings of said plural data output signals.

12. The metering system as claimed in claim 11 wherein said magnetic tape recorder includes a source of demand interval pulse signals being applied to said means for receiving said demand interval pulses and further wherein said recorder includes a further recording head for recording said demand interval pulse signal concurrently with the recording of the plural pulse data output signals.

13. The metering system as claimed in any one of claims 1 to 12 wherein said

calculating means includes a sequence controller and calculator subsystem having a programmed sequence of operation.

14. The metering system as claimed in claim 13 wherein said sequence controller and calculator subsystem includes a source of clock signals for synchronizing operation of the sequence controller and calculator subsystem, and wherein said clock source provides clock signals to said sample timer means, and said sample timer means includes a counter circuit arrangement for producing said pulse signals at a rate related to a predetermined ratio of the rate of said clock signals.

15. The metering system as claimed in claim 14 wherein said sample timer means with said counter circuit arrangement includes different preselectable outputs for selecting different fixed predetermined output rates for said pulse signals.

16. The metering system as claimed in claim 15 wherein pulse signals produced from said sample timer means are applied to said sequence controller and calculator subsystem with the subsystem having a random delay for producing a sampling control signal to said signal sample means at randomly varying time delays following each of said pulse signals and for producing a resetting signal to said sample timer means.

17. The metering system as claimed in claim 16 wherein said random delay is derived from a source of a predetermined sequence of randomly occurring numbers having a mean value and wherein said random delay further is distinguished by a predetermined quantity of different time delay periods each corresponding to a different number in said sequence of randomly occurring numbers, a separate one of said randomly occurring numbers being detected prior to the occurrence of said sampling control signal whereupon a corresponding time delay period occurs before said sampling control signal is initiated.

18. The metering system as claimed in claim 17 wherein said pulse signals from said signal sample means initiate the beginning of said time delay periods, and wherein said different time delay periods include equal quantized delay values, and the mean of the randomized delay periods produces a predetermined average sampling interval time period.

19. The metering system as claimed in any one of claims 1 to 18 including a power supply having an output for supplying solid state circuits included in said metering system, said power supply receiving primary power from an AC electric utility source, said output of said power supply means including a temporary storage capacity for supplying power to said system for a temporary time period following an outage of said primary power input.

20. The metering system as claimed in claim 19 wherein said accumulator means includes a random access memory for storing data while being energized from said power supply means.

21. The metering system as claimed in claim 20 wherein said power supply means includes a battery chargeable from said primary power and effective to maintain said random access memory energized following an outage of said primary power.

22. The metering system as claimed in claim 19, 20, or 21 wherein said power supply includes a monitoring circuit for producing a power fail signal when an outage of primary power occurs.

23. The metering system as claimed in claim 22 wherein said sequence controller and calculator subsystem receives said power fail signal and initiates a system stop signal to said power supply means, and wherein said power supply means includes a gating circuit responsive to both said power fail signal and said stop signal to initiate a reset signal (SYSINT) effective to reset said sequence controller and calculator subsystem.

24. The metering system as claimed in claim 23 wherein said sample timer includes means for producing a second SYSINT signal in response to a first time period being longer than a second time period with said second time period being approximately equal to the average time period for pulse signals produced from said sample timer means and with said first time period occurring only if said pulse signal is not produced, to reset said sequence controller and calculator subsystem.

25. The metering system as claimed in any one of claims 13 to 24 wherein said calculator subsystem includes a programmed sequence of operation being stored in a read only memory included in said calculator subsystem.

26. The metering system as claimed in claim 25 wherein said sequence controller is a microprocessor type central processing unit connected to said read

only memory and wherein said accumulator means is connected to said read only memory and to said central processing unit.

27. The metering system as claimed in claim 25 or 26 wherein said read only memory includes permanently stored system constants including limit values for stored values in said accumulator means.

28. The metering system as claimed in claim 27 wherein said system constants are stored in said accumulator means and whereupon said sequence of operation of said and calculating means includes comparison of the system constants stored in said accumulator means with the system constants stored in said read only memory, said calculating means further including means for preventing further operation if said system constants stored in said accumulator means are not the same as the system constants stored in said read only memory.

29. A metering system, substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

RONALD VAN BERLYN.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1980
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1578174 COMPLETE SPECIFICATION

4 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

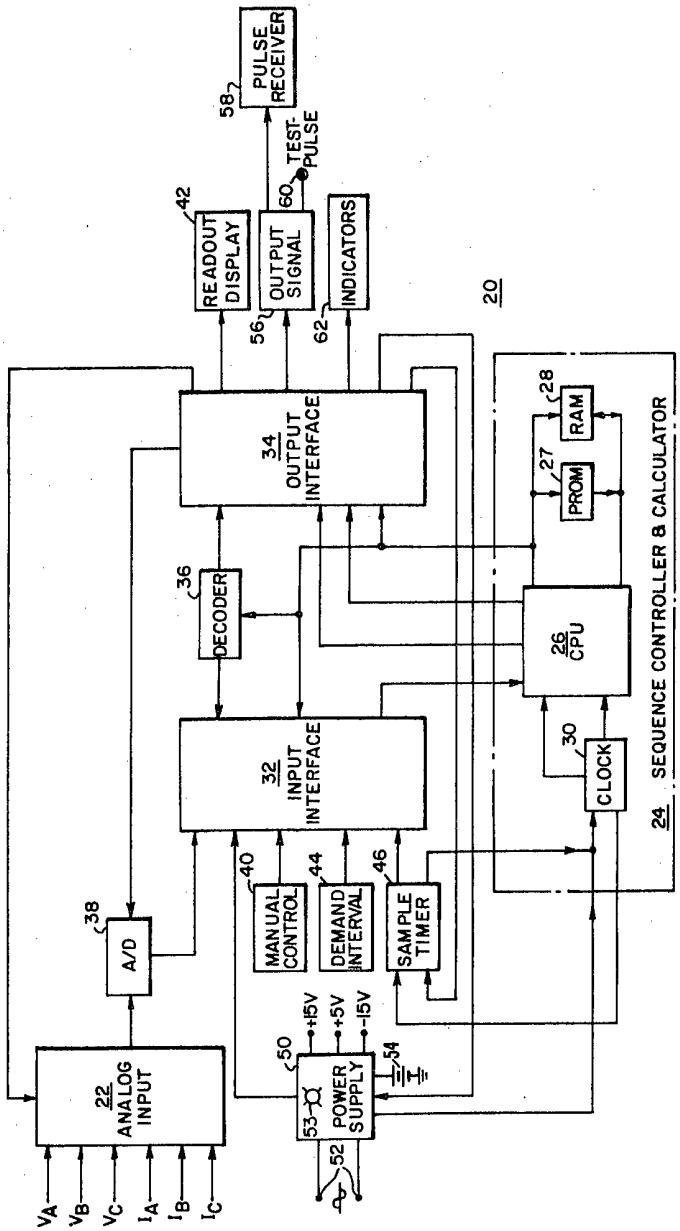

FIG. 1

1578174 COMPLETE SPECIFICATION

4 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 2

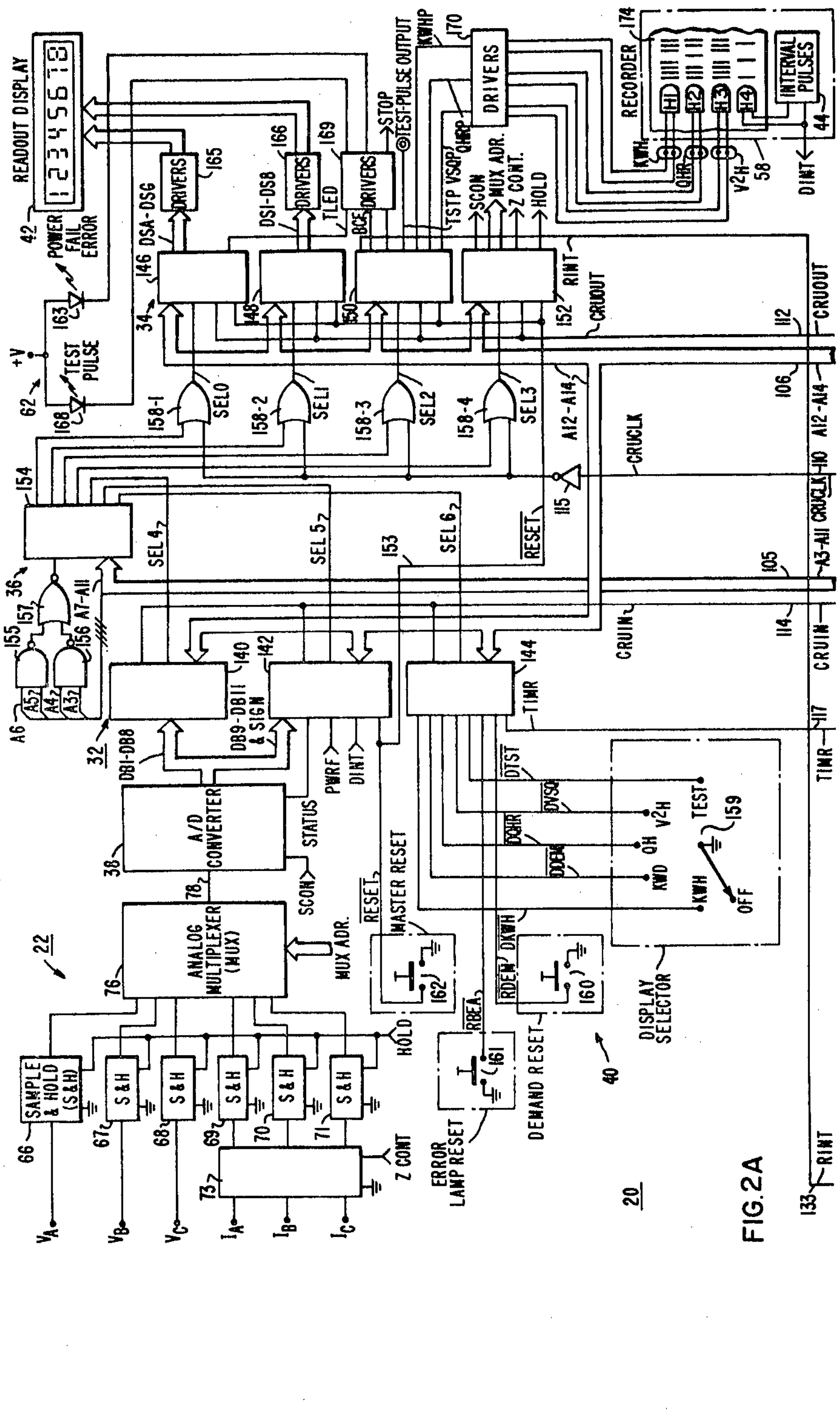

FIG.2A

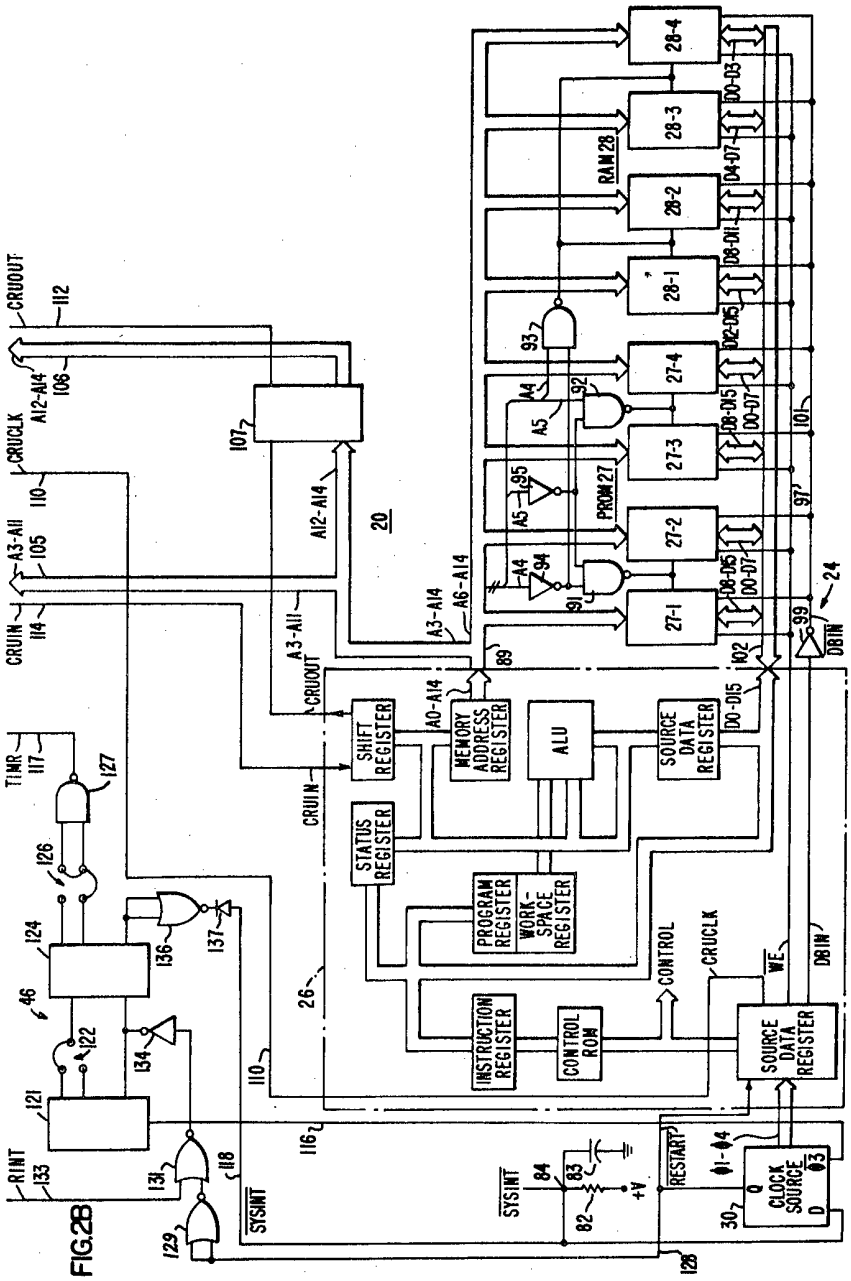
CRUOUT
112
A12-A14
106
CRUCLK
110
A3-A11
105
CRUIN
114
TIMR
117
127
126
124
136
137
46
122
134
121
RINT
133
131
118
129
SYSINT
116
110
107
A12-A14
20
A3-A11
CRUOUT
CRUIN
A6-A14
A3-A14
89
SHIFT REGISTER
STATUS REGISTER
A0-A14
MEMORY ADDRESS REGISTER
ALU
SOURCE DATA REGISTER
D0-D15
PROGRAM REGISTER
WORK-SPACE REGISTER
INSTRUCTION REGISTER
CONTROL ROM
26
CONTROL
CRUCLK
WE
DBIN
SOURCE DATA REGISTER
RAM 28
28-4
28-3
28-2
28-1
PROM 27
27-4
27-3
27-2
27-1
D0-D3
D4-D7
D8-D11
D12-D15
D8-D15
D0-D7
93
92
91
94
95
A4
A5
97
101
102
99
24
DBIN
SYSINT
84
83
82
+V
RESTART
Φ1-Φ4
CLOCK SOURCE
30
128

FIG.2B

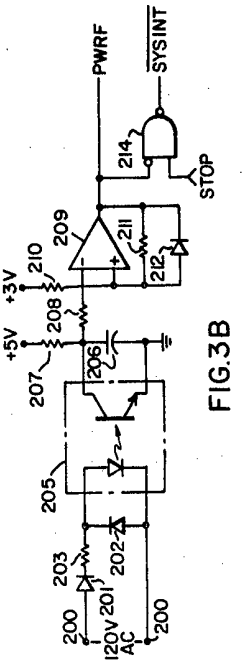

FIG.3B

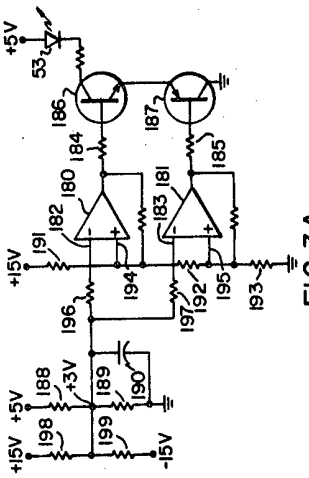

FIG.3A

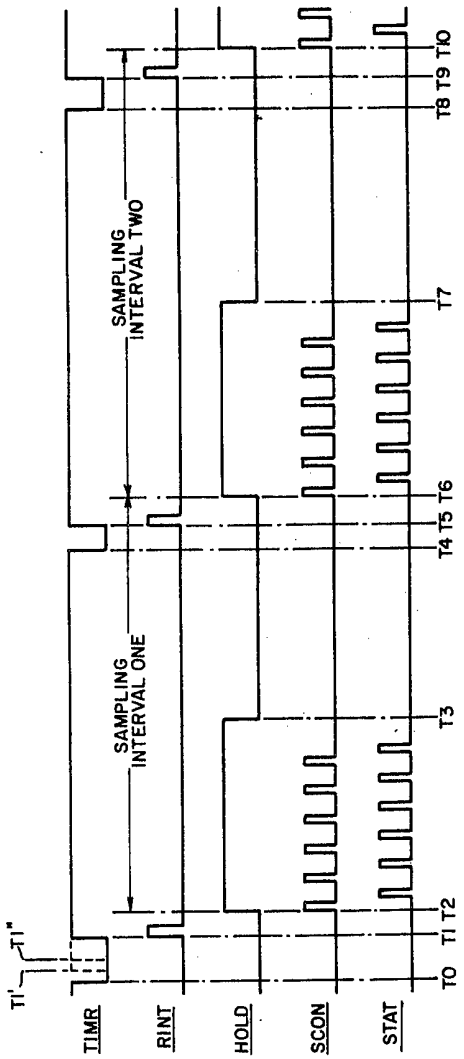

FIG.4