(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 June 2010 (17.06.2010)

PCT

(10) International Publication Number
WO 2010/067243 A1

(51) International Patent Classification:
G06F 13/38 (2006.01) *G06F 13/42* (2006.01)

(21) International Application Number:
PCT/IB2009/055316

(22) International Filing Date:
24 November 2009 (24.11.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
08105961.0 10 December 2008 (10.12.2008) EP

(71) Applicant *(for all designated States except US)*: **NXP B.V.** [NL/NL]; High Tech Campus 60, NL-5656 AG Eindhoven (NL).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **LI JUHUI, Juhui** [CN/SG]; c/o NXP B.V., Intellectual Property & Licensing Department, High Tech Campus 32, NL-5656 AE Eindhoven (NL).

(74) Agents: **KROTT, Michel Willy François Maria** et al.; c/o NXP B.V, Intellectual Property & Licensing Department, High Tech Campus 32, NL-5656 AE Eindhoven (NL).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: AUTOMATIC DATA TRANSFER MODE DETECTION

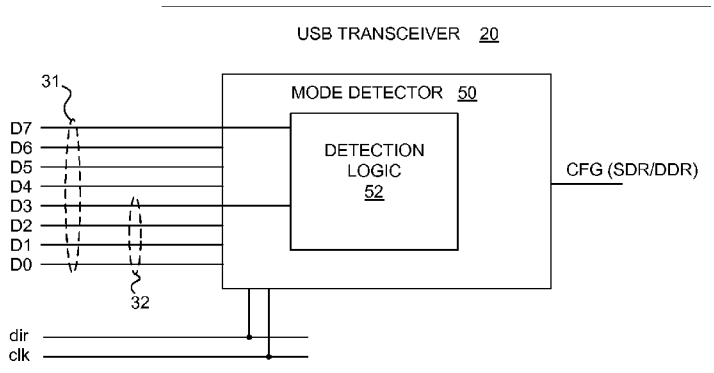

FIG. 3

(57) **Abstract**: A circuit (20) comprises an interface (30) for communicating with another circuit (10). The interface (30) comprises a parallel data bus having a set of data lines (31) which are operable in a first data transfer mode in which the set of data lines (31) are used to transfer data and in a second data transfer mode in which a sub-set (32) of the data lines are used to transfer data. A mode detection module (50) determines which of the data transfer modes is in use by detecting a state of at least one of the data lines which is only used by the first data transfer mode and detecting a state of at least one line from the sub-set of data lines. The mode detection module (50) can detect logic values received on the data lines at a time when a command having known logic values is expected to be received over the interface and determine the data transfer mode according to which of the data lines the known logic values are detected on.

WO 2010/067243 A1

DESCRIPTION

AUTOMATIC DATA TRANSFER MODE DETECTION

This invention relates to integrated circuit devices.

There are increasing pressures to reduce the pin count of integrated circuit devices, and interfaces connecting such devices. The Universal Serial Bus 2.0 Transceiver Macrocell Interface (UTMI) is an interface which connects a USB transceiver to another device, such as an ASIC or a FPGA of a host or device. The UTMI Low Pin Interface (ULPI) has been proposed as a way of implementing the UTMI with a reduced number of connecting lines. This allows devices at each end of the UTMI to have a reduced pin count. Examples of existing implementations of a USB Transceiver supporting the ULPI are given in datasheets for NXP Semiconductor devices ISP1504 and ISP1508. It is desirable to further reduce the pin count. Conventionally, reducing the pin count has been at the expense of a reduced set of features. It is desirable to reduce the pin count without sacrificing features of the integrated circuit.

Accordingly, a first aspect of the present invention provides a circuit comprising:

- an interface for communicating with another circuit, the interface comprising a parallel data bus having a set of data lines, wherein the interface is operable in a first data transfer mode in which the set of data lines are used to transfer data and in a second data transfer mode in which a sub-set of the data lines are used to transfer data;
- a mode detection module which is arranged to determine which of the data transfer modes is in use by detecting a state of at least one of the data lines

which is only used by the first data transfer mode, the mode detection module generating a configuration output indicative of the determined data transfer mode for configuring operation of the circuit.

An advantage of the circuit detecting, by itself, which data transfer mode is in use is that there is no need for the circuit to receive a control signal which specifies which data transfer mode is in use. This avoids the need to provide a pin to receive the control signal on the package housing the circuit, and this saving in pin count can be made without a reduction in the feature-set of the circuit. This also avoids the need to provide a connecting line to the circuit carrying a configuration signal which instructs the circuit of the data transfer mode. Further advantages are a saving in cost and board area. The configuration output is used to configure operation of other modules and devices within the circuit. The detection of the data transfer mode can be performed without affecting the interface timing.

The detection can be made by monitoring for any activity on the data lines. Advantageously, a particularly quick and reliable detection of the data transfer mode can be made by the mode detection module detecting logic values received on the data lines at a time when a command having known logic values is expected to be received over the interface. The data transfer mode is determined according to which data lines the known logic values are detected on. The logic value can be signalled on a data line by a voltage value, or by a change in voltage value.

Advantageously, the mode detection module is arranged to perform the detection immediately following power-up.

A further aspect of the invention provides a method of operating a circuit, the circuit comprising an interface for communicating with another circuit, the interface comprising a parallel data bus having a set of data lines, the interface being operable in a first data transfer mode in which the set of data lines are used to transfer data and in a second data transfer mode in which a sub-set of the data lines are used to transfer data, the method comprising:

- determining which of the data transfer modes is in use by detecting a state of at least one of the data lines which is only used by the first data transfer mode; and,
- generating a configuration output indicative of the determined data transfer mode for configuring operation of the circuit.

Embodiments of the invention are described in which the interface is the UTMI Low Pin Interface (ULPI). The circuit can be a USB or a Wireless USB (WUSB) integrated circuit. It will be appreciated that while ULPI is an advantageous example of an interface, the invention can be more generally applied to other types of interface which support multiple modes of operation, with different numbers of data lines being used in the different modes.

The functionality described here can be implemented in software, hardware or a combination of these. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed processor. Accordingly, another aspect of the invention provides a machine-readable product carrying machine-executable instructions (software) for implementing the described functionality. The software may be stored on an electronic memory device, hard disk, optical disk or other machine-readable storage medium. The software may be downloaded directly to a processing device via a network connection.

Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 shows a UTMI Low Pin Interface (ULPI) between a transceiver and a host device;

Figure 2 shows SDR and DDR operation on a data line of the interface;

Figure 3 shows a mode detector within the transceiver;

Figure 4 shows data transfer of a command in SDR and DDR modes;

Figure 5 shows logic to implement the mode detector;

Figure 6 shows waveforms of the logic of Figure 5 when the SDR mode is in use;

Figure 7 shows waveforms of the logic of Figure 5 when the DDR mode is in use.

Figure 1 shows an example application of an embodiment of the invention. A USB Transceiver 20 and another device, such as a host processor 10, are connected by a UTMI Low Pin Interface (ULPI) 30. The ULPI 30 comprises a data bus formed by a set of data lines D7-D0, a direction controlling line (dir), clock (clk), and the lines stp and nxt. Transceiver 20 and host processor 10 are each implemented as an integrated circuit. The UTMI Low Pin Interface (ULPI) supports two data transfer modes: a first mode called Single Data Rate (SDR) and a second mode called Dual Data Rate (DDR). The single data rate mode toggles a data line only on a rising clock edge and uses a parallel data bus which is 8 bits wide, i.e. it uses the set 31 of data lines D7-D0. This version of the ULPI has eight data lines and a total of twelve lines, and is shown in Figure 1. The dual data rate mode (DDR) toggles a data line on the rising and falling clock edges and uses a parallel data bus which is 4 bits wide, i.e. it uses the sub-set 32 of data lines D3-D0 and does not use the data lines D7-D4. This version of the ULPI has four data lines and a total of eight lines. Figure 2 shows a data signal on one of the data lines in both the SDR and DDR modes of operation. In the DDR mode each data line operates at twice the rate as a data line in SDR mode. The two modes achieve the same overall data rate as DDR uses half as many lines as SDR, with each line operating at twice the data rate of SDR.

The USB transceiver is capable of supporting both the SDR and DDR modes of operation. Only one mode can be used at any time. To support both modes of operation, the transceiver interface has eight data lines D7-D0. It is known to dedicate a further top level pin on the transceiver device to receive a control signal which instructs the transceiver to perform SDR or DDR operation, but this requires an external pin on the integrated circuit package. A device of this kind is shown in the datasheet for NXP Semiconductor device ISP1508, with a configuration pin CFG0 receiving a signal to select SDR/DDR mode. The transceiver shown in Figures 1 and 3 improves on this by deriving a configuration

signal CFG for itself, indicating which date rate (SDR/DDR) is being used, by monitoring the data lines 31.

Figure 3 shows a USB transceiver 20 with a mode detector 50. The mode detector connects to selected ones of the data lines D7-D0. Embodiments will be described in which the mode detector 50 connects to one, two or a larger number of the data lines. The mode detector 50 also advantageously connects to the other lines of the interface such as clock (clk) and direction (dir). Mode detection logic 52 detects activity on the selected data line(s) and decides, on the basis of the detected activity, which data rate the interface is using. This allows the transceiver 20 to determine the data rate for itself, without requiring an external configuration input. Mode detector 50 outputs a configuration signal CFG which indicates the detected mode, i.e. SDR or DDR. The configuration signal can be used to configure operation of the USB transceiver circuit 20, such as configuring which data bus lines D7-D0 the transceiver should transmit and receive on, timing for transmit/receive operations and any other parameter which is dependent on the data mode. The mode detector 50 can operate in one of a number possible ways:

(i) The mode detector 50 connects to at least one of the data lines (e.g. D7) which is only used during the SDR mode of operation. Mode detection logic 52 monitors activity on the data line. If activity is detected on the line, the interface must be operating in the SDR mode, as this line is not used during DDR mode. Advantageously, the detection is performed at a time when it is known that data is received.

(ii) An improvement of (i) above. The mode detector 50 connects to at least one of the data lines (e.g. D7) which is only used during the SDR mode of operation and also to at least one of the data lines which is used both during SDR and DDR modes (e.g. D3). The mode detection logic 52 monitors activity on the data lines. If activity is detected on line D7 then the interface must be operating in the SDR mode. If activity is detected on line D3 but not on D7 then the interface must be operating in the DDR mode.

In options (i) and (ii) above it is possible to monitor for any activity occurring on the monitored data lines. It is advantageous that the decision of which data rate is being used is made as quickly and correctly as possible. A quicker decision can be made by monitoring for logic values of a predetermined command at a time when the command is expected to be received over the interface, e.g. an initial command received immediately following power-up. This feature can be combined with any of (i) or (ii). An embodiment of the mode detector 50 will now be described which follows (ii) above and monitors for the presence of a particular command following power-up. The mode detector 50 connects to data line D7 (i.e. a data line which is only used in SDR mode) and data line D3 (i.e. a data line which is used during SDR and DDR mode) and looks at selected bits of the first byte of a predetermined command received on these lines. It will be appreciated that as the data lines form a parallel data bus, the monitored data line, or lines, determine which bit(s) of a transferred byte are inspected. The data lines on which the expected logic value is received determines which data rate is in use.

Figure 4 shows data transfer in SDR and DDR modes. The set of data lines D7-D0 is shown. An example command is considered with the value 0X85 (= 10001010 in binary). In the SDR mode, this command will be sent in parallel across data lines D7-D0 as a byte. In the DDR mode this command will be sent across only data lines D3-D0 in two nibbles. The time taken to transmit the two nibbles in DDR mode is the same as the time taken to transmit the byte in SDR mode. The example command shown in Figure 4 is a transmit command (TXCMD) to perform a soft-reset, and is the first command expected to be received from device 10 in the ULPI specification. Consider that only data lines D7 and D3 are monitored. In the SDR mode, this command will be sent across data lines D7-D0 with the value of D[7] = “1”. In the DDR case this command will be sent across data lines D3-D0 in two nibbles, with the value of D[3] = “1”. Lines D[7:4] are set to 0. Accordingly, if a logic value of “1” is seen on data line D7 and a logic value of “0” is seen on data line D3, the mode is determined to be

SDR. If a logic value of "0" is seen on data line D7 and a logic value of "1" is seen on data line D3, the mode is determined to be DDR.

It is possible to improve the reliability of the detection by increasing the number of data lines which the mode detector connects to. For the example command shown in Figure 4, data lines D7, D6, D3 and D2 can be monitored. If the logic values "10" are seen on data lines D[7:6] the mode is determined to be SDR whereas if the logic values "10" are seen on data lines D[3:2] the mode is determined to be DDR.

Increasing the number of data lines which are monitored and compared against a stored value increases the number of bits of the first command which are compared against the stored command. All of the lines can be monitored, if desired. It is possible to make a decision of which data rate mode (SDR/DDR) is in use after receiving just the first byte of the first command.

An implementation of the invention applied to the ULPI interface will now be described in more detail. Immediately following power-up a USB transceiver waits to receive commands from device 10 on the ULPI interface 30. Data lines D7 and D3, or D7, D6, D3 and D2 are monitored as described above. The signal DIR is also defined in the ULPI specification. It is an output signal from the USB transceiver to indicate the data bus direction. Only when DIR is low, device 10 can drive TXCMD. Advantageously, the line "dir" is also connected to the detection circuit so that the detection of the values on data lines D7, D6, D3, D2 is performed after signal DIR has changed to allow the device 10 to transmit. Detecting the data values D[7:6] = "10" on lines D7, D6 indicates that SDR is in use. Detecting the data values D[3:2] = "10" on lines D3, D2 and detecting the data values D[7:6] = "00" on lines D7, D6 indicates that DDR is in use. It is also advantageous that the data lines D[7:0] of the USB transceiver 20 should be pull down enabled after power up and before the end of the rate detection. This is to prevent unknown status on the data bus when both sides are not driving the data bus. After the SDR/DDR detection, the USB transceiver 10 can remove the pull down on its data bus and both USB transceiver 20 and other device 10 are in normal functional status.

A more detailed embodiment of logic to perform the rate detection is shown in Figure 5 and waveforms showing operation of the circuit are shown in Figures 6 and 7. Pull down enable on the data bus is not shown in these figures.

The inputs to the logic circuit are: Dir_d (direction of data transmission); D7_d, D6_d, D3_d and D2_d (data lines of the data bus). The default mode of the USB transceiver is DDR. This is because there is some time margin in SDR case and DDR is very timing stringent.

If there is '1' on "HIGH BITS", it means that device 10 is performing SDR. The value of "HIGH BITS" is latched by DFF1. At the same time, the result of "LOW BITS" is also latched by DFF2. The outputs of M2 and M4 are decoded as shown in Table 1 to generate an internal configuration signal CFG which has a value of "1" to denote DDR and a value of "0" to denote SDR.

Module 63 detects when the first TXCMD command is received on the interface, following power up and outputs a signal EN which is applied to other modules. Note, that module 63 only indicates when the first command is received. Module 61 checks whether the first command has the required logic values. Module 61 generates outputs "HIGH BITS" and "LOW BITS" which indicate when logic values on the data lines D7, D6, D3, D2 meets values of the first expected command. Module 62 latches logic values and decodes a set of inputs to generate the output CFG which indicates whether the data rate is SDR or DDR.

At power up, Dir_d and EN both are high. Logic0 goes through M1 and M2, Logic1 goes through M3 and M4. This forces the decoder to default to the mode of DDR. Signal EN denotes when the first TXCMD is received over the interface. EN changes to '0' when the first TXCMD is received. After that, EN will not change anymore.

After Dir_d goes low, "HIGH BITS" and "LOW BITS" go through AND1 and M5. As long as a '1' happens at AND1.O (indicating that a high value has been received on at least one of the monitored data lines), DFF3.D will be '1' and it will be latched on DFF3. EN goes to 0 immediately and M5 picks up the output of DFF3.Q, then DFF3 and M5 enter Latch mode. EN will not change anymore

even when there are changes on Dir_d, “HIGH BITS” and “LOW BITS”. “HIGH BITS” goes through M1 and M2 when Dir_d is ‘0’ and EN is ‘1’. “LOW BITS” goes through M3 and M4 when Dir_d is ‘0’ and EN is ‘1’. “HIGH BITS” and “LOW BITS” will be captured by DFF1 and DFF2 at the falling edge of Clk60MHz. If “HIGH BITS” or “LOW BITS” changes, EN will change from ‘1’ to ‘0’. M2 and M4 will pick up values from DFF1 and DFF2 other than “HIGH BITS” and “LOW BITS”. M2, DFF1 and M4, DFF2 will enter latch mode. This means the value of M2.O and M4.O will not be changed anymore by “HIGH BITS” and “LOW BITS” unless PoR_n changes to ‘0’. The signal Power on Reset (PoR) initialises all of the flip-flops in this circuit to be in a default value, for example, to initialize the detection to be in DDR mode and EN to be ‘1’.

The operation of the Decoder block is described by Table 1. In Table 1, outputs M2.O, M4.O = “01” from multiplexers M2, M4 indicate DDR operation. This means that the logic values of the first command were not found on the data lines D7, D6 and the expected logic values of the first command were found on the data lines D3, D2. Outputs M2.O, M4.O = “10” indicate a SDR operation. This means the expected logic values of the first command were found on the data lines D7, D6 and a logic value of “0” was found on the data lines D3, D2. Outputs M2.O, M4.O = “11” indicate a SDR operation. This means the expected logic values of the first command were found on the data lines D7, D6 and a logic value of “1” was found on the data lines D3, D2. In this circuit, the condition where outputs M2.O, M4.O = “00” is an impossible status.

M2.O	M4.O	CFG	MODE
0	1	1	DDR
1	0	0	SDR
1	1	0	SDR

Table 1 - CFG Decoding

If nothing happens on the data bus, “HIGH BITS” and “LOW BITS” both are “00”, M2.O and M4.O are “01” and the USB transceiver is in the default DDR mode. When the first TXCMD is received, if it is a DDR command, CFG will not

change. If the first TXCMD is a SDR command, CFG will change to '0' (switching the transceiver into SDR mode) in a very short time (some gates delay). It can be seen that this detection scheme allows the USB transceiver to be set into SDR/DDR mode without significant interface timing influence.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The words "comprising" and "including" do not exclude the presence of other elements or steps than those listed in the claim. Where the system/device/apparatus claims recite several means, several of these means can be embodied by one and the same item of hardware.

The various illustrative logical blocks, modules, circuits, and algorithm steps described above may be implemented as electronic hardware, as software modules executed by a processor, or as combinations of both. The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination designed to perform the described functions.

In the description above, and with reference to the Figures, there is described a method and apparatus for circuit 20 comprises an interface 30 for communicating with another circuit 10. The interface 30 comprises a parallel data bus having a set of data lines 31 which are operable in a first data transfer mode in which the set of data lines 31 are used to transfer data and in a second data transfer mode in which a sub-set 32 of the data lines are used to transfer data. A mode detection module 50 determines which of the data transfer modes is in use by detecting a state of at least one of the data lines which is only used by the first data transfer mode and detecting a state of at least one line from the sub-set of data lines. The mode detection module can detect logic values

received on the data lines at a time when a command having known logic values is expected to be received over the interface and determine the data transfer mode according to which of the data lines the known logic values are detected on.

CLAIMS:

1. A circuit comprising:

- an interface for communicating with another circuit, the interface comprising a parallel data bus having a set of data lines, wherein the interface is operable in a first data transfer mode in which the set of data lines are used to transfer data and in a second data transfer mode in which a sub-set of the data lines are used to transfer data;

- a mode detection module which is arranged to determine which of the data transfer modes is in use by detecting a state of at least one of the data lines which is only used by the first data transfer mode, the mode detection module generating a configuration output indicative of the determined data transfer mode for configuring operation of the circuit.

2. A circuit according to claim 1 wherein the mode detection module is arranged to determine the data transfer mode by detecting a state of at least one of the data lines which is only by the first data transfer mode and by detecting a state of at least one line from the sub-set of data lines.

3. A circuit according to claim 2 wherein the mode detection module is arranged to:

detect logic values received on the data lines at a time when a command having known logic values is expected to be received over the interface;

determine the data transfer mode according to which of the data lines the known logic values are detected on.

4. A circuit according to claim 3 wherein the mode detection module is arranged to:

determine that the second data transfer mode is in use if the expected logic values are detected on the sub-set of data lines, and the expected logic values are not detected on at least one of the data lines which are only used when operating in the first data transfer mode.

5. A circuit according to claim 3 or 4 wherein the mode detection module is arranged to perform the detection immediately following power-up.

6. A circuit according to any one of claims 3 to 5 wherein the mode detection module is further arranged to detect when a direction of communication signal changes to allow a first command to be received over the interface and performing the detection on the next received command.

7. A circuit according to any one of the preceding claims wherein in the second data transfer mode, the data rate on each data line is double the data rate on each data line in the first data transfer mode.

8. A circuit according to any one of the preceding claims wherein the mode detection module is further arranged to pull down the data lines when performing the detection.

9. A circuit according to any one of the preceding claims wherein the interface is a UTMI Low Pin Interface.

10. A circuit according to any one of the preceding claims in the form of a USB transceiver.

11. An integrated circuit package comprising the circuit according to any one of the preceding claims.

12. A method of operating a circuit, the circuit comprising an interface for communicating with another circuit, the interface comprising a parallel data bus having a set of data lines, the interface being operable in a first data transfer mode in which the set of data lines are used to transfer data and in a second data transfer mode in which a sub-set of the data lines are used to transfer data, the method comprising:

- determining which of the data transfer modes is in use by detecting a state of at least one of the data lines which is only used by the first data transfer mode; and,
- generating a configuration output indicative of the determined data transfer mode for configuring operation of the circuit.

13. A method according to claim 12 wherein the step of determining which of the data transfer modes is in use detects a state of at least one of the data lines which is only used by the first data transfer mode and detects a state of at least one line from the sub-set of data lines.

14. A method according to claim 13 wherein the step of determining which of the data transfer modes is in use detects logic values received on the data lines at a time when a command having known logic values is expected to be received over the interface;

determine the data transfer mode according to which of the data lines the known logic values are detected on.

15. Machine-executable instructions which, when executed by a processor, cause the processor to perform the method of any one of claims 12 to 14.

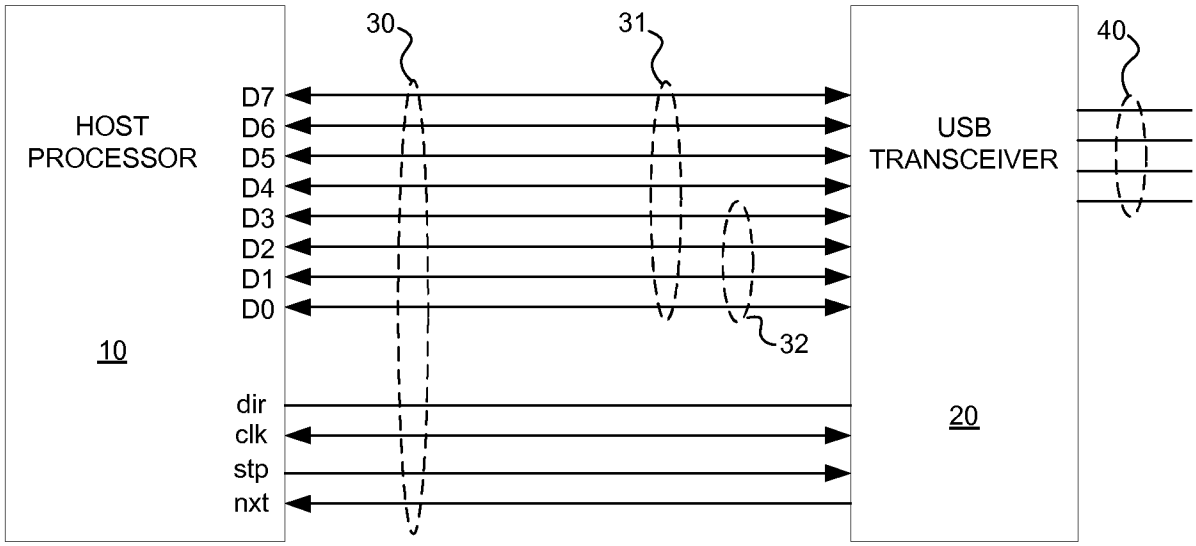
HOST
PROCESSOR
10
D7
D6
D5
D4
D3
D2
D1
D0
dir
clk
stp
nxt
30
31
32
40
USB
TRANSCEIVER
20

FIG. 1

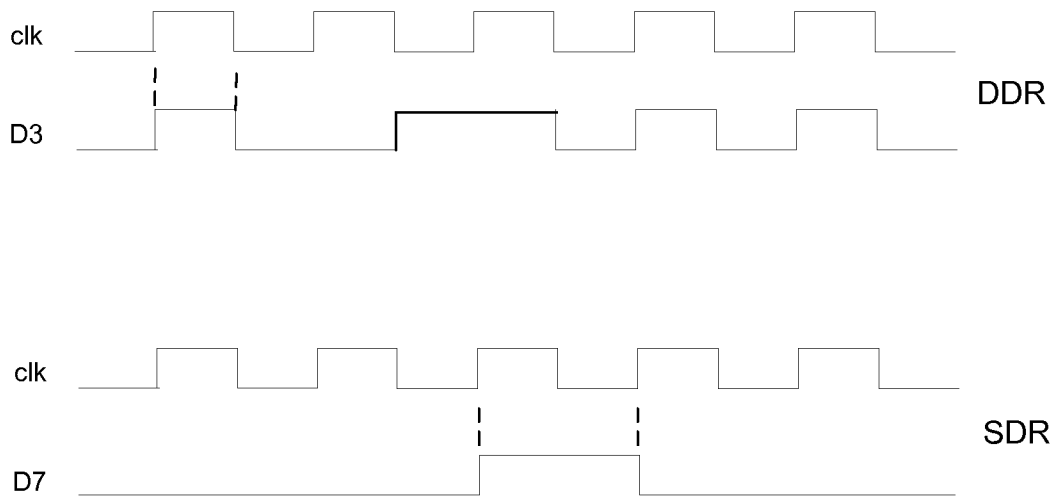
clk
D3
DDR
clk
D7
SDR

FIG. 2

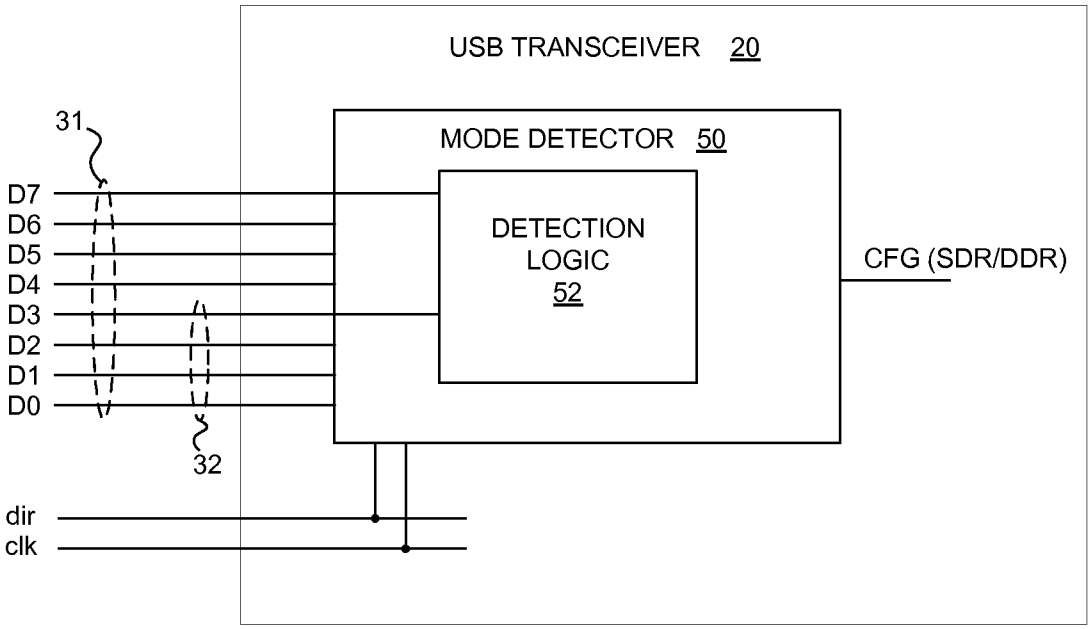
USB TRANSCEIVER 20
MODE DETECTOR 50
DETECTION LOGIC 52
CFG (SDR/DDR)
31
32
D7
D6
D5
D4
D3
D2
D1
D0
dir
clk

FIG. 3

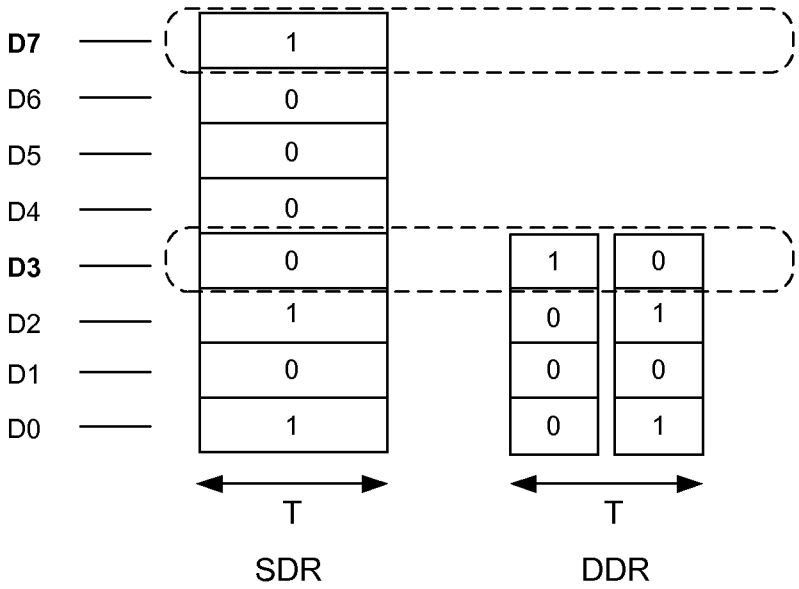
D7
D6
D5
D4
D3
D2
D1
D0
1
0
0
0
0
1
0
1
1
0
0
0
1
0
1
T
T
SDR
DDR

FIG. 4

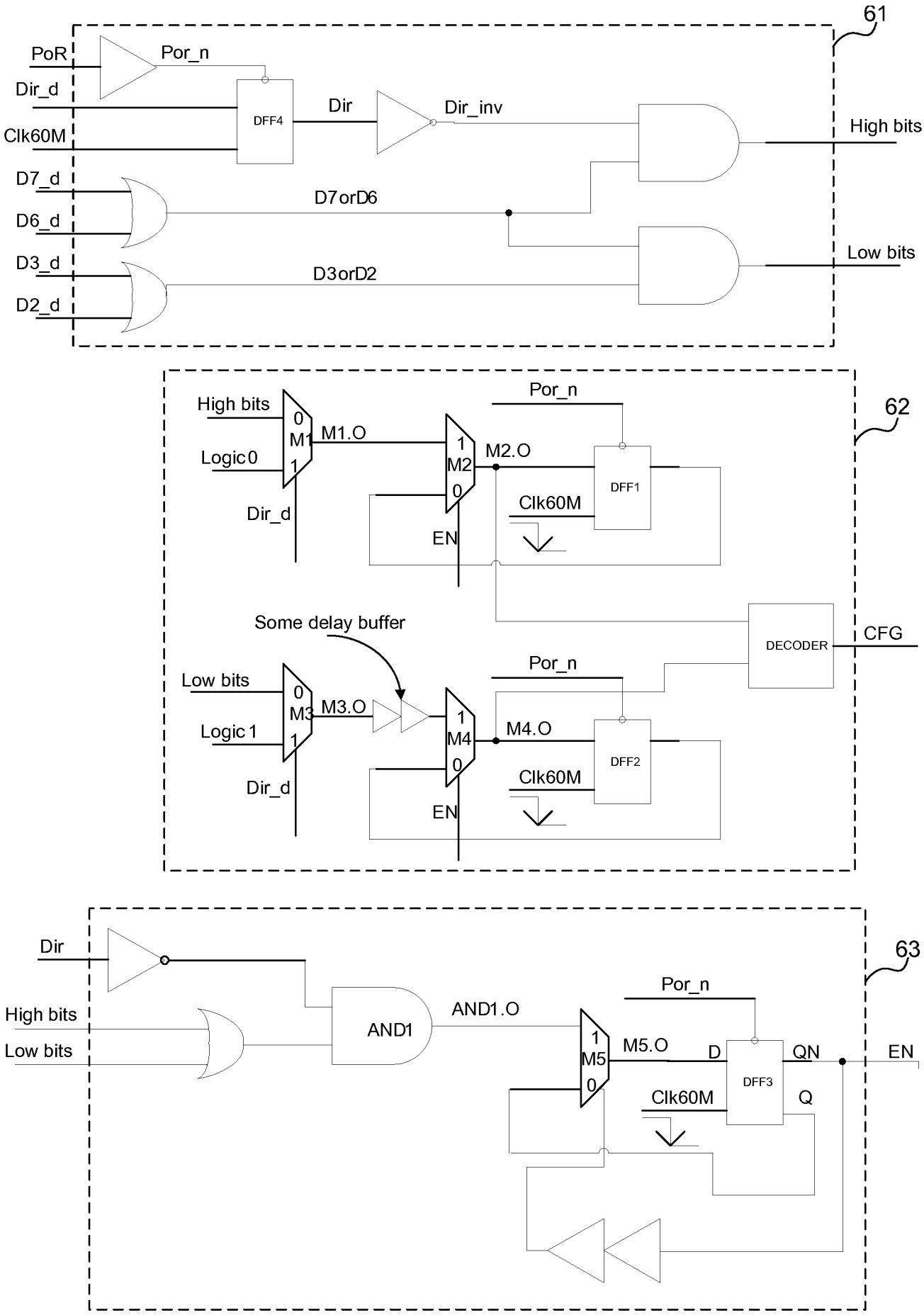
61
PoR
Por_n
Dir_d
DFF4
Dir
Dir_inv
Clk60M
High bits
D7_d
D7orD6
D6_d
D3_d
Low bits
D3orD2
D2_d
62
High bits
Por_n
0
M1
1
M1.O
Logic0
1
M2
0
M2.O
DFF1
Clk60M
Dir_d
EN
Some delay buffer
DECODER
CFG
Low bits
Por_n
0
M3
1
M3.O
Logic1
1
M4
0
M4.O
DFF2
Clk60M
Dir_d
EN
63
Dir
High bits
Low bits
AND1
AND1.O
Por_n
1
M5
0
M5.O
D
DFF3
QN
EN
Clk60M
Q

FIG. 5

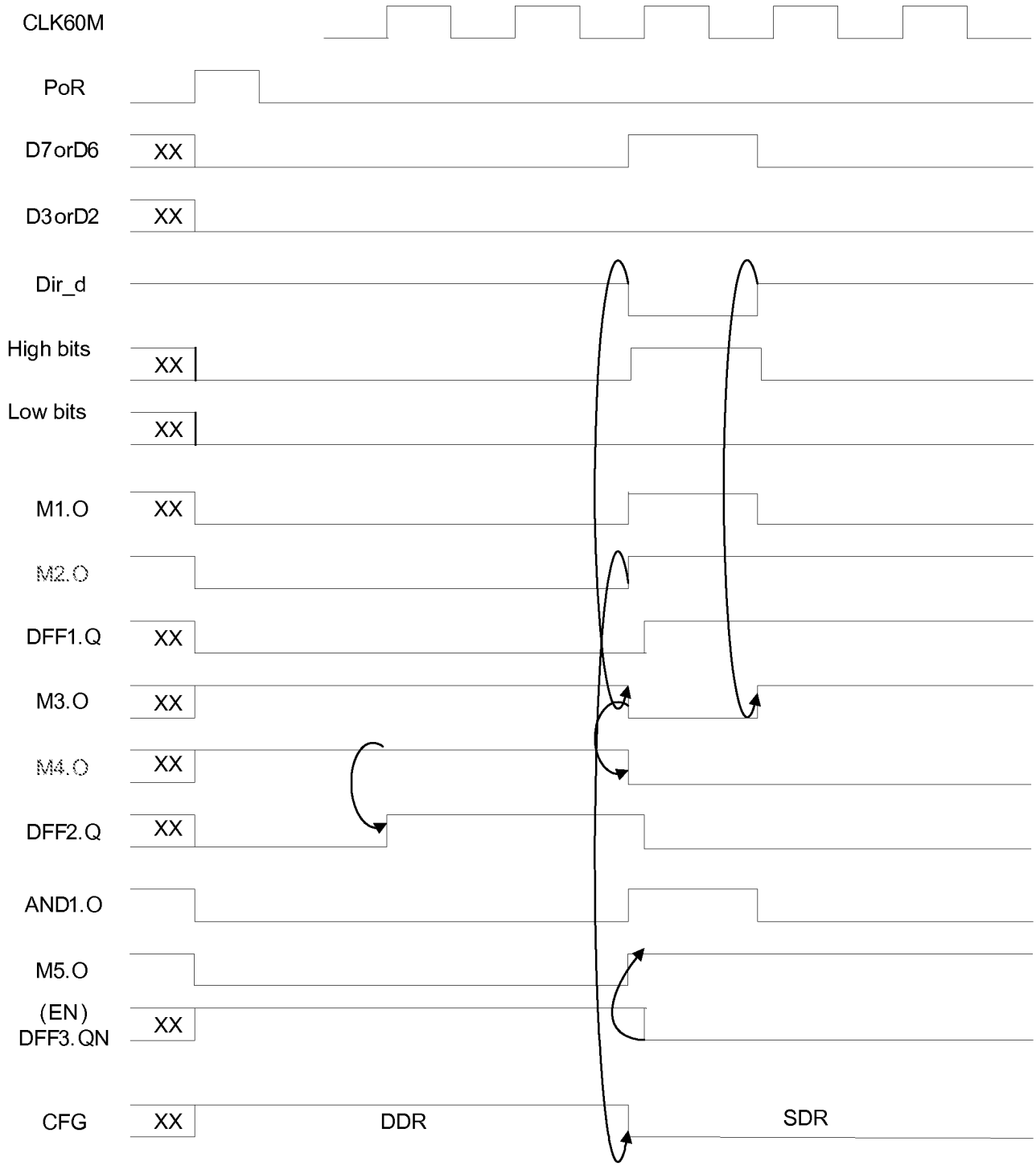
CLK60M
PoR
D7orD6
XX
D3orD2
XX
Dir_d
High bits
XX
Low bits
XX
M1.O
XX
M2.O
DFF1.Q
XX
M3.O
XX
M4.O
XX
DFF2.Q
XX
AND1.O
M5.O
(EN)
DFF3.QN
XX
CFG
XX
DDR
SDR

FIG. 6

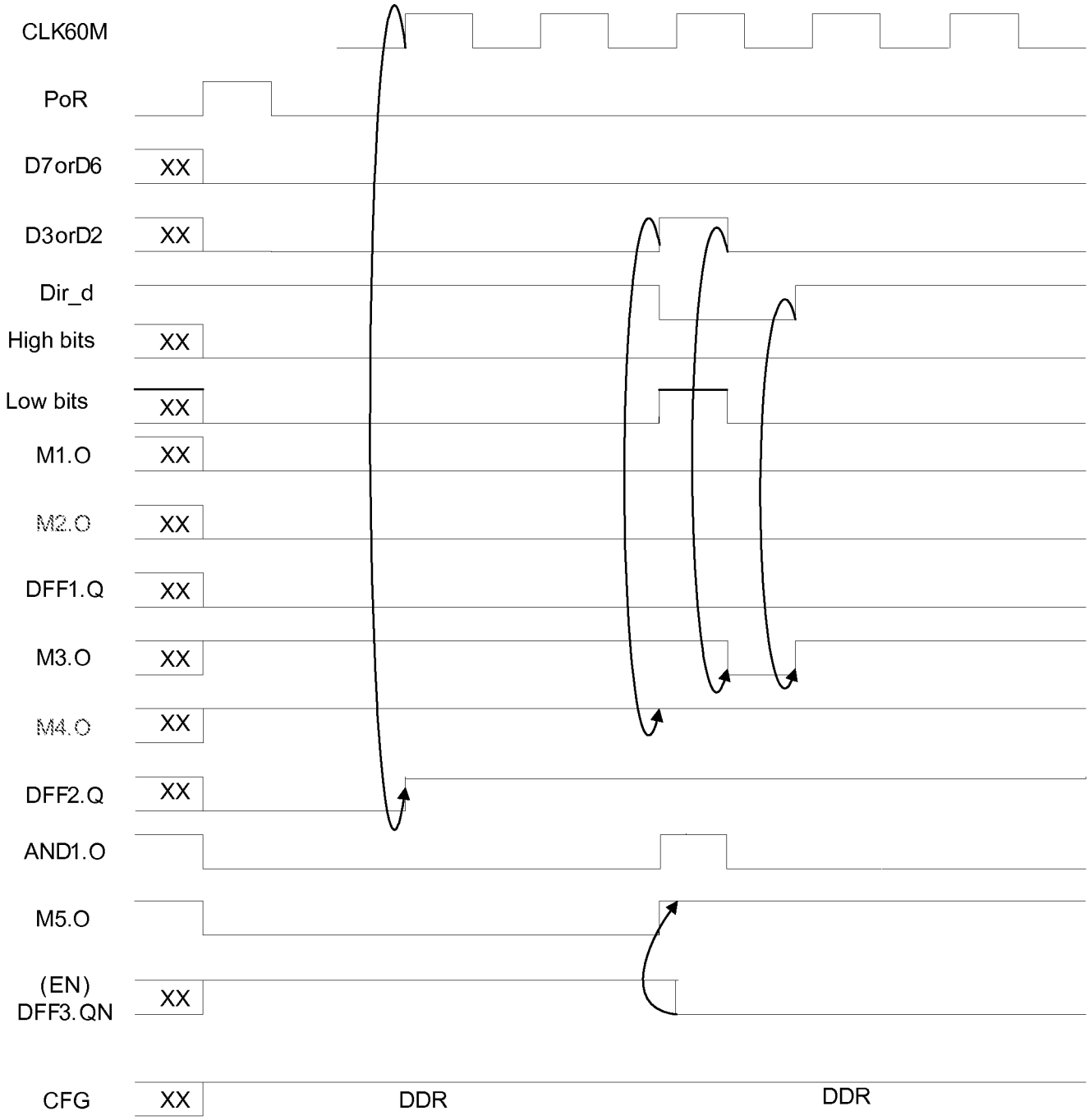
CLK60M
PoR
D7orD6
XX
D3orD2
XX
Dir_d
High bits
XX
Low bits
XX
M1.O
XX
M2.O
XX
DFF1.Q
XX
M3.O
XX
M4.O
XX
DFF2.Q
XX
AND1.O
M5.O
(EN)
DFF3.QN
XX
CFG
XX
DDR
DDR

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/055316

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/38 G06F13/42

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2004/051491 A1 (NOKIA CORP [FI]; MYLLY KIMMO [FI]; FLOMAN MATTI [FI]) 17 June 2004 (2004-06-17)	1-8, 12-15
Y	abstract page 10, line 10 - page 11, line 31 figure 3	9-11

X	EP 1 293 931 A2 (TOSHIBA KK [JP]) 19 March 2003 (2003-03-19)	1-8
Y	paragraphs [0042] - [0048] figure 8	9-11

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2010	12/02/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Albert, Jozsef

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/055316

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	STMicroelectronics: "HS USB ULPI transceiver" www.st.com August 2007 (2007-08), XP002566061 Retrieved from the Internet: URL:http://www.st.com/stonline/products/literature/bd/13859.pdf> [retrieved on 2010-01-29] the whole document -----	9-11

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2009/055316

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2004051491 A1	17-06-2004	AU 2003302513 A1	23-06-2004
		FI 20022113 A	06-08-2004
		US 2004137805 A1	15-07-2004
EP 1293931 A2	19-03-2003	DE 60221328 T2	17-04-2008
		JP 3813849 B2	23-08-2006
		JP 2003091703 A	28-03-2003
		US 2003056050 A1	20-03-2003