United States Patent [19]

Miller

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[45] **May 27, 1975**

[54] **BIPOLAR TRANSISTOR CONSTRUCTION METHOD**

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[73] Assignee: **TRW Inc.,** Redondo Beach, Calif.

[22] Filed: **May 25, 1973**

[21] Appl. No.: **363,995**

[52] **U.S. Cl.** **148/1.5;** 145/187; 357/91

[51] **Int. Cl.** **H011 7/54**

[58] **Field of Search** 317/235; 148/187, 1.5

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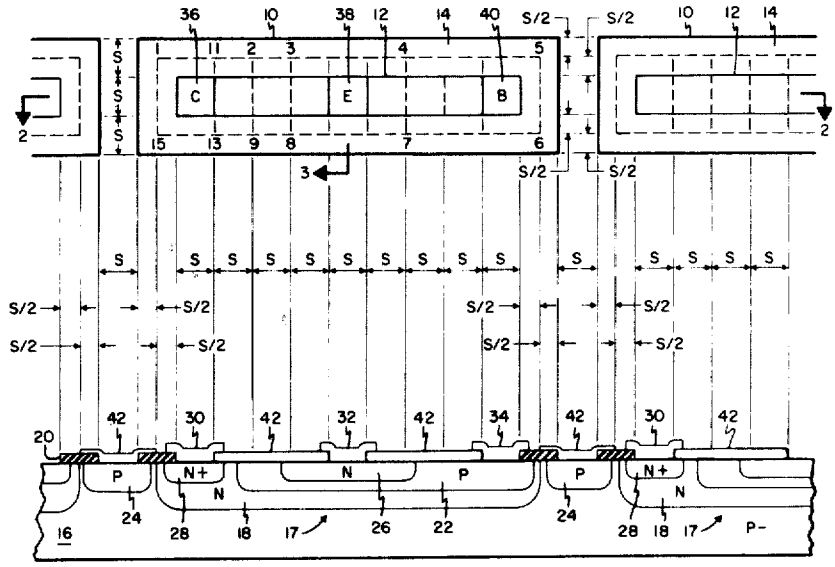
Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—J. M. Davis
Attorney, Agent, or Firm—Daniel T. Anderson; Jerry A. Dinardo; Stephen J. Koundakjian

[57] **ABSTRACT**

A layer of silicon nitride deposited on a semiconductive substrate is etched to form an opening that defines the outer boundaries of a diffused transistor. The silicon nitride layer serves as a permanent, fixed diffusion mask. The first diffusion is performed through the permanent mask opening. Thereafter, portions of the permanent mask opening are masked by depositing layers of silicon dioxide therein and subsequent diffusions are performed through different unmasked portions of the permanent mask opening.

12 Claims, 25 Drawing Figures



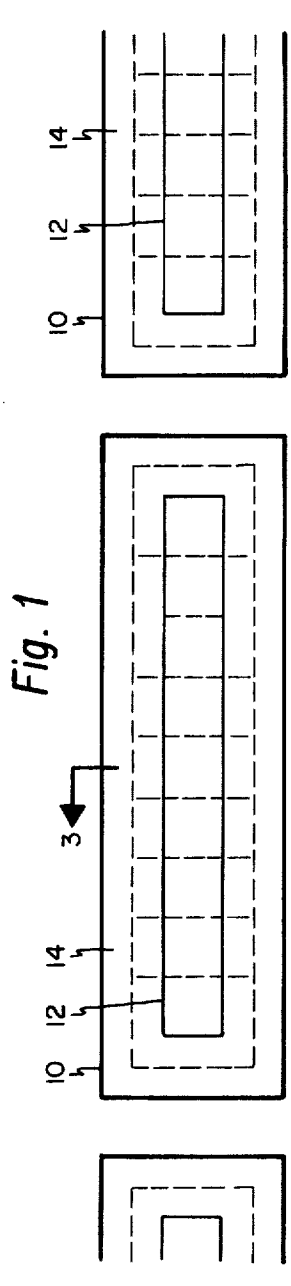


Fig. 1

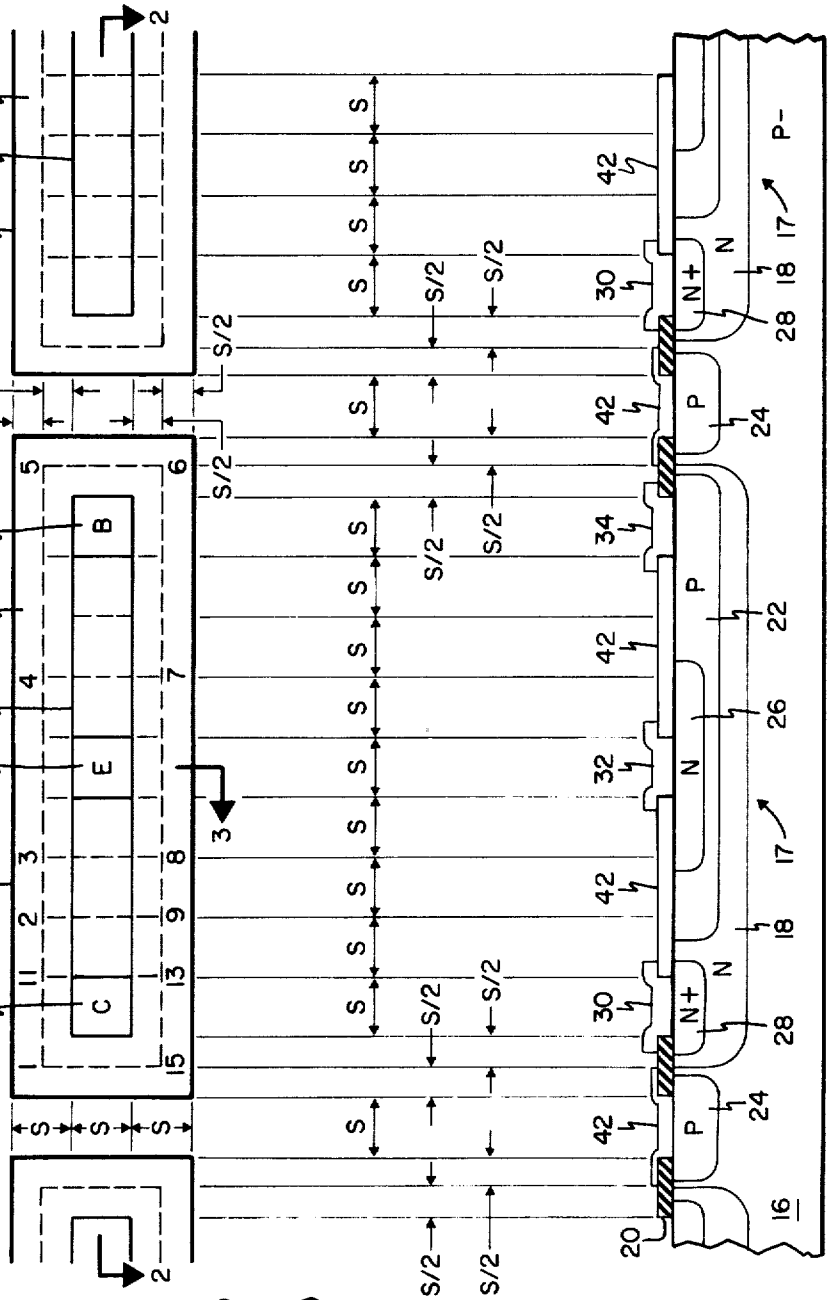


Fig. 2

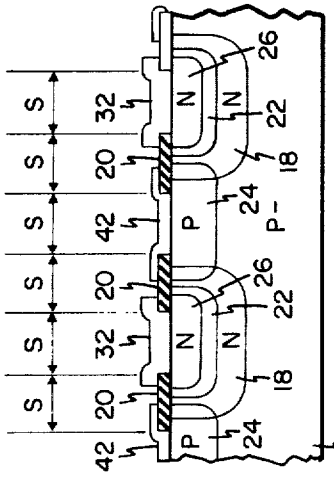


Fig. 3

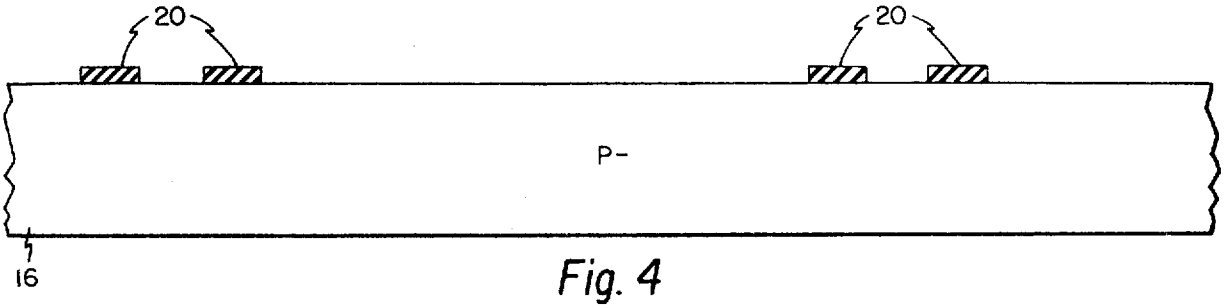


Fig. 4

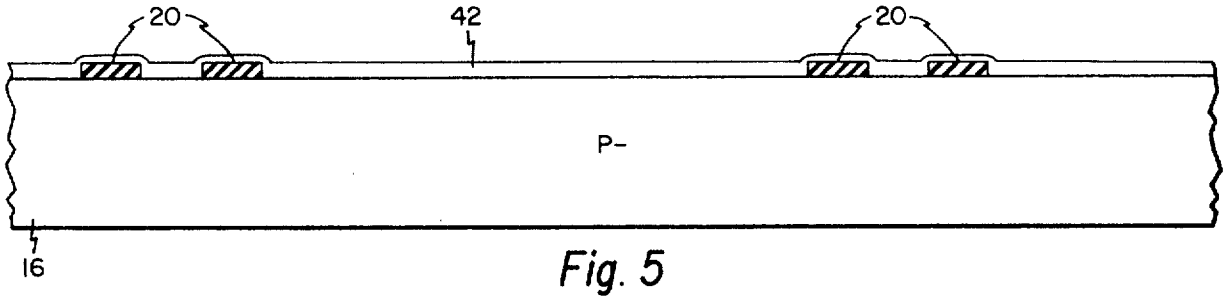


Fig. 5

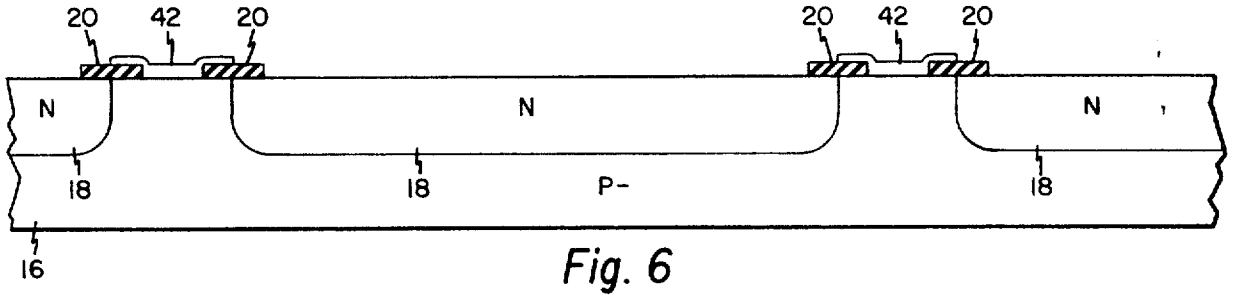


Fig. 6

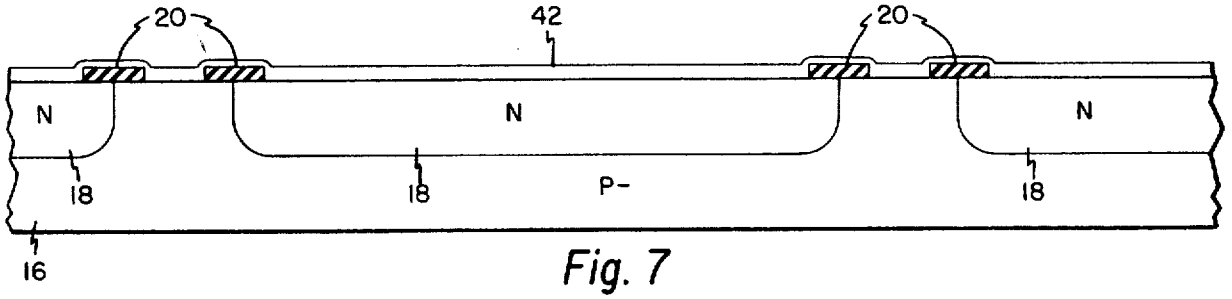


Fig. 7

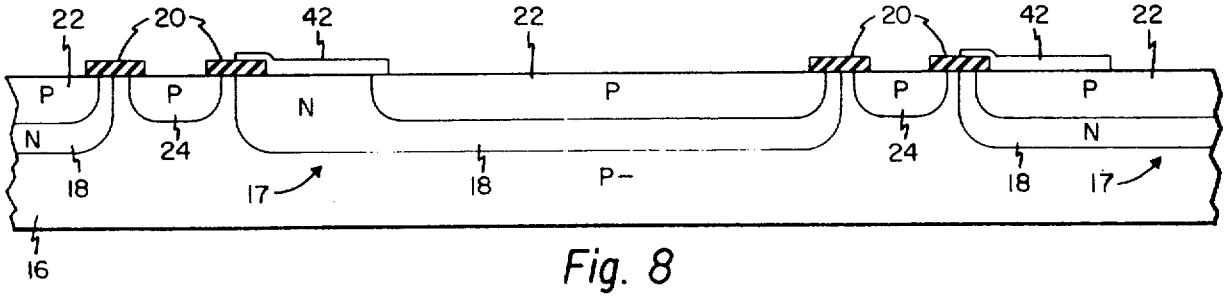


Fig. 8

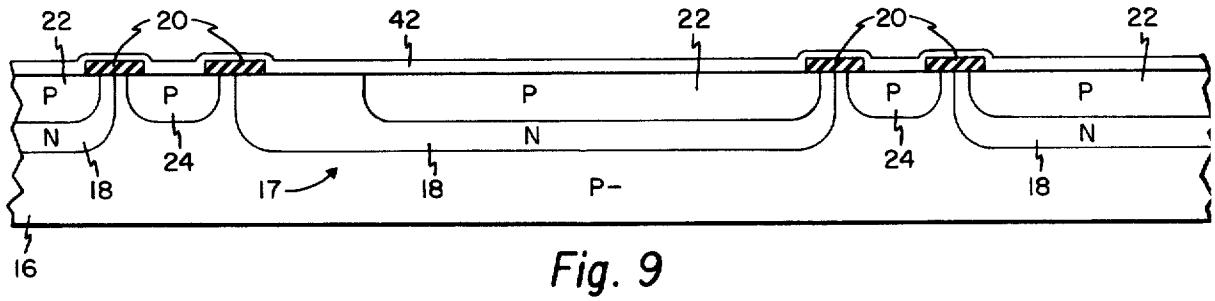


Fig. 9

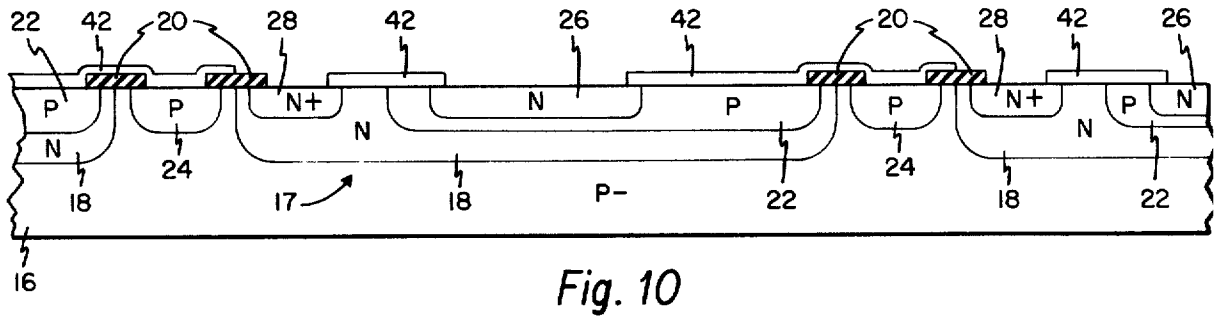


Fig. 10

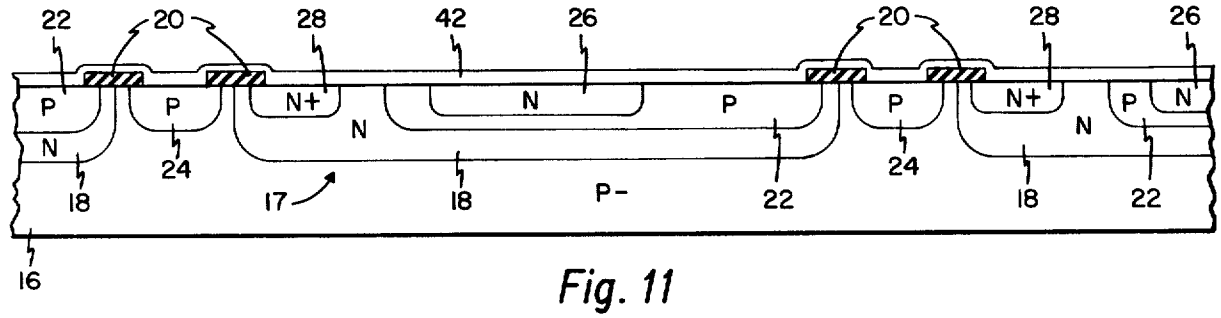


Fig. 11

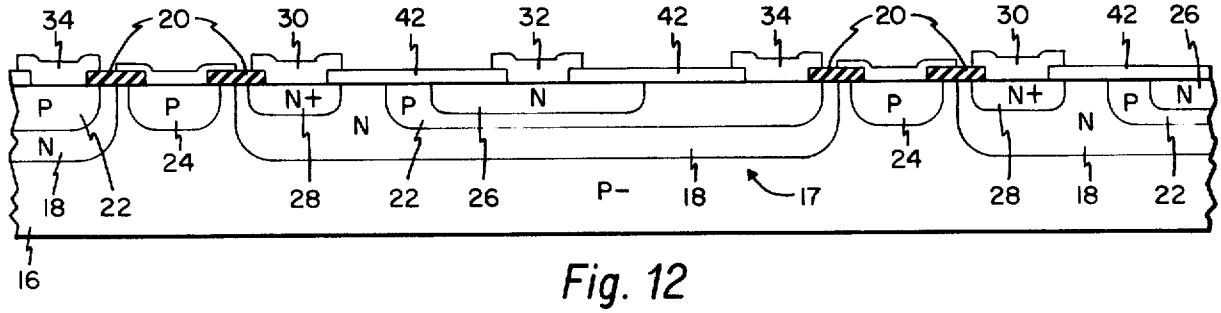


Fig. 12

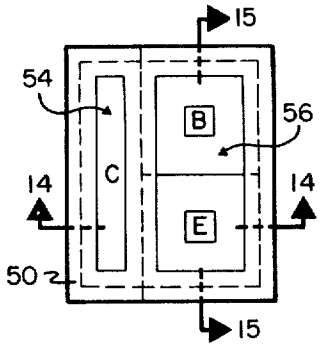


Fig. 13

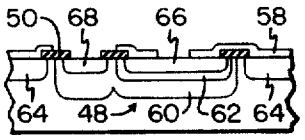


Fig. 14

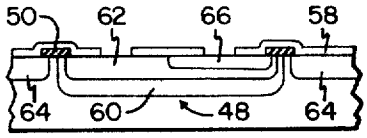


Fig. 15

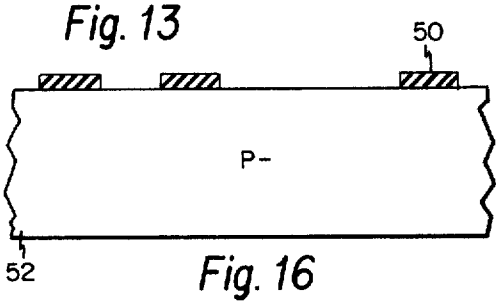


Fig. 16

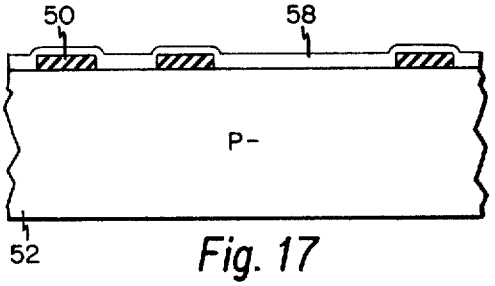


Fig. 17

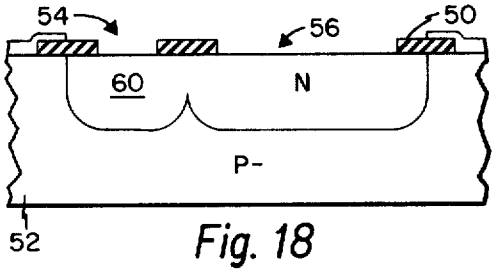


Fig. 18

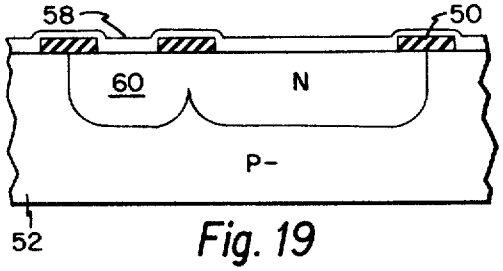


Fig. 19

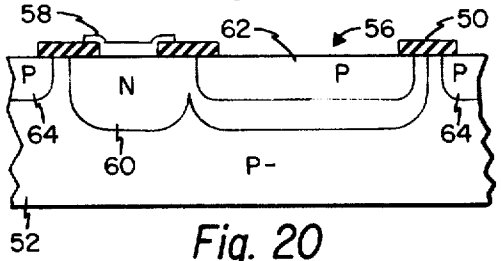


Fig. 20

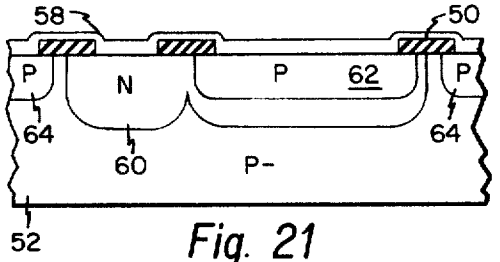


Fig. 21

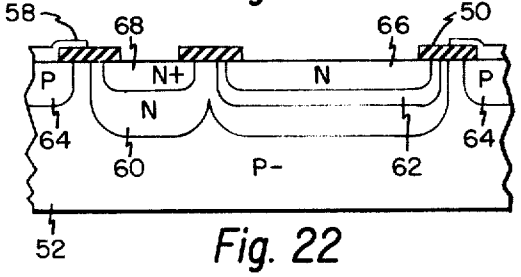


Fig. 22

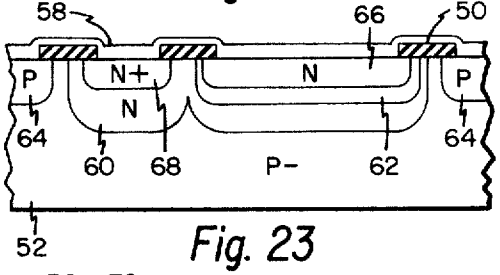


Fig. 23

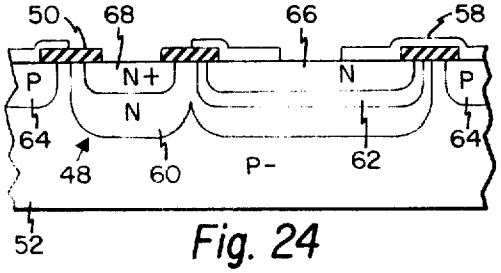


Fig. 24

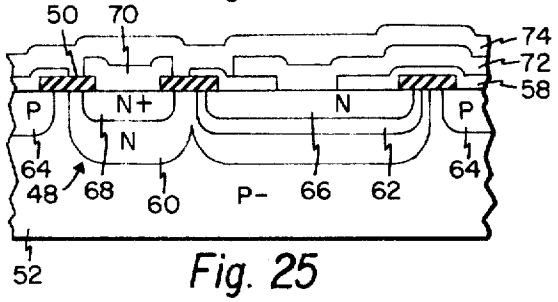


Fig. 25

BIPOLAR TRANSISTOR CONSTRUCTION METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

This application discloses subject matter that is similar in some respects to that disclosed in concurrently filed, copending application Ser. No. 364,148 of James L. Buie entitled BIPOLAR TRANSISTOR CONSTRUCTION METHOD, and assigned to the same assignee herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to LSI circuit construction of bipolar transistors, and more particularly to a method of fabricating such transistors which results in greatly reduced size.

2. Description of the Prior Art

There are presently two major objectives in current designs of large scale integrated circuits (LSI). First, to provide the maximum number of devices on a chip which is not so large as to be impractical to produce; and second, to maintain a specified operating speed while keeping the power dissipation low. For bipolar LSI, power dissipation is a severe problem. It is common to dissipate one milliwatt per device. For a chip containing 5,000 devices, this results in 5 watts of power dissipation per chip. It is apparent that this problem could become quite severe for chips containing 40 or 50 thousand devices.

Both of the problems given above can be attacked by reducing the size of an individual transistor. This allows more transistors to be placed upon a given sized chip and it reduces the parasitic capacitances of the transistor. The latter result permits operation at a given speed at a higher impedance level thereby resulting in lower power dissipation.

In conventional LSI circuit construction, bipolar transistors are fabricated by a process which involves several steps of selective impurity diffusion into a semiconductive body or substrate. This process is sometimes called a triple diffusion process because three separate diffusion steps are carried out to form the collector, base, and emitter regions, one within the other.

In order to define the regions where the diffusions will occur, a separate masking operation is performed for each of the several diffusions. The masking operation is performed by a photolithographic process that involves growing a masking oxide layer on the semiconductive substrate, coating the oxide layer with a photoresist, exposing the photoresist to light through a masking pattern, developing the photoresist pattern, and etching the oxide layer through the photoresist pattern until the semiconductor surface is bare. The oxide acts as a diffusion barrier and the diffusion regions are thereby defined when the wafer is subjected to a diffusant.

The primary factor limiting the reduction of the size of a triple diffused transistor is the registration tolerance of the photolithographic process. The fabrication of a triple diffused bipolar transistor can be thought of in a simplified form as analogous to the fabrication of three nested bath tubs referred to as collector, base, and emitter in descending size. The collector is the largest region and is diffused into the substrate. The base is intermediate in size and is diffused into the collector region. The emitter is the smallest region and is diffused into the base region.

An important design rule for a transistor is that the surfaces of the diffused regions or tubs must not touch one another. This requires that in the vertical dimension, the emitter diffusion layer is shallower than the base diffusion layer and the base diffusion layer is shallower than the collector diffusion layer. In the horizontal dimensions, it requires that the difference in size between adjacent regions or tubs be sufficient to assure that the tolerance with which they are placed within one another does not cause their edges to touch. This tolerance is the factor which limits the reduction of the size of triple diffused transistors.

SUMMARY OF THE INVENTION

In accordance with the invention, a process of self-alignment of the three diffused regions of a bipolar transistor is provided by establishing a single tolerance region for all three diffusion layers rather than individual tolerance regions between the adjacent diffusion layers. The single tolerance region so established defines an annular region where deposition is prohibited.

More specifically, in accordance with one embodiment, a silicon nitride layer deposited in a semiconductive substrate is provided in annular form with a single opening that defines the outer boundaries of the first diffusion region. The silicon nitride layer serves as a permanent mask for all three diffusions. For the first diffusion it serves as the sole mask within the transistor region. For the second diffusion, a portion of the opening in the silicon nitride layer is covered by a layer of silicon dioxide and the two layers comprising silicon nitride and silicon dioxide form a composite mask for the second diffusion. For the third diffusion, a second silicon dioxide layer is formed to cover a different portion of the opening in the silicon nitride layer. The composite mask formed by the silicon nitride layer and the new silicon dioxide layer defines the region for the third diffusion.

The only registration requirement for the silicon dioxide masks is that their edges must lie within the tolerance region established by the silicon nitride mask.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a top plan view of a portion of an LSI circuit incorporating an array of bipolar transistors of elongated extent;

FIG. **2** is a sectional view taken along line **2—2** of FIG. **1**;

FIG. **3** is a sectional view taken along line **3—3** of FIG. **1**;

FIG. **4–12** are sectional views illustrating the step by step fabrication of the LSI structure of FIGS. **1–3**;

FIG. **13** is a top plan view of a portion of an LSI circuit incorporating an array of bipolar transistors of square extent;

FIG. **14** is a sectional view taken along line **14—14** of FIG. **13**;

FIG. **15** is a sectional view taken along line **15—15** of FIG. **13**; and

FIGS. **16–25** are sectional views illustrating the step by step fabrication of the LSI structure of FIGS. **13–15**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIGS. **1–3** there is shown a portion

of an LSI circuit incorporating an array of bipolar transistors fabricated according to the method of the invention. The transistors are illustrated as being of the NPN type, although it is understood that the method of the invention is applicable as well to fabricating transistors of the PNP type. Each of the transistors in the top plan view of FIG. **1** is shown as being encompassed within a large elongated outer rectangle **10**, two of which are shown in full and four others being shown only partially. Lying concentrically within each large rectangle **10** is a smaller elongated inner rectangle **12**. The annular area **14** between the two rectangles **10** and **12** represents a tolerance region within which must lie the openings of masking structures for the several diffusions of the transistors.

Each annular area **14** represents the boundary of a permanent masking structure over which is superimposed other individual masking structures which serve to mask different portions of the area bounded by the inner rectangle **12**. The entire area within the inner rectangle **12** defines the region of the semiconductor or substrate that is exposed to the first impurity diffusion, whereas different portions of that rectangular area that are subsequently left unmasked serve to define the regions for the diffusions occurring after the first diffusion. More particularly, the annular area **14** is formed by selective deposition of silicon nitride, and portions of the area within the inner rectangle **12** are masked by selectively forming silicon dioxide thereon.

The width of the inner rectangle **12** is identified as having a dimension "S", and the length thereof is divided into nine equal parts, each with a length equal to the dimension S. The large rectangle **10** is spaced from the smaller rectangle **12** by the dimension S. All of the large rectangles **10** are spaced from each other longitudinally and laterally by the same distance equal to the dimension S. The dimension S represents the smallest dimension practical for registration tolerances, which according to the present state of the art is 0.1 mil. The significance of the dimension S will become clearer as the description of the fabrication of the transistor structure proceeds.

Reference is now made to FIGS. **2** and **3** which show sectional views of the transistor structure. The LSI bipolar transistor array includes a substrate **16** or body of semiconductive material, in this case P type silicon. The substrate **16** contains a multiplicity of transistors **17** that are formed by diffusing various impurities in different regions of the substrate.

In the first operation, collector regions **18** are formed by diffusing an N type impurity within the substrate **16**. This is accomplished by forming a permanent mask **20** of silicon nitride in the regions represented by the annular areas **14** and then superimposing a second mask of silicon dioxide over the permanent mask **20** and portions of the substrate **16**, leaving only a rectangular opening concentrically between the rectangles **10** and **12**. In FIG. **1**, this first rectangular opening is represented by a horizontal line between points **1** and **5**, a vertical line between points **5** and **6**, a horizontal line between points **6** and **15**, and a vertical line between points **15** and **1**.

In the second operation, base regions **22** are formed by diffusing a P type impurity within the collector region **18**. This is accomplished by superimposing a mask of silicon dioxide over the permanent mask **20** and portions of the substrate **16**, leaving a rectangular opening between points **2, 5, 6, 9** and leaving exposed all of the substrate regions between the large rectangles **10**. The rectangular opening is represented by a horizontal line between points **2** and **5**, a vertical line between points **5** and **6**, a horizontal line between points **6** and **9**, and a vertical line between points **9** and **2**. In addition to forming the P type collector regions **22**, this P type diffusion forms P type isolation regions **24** surrounding each of the transistors **17**.

In the third operation, an N type impurity diffusion is performed to form an N type emitter region **26** within the base region **22** and an N+ type collector contact region **28** within the collector region **18**. This diffusion is accomplished by superimposing a mask of silicon dioxide over the permanent mask **20** and portions of the substrate **16**, leaving a rectangular opening between points **3, 4, 7, 8** and another rectangular opening between points **1, 11, 13, 15**. One rectangular opening is represented, for example, by a horizontal line between points **3** and **4**, a vertical line between points **4** and **7**, a horizontal line between points **7** and **8**, and a vertical line between points **8** and **3**.

Finally, ohmic metallic contacts are made to the collector, emitter and base regions respectively. Thus a collector contact **30** is made to the collector region **18** by depositing metal on the collector contact region **28**; an emitter contact **32** is made to the emitter region **26** by depositing metal on the emitter region **26**; and a base contact **34** is made to the base region **22** by depositing metal on the base region **22**. The ohmic metallic contacts to the semiconductor, collector, emitter, and base regions are made by superimposing a silicon dioxide contact mask over the permanent mask **20** and over all semiconductor surface regions. The square surface areas **36, 38, 40** exposing portions of the collector contact region **28**, emitter region **26** and base region **22** respectively, are formed by regions left open in both the permanent mask **20** and the silicon dioxide contact mask. The silicon dioxide mask is indicated by the reference numeral **42** in FIGS. **2** and **3**. In FIG. **1**, the surface areas **36, 38, 40** are also labeled C, E, B, respectively, to indicate where contacts are made to the collector, emitter, and base.

Reading from left to right in FIGS. **1** and **2** it is seen that a spacing S is provided to form the diffused isolation region **24**. Another spacing S is provided to space the isolation region **24** from the collector contact region **28**, and yet another spacing S is provided to form the collector contact region **28**. A spacing S is provided to space the collector contact region **28** from the base region **22**, and another spacing S spaces the base region **22** from the emitter region **26**. Finally, a spacing S is provided to space the emitter contact **32** from the edge of the emitter region **26** and another spacing S is provided to form the emitter contact **32**. A spacing of S/2 is provided between the innermost edge of the permanent mask **20** and the innermost edge of the silicon dioxide mask **42** to allow a tolerance region for misregistration of the masks.

Referring to FIG. **3**, a space S is provided to form the emitter contact **32**, another space S is provided to space the isolation region **24** from the base region **22**, and another space S is provided to form the isolation region **24**. The isolation regions **24** and the collector regions **18** are allowed to overlap without any adverse effects.

Reference will now be made to FIGS. 4–12 for a step by step description of the process of fabricating the transistor 17 according to the invention. On a substrate 16 of silicon that is doped with a P type impurity, such as boron, there is formed a permanent mask 20 of silicon nitride, as shown in FIG. 4. The mask 20 is preferably formed by a photolithographic technique well known in the semiconductor art.

According to this art, a thin layer of silicon dioxide of about 400 to 500 Angstroms thick is first formed on the semiconductive surface, and then a continuous layer of silicon nitride is formed on the silicon dioxide layer. The silicon dioxide layer is needed to stabilize the silicon semiconductive surface electrically, for if the silicon nitride is laid down directly on the silicon substrate, it would tend to exchange charge with the silicon. The silicon nitride layer is formed by reacting silicon tetrachloride ($SiCl_4$) with ammonia (NH_3) to form silicon nitride (Si_3N_4). Hydrochloric acid gas is given off as a byproduct. A layer of silicon nitride is formed that is about 3,000 angstroms thick.

The layer of silicon nitride is covered with 500 A of silicon dioxide which in turn is covered by photo-resist. The photoresist is patterned and then used as a mask to etch the silicon dioxide. The silicon dioxide is then used as a mask to etch the silicon nitride using hot phosphoric acid. The thin silicon dioxide layer that is left exposed is then etched away with buffered hydrofluoric acid.

The next operations involve forming the several masks of silicon dioxide for selective diffusion of impurities to form the collector, base, and emitter regions. Turning now to FIG. 5, the substrate 16 and permanent mask 20 are coated with a continuous layer 42 of silicon dioxide. The silicon dioxide layer 42 may be thermally grown by heating the substrate 16 in oxygen saturated with water vapor. For forming a layer 42 that is 2,000 angstroms thick, the substrate 16 may be heated at 900°C for about 1 hour. It should be noted that the silicon dioxide layer that forms on the silicon nitride layer is only a small fraction of the thickness of oxide layer that is formed on the bare silicon.

By a photolithographic masking and etching technique similar to that described above, portions of the silicon dioxide layer 42 are removed from the regions of the substrate 16 where diffusions are to occur to form the collector regions. As shown in FIG. 6, the silicon dioxide layer 42 is left standing in regions where no diffusions are to occur. The state of the process shown in FIG. 6 corresponds to the formation in FIG. 1 of a silicon dioxide mask superimposed on the permanent mask 20, with the edges of the silicon dioxide mask forming a rectangular opening running between points 1, 5, 6, 15. Buffered hydrofluoric acid is used to etch the silicon dioxide layer 42. The silicon nitride layer is left intact during this etching operation because it is selectively inert in the hydrofluoric acid etchant.

FIG. 6 also illustrates the next step which is to diffuse an N type impurity into the P type substrate 16, shown as a P- region, to form the collector regions 18 which define the extent of each transistor 17. The collector regions 18 may be formed, for example, either by thermally diffusing arsenic into the semiconductor substrate 16 or by implanting phosphorous ions into the substrate and thereafter thermally distributing the impurity atoms. The ion implantation process has certain advantages in that the concentration of impurities is more uniform over the region and more controllable.

After the collector regions 18 are formed, another silicon dioxide layer 42 is grown to cover the substrate 16, as shown in FIG. 7. Next, portions of the silicon dioxide layer 42 are removed to define the regions where the next diffusion is to occur to form the base regions. This stage of the process is shown in FIG. 8 and corresponds to the formation in FIG. 1 of a silicon dioxide mask over portions of the substrate 16 and within the inner rectangle 12, leaving a rectangular opening between points 2, 5, 6, 9 and leaving exposed all of the regions between the large rectangles 10 that are not covered by the permanent mask.

The next step in the process is to convert a portion of the N type collector regions 18 into the P type base regions 22, and also to form the P type isolation regions 24 within the P- region of the substrate 16 so that the isolation regions 24 surround the transistors 17. This is done by thermally diffusing a P type impurity such as boron.

After the base regions 22 and the isolation regions 24 are formed, another silicon dioxide layer 42 is grown to cover the substrate 16, as shown in FIG. 9. Next, portions of the silicon dioxide layer 42 are removed to define the regions where the next diffusion is to occur to form the emitter regions and the collector contact regions. This stage of the process is shown in FIG. 10, and corresponds to the formation in FIG. 1 of a silicon dioxide mask over the permanent mask 20 and portions of the substrate 16, leaving a rectangular opening between points 3, 4, 7, 8, and another rectangular opening between points 1, 11, 13, 15.

The next step of the process is also shown in FIG. 10 and that is the diffusion of an N type impurity, such as arsenic or phosphorus, to form the emitter regions 26 within the P type base regions 22 and also the N+ collector contact regions 28 within the collector regions 18.

After the emitter regions 26 and collector contact regions 28 are formed, the next step in the process is to cover the substrate 16 with another silicon dioxide layer 42, as shown in FIG. 11. Portions of the silicon dioxide layer 42 are then removed to define the regions where ohmic contacts will be made to the collector, base, and emitter by depositing metal thereon. As shown in FIG. 12, which is similar to FIG. 2, holes are formed in the silicon dioxide layer 42 over the N+ collector contact region 28, over the emitter region 26 and over the base region 22. In these holes are deposited metallic contacts which are identified as collector contact 30, emitter contact 32, and base contact 34. The metallic contacts may extend over the silicon dioxide layer 42 in the form of strips or bands to form various desired interconnection paths.

By way of example, typical values of resistivity, depth junction and surface impurity concentration will now be given. The resistivity of the substrate is 3 ohm-centimeters corresponding to a concentration of boron impurity atoms of 2×10^{15} per cubic centimeters (cm^3). For the first diffusion, the N type region 18 has a depth of its junction with the P type zone of the substrate 16 from the surfaces of the substrate 16 of 4.2×10^{-4} cm. The sheet resistance of the N type region 18 is 88 ohms per square with a surface concentration of 1.8×10^{18} impurity atoms per cm^3.

For the second diffusion, the sheet resistance of the P type region 22 and P region 24 is 116 ohms per

square and the depth of the junctions from the surface is 1.9×10^{-4} cm. The surface concentration is 1.5×10^{19} boron atoms per cm^3. Finally, for the third diffusion, the sheet resistance of the N type region **26** and N+ type region **28** is 4.2 ohms per square. The producibility is improved when the permanent work is not used to form the edge of the metallic contact. This leaves a larger space between the junction and the metal, thereby permitting greater anomalies of diffusion of the metal into the silicon. The parasitic collector resistance can be reduced by moving the collector contact from the end opposite the base contact to the side of the transistor. The depth of the junctions from the surfaces is 1.4×10^{-4} cm and the concentration of impurity atoms per cm^3 is 1.5×10^{21}.

The P isolation regions **24** are needed to isolate the transistors from each other. If the P isolation regions **24** were omitted, the lightly doped P regions where they are omitted normally contain a thin surface layer of N type conductivity that causes conducting channels to form between the transistors. The P isolation regions **24** prevent these conducting channels from forming.

While silicon nitride is preferred as the material for the permanent mask **20**, it is possible to use other materials that are relatively inert in the etchant used for the silicon dioxide. Such other materials may include zirconium dioxide (ZrO_2) or aluminum oxide (Al_2O_3).

The thin elongated transistor structure above described has the virtue of greatly reduced size. However, in some cases it may be preferred to sacrifice some space saving in order to improve performance and producibility. A structure with both of the above modifications and its fabrication process will now be described with reference to FIGS. **13–25.** For simplicity, only one transistor **48** is shown and the formation of the isolation regions will only be referred to generally and not in detail. Referring to FIGS. **13–25,** a permanent mask **50** of silicon nitride is formed on a P type semiconductor substrate **52.** The permanent mask **50** is annular and generally square overall, but has two openings **54** and **56** instead of one, much in the fashion of a figure eight. One of the openings **56** is wider than the other opening **54.**

Over the substrate **52** and permanent mask **50** is deposited a continuous layer **58** of silicon dioxide as shown in FIG. **17.** The silicon dioxide layer **58** is then etched away in regions to prepare the substrate for the first diffusion, as shown in FIG. **18.** For this diffusion, both openings **54** and **56** in the permanent mask **50** are left uncovered, and an N type diffusion is performed so that the two regions beneath the openings **54** and **56** merge into a single N type collector region **60.**

The substrate **52** and permanent mask is again coated with a silicon dioxide layer **58** as shown in FIG. **19,** and the silicon dioxide layer **58** is etched once again preparatory to the second diffusion. As shown in FIG. **20,** the second diffusion is P type to form a base region **62** beneath the larger opening **56** while masking the smaller opening **54.** During this same diffusion, it is preferred to form the P isolation regions **64** surrounding the transistor **48.**

The next steps are to grow another silicon dioxide layer **58** as shown in FIG. **21,** and then etch the layer **58** preparatory to the third diffusion as shown in FIG. **22.** The third diffusion is N type and forms the N type emitter region **66** within a half portion of the P type base region **62** by masking one half of the large opening **56,** as shown more clearly in FIGS. **13** and **15.** The third diffusion also forms the N+ type collector contact region **68** through the unmasked smaller opening **54.**

FIGS. **23** through **25** illustrate the location and formation of the metallic contacts for the elements of the transistor **48.** This procedure involves forming another silicon dioxide layer **58,** etching the layer **58** to form holes registered with the collector, base, and emitter regions, and depositing metallic contacts in those holes. FIG. **25** shows a collector contact **70,** an emitter contact **72,** and a passivating layer **74** of silicon dioxide. The base contact, which is not shown, is deposited in the region labeled B in FIG. **13.** The regions labeled C and E indicate the location of the collector contact **70** and emitter contact **72.**

What is claimed is:

1. A method of fabricating a bipolar transistor in integrated circuit form by a triple deposition process, comprising:

A. forming on a semiconductor substrate surface of first conductivity type a permanent mask from a layer of a first masking material having an inner boundary defining a rectangular opening of predetermined length and width and an outer boundary spaced equidistant from said inner boundary, said inner and outer boundaries defining an annular tolerance region within which must lie edges of subsequent masks of a second material, said first masking material being readily etchable by a first etchant but not by a second etchant;

B. superimposing over said permanent mask a first mask of a second masking material with all four edges thereof lying within said tolerance region so as to mask regions in said substrate surrounding said permanent mask while leaving unmasked the entire area of said substrate lying within said rectangular opening, said second masking material being readily etchable by said second etchant but not by said first etchant;

C. introducing firstly an impurity of second conductivity type through said rectangular opening to form a collector region of second conductivity type within said substrate;

D. superimposing over said permanent mask a second mask of said second masking material with at least one edge thereof crossing said rectangular opening and with the remaining edges thereof lying within said tolerance region so as to partially mask said rectangular opening while leaving unmasked only an area portion of said collector region;

E. introducing secondly an impurity of said first conductivity type into the unmasked area portion of said collector region to form a base region of said first conductivity type within said collector region;

F. superimposing over said permanent mask a third mask of said second masking material with at least three edges thereof crossing said rectangular opening and with the remaining edges thereof lying within said tolerance region so as to partially mask said rectangular opening while leaving unmasked an area portion only of said collector region and an area portion only of said base region; and

G. introducing thirdly an impurity of said second conductivity type into the unmasked area portions of said collector and base regions to form a collector contact region within said collector region and

an emitter region within said base region, respectively.

2. The invention according to claim 1, wherein said first masking material is silicon nitride and said second masking material is silicon dioxide.

3. The invention according to claim 1, wherein at least one of said impurity deposition steps is performed by ion implantation.

4. The invention according to claim 1, wherein at least one of said impurity deposition steps is performed by diffusion.

5. A method of fabricating a bipolar transistor in integrated circuit form by a triple deposition process, comprising:

A. forming on a semiconductor substrate of first conductivity type a permanent mask from a layer of silicon nitride having an inner boundary defining a rectangular opening of width S and length 9S, and an outer boundary, spaced a distance S from said inner boundary, where S is about 0.1 mil, said inner and outer boundaries defining an annular tolerance region within which must lie edges of subsequent masks of silicon dioxide, said rectangular opening being capable of division into nine square zones of equal area arranged in a row and identified as zones 1 through 9 taken consecutively;

B. superimposing over said permanent mask a first mask of silicon dioxide with all four edges thereof lying within said tolerance region so as to mask regions of said substrate surrounding said permanent mask while leaving unmasked the entire surface of said substrate lying within said rectangular opening;

C. performing a first impurity deposition of second conductivity type through all nine zones of said rectangular opening to form a collector region of second conductivity type within said substrate;

D. superimposing over said permanent mask a second mask of silicon dioxide with one edge thereof crossing said rectangular opening and with the remaining edges lying within said tolerance region so as to mask areas of said substrate surface coinciding with zones 1 and 2;

E. performing a second impurity deposition of first conductivity type through zones 3 through 9 of said rectangular opening to form a base region within said collector region;

F. superimposing over said permanent mask a third mask of silicon dioxide with three edges thereof crossing said rectangular opening and with the remaining edges lying within said tolerance region so as to mask areas of said substrate surface coinciding with zones 2, 3, 7, 8, 9 of said rectangular opening;

G. performing a third impurity deposition of second conductivity type through zones 1, 4, 5, 6 of said rectangular opening to form a collector contact region within said collector region and an emitter region within said base region;

H. superimposing over said permanent mask a fourth mask of silicon dioxide with four edges thereof crossing said rectangular opening and with the remaining edges thereof lying within said tolerance region so as to mask areas of said substrate surface coinciding with zones 2, 3, 4, 6, 7, 8 of said rectangular opening; and

I. depositing metal through zones 1, 5, 9 of said rectangular opening to form metallic contacts to said collector contact, emitter, and base regions, respectively.

6. The invention according to claim 5, wherein said semiconductor substrate is formed of P type silicon and said first, second, and third impurity depositions are performed by depositing an N type impurity, a P type impurity, and an N type impurity, respectively.

7. The invention according to claim 5, and further including the step of depositing an impurity of first conductivity type in a region of width S surrounding said mask to form an isolation region.

8. The invention according to claim 7, wherein said further impurity deposition step is performed simultaneously with said second impurity deposition.

9. A method of fabricating a bipolar transistor in integrated circuit form by a triple deposition process, comprising:

A. forming on a semiconductor substrate surface of first conductivity type a permanent mask from a layer of a first masking material in the form of a rectangular figure eight with one rectangular opening thereof being wider than the other one, said mask having an outer boundary spaced equidistant from each opening by a distance equal to the spacing between said openings to define a tolerance region within which must lie the edges of subsequent masks, said first material being readily etchable by a first etchant but not a second etchant;

B. superimposing over said permanent mask a first mask of a second masking material with all edges thereof lying within said tolerance region so as to mask regions of said substrate surrounding said permanent mask while leaving unmasked the entire area of said substrate lying within said figure eight, said second masking material being readily etchable by said second etchant but not by said first etchant;

C. performing a first impurity deposition of second conductivity type through both said rectangular openings to form a collector region within said substrate;

D. superimposing over said permanent mask a second mask of said second masking material with all edges thereof lying within said tolerance region surrounding the wider one of said rectangular openings so as to mask the narrower one of said rectangular openings;

E. performing a second impurity deposition of first conductivity type through said wider rectangular opening to form a base region within said collector region;

F. superimposing a third mask of said second masking material over said permanent mask with one edge thereof crossing said wider rectangular opening and the remaining edges lying within said tolerance region so as to mask approximately a half area portion of said wider rectangular opening as measured along its length; and

G. performing a third impurity deposition of second conductivity type through the unmasked half of said wider rectangular opening to form an emitter region within said base region and through said narrower opening to form a collector contact region within said collector region.

10. The invention according to claim 9, wherein said permanent mask is formed by depositing and etching a layer of silicon nitride on said semiconductor substrate.

11. The invention according to claim 10, wherein said rectangular openings are masked by superimposing layers of silicon dioxide over said permanent mask and thereafter selectively etching said silicon dioxide layers.

12. The invention according to claim 9 and further including the steps of applying metallic contacts to said collector contact, base, and emitter regions, respectively.

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