Title: PROCESSING DEVICE WITH RESTRICTED POWER DOMAIN WAKEUP RESTORE FROM NONVOLATILE LOGIC ARRAY

Abstract: A processing device handles two or more operating threads. A non-volatile logic controller (1806) stores first program data from a first program in a first set of non-volatile logic element arrays (1812) and second program data from a second program in a second set of non-volatile logic element arrays (1814). The first program and the second program can correspond to distinct executing threads, and the storage can be completed in response to receiving a stimulus regarding an interrupt for the computing device apparatus or in response to a power supply quality problem for the computing device apparatus. When the device needs to switch between processing threads, the non-volatile logic controller (1806) restores the first program data or the second program data from the non-volatile logic element arrays (1810) in response to receiving a stimulus regarding whether the first program or the second program is to be executed by the computing device apparatus.
Declarations under Rule 4.17:

— as to applicant’s entitlement to apply for and be granted a patent (Rule 4.17(H))

— as to the applicant’s entitlement to claim the priority of the earlier application (Rule 4.17(H))

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