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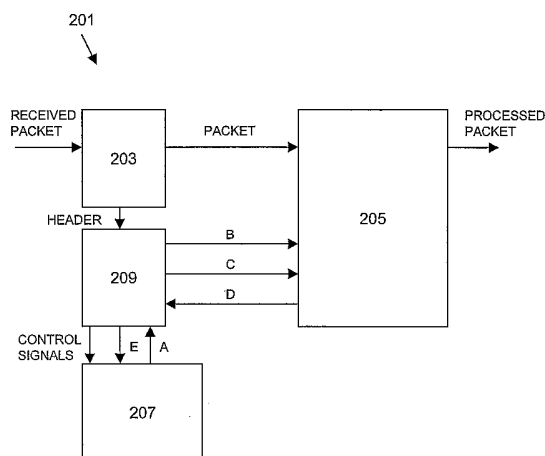
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(54) Title: IMPROVEMENTS IN AND RELATING TO DATA PROCESSING



(57) Abstract: There is provided a method and apparatus for receiving and processing data packets. Each data packet comprises an instruction portion, the instruction portion defining processing instructions for the data packet. The processing instructions may include mask data defining any sections of the instruction portion which are not to be used in comparison with other instruction portions. When a data packet is received, the instruction portion of the received data packet is compared with instruction portions stored in a memory, which stores already processed instruction portions together with the associated processing instructions. If the received instruction portion matches an instruction portion stored in the memory, the processing instructions can be used, thereby bypassing the processing of a packet whose instruction portion has already been processed. If the received instruction portion does not match an instruction portion stored in the memory, the data packet can be processed as usual and the instruction portion and processing instructions can be stored in the memory for later use.

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Improvements in and relating to Data Processing

Field of the Invention

The invention relates to a method and apparatus for receiving and processing
5 data packets. In particular, the invention relates to a method and apparatus for
receiving and processing data packets, each data packet including an
instruction portion defining processing instructions for the data packet.

Background of the Invention

- 10 For network processing, switching, routing and inter working silicon devices, it is
well known that important considerations are the chip size and the power
consumption, as increased chip size and power consumption obviously
increase costs.
- 15 In known arrangements for receiving and processing data, the buffer memory
must be big enough to store all the received data while processing it. In
addition, the processing power has to be fast enough so that the buffer memory
(in the software, firmware or hardware) does not overflow. One such known
arrangement for receiving and processing data packets is shown schematically
20 in Figure 1. The arrangement 101 includes a receiver 103 and a processor 105
connected to the receiver 103. The receiver 103 receives the incoming data
packets. Each packet is sent to the processor 105 where it is processed and
then dealt with appropriately.
- 25 In the arrangement of Figure 1, every single data packet has to be processed
by the processor 105. Processing of each packet may require many processing
cycles for parsing it, performing memory look ups for example to detect
destinations or exceptions, analyzing protocol types, performing security
checks, editing the packet and so on. With the arrangement of Figure 1, as
30 feature requirements increase, the chip size will increase since the chip will
need more logic and, as bandwidth requirements increase, the chip size will
increase since the memory size will need to be big enough to store the

increasing amount of incoming data and the chip will need more logic for faster processing.

Summary of the Invention

- 5 It is an object of the invention to provide an apparatus and method for receiving and processing data packets which mitigates or substantially overcomes the problems of prior art arrangements described above.

According to the invention, there is provided a method for receiving and
10 processing data packets, the method comprising the steps of:

providing a processor for processing data packets, each data packet including an instruction portion defining processing instructions for the data packet;

providing a memory for storing instruction portions of processed data
15 packets and associated processing instructions;

receiving a data packet, the data packet including an instruction portion;
comparing the instruction portion of the received data packet with
instruction portions stored in the memory; and

if the instruction portion of the received data packet matches an
20 instruction portion stored in the memory, sending the processing instructions associated with the instruction portion to the processor; or

if the instruction portion of the received data packet does not match an
instruction portion stored in the memory, processing the data packet and storing
the instruction portion and associated processing instructions in the memory.

25

If the instruction portion of the received data packet matches one already stored in the memory, the processing instructions associated with the instruction portion are sent to the processor. Therefore, processing of that data packet can be bypassed, as the processor can simply read the processing instructions from
30 the memory and process the data packet accordingly.

On the other hand, if the instruction portion of the received data packet does not match one already stored in the memory, the data packet is processed in the usual way and the instruction portion and associated processing instructions are stored in the memory for later use.

5

The instruction portion is preferably a header. The header may be a header defined in network standards e.g. an Ethernet header, ATM header, AAL5 header or IP/PPP header. Alternatively, the header may be defined by a user to define network flow, packet destination etc.

10

The term "processing instructions" should be interpreted broadly. Processing instructions might include the higher layer protocol or Quality of Service, the priority to assign to the data packet, whether to discard the data packet, where to transmit the data packet and so on.

15

In one embodiment, the processing instructions defined by the instruction portion include mask data, the mask data defining the section or sections of the instruction portion which are to be excluded when the instruction portion is compared with another instruction portion. In that embodiment, the step of

20 comparing the instruction portion of the received data packet with instruction portions stored in the memory may comprise comparing the instruction portion, excluding any sections defined by the respective mask data, of the received data packet with instruction portions, excluding any sections defined by the respective mask data, stored in the memory.

25

The step of receiving a data packet may comprise a receiver receiving the data packet. The receiver is preferably connected to the processor. The receiver is preferably connected to the memory. The receiver may be directly or indirectly connected to the processor and/or the memory.

30

In one embodiment, the step of comparing the instruction portion of the received data packet with instruction portions stored in the memory comprises a memory

controller comparing the instruction portion of the received data packet with instruction portions stored in the memory. The memory controller is preferably connected to the processor.

- 5 In that embodiment of the invention, the step of sending the processing instructions associated with the instruction portion to the processor, if the instruction portion of the received data packet matches an instruction portion stored in the memory, may comprise the memory controller sending the processing instructions associated with the instruction portion to the processor.

10

Preferably the memory controller is a cache controller. That is, the memory is preferably used as a cache memory.

- 15 In one embodiment of the invention, the step of processing the data packet, if the instruction portion of the received data packet does not match an instruction portion stored in the memory, comprises the processor processing the data packet.

- 20 According to the invention, there is also provided a method for processing data packets, each data packet including a header defining processing instructions for the data packet, the processing instructions including mask data defining any sections of the header which are to be excluded when the header is compared with another header, the method comprising the steps of:

- 25 providing a processor for processing data packets;
providing a memory for storing headers of processed data packets and associated processing instructions;
receiving a data packet;
comparing the header, excluding any sections defined by the respective mask data, of the received data packet with headers, excluding any sections
30 defined by the respective mask data, stored in the memory; and
if the header of the received data packet matches a header stored in the memory, sending the processing instructions associated with the header to the

processor so that processing of the data packet in the processor can be bypassed; or

- if the header of the received data packet does not match a header stored in the memory, processing the data packet and storing the header and
5 associated processing instructions in the memory.

According to the invention, there is also provided apparatus for receiving and processing data packets, the apparatus comprising:

- a receiver for receiving data packets, each data packet including an
10 instruction portion defining processing instructions for the data packet;
- a processor for processing data packets;
- a memory for storing instruction portions of processed data packets and associated processing instructions; and
- a memory controller arranged to compare the instruction portion of a
15 received data packet with instruction portions stored in the memory,
wherein the memory controller is arranged, if the instruction portion of the received data packet matches an instruction portion stored in the memory, to send the processing instructions associated with the instruction portion to the processor, and the processor is arranged, if the instruction portion of the
20 received data packet does not match an instruction portion stored in the memory, to process the data packet and store the instruction portion and associated processing instructions in the memory.

Thus, if the instruction portion of the received data packet matches one already
25 stored in the memory, the processing instructions associated with the instruction portion are sent to the processor so processing of that data packet can be skipped. In that way, the processing is bypassed if the instruction portion of the received data packet has previously been processed.

30 On the other hand, if the instruction portion of the received data packet does not match one already stored in the memory, the processor processes the data

packet in the usual way and the instruction portion and associated processing instructions are stored in the memory for later use.

5 The instruction portion is preferably a header. The header may be a header defined in network standards e.g. an Ethernet header, ATM header, AAL5 header or IP/PPP header. Alternatively, the header may be defined by a user to define network flow, packet destination etc.

10 The term "processing instructions" should be interpreted broadly. Processing instructions might include the higher layer protocol or Quality of Service, what priority to assign to the data packet, whether to discard the data packet, where to transmit the data packet and so on.

15 In one embodiment, the processing instructions include mask data, the mask data defining the section or sections of the instruction portion which are to be excluded when the instruction portion is compared with another instruction portion. In that embodiment, the memory controller may be arranged to compare the instruction portion, excluding any sections defined by the respective mask data, of the received data packet with instruction portions, excluding any sections defined by the respective mask data, stored in the
20 memory.

Preferably the memory controller is a cache controller. That is, the memory is preferably used as a cache memory.

25

According to the invention, there is also provided apparatus for processing data packets, each data packet including a header defining processing instructions for the data packet, the processing instructions including mask data defining any sections of the header which are to be excluded when the header is
30 compared with another header, the apparatus comprising:

- a receiver for receiving data packets;
- a processor for processing data packets;

a memory for storing headers of processed data packets and associated processing instructions; and

a memory controller arranged to compare the header, excluding any sections defined by the respective mask data, of a received data packet with

5 headers, excluding any sections defined by the respective mask data, stored in the memory,

wherein the memory controller is arranged, if the header of the received data packet matches a header stored in the memory, to send the processing

10 instructions associated with the header to the processor so that processing of the data packet in the processor can be bypassed, and

the processor is arranged, if the header of the received data packet does not match a header stored in the memory, to process the data packet and store the header and associated processing instructions in the memory.

15 **Brief Description of the Drawings**

A known arrangement has already been described with reference to Figure 1, which is a schematic diagram showing a known arrangement for receiving and processing data packets.

20 An exemplary embodiment of the invention will now be described with reference to Figure 2, which is a schematic diagram of an arrangement for receiving and processing data packets, according to an embodiment of the invention.

Detailed Description of Preferred Embodiment

25 Figure 2 is a schematic diagram of an embodiment of the invention. The arrangement 201 includes a receiver 203 and a processor 205, just as in known arrangements. The arrangement 201 additionally includes a memory in the form of a cache memory 207 and a memory controller in the form of a cache controller 209. The cache memory and the cache controller may or may not be
30 integrated into the receiver and/or processor.

The receiver is able to receive many types of protocol header. One protocol header may be received back to back with another protocol header since it is usual for one complete set of data to be segmented into pieces and sent over a network e.g. Ethernet or ATM. Some types of protocol header defined in
5 network standards are ATM, Ethernet, AAL5 and IP/PPP. The term "protocol header" should be taken to include, not only protocol headers defined in network standards, but also a field specified by a user, which can eventually uniquely determine network flow, destination, required processing etc within the device.

10

The cache memory stores already processed headers and associated data as will be described in more detail below. The cache controller 209 is able to send control signals to the cache memory 207, to read data from the cache memory 207 and to write data to the cache memory 207.

15

The operation of the arrangement of Figure 2 will now be described.

For each packet received by the receiver 203, the entire packet will be sent to the processor 205 and the instruction portion in the form of the header will be
20 sent to the cache controller 209. The cache controller 209 will then read data (arrow A) from the cache memory 207 and compare the received header with the headers read from the cache memory 207.

If there is a match between the received header and one already stored in the
25 cache memory 207, the cache controller 209 will indicate to the processor 205 that there is a match and will send the processing instructions associated with that header to the processor (arrow B). The processing instructions include, for example, where to transmit or whether to discard the packet, what priority is to be used in a transmit queue and what is the new data structure in the header or
30 payload. The processing instructions may also include mask data which indicates the portions of the header which should be masked when the header is compared with another header i.e. which portion(s) should not be involved in

a comparison. The processor 205 can then use the supplied processing instructions to bypass processing for that packet. Thus, any header that has already been processed by the processor and is thus stored in the cache memory, will not need to be processed again.

5

If, on the other hand, there is no match between the received header and one already stored in the cache memory 207 (either because there is a mismatch or because there is no data stored in the cache memory), the cache controller 209 will indicate this to the processor 205 (arrow C). The packet will then be processed as normal by the processor 205 and the processor will feed back the processing instructions (including the required mask pattern) to the cache controller 209 (arrow D). The cache controller will then update the cache memory 207 with the new data (arrow E), so that when the same header arrives next, processing can be bypassed.

10

15

Thus, as new types of header are processed, data is added to the cache memory so that processing the same header more than once is avoided. The size (width and depth) of the cache memory should be sufficiently large to cover all frequently used protocols and their headers. If, when the cache controller 209 tries to write new data to the cache memory (arrow E), the cache memory is found to be full, one of the existing entries is replaced by the latest data. Ideally, the replaced entry is the entry which is the least recently or frequently used.

20

25

In practice, the header is sent to the cache controller piece by piece (probably in 1 byte or 2 byte pieces) because the physical interface is arranged to receive that amount of data at a time. This is taking place as the entire data packet is being sent to the processor 205. Comparison of the received header and headers already stored in the memory can begin once the first piece of the header is received; there is no need to wait until the entire header is received.

30

It should be understood that where the term "data packet" is used, this may comprise any type of data bundle including a data packet or a data frame.

Thus, the problems of the known arrangements are overcome. The cache
5 memory is able to store headers of packets along with parsing, lookup and
other relevant results to be used later. Once it has been detected that the
received packet header is the same as one stored in the cache memory, the
arrangement can bypass actual frame or packet processing flow and can simply
read the results from the cache memory to decide what action to take on the
10 frame or packet for example whether to transmit it or discard it. By bypassing
the repeated processing flow, the invention can increase the bandwidth
because the average processing time for a frame or packet is reduced. This
cannot be achieved by known arrangements which process every frame or
packet individually.

15 Because the arrangement is able to deal with many different types of header,
each of which may be stored in the cache memory, the arrangement may be
used in a large number of different situations. Thus, the invention is applicable
to many different devices, using a variety of different defined network protocols.

20

Claims:

1. A method for receiving and processing data packets, the method comprising the steps of:
 - providing a processor for processing data packets, each data packet
 - 5 including an instruction portion defining processing instructions for the data packet;
 - providing a memory for storing instruction portions of processed data packets and associated processing instructions;
 - receiving a data packet, the data packet including an instruction portion;
 - 10 comparing the instruction portion of the received data packet with instruction portions stored in the memory; and
 - if the instruction portion of the received data packet matches an instruction portion stored in the memory, sending the processing instructions associated with the instruction portion to the processor; or
 - 15 if the instruction portion of the received data packet does not match an instruction portion stored in the memory, processing the data packet and storing the instruction portion and associated processing instructions in the memory.
2. A method according to claim 1 wherein the instruction portion is a
- 20 header.
3. A method according to claim 1 or claim 2 wherein the processing instructions include mask data defining the section or sections of the instruction portion which are to be excluded when the instruction portion is compared with
- 25 another instruction portion.
4. A method according to claim 3 wherein the step of comparing the instruction portion of the received data packet with instruction portions stored in the memory comprises comparing the instruction portion, excluding any
- 30 sections defined by the respective mask data, of the received data packet with instruction portions, excluding any sections defined by the respective mask data, stored in the memory.

5. A method according to any one of the preceding claims wherein the step of receiving a data packet comprises a receiver receiving the data packet.

5 6. A method according to claim 5 wherein the receiver is connected to the processor.

7. A method according to claim 5 or claim 6 wherein the receiver is connected to the memory.

10

8. A method according to any one of the preceding claims wherein the step of comparing the instruction portion of the received data packet with instruction portions stored in the memory comprises a memory controller comparing the instruction portion of the received data packet with instruction portions stored in
15 the memory.

9. A method according to claim 8 wherein the memory controller is connected to the processor.

20 10. A method according to claim 8 or claim 9 wherein the step of sending the processing instructions associated with the instruction portion to the processor, if the instruction portion of the received data packet matches an instruction portion stored in the memory, comprises the memory controller sending the processing instructions associated with the instruction portion to the processor.

25

11. A method according to any one of claims 8 to 10 wherein the memory controller is a cache controller.

12. A method according to any one of the preceding claims wherein the step
30 of processing the data packet, if the instruction portion of the received data packet does not match an instruction portion stored in the memory, comprises the processor processing the data packet.

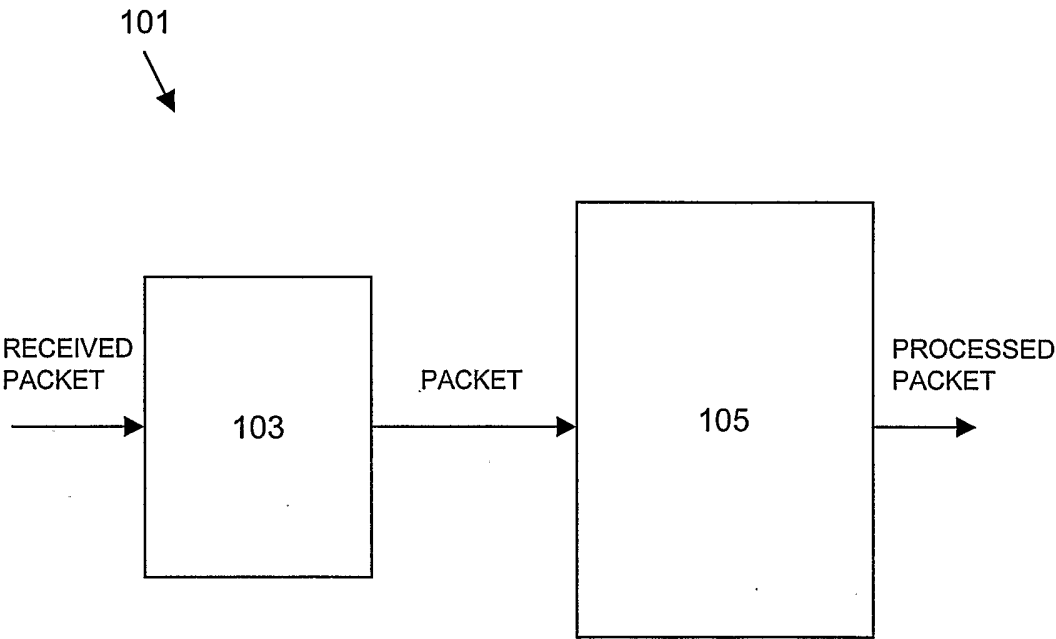
13. Apparatus for receiving and processing data packets, the apparatus comprising:

- 5 a receiver for receiving data packets, each data packet including an instruction portion defining processing instructions for the data packet;
- a processor for processing data packets;
- a memory for storing instruction portions of processed data packets and associated processing instructions; and
- 10 a memory controller arranged to compare the instruction portion of a received data packet with instruction portions stored in the memory, wherein the memory controller is arranged, if the instruction portion of the received data packet matches an instruction portion stored in the memory, to send the processing instructions associated with the instruction portion to the processor, and the processor is arranged, if the instruction portion of the
- 15 received data packet does not match an instruction portion stored in the memory, to process the data packet and store the instruction portion and associated processing instructions in the memory.

14. Apparatus according to claim 13 wherein the instruction portion is a header.

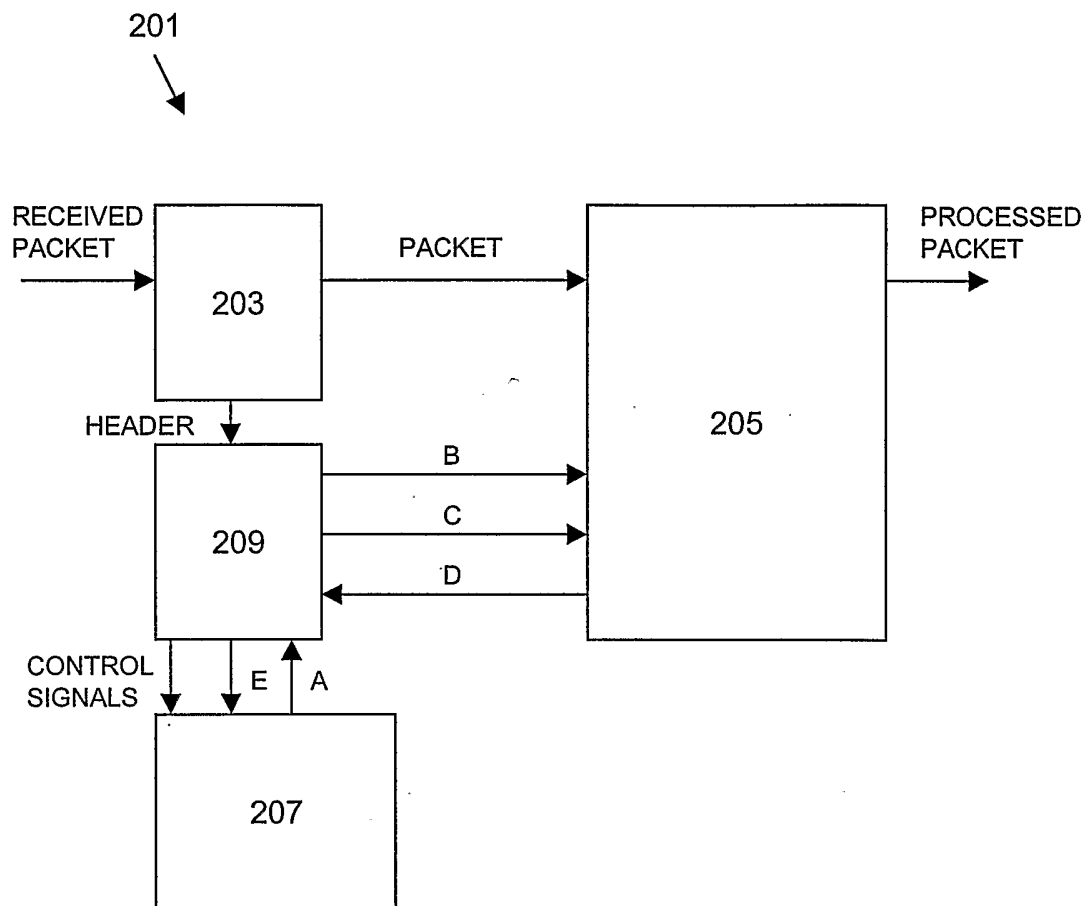
15. Apparatus according to claim 13 or claim 14 wherein the memory controller is a cache controller.

Figure 1



2/2

Figure 2



INTERNATIONAL SEARCH REPORT

International Application No
PC 17 SG2005/000021

A. CLASSIFICATION OF SUBJECT MATTER H04L29/06		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H04L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data, IBM-TDB, INSPEC, COMPENDEX		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00/52897 A (SUN MICROSYSTEMS, INC) 8 September 2000 (2000-09-08) abstract page 4, line 19 - page 5, line 11 page 9, line 9 - page 66, line 5 figures 1-7	1-15
X	WO 03/034670 A (REDDO NETWORKS AB; BERGLUND, JAN; GABRIELSSON, STEFAN; GERHARDSSON, JO) 24 April 2003 (2003-04-24) abstract page 3, line 30 - page 6, line 13 page 7, line 1 - page 18, line 11 figures 1-7	1-15
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☒ Further documents are listed in the continuation of box C. ☒ Patent family members are listed in annex.		
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Date of the actual completion of the international search 15 November 2005		Date of mailing of the international search report 22/11/2005
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer Körbler, G

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International Application No
PCT/SG2005/000021

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/161919 A1 (BOUCHER LAURENCE B ET AL) 31 October 2002 (2002-10-31) abstract paragraph '0016! - paragraph '0020! paragraph '0049! - paragraph '0141! figures 1-23 -----	1-15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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