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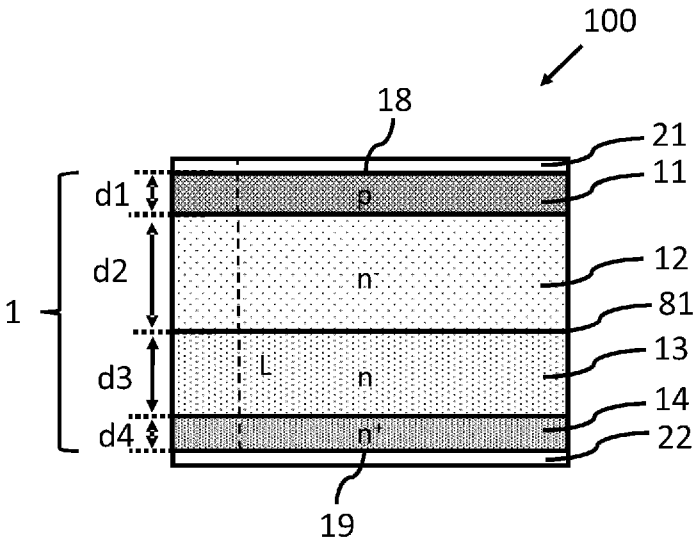

(57) Abstract: A power semiconductor device (100) comprises in the following order: a first electrode layer (21); a first semiconductor layer (11) of a first conductivity type; a second semiconductor layer (12) of a second conductivity type different from the first conductivity type, which has a doping concentration of less than $2\text{-}10^{14}$ cm^{-3} and a maximal thickness of less than 100 μm; a third semiconductor layer (13) of the second conductivity type, which has a different doping concentration than the second semiconductor layer (12) and a maximal thickness which is less than 100 μm; and a second electrode layer (22). The power semiconductor device is characterized in that the third semiconductor layer (13) has a doping concentration of less than $2\text{-}10^{14}$ cm^{-3}, and in that it further comprises a fourth semiconductor layer (14) of the second conductivity type arranged between the second main side (19) and the third semiconductor layer (13), the fourth semiconductor layer (14) having a maximal thickness of less than 2 μm and a higher doping concentration than the second and third semiconductor layer (12, 13), the doping concentration being in a range from $5\text{-}10^{15}$ to $5\text{-}10^{18}$ cm^{-3}.

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A dual base thin wafer power semiconductor device and method for manufacturing the same

Description

Field of the invention

The present invention relates to a low voltage power semiconductor device for blocking voltages below 2000 V, for example a power diode, a power MOSFET or an insulated gate bipolar transistor (IGBT), and to a method for manufacturing the same.

Background of the invention

To achieve the best possible electrical characteristic for low voltage power semiconductor devices, the thickness of the active zone (drift layer) of the semiconductor device must be selected to be as close as possible to the physical material boundaries to be as thin as possible. This is because the thickness has a direct effect on on-state losses. For example, for devices with a breakdown voltage below 2000 V, having a thickness of less than 200 µm would be desirable.

However, such small thicknesses are a big problem in the production of semiconductor devices, because wafers having a diameter of 100 mm and more should have a significantly larger thickness in order to minimize the risk of breakage during manufacture.

This problem may be overcome by using the epitaxial crystal growth technique, which involves growing an electrically active region on a thick mounting substrate ensuring the robustness for the semiconductor device produced. For example, the n-type region of an insulated gate bipolar transistor (IGBT) can be formed by epitaxial crystal growth on a thick p-type substrate, which forms the anode or collector in the final device. However, epitaxially growing the entire n-type region of an IGBT is a lengthy and complicated process, so that this approach is quite expensive.

From DE 198 60 582 A1 it is known an alternative manufacturing method, in which a buffer layer is added to a weakly doped n^--type wafer by n^+-type doping from a side of the wafer which is opposite to the future cathode and diffusing the dopants deep into the wafer, at least over half the thickness of the wafer, at high temperatures (>1200 °C). This produces a doping profile whose local doping concentration gradually increases towards the future anode. After the processing on the cathode side (e.g. forming MOS cells and electrodes), the wafer is thinned to such an extent that the doping profile is removed down to a weakly doped end region which essentially forms the buffer layer. Finally, a weakly doped p-type anode and an anode electrode are applied on the side opposite to the cathode side. The buffer layer has a doping concentration of at least $5 \cdot 10^{14}$ cm^{-3}, exemplarily above $1 \cdot 10^{15}$ cm^{-3} and serves to attenuate the electric field before the anode and thus to keep it away from the latter, because, if the electric field were to reach the anode, the semiconductor device would be destroyed. The drawback of this manufacturing method is, however, that the n-type layer from which the buffer layer is made, has to be thinned down precisely. If thinning the wafer is performed to a wrong extent such that the doping concentration is too low for the buffer layer, the device does not have its soft-punch-through properties anymore. The buffer layer may be made thicker than electrically necessary to assure the punch-through properties. However, a thicker buffer layer creates higher losses and variations in bipolar gain. Furthermore, the device has non-uniform current.

To improve on this, US 9 006 041 B2 presents a different manufacturing method, according to which a high-doped n-type wafer with a doping concentration of $5 \cdot 10^{14}$ to $5 \cdot 10^{16}$ cm^{-3} is provided. On a first side of the wafer (cathode side) a low-doped n^--type layer at a concentration of $3 \cdot 10^{13}$ cm^{-3} to $2 \cdot 10^{14}$ cm^{-3} is formed by epitaxial crystal growth. Thereafter, a diffusion step is performed at high temperatures (>1200 °C), by which a diffused inter-space region is created which comprises parts of the high-doped layer and the low-doped layer. Within the inter-space region the doping profile increases steadily from the concentration of the low-doped layer to the concentration of the high-doped layer, thus forming a smooth junction. The remaining part of the low-doped layer forms a drift layer. Thereafter the cathode side is processed (e.g. forming MOS cells and

electrodes). After the processing on the first side, the wafer is thinned on the second side within the high-doped layer, so that a buffer layer is created, which includes the inter-space region and the remaining part of the high-doped layer. Finally, a p-type anode and an anode electrode are applied on the side of the wafer opposite to the cathode side.

The semiconductor devices produced according to the latter two methods have a gradually rising doping profile at the interface (smooth or soft junction) between the low-doped drift layer and the high-doped buffer region. Such a smooth junction attenuates the electrical field more smoothly and has a beneficial effect on the switching behavior of the device in that it reduces an overshoot voltage compared to a hard junction. This effect is illustrated in Fig. 9 which shows turn-off waveforms for two different low-voltage IGBTs having the same buffer resistivity but different characteristics of a junction between a low-doped drift layer and a high-doped buffer region. The dot and dash line refers to a low-voltage IGBT having a soft junction and the solid line refers to a low voltage IGBT having a hard junction with a step-like doping profile. In the case of a soft junction the overshoot voltage can be reduced to less than 1200 V, whereas in the case of a hard junction, the overshoot voltage is close to 1300°V. On the downside, however, having a smooth junction also reduces the blocking capability and thus limits the device in terms of low temperature operation. This effect is shown in Fig. 10 which depicts the leakage current as a function of the collector-to-emitter voltage (Vces) for the soft junction IGBT (dot and dash line) and the hard junction IGBT (solid line), respectively. The soft junction IGBT yields a blocking voltage reduction (ΔVbr) of about 130 V. To compensate for this reduction in blocking capability, the thickness of the drift layer may be increased. As shown Fig. 11, a drift layer of which the thickness has been increased by 10 µm compared to the standard thickness may lead to a blocking voltage increase (ΔVbr) of 90 V. This, however, increases on-state losses and manufacturing costs due to the need of growing a thicker epitaxial layer.

Summary of the invention

It is therefore an object of the invention to provide a low voltage power semiconductor device, which is as thin as possible and provides optimized performance

and an economic manufacturing method thereof. Herein, a low voltage power semiconductor device refers to a power semiconductor device designed for blocking voltages below 2000 V.

The object of the invention is attained by a power semiconductor device comprising a semiconductor wafer having a first main side and a second main side opposite to the first main side; a first electrode layer on the first main side; and a second electrode layer on the second main side. The semiconductor wafer includes in the order from the first main side to the second main side: a first semiconductor layer having a first doping concentration of a first conductivity type which is in electrical contact with the first electrode layer; a second semiconductor layer having a second doping concentration of a second conductivity type different from the first conductivity type and which forms a first p-n junction with the first semiconductor layer; and a third semiconductor layer having a third doping concentration of the second conductivity type which is substantially constant along a thickness direction. Here and in what follows, a substantially constant doping concentration means a doping profile in which the highest doping concentration is not more than 1.05 times of the lowest doping concentration. The second doping concentration of the second semiconductor layer is less than $2 \cdot 10^{14}$ cm^{-3} and the second semiconductor layer has a thickness of less than 100 µm. A thickness of the third semiconductor layer is less than 100 µm and the third doping concentration of the third semiconductor layer is different from the second doping concentration of the second semiconductor layer (i.e. along a thickness direction all local doping concentrations in the doping profile of the second semiconductor layer are either higher than all local doping concentrations in the doping profile of the third semiconductor layer, or all local doping concentrations in the doping profile of the second semiconductor layer are lower than all local doping concentrations in the doping profile of the third semiconductor layer). The power semiconductor device according to the invention is characterized in that the third semiconductor layer has a third doping concentration which is less than $2 \cdot 10^{14}$ cm^{-3} and in that it further comprises a fourth semiconductor layer of the second conductivity type arranged between the second main side and the third semiconductor layer, the fourth semiconductor layer having a thickness of less than 2 µm and a fourth doping concentration which is in a range from $5 \cdot 10^{15}$ to $5 \cdot 10^{18}$ cm^{-3} (i.e. all local doping

concentrations in the doping profile along the thickness direction of the fourth semiconductor layer are higher than $5 \cdot 10^{15}$ $cm^{-3}$and lower $5 \cdot 10^{18}$ cm^{-3}).

Throughout this disclosure, a thickness of a layer refers to the distance between an upper and a lower surface of the layer and a thickness direction refers to a direction perpendicular to the layer, i.e. perpendicular to the first and second main sides of the semiconductor wafer.

The inventors found out that by increasing the resistivity of the third semiconductor layer the blocking voltage can be increased. This effect is illustrated in Fig. 12 which depicts blocking curves of an exemplary IGBT with epitaxial layer and two different buffer resistivity. In the case of the higher buffer resistivity (dot and dash line) a higher blocking voltage is obtained than in the case of the lower buffer resistivity (solid line). Therefore, according to the present invention, the third doping concentration of the third semiconductor layer is in a lower range compared to devices of the prior art. Having a lower doping concentration means having a higher resistivity and therefore improved blocking capabilities. Hence, for a given breakdown voltage, the thickness of the second semiconductor layer can be reduced compared to prior art devices, and thus a thinner device may be obtained. Moreover, manufacturing costs may be reduced because the thickness of the epitaxial layer forming the second semiconductor layer can be smaller.

However, as also visible from Fig. 12, having a higher resistivity increases leakage currents. To compensate for the increased leakage currents the power semiconductor device further comprises a thin (thickness < 2 μm) high doped fourth semiconductor layer of the second conductivity type at the second main side of the semiconductor wafer adjacent to the third semiconductor layer. The fourth semiconductor layer functions as a leakage buffer and reduces the leakage currents, which is particularly beneficial for high temperature operation. Furthermore, the fourth semiconductor layer also supports a voltage blocking capability of the device. In combination, these features allow to produce a thinner power semiconductor device with improved performance and at lower costs.

Further developments of the power semiconductor device according to the invention are specified in the dependent claims 2 to 10.

In an exemplary embodiment, a doping profile of the second semiconductor layer along the thickness direction has a first portion in which

$\left|\frac{d}{dz}(log_{10}(n_2(z)\cdot cm^3)\right| < 0.02/\mu m$ and

a step-like second portion connecting the first portion with a third portion of a doping profile of the third semiconductor layer, wherein in the second portion

$\left|\frac{d}{dz}(log_{10}(n_2(z)\cdot cm^3)\right| \geq 0.02/\mu m$ and

a maximum for $\left|\frac{d}{dz}(log_{10}(n_2(z)\cdot cm^3)\right|$ in the second portion is at least 0.2/µm, exemplarily at least 0.5/µm, and $n_2(z)$ is the doping concentration in the second semiconductor layer at a position z along the thickness direction. In other words, in contrast to the prior art, the semiconductor device does not have a smooth junction at the interface between the second semiconductor layer and the third semiconductor layer but a sharp (or hard) junction. Thus, for a given blocking voltage, the thickness of the second semiconductor layer can be reduced and thus also manufacturing costs thereof. The loss of softness due to having a sharp transition is counterbalanced by having a lower doping concentration in the third semiconductor layer than in the prior art as explained with reference to Fig. 12.

In a further development of the embodiment above, following relationship is fulfilled: $\frac{|n_2(z_0)-\overline{n_3}|}{\overline{n_3}} \geq 0.05$, exemplarily $\frac{|n_2(z_0)-\overline{n_3}|}{\overline{n_3}} \geq 0.1$, wherein $n_2(z_0)$is a local doping concentration in the doping profile of the second semiconductor layer along the thickness direction at a point z_0, where the first portion connects to the second portion, and $\overline{n_3}$ is a mean doping concentration in the doping profile of the third semiconductor layer along the thickness direction.

Here and in what follows, a mean doping concentration of a semiconductor layer is the arithmetic mean value of the local doping concentration values. The mean value of a doping concentration in a doping concentration profile along thickness direction z is

computed as $\overline{n_j} = \frac{1}{m}\sum_{i=1}^{m} n_j(z_i)$, wherein $n_j(z_i)$ is the local doping concentration of the j-th semiconductor layer at a position z_i in the thickness direction and z_1 and z_m are the first point and last point in the thickness direction belonging to the j-th semiconductor layer, and wherein the distance between z_l and z_{l+1} is the same for all l from 1 to m-1.

In an exemplary embodiment, an electric field reaches the fourth semiconductor layer when 80 % of a breakdown voltage is applied. In other words, in contrast to the prior art, the power semiconductor device according to the invention does not rely exclusively on the third semiconductor layer to stop the electric field. This is accomplished by the fourth semiconductor layer. Thus, the thickness of the second semiconductor layer and the thickness of the third semiconductor layer can be smaller. Overall, this allows producing a thinner device.

In an exemplary embodiment, the ratio of the maximal thickness of the second semiconductor layer over the thickness of the third semiconductor layer is greater than 0.8 and less than 1.2, i.e. $0.8 < \frac{\mathrm{d_2}}{\mathrm{d_3}} < 1.2$, $\mathrm{d_2}$ being the thickness of the second semiconductor layer and $\mathrm{d_3}$ being the thickness of the third semiconductor layer.

In an exemplary embodiment, a combined thickness ($d_{23} = d_2 + d_3$) of the second semiconductor layer and the third semiconductor layer fulfils $d_{23} < 0.12 \cdot \frac{\mu m}{Volt} \cdot U$, wherein U is the breakdown voltage of the device in Volt.

In exemplary embodiment, the doping concentration of all points in the second semiconductor layer is larger than the doping concentration of all points in the third semiconductor layer. In other words, a minimum doping concentration in the second semiconductor layer is higher than a maximum doping concentration in the third semiconductor layer.

In an exemplary embodiment, a ratio of a mean doping concentration $\overline{n_2}$ in the doping profile along a thickness direction of the second semiconductor layer and a mean

doping concentration $\overline{n_4}$ along the thickness direction of the fourth semiconductor layer is greater than 0.025 i.e. $\frac{\overline{n_2}}{\overline{n_4}} > 0.025$.

In an exemplary embodiment, a fifth semiconductor layer of the first conductivity type is arranged between the fourth semiconductor layer and the second main side. The fifth semiconductor layer has a fifth doping concentration in a range from $1 \cdot 10^{17}$ cm^{-3} to $5 \cdot 10^{20}$ cm^{-3} (i.e. all local doping concentrations in the doping profile along the thickness direction of the fifth semiconductor layer are higher than $1 \cdot 10^{17}$ cm^{-3} and lower $5 \cdot 10^{20}$ cm^{-3}) and forms a second p-n junction with the fourth semiconductor layer. The fifth semiconductor layer is in electrical contact with the second electrode layer. Moreover, a sixth semiconductor layer having a sixth doping concentration of the second conductivity type is arranged between the first main side and the first semiconductor layer. The sixth semiconductor layer is in electrical contact with the first electrode layer and forms a third p-n junction with the first semiconductor layer. In addition, a third electrode layer is arranged at the first main side of the semiconductor wafer and is electrically separated from the first semiconductor layer, the first electrode layer and the sixth semiconductor layer.

In a further development of this embodiment, a ratio of a mean doping concentration $\overline{n_4}$ of a doping profile along the thickness direction of the fourth semiconductor layer and a mean doping concentration $\overline{n_5}$ of a doping profile along the thickness direction of the fifth semiconductor layer may be greater than 0.01 and less than 1, i.e. $0.01 < \frac{\overline{n_4}}{\overline{n_5}} < 1$.

The object of the invention is also attained by a method for manufacturing a power semiconductor device. The method comprises a step of forming a semiconductor wafer which has a first main side and a second main side opposite to the first main side and which includes in the order from the first main side to the second main side the following layers: a first semiconductor layer having a first doping concentration of a first conductivity type; a second semiconductor layer of a second conductivity type different from the first conductivity type and forming a first p-n junction with the first semiconductor layer, the second semiconductor layer having a second doping

concentration of less than $2 \cdot 10^{14}$ cm^{-3} and a maximal thickness of less than 100 µm; a third semiconductor layer of the second conductivity type, the third semiconductor layer having a maximal thickness of less than 100 µm and a third doping concentration different from the second doping concentration of the second semiconductor layer, the third doping concentration being substantially constant along a thickness direction of the third semiconductor layer and less than $2 \cdot 10^{14}$ cm^{-3}; and a fourth semiconductor layer of the second conductivity type arranged between the second main side and the third semiconductor layer, the fourth semiconductor layer having a thickness of less than 2 µm and a fourth doping concentration being in a range from $5 \cdot 10^{15}$ to $5 \cdot 10^{18}$ cm^{-3}. The method further comprises a step of forming a first electrode layer on the second main side in electrical contact with the first semiconductor layer and a step of forming a second electrode layer on the second main side. The step of forming a semiconductor wafer comprises: providing a semiconductor substrate having a first side and a second side opposite to the first side, the semiconductor substrate having the second conductivity type and the third doping concentration; growing an epitaxial layer of the second conductivity type on the first side of the semiconductor substrate, the epitaxial layer having a fourth side at (e.g. adjacent to) the first side of the semiconductor substrate and a third side opposite to the fourth side; after the step of growing the epitaxial layer, forming the first semiconductor layer at the third side of the epitaxial layer (e.g. inside and/or on the epitaxial layer), the first semiconductor layer having a sixth side at (e.g. adjacent to) the third side of the epitaxial layer and a fifth side opposite to the sixth side; thinning the semiconductor substrate by removing material at its second side, (before or after the thinning step) applying dopants of the second conductivity type at the second side of the semiconductor substrate; and activating the applied dopants of the second conductivity type while avoiding temperature levels above 450°C at the first main side of the semiconductor wafer.

Further developments of the method for manufacturing a power semiconductor device according to the invention are specified in the dependent claims 11 to 15.

In an exemplary embodiment of the method, the method further comprises a step of forming a fifth semiconductor layer by applying dopants of the first conductivity type at

the second side of the semiconductor substrate to form a second p-n junction with the fourth semiconductor layer. The method also comprises a step of activating the applied dopants of the first conductivity type while avoiding temperature levels above 450°C at the first main side of the semiconductor wafer (e.g. at the first electrode layer); a step of forming a sixth semiconductor layer at (e.g. adjacent to) the fifth side of the first semiconductor layer such that the sixth semiconductor layer and the first semiconductor layer form a third p-n junction; and a step of forming a third electrode layer at the first main side of the semiconductor wafer (e.g. on the third side of the epitaxial layer) such that the third electrode layer is electrically separated from the first semiconductor layer, the sixth semiconductor layer and the first electrode layer. Moreover, in the step of forming the second electrode layer, the second electrode layer is formed to be in electrical contact with the fifth semiconductor layer.

In an exemplary embodiment of the method, the applied dopants of the second conductivity type and the applied dopants of the first conductivity type are activated in the same activation step. By performing both activations in the same activation step, the thermal budget to the power semiconductor device is reduced. This may be beneficial for obtaining a sharp (or hard) junction between the second semiconductor layer and the third semiconductor layer.

In an exemplary embodiment, after the step of growing the epitaxial layer a temperature at an transition region (e.g. at an interface) between the second semiconductor layer and the third semiconductor layer is kept below 1200°C, exemplarily below 1000°C, and does not exceed 700°C for longer than 16 hours, exemplarily longer than 8 hours. By this a thermal budget is kept sufficiently low to minimize dopant diffusion between the second and third semiconductor layers, so that a sharp (or hard) junction at the transition region between the second semiconductor layer and the third semiconductor layer is maintained.

In an exemplary embodiment of the method, the step of thinning the semiconductor substrate is performed after the at least one electrode forming step at the first main side of the semiconductor wafer; the at least one step of applying dopants is performed by ion

implantation and performed after the step of thinning the semiconductor substrate, and the at least one step of activating the applied dopants is performed by laser annealing.

Brief description of the drawings

Detailed embodiments of the invention will be explained below with reference to the accompanying figures, in which:

Fig. 1 is the vertical cross section of a power semiconductor device according to the first embodiment in which the power semiconductor device is a power diode (PIN diode);

Fig. 2 shows a doping profile and an electrical field distribution of the first embodiment along a line L shown in Fig. 1;

Fig. 3 is vertical cross section of a power semiconductor device according to a second embodiment in which the semiconductor device is a power MOSFET;

Fig. 4 is vertical cross section of a power semiconductor device according to a third embodiment in which the power semiconductor device is an IGBT;

Fig. 5 shows a doping profile and an electrical field distribution of the third embodiment along a line L' shown in Fig. 4;

Fig. 6A-G show manufacturing steps for manufacturing a power semiconductor device according to the first to third embodiments;

Fig. 7A-H show manufacturing steps for manufacturing a power semiconductor device according to second to third embodiment;

Fig. 8A-B show manufacturing steps for manufacturing a power semiconductor device according to the third embodiment;

Fig. 9 shows the increased voltage overshoot of sharp junction compared to a smooth junction during switching;

Fig. 10 shows the decreased blocking voltage of a soft junction compared to a smooth junction;

Fig. 11 shows the increased blocking voltage of a thick drift layer compared to a thin drift layer; and

Fig. 12 shows the increased blocking voltage of a lower doped buffer layer compared to a higher doped buffer layer.

The reference signs used in the figures and their meanings are summarized in the list of reference signs. Generally, similar elements have the same reference signs throughout the specification. The described embodiments are meant as examples and shall not limit the scope of the invention.

Detailed description of exemplary embodiments

In Fig. 1 there is shown a vertical cross section of a power diode 100, which is a first exemplary embodiment of the power semiconductor device according to the invention. The power diode 100 may be a low-voltage diode for voltage classes of 2000 V or below. The power diode 100 comprises a semiconductor wafer 1 having a first main side 18 and a second main side 19 opposite and parallel to the first main side 18. The semiconductor wafer 1 is, for example, a silicon (Si) wafer. The plane of drawing in Fig. 1 is a plane perpendicular to the first main side 18. In an order from the first main side 18, which is an anode side of the power diode 100, to the second main side 19, which is a cathode side of the power diode 100, the semiconductor wafer 1 comprises a first semiconductor layer 11 having a first doping concentration n_1 of a first conductivity type,

e.g. a p-type layer, a second semiconductor layer 12 having a second doping concentration n_2 of a second conductivity type, e.g. a n^--type layer, a third semiconductor layer 13 having a third doping concentration n_3 of the second conductivity type, e.g. a n-type layer, which is different from the second doping concentration n_2 of the second semiconductor layer 12, and a forth semiconductor layer 14 having a forth doping concentration n_4 of the second conductivity type, e.g. a n^+-type , which is higher than the second doping concentration and the third doping concentration.

The first semiconductor layer 11 is electrically contacted by a first electrode layer 21 arranged on the first main side 18 of the semiconductor wafer 1 to form an ohmic contact with the first semiconductor layer 11. The first electrode layer 21 functions as an anode electrode of the power diode 100 and may be implemented as a metallization layer, for example, comprising aluminum (Al). The fourth semiconductor layer 14 is electrically contacted by a second electrode layer 22 arranged on the second main side 19 of the semiconductor wafer 1 to form an ohmic contact with the fourth semiconductor layer 14. The second electrode layer 22 functions as a cathode electrode of the power diode 100 and may be implemented as a metallization layer, for example, comprising aluminum (Al).

An exemplary thickness of the first semiconductor layer 11 is about 4 µm and a maximal doping concentration of the first doping concentration is about $1 \cdot 10^{18}$ cm^{-3}. In a thickness direction the first doping concentration of the first semiconductor layer 11 is decreasing from the maximal doping concentration at the first main side to about $1 \cdot 10^{12}$ cm^{-3}. Values for the thickness and the first doping concentration of the first semiconductor layer 11 may however deviate from these values depending on the device. As an alternative, the first doping concentration of the first semiconductor layer 11 may also be substantially constant along a thickness direction.

The second doping concentration n_2 of the second semiconductor layer 12 is in a range between $2 \cdot 10^{12}$ - $5 \cdot 10^{14}$ cm^{-3}, exemplarily in a range between $2 \cdot 10^{12}$ - $2 \cdot 10^{14}$ cm^{-3}. The second semiconductor layer 12 forms a p-n junction (first p-n junction in the claims) with the first semiconductor layer 11. The second semiconductor layer 12 may function

as a first drift region. A thickness of the second semiconductor layer 12 is in a range between 20 µm - 100 µm, exemplarily in a range between 40 µm – 80 µm. According to some exemplary embodiments, the second doping concentration n_2 may be substantially constant along a thickness direction, which means that in the doping profile along the thickness direction the highest doping concentration is not more than 1.05 time of the lowest doping concentration. According to a different embodiment (not shown), the second doping concentration n_2 may vary along a thickness direction, for example may increase and/or may decrease.

The third doping concentration n_3 of the third semiconductor layer 13 is in a range between $2 \cdot 10^{12}$ - $5 \cdot 10^{14}$ cm^{-3}, exemplarily in a range between $2 \cdot 10^{12}$ - $2 \cdot 10^{14}$ cm^{-3}. The third doping concentration n_3 is substantially constant along a thickness direction of the third semiconductor layer 13. The third semiconductor layer 13 may function as a second drift region. A thickness of the third semiconductor layer 13 is in a range between 20 µm - 100 µm, exemplarily in a range between 40 µm – 80 µm.

The doping concentrations and the thicknesses of the second semiconductor layer 12 and the third semiconductor layer 13 depend on the blocking capability specifications of the device. The doping concentration for a higher voltage device typically is lower than for a lower voltage device. According to some exemplary embodiments a mean doping concentration $\overline{n_2}$ in a doping profile along the thickness direction of the second semiconductor layer 12 is lower than a mean doping concentration $\overline{n_3}$ in a doping profile along the thickness direction of the third semiconductor layer 13. In such an embodiment, the second doping concentration n_2 of the second semiconductor layer 12 and the third doping concentration n_3 of the third semiconductor layer may be selected such that following relationship is fulfilled: $0.01 < \frac{\overline{n_2}}{\overline{n_3}} < 0.95$, exemplarily $0.4 < \frac{\overline{n_2}}{\overline{n_3}} < 0.7$. According to another exemplary embodiments (not shown) a mean doping concentration $\overline{n_2}$ in a doping profile along the thickness direction of the second semiconductor layer 12 is higher than a mean doping concentration $\overline{n_3}$ in a doping profile along the thickness direction of the third semiconductor layer 13. In such an embodiment, the second doping concentration n_2 of the second semiconductor layer 12 and the third doping concentration

n_3 of the third semiconductor layer may be selected such that following relationship is fulfilled: $0.01 < \frac{\overline{n_3}}{\overline{n_2}} < 0.95$, exemplarily $0.4 < \frac{\overline{n_3}}{\overline{n_2}} < 0.7$. In such an embodiment the doping concentration of all points in the second semiconductor layer 12 may be larger than the doping concentration of all points in the third semiconductor layer 13.

A thickness for a higher voltage device is typically larger than for a lower voltage device. A combined thickness ($d_{23} = d_2 + d_3$) of the second semiconductor layer 12 and the third semiconductor layer 13 may, for example, fulfil $d_{23} < 0.12 \cdot \frac{\mu m}{Volt} \cdot U$, wherein U is the breakdown voltage of the device. This means, a combined thickness d_{23} of a power semiconductor device with a breakdown voltage of 900 V may be less than 108 µm, or combined thickness d_{23} of a power semiconductor device with a breakdown voltage of 1200 V may be less than 144 µm etc. A ratio of a thickness d_2 of the second semiconductor layer 12 over a thickness d_3 of the third semiconductor layer 13 may, for example, be greater than 0.8 and less than 1.2, i.e. $0.8 < \frac{d_2}{d_3} < 1.2$. In an exemplary embodiment, the thickness d_2 of the second semiconductor layer 12 may be the same as the thickness d_3 of the third semiconductor layer 13.

A minimal value of the fourth doping concentration of the fourth semiconductor layer 14 is higher than a maximal value of the second doping concentration of the second semiconductor layer 12 and a maximal value of the third doping concentration of the third semiconductor layer 13. The fourth semiconductor layer 14 functions as a leakage-buffer. A ratio of a mean doping concentration $\overline{n_2}$ in a doping profile along the thickness direction of the second semiconductor layer 12 over a mean doping concentration $\overline{n_4}$ in a doping profile along the thickness direction of the fourth semiconductor layer 14 may, for example, be greater than 0.025 and less than 0.04, i.e. $0.025 < \frac{\overline{n_2}}{\overline{n_4}} < 0.04$. The fourth doping concentration n_4 of the fourth semiconductor layer may for example be in a range between $5 \cdot 10^{15}$ and $5 \cdot 10^{18}$ cm^{-3}. A thickness d_4 of the fourth semiconductor layer 14 is less than a thickness d_2 of the second semiconductor layer 12 and less than a thickness d_3 of the third semiconductor layer 13. A thickness d_4 of the fourth

semiconductor layer is for example less than 5 µm or less than 2 µm. A thickness of the fourth semiconductor layer d_4 is more than 0.5 µm or more than 1 µm.

According to some exemplary embodiments a doping profile along a thickness direction of the semiconductor wafer 1 has a step shape at a transition region 82 between the second semiconductor layer 12 and third semiconductor layer 13, where the doping profile increases sharply (see Fig. 2). More specifically, the second doping concentration of the second semiconductor layer 12 is such that a doping profile along a thickness direction has a first portion and a second portion. In the first portion the doping profile has a shallow slope, i.e. $\left|\frac{d}{dz}(log_{10}(n_2(z)\cdot cm^3)\right| < 0.02/\mu m$, wherein $n_2(z)$ represents the doping profile along the thickness direction z and $\frac{d}{dz}$ represents a derivation. The second portion connects the doping profile of the first portion with a third portion of a doping profile of the third semiconductor layer 13. The second portion has a step-like shape (e.g. an ascending step or a descending step). Within the second portion a maximum for $\left|\frac{d}{dz}(log_{10}(n_2(z)\cdot cm^3)\right|$ is at least 0.2/µm, exemplarily at least 0.5/µm. According to other embodiments (not shown), where the second doping concentration of the second semiconductor layer 12 is higher than the third doping concentration of the third semiconductor layer 13, the doping profile may decrease sharply at the transition region 82 (i.e. the second portion has a descending step-shape). Moreover, when $n_2(z_0)$ is the doping concentration in the doping profile of the second semiconductor layer 12 along a thickness direction at a point z_0, where the first region connects to the second region, and $\overline{n_3}$ is a mean doping concentration in the doping profile of the third semiconductor layer (13) along the thickness direction, following relationship may be fulfilled: $\frac{|n_2(z_0)-\overline{n_3}|}{\overline{n_3}} \geq 0.05$, exemplarily $2 \geq \frac{|n_2(z_0)-\overline{n_3}|}{\overline{n_3}} \geq 0.1$.

Moreover, under reverse bias, i.e. in a blocking condition, an electric field decreases along a thickness direction of the semiconductor wafer 1. The electric field may be nonzero in the second semiconductor layer 12 and the third semiconductor layer 13. The electric field may extend into the fourth semiconductor layer 14 and reach zero in the fourth semiconductor layer 14. A space charge region may extend into the fourth

semiconductor layer 14. By allowing that the electrical field extends into the fourth semiconductor layer 14, the second semiconductor layer 12 and the third semiconductor layer 13 may be thinner, and thus a thinner device may be obtained. However, in a different embodiment (not shown) the electric field may have already reached zero in the third semiconductor layer 13 and accordingly a space charge region may not extent into the fourth semiconductor layer 14.

In Fig. 3 it is shown a vertical cross section of a power metal oxide semiconductor field-effect transistor (power MOSFET) 200, which is a second exemplary embodiment of a power semiconductor device according to the invention. Due to the many similarities between the first embodiment and the second embodiment only differences are described. The remaining features are the same as explained with respect to Figs. 1 and 2 and for an explanation thereof it is referred to the discussion above.

In the second exemplary embodiment, the semiconductor wafer 1 comprises a sixth semiconductor layer 16 of the second conductivity type, i.e. of the n-type. The doping concentration n_6 of the sixth semiconductor layer 16 is higher than that of the second semiconductor layer 12. The sixth semiconductor layer 16 is arranged between the first main side 18 and the first semiconductor layer 11. The sixth semiconductor layer 16 is surrounded by the first semiconductor layer 11. The first semiconductor layer 11 and the sixth semiconductor layer 16 form a p-n junction (third p-n junction in the claims). The sixth semiconductor layer 16 forms an ohmic contact with the first electrode layer 21. The first electrode layer 21 may function as a source electrode of the power MOSFET 200. The second electrode layer 22 may function as a drain electrode of the power MOSFET 200. The sixth semiconductor layer 16 may function as a source region. The power semiconductor device according to the second embodiment further comprises a third electrode layer 23 at the first main side 18. The third electrode layer 23 may be implemented as a metallization layer as described above. The third electrode layer 23 is electrically separated from the first electrode layer 21, from the first semiconductor layer 11, from the second semiconductor layer 12, and from the sixth semiconductor layer 16, for example by an electrically insulating layer 41. The electrically insulating layer 41 may be arranged at the first main side 18 of the semiconductor wafer 1 between the third

electrode layer 23 and the first to third semiconductor layers 11, 12, 13 such that direct contact with the third electrode layer 23 is prevented. The electrically insulating layer 41 may comprise a plurality of electrically insulating layers. The third electrode layer 23 is a gate electrode of the power MOSFET 200, and the insulating layer 41 is a gate insulating layer of the power MOSFET 200. Exemplarily the insulating layer 41 is made of silicon dioxide.

In Fig. 4 it is shown an insulated gate bipolar transistor (IGBT) 300, which is a third exemplary embodiment of the power semiconductor device according to the invention. Due to the many similarities between the second embodiment and the third embodiment only differences of these embodiments are described. The remaining features are as described with respect to the first embodiment and the second embodiment and for an explanation thereof reference is made to the discussions above. An electric field distribution and a doping profile along a thickness direction of the device as indicated by line L' is shown in Fig 5.

The IGBT 300 according to the third embodiment comprises a fifth semiconductor layer 15 of the first conductivity type, i.e. p-type, arranged between the fourth semiconductor layer 14 and the second main side 19 of the semiconductor wafer 1. The fifth semiconductor layer 15 is high doped and may, for example, have a concentration n_5 in a range from $1 \cdot 10^{17}$ cm^{-3} to $1 \cdot 10^{20}$ cm^{-3}. The doping concentration may, for example, be the same or no more than two orders of magnitude higher than the doping concentration of the fourth semiconductor layer to improve leakage current reduction. The fifth layer 15 may be an anode layer. The thickness d_5 of the fifth semiconductor layer 15 may be in a range between 0.2 µm and 2 µm, exemplarily in a range between 0.2 µm and 0.5 µm. The fifth semiconductor layer 15 forms a p-n junction (second p-n junction in the claims) with the fourth semiconductor layer 14. The fifth semiconductor layer 15 forms an ohmic contact with the second electrode layer 22. The second electrode layer 22 functions as the collector electrode of the IGBT, whereas the first electrode layer 21 functions as the emitter electrode of the IGBT.

According to Fig. 5, the electric field reaches zero in the third semiconductor layer 13. However, as described above with respect to Fig. 2, according to a different embodiment (not shown), the electric field may not reach zero in the third semiconductor layer 13 but reach zero only in the fourth semiconductor layer 14. In either case, the electric field may not reach into the fifth semiconductor layer 15.

Fig. 6A-G illustrate steps of a method for manufacturing a power semiconductor device according to the invention, for example according to the first to third embodiments. Referring to Fig. 6A, the method comprises a step of providing a semiconductor substrate 131 of the second conductivity type, i.e. of n-type conductivity, and having a first main side 138 and a second main side 139 opposite and parallel to the first main side 138. The semiconductor substrate 131 may comprise silicon (Si). The doping concentration of the semiconductor substrate 131 corresponds to the doping concentration of the third semiconductor layer 13 described above and is substantially constant in a thickness direction of the substrate. The thickness of the semiconductor substrate 131 is larger than the thickness d_3 of the third semiconductor layer 13, for example larger than 300 µm or larger than 500 µm. A thick semiconductor substrate 131 can be advantageous during the manufacturing because it ensures enough mechanical robustness during the individual steps of the manufacturing. In other words, a thick semiconductor substrate 131 facilitates handling of the device during the manufacturing process.

After the step of providing the semiconductor substrate 131, the method comprises a step of forming an epitaxial layer 121 on the first side 138 of the semiconductor substrate 131 (Fig. 6B). This involves growing an epitaxial layer from gaseous or liquid precursors which deposit on the first side 138 of the semiconductor substrate 131. By adding impurities (e.g. phosphorous) to the gaseous or liquid precursors, the epitaxial layer 121 may be doped during the deposition. The epitaxial layer may, for example, be doped such that its doping concentration corresponds to the doping concentration of the second semiconductor layer 12. The doping concentration may, for example, be in a range between $5 \cdot 10^{13}$ and $5 \cdot 10^{14}$ cm^{-3} or between $5 \cdot 10^{13}$ and $2 \cdot 10^{14}$ cm^{-3}. The epitaxial layer 121 is at least grown to the thickness of the second semiconductor layer 12. The epitaxial layer

121 has a fourth side 129 at the first side 138 of the semiconductor substrate 131 and a third side 128 opposite to the fourth side 129.

After the step of forming the epitaxial layer 121, the method comprises a step of forming the first semiconductor layer 11 (Fig. 6C). The first semiconductor layer 11 is formed by introducing dopants 83 of the first conductivity type, e.g. p-type dopants (e.g. Boron), for example by diffusion or ion implantation followed by an activation step. These process steps are generally known in the art. The first semiconductor layer 11 has a sixth side 119 at the third side of the epitaxial layer 121 and a fifth side 118 opposite to the sixth side 119. To keep a sharp junction, a thermal budget to a transition region 82 (e.g. at the interface 81) between the epitaxial layer 121 and the semiconductor substrate 131 is kept low to minimize dopant diffusion between these two layers. This may, for example, be achieved by keeping a temperature at the transition region 82 (e.g. at the interface 81) between the epitaxial layer 121 and the semiconductor substrate 131 below 1200°C, or below 1000°C, while not exceeding a temperature of 700°C for longer than 16 hours or longer than 8 hours. Alternatively, a smooth junction may be formed. To form a smooth junction a thermal treatment is applied (e.g. a heating above 1200°C) to the transition region 82 (e.g. to the interface 81). The second semiconductor layer 12 corresponds to a remaining portion of the epitaxial layer 121, i.e. a portion of the epitaxial layer 121 which has not been doped with the dopants of the first conductivity type.

Referring to Fig. 6D, the method further comprises a step of forming a first electrode layer 21 at the third side of the epitaxial layer 121 as illustrated in Fig. 6D. The first electrode layer 21 is formed to make an ohmic contact with the first semiconductor layer 11. The corresponding process steps are generally known in the art and may involve, for example, depositing a metallization layer by sputtering. After the application of the metallization, the semiconductor should no longer be exposed to higher temperatures (for example a temperature above 450°C) as they may damage the metallization. Therefore, it may be beneficial to perform the electrode forming step after the step of forming the first semiconductor layer 11, and in particular in case a high temperature treatment is performed.

Referring to Fig. 6E, the method further comprises a step of reducing the thickness (thinning) of the semiconductor substrate 131 by removing material at the second side 138 of the semiconductor substrate 131, for example over the whole plane of the semiconductor substrate 131 on the second side 139 and parallel to the second main side 139. Any appropriate method well-known to the skilled person can be used for thinning, for example grinding, polishing, cutting or etching. The second side 139' of the thinned semiconductor substrate 131' may form the second main side 19 of the semiconductor wafer 1. A second side 139' of the thinned semiconductor substrate 131' may be termed a second side 139 in the claims. Since a thick semiconductor substrate 131 provides mechanical robustness, it may be advantageous to perform the step of forming the first electrode layer 21 (or other processing steps on the first main side 18 of the semiconductor wafer 1) before the thinning step.

Referring to Fig. 6F, the method comprises a step of forming the fourth semiconductor layer 14 at the second main side 19 of the semiconductor wafer 1 (e.g. at a side of the semiconductor substrate 131 which is opposite to the first side 138). The fourth semiconductor layer 14 is formed by applying dopants of the second conductivity type 84, e.g. n-type dopants, at the second side 139 of the semiconductor substrate 131 or at the second side 139' of the thinned semiconductor substrate 131', for example by diffusion or ion implantation. Thus, the step of forming the fourth semiconductor layer 14 may be performed before the thinning step or after the thinning step. When performed before the thinning, the dopants are implanted or diffused to a depth which is deeper below the second side 139 of the semiconductor substrate 131 than is the thickness of the material to be removed in the thinning step. For example, when a thickness of fourth layer is to be 2 μm and a thickness of 200 μm is to be removed in the thinning step, then the dopants are introduced down to a depth of 202 μm below the second side 139 of the semiconductor substrate 131 such that after the thinning a 2 μm thick layer of the second conductivity type remains. When the step of forming the fourth semiconductor layer 14 is performed after the thinning step, then the dopants are introduced to the depth to which the fourth semiconductor layer 14 is supposed to extent, e.g. 2 μm below the surface of the second side 139' of the thinned semiconductor substrate 131'. Thereafter, applied dopants are activated while avoiding excess temperature levels above 450°C at the first

main side 18 of the semiconductor wafer 1 (e.g. at the first electrode layer 21). Thus, damages to the first electrode layer 21 on the first main side 18 can be prevented. For activation laser annealing, flash lamp annealing or rapid thermal process may for example be used. Laser annealing may be particularly advantageous in view of reducing the thermal budget to other parts of the power semiconductor device. To facilitate laser annealing, having a fourth semiconductor layer 14 with a thickness of less than 2 μm or less than 1μm may be beneficial. After, the activation step, the second electrode layer 22 is formed on the second main side 19 of the semiconductor wafer (Fig. 6G), for example by metallization as described above.

Fig. 7A-H illustrates additional steps for manufacturing a power semiconductor device according to the invention, for example the power semiconductor device according to the second or the third embodiments. Referring to Fig. 7B a sixth semiconductor layer 16 is formed between the first main side 18 of the semiconductor wafer 1 and the first semiconductor layer 11 such that the sixth semiconductor layer 16 of the second conductivity type and the first semiconductor layer 11 form a third p-n junction. How to form the sixth semiconductor layer 16 is known in the art and may, for example, be achieved by ion implantation and/or diffusion. The sixth semiconductor layer 16 may, for example, be formed before (not shown) or after the forming (Fig. 7B) of the first semiconductor layer 11. Referring to Fig. 7C, an insulating layer 41 as described above is formed on the first main side 18 of the semiconductor wafer 1. Referring to Fig. 7D, a third electrode layer 23 is formed on the insulating layer 41 such that the third electrode layer 23 is electrically separated from the first semiconductor layer 11, the sixth semiconductor layer 16 and the first electrode layer 21 (see Fig. 7E). Referring to Fig. 7E, the first electrode layer 21 is formed such that it is in electrical contact with the first semiconductor layer 11 and the sixth semiconductor layer 16. The first electrode layer 21 may be formed before forming the third electrode layer 23 and the insulating layer 41 (not shown) or thereafter (shown in Fig. 7E). Referring to Fig. 7F, the semiconductor substrate 131 is thinned at its second side 139. Thereafter, referring to Figs. 7G and 7H, the fourth semiconductor layer 14 and the second electrode layer 22 are formed at the second main side 19 of the semiconductor wafer 1 as described above.

Figs. 8A-B illustrate additional steps for manufacturing a power semiconductor device according to the invention, for example the power semiconductor device according to the third embodiment. Referring to Fig. 8A, a fifth semiconductor layer 15 of the first conductivity type of formed between the second main side 19 of the semiconductor wafer 1 and the fourth semiconductor layer 14 by applying dopants 83 of the first conductivity type at the second main side 19 of the semiconductor wafer 1, for example by ion implantation and/or diffusion. Thereafter, the applied dopants are activated as described above with respect to the fourth semiconductor layer 14. The activation of the fifth semiconductor layer 15 may for example be performed before, after or together with the activation of the fourth semiconductor layer 14. Referring to Fig. 8B, the second electrode layer 22 is formed as described above.

In the description above, specific embodiments of the invention were described. However, alternatives and modifications of the above described embodiments are possible without departing from the idea of the invention as defined by the appended claims.

The power semiconductor device according to the invention may also be a reverse conducting (RC) device, for example a RC-IGBT.

For example, in the embodiment shown above the third electrode layer 23 (gate electrode) was formed as a planar electrode. However, the gate electrode may also be formed as a trench gate electrode.

The embodiments were explained with specific conductivity types. The conductivity types of the semiconductor layers in the above-described embodiments may be switched, so that all layers which are described as p-type layers would be n-type layers and all layers which were described as n-type layers would be p-type layers.

It should be noted that the term “comprising” does not exclude other elements or steps and that the indefinite article “a” or “an” does not exclude the plural. Also elements or features described in association with different embodiments may be combined.

List of reference signs

1	semiconductor wafer
11	first semiconductor layer
12	second semiconductor layer
13	third semiconductor layer
14	fourth semiconductor layer
15	fifth semiconductor layer
16	sixth semiconductor layer
18	first main side of the semiconductor wafer
19	second main side of the semiconductor wafer
21	first electrode layer
22	second electrode layer
23	third electrode layer
41	insulating layer
81	interface between the second and third semiconductor layer
82	transition region between the second and third semiconductor layer
83	applying and activating dopants of the first conductivity type
84	applying and activating dopants of the second conductivity type
100	power diode
118	fifth side of the first semiconductor layer
119	sixth side of the first semiconductor layer
121	epitaxial layer
128	third side of the epitaxial layer
129	fourth side of the epitaxial layer
131	semiconductor substrate
131'	thinned semiconductor substrate
138	first main side of the semiconductor substrate
139	second main side of the semiconductor substrate
139'	second main side of the thinned semiconductor substrate
200	power MOSFET
300	IGBT

d_j thickness of the j-th semiconductor layer, j = 1 to 6

n_j doping concentration of the j-th semiconductor layer

$\bar{n}_j$ mean doping concentration in the j-th semiconductor layer$n_{j,min}$ minimum doping concentration in the j-th semiconductor layer

$n_{j,max}$ minimum doping concentration in the j-th semiconductor layer

z position along the thickness direction

Claims

1. A power semiconductor device comprising:

a semiconductor wafer (1) having a first main side (18) and a second main side (19) opposite to the first main side (18);

a first electrode layer (21) on the first main side (18);

a second electrode layer (22) on the second main side (19);

wherein the semiconductor wafer (1) includes in the order from the first main side (18) to the second main side (19) following layers:

a first semiconductor layer (11) of a first conductivity type in electrical contact with the first electrode layer (21), the first semiconductor layer (11) having a first doping concentration n_1;

a second semiconductor layer (12) of a second conductivity type different from the first conductivity type, the second semiconductor layer (12) forming a first p-n junction with the first semiconductor layer (11), the second semiconductor layer (11) having a second doping concentration n_2 of less than $2 \cdot 10^{14}$ cm^{-3} and a thickness d_2 of less than 100 µm;

a third semiconductor layer (13) of the second conductivity type having a third doping concentration n_3 which is substantially constant along a thickness direction, which is a direction perpendicular to the first main side (18) and the second main side (19), the third doping concentration n_3 being different from the second doping concentration n_2 of the second semiconductor layer (12), a thickness d_3 of the third semiconductor layer (13) being less than 100 µm,

characterized in that

the third doping concentration n_3 is less than $2 \cdot 10^{14}$ cm^{-3}, and

the power semiconductor device further comprises a fourth semiconductor layer (14) of the second conductivity type arranged between the second main side (19) and the third semiconductor layer (13), the fourth semiconductor layer (14) having a thickness d_4 of less than 2 µm and a fourth doping concentration n_4 in a range from $5 \cdot 10^{15}$ to $5 \cdot 10^{18}$ cm^{-3}.

2. The power semiconductor device according to claim 1, wherein an electric field reaches the fourth semiconductor layer (14) when a voltage corresponding to 80 % of a breakdown voltage is applied.

3. The power semiconductor device according to anyone of claims 1 to 2, wherein $0.8 < \frac{d_2}{d_3} < 1.2$.

4. The power semiconductor device according to anyone of claims 1 to 3, wherein the second semiconductor layer (12) has a doping profile along a thickness direction with a first portion for which $\left|\frac{d}{dz}(log_{10}(n_2(z) \cdot cm^3)\right| < 0.02/\mu m$ and a step-like second portion connecting the first portion with a third portion of a doping profile of the third semiconductor layer (13), wherein for the second portion $\left|\frac{d}{dz}(log_{10}(n_2(z) \cdot cm^3)\right| \geq 0.02/\mu m$ and wherein for the second portion the maximum for $\left|\frac{d}{dz}(log_{10}(n_2(z) \cdot cm^3)\right|$ is at least 0.2/µm, exemplarily at least 0.5/µm, and wherein z is a position along the thickness direction.

5. The power semiconductor device according to claim 4, wherein $\frac{|n_2(z_0)-\overline{n_3}|}{\overline{n_3}} \geq 0.05$, or $\frac{|n_2(z_0)-\overline{n_3}|}{\overline{n_3}} \geq 0.1$, and

wherein $n_2(z_0)$ is the doping concentration in the doping profile of the second semiconductor layer (12) along the thickness direction at a point z_0, where the first portion connects to the second portion, and $\overline{n_3}$ is a mean doping concentration in the doping profile of the third semiconductor layer (13) along the thickness direction.

6. The power semiconductor device according to anyone of claims 1 to 5, wherein a combined thickness ($d_{23} = d_2 + d_3$) of the second semiconductor layer (12) and the third semiconductor layer (13) fulfils $d_{23} < 0.12 \cdot \frac{\mu m}{Volt} \cdot U$, U being the breakdown voltage of the device in Volt.

7. The power semiconductor device according to anyone of claims 1 to 6, wherein a minimum doping concentration $n_{2,min}$ in the second semiconductor layer (12) is larger than a maximum doping concentration $n_{3,max}$ in the third semiconductor layer (13).

8. The power semiconductor device according to anyone of claims 1 to 7, wherein $\frac{\overline{n_2}}{\overline{n_4}} > 0.025$, $\overline{n_2}$ is a mean doping concentration in the doping profile along the thickness direction of the second semiconductor layer (12) and $\overline{n_4}$ is a mean doping concentration in the doping profile along the thickness direction of the fourth semiconductor layer (14).

9. The power semiconductor device according to anyone of the claims 1 to 8, further comprising

a fifth semiconductor layer (15) of the first conductivity type arranged between the fourth semiconductor layer (14) and the second main side (19), the fifth semiconductor layer (15) having a fifth doping concentration n_5 in a range from $1 \cdot 10^{17}$ to $5 \cdot 10^{20}$ cm^{-3}, the fifth semiconductor layer (15) forming a second p-n junction with the fourth semiconductor layer (14), the fifth semiconductor layer (15) being in electrical contact with the second electrode layer (22);

a sixth semiconductor layer (16) of the second conductivity type arranged between the first main side (18) and the first semiconductor layer (11), the sixth semiconductor layer (16) having a sixth doping concentration n_6 and being in electrical contact with the first electrode layer (21), the sixth semiconductor layer (16) and the first semiconductor layer (11) forming a third p-n junction; and

a third electrode layer (23) arranged at the first main side (18), the third electrode layer (23) being electrically separated from the first semiconductor layer (11), the first electrode layer (21) and the sixth semiconductor layer (16).

10. The power semiconductor device according to claim 9, wherein $0.01 < \frac{\overline{n_4}}{\overline{n_5}} < 1$, $\overline{n_4}$ being a mean doping concentration of a doping profile along the thickness direction of the fourth semiconductor layer (14) and $\overline{n_5}$ being a mean doping concentration of a doping profile along the thickness direction of the fifth semiconductor layer (15).

11. A method for manufacturing the power semiconductor device according to anyone of claims 1 to 10, the method comprising following steps:

a step of forming a semiconductor wafer (1) which has a first main side (18) and a second main side (19) opposite to the first main side (18) and which includes in the order from the first main side (18) to the second main side (19) the following layers:

a first semiconductor layer (11) of a first conductivity type having a first doping concentration n_1;

a second semiconductor layer (12) of a second conductivity type different from the first conductivity type and forming a first p-n junction with the first semiconductor layer (11), the second semiconductor layer (12) having a second doping concentration n_2 of less than $2 \cdot 10^{14}$ cm^{-3} and a thickness d_2 of less than 100 µm;

a third semiconductor layer (13) of the second conductivity type, the third semiconductor layer (13) having a third doping concentration n_3 which is different from the second doping concentration n_2 of the second semiconductor layer (12), the third doping concentration n_3 being substantially constant along a thickness direction of the third semiconductor layer (13), which is a direction perpendicular to the first main side (18) and the second main side (19), the third doping concentration n_3 being less than $2 \cdot 10^{14}$ cm^{-3}, and the third semiconductor layer (13) having a thickness d_3 of less than 100 µm;

a fourth semiconductor layer (14) of the second conductivity type arranged between the second main side (19) and the third semiconductor layer (13), the fourth semiconductor layer (14) having a thickness d_4 of less than 2 µm and a fourth doping concentration n_4 in a range from $5 \cdot 10^{15}$ to $5 \cdot 10^{18}$ cm^{-3},

a step of forming a first electrode layer (21) on the second main side (19) in electrical contact with the first semiconductor layer (11);

a step of forming a second electrode layer (22) on the second main side (19);

wherein the step of forming a semiconductor wafer (1) comprises:

providing a semiconductor substrate (131) having a first side (138) and a second side (139) opposite to the first side (138), the semiconductor substrate (131) having the second conductivity type and the third doping concentration n_3 of the third semiconductor layer (13),

growing an epitaxial layer (121) of the second conductivity type on the first side (138) of the semiconductor substrate (131), the epitaxial layer (121) having a fourth side (129) at the first side (138) of the semiconductor substrate (131) and a third side (128) opposite to the fourth side (129),

after the step of growing the epitaxial layer (121), forming the first semiconductor layer (11) at the third side (128) of the epitaxial layer (121), the first semiconductor layer (11) having a sixth side (119) at the third side of the epitaxial layer (121) and a fifth side (118) opposite to the sixth side (119),

thinning the semiconductor substrate (131) by removing material at its second side (139),

applying dopants of the second conductivity type at the second side (139) before or after thinning of the semiconductor substrate (131), and

activating the applied dopants of the second conductivity type while avoiding temperature levels above 450°C at the first main side (18) of the semiconductor wafer (1).

12. The method according to claim 11, wherein

the step of forming the semiconductor wafer (1) further comprises:

forming a fifth semiconductor layer (15) by applying dopants of the first conductivity type at the second side (139) of the semiconductor substrate (131) to form a second p-n junction with the fourth semiconductor layer (14),

activating the applied dopants of the first conductivity type while avoiding temperature levels above 450°C at the first main side (18) of the semiconductor wafer (1),

forming a sixth semiconductor layer (16) of the second conductivity type at the fifth side (118) of the first semiconductor layer (11), the sixth semiconductor layer (16) and the first semiconductor layer (11) forming a third p-n junction; and

the method further comprises

a step of forming a third electrode layer (23) at the first main side of the semiconductor wafer (1), the third electrode layer (23) being electrically separated from the first semiconductor layer (11), the sixth semiconductor layer (16) and the first electrode layer (11), and

wherein in the step of forming the second electrode layer (22), the second electrode layer (22) is formed to be in electrical contact with the fifth semiconductor layer (15).

13. The method according to claim 12, wherein the applied dopants of the second conductivity type and the applied dopants of the first conductivity type are activated in the same activation step.

14. The method according to anyone of the claims 11 to 13, wherein after the step of growing the epitaxial layer (121) a temperature at an interface (81) between the

second semiconductor layer (12) and the third semiconductor layer (13) is kept below 1200°C, exemplarily below 1000°C and does not exceed 700°C for longer than 16 hours, exemplarily 8 hours.

15. The method according to anyone of claims 11 to 14, wherein

the step of thinning the semiconductor substrate (131) is performed after the at least one electrode forming step at the first main side (18) of the semiconductor wafer (1);

the at least one step of applying dopants is performed by ion implantation and performed after the step of thinning the semiconductor substrate (131), and

the at least one step of activating the applied dopants is performed by laser annealing.

Fig. 1

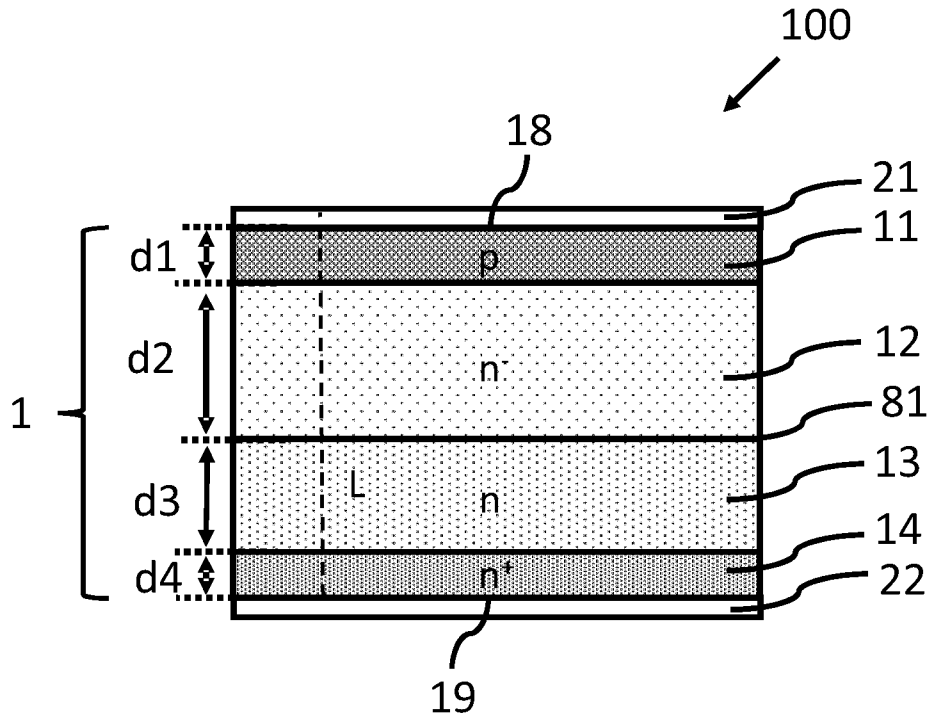


Fig. 2

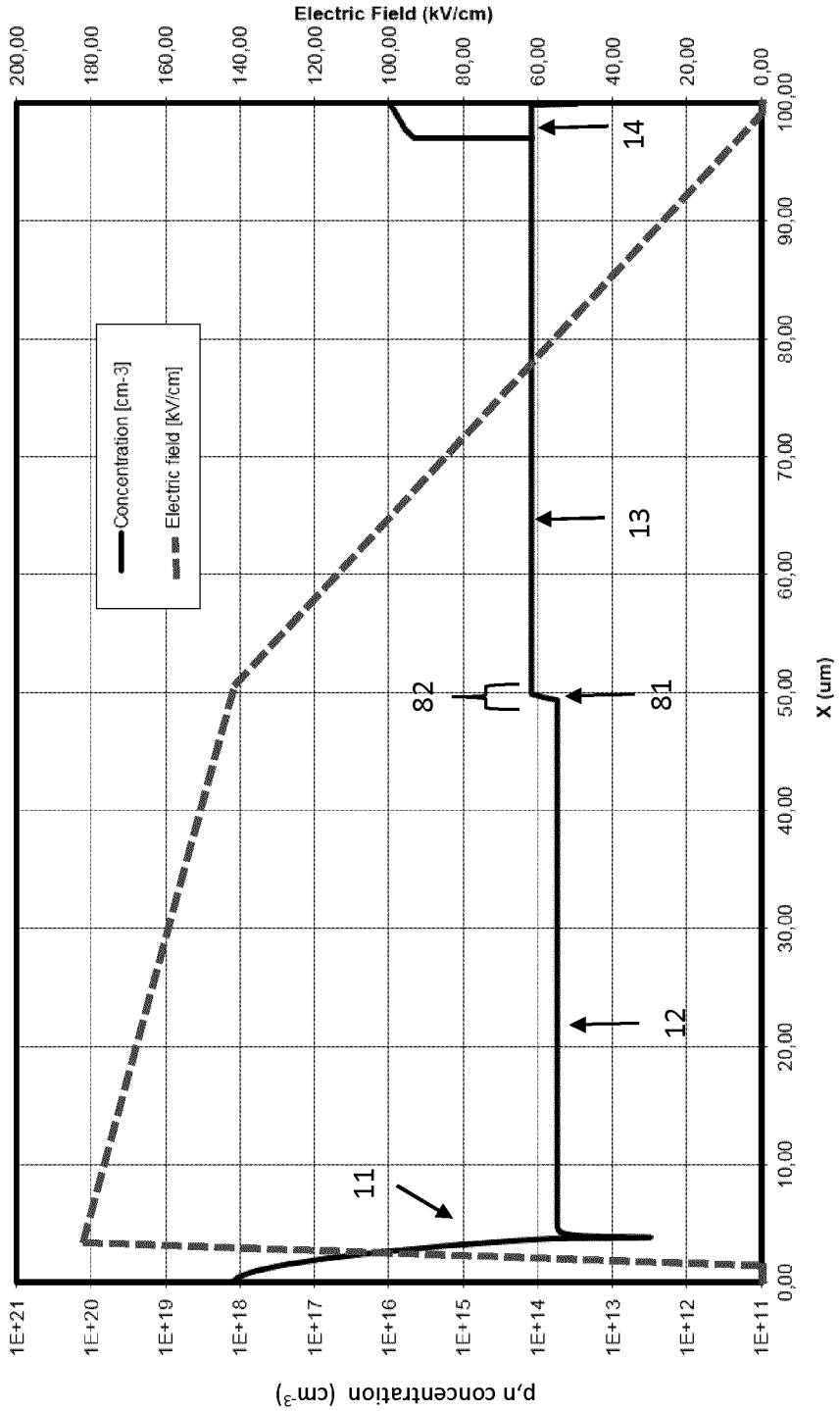

Electric Field (kV/cm)
200,00
180,00
160,00
140,00
120,00
100,00
80,00
60,00
40,00
20,00
0,00
Concentration [cm-3]
Electric field [kV/cm]
11
12
13
14
81
82
X (um)
0,00
10,00
20,00
30,00
40,00
50,00
60,00
70,00
80,00
90,00
100,00
1E+21
1E+20
1E+19
1E+18
1E+17
1E+16
1E+15
1E+14
1E+13
1E+12
1E+11
p,n concentration (cm-3)

Fig. 3

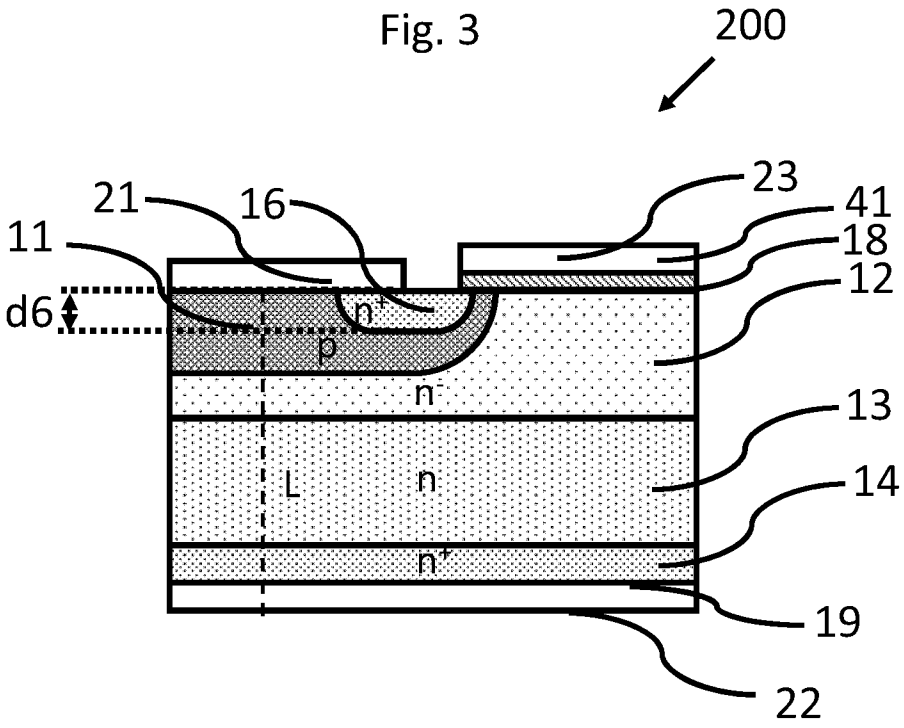

200
21
16
23
41
11
18
12
d6
n+
p
n-
13
L
n
14
n+
19
22

Fig. 4

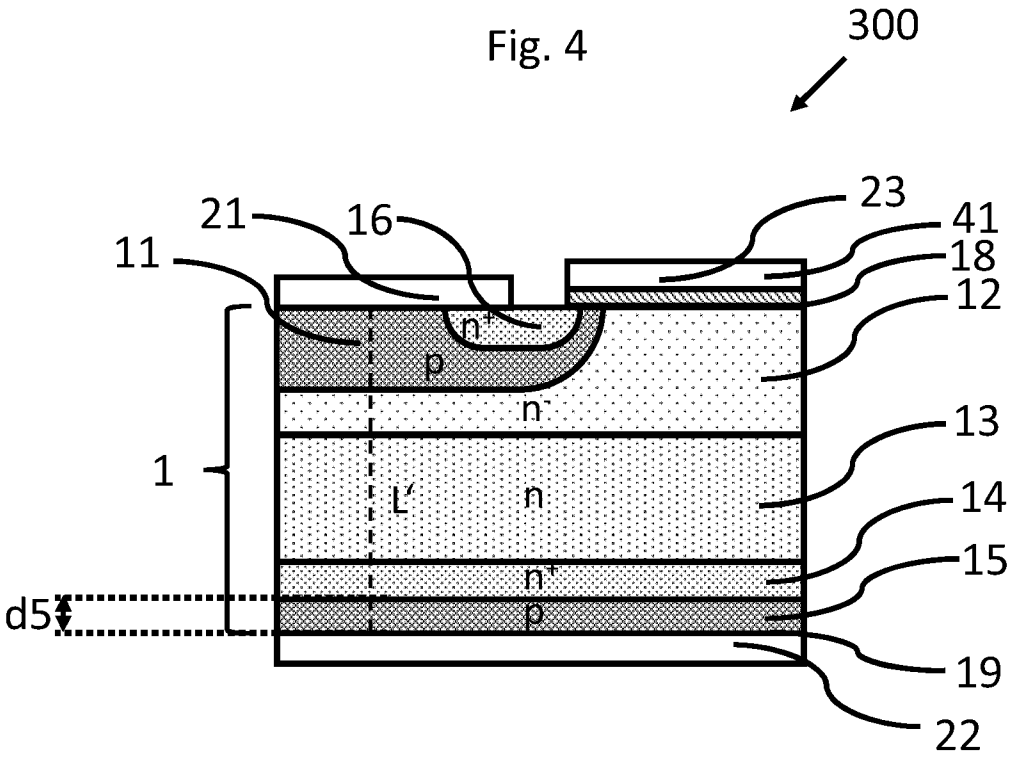
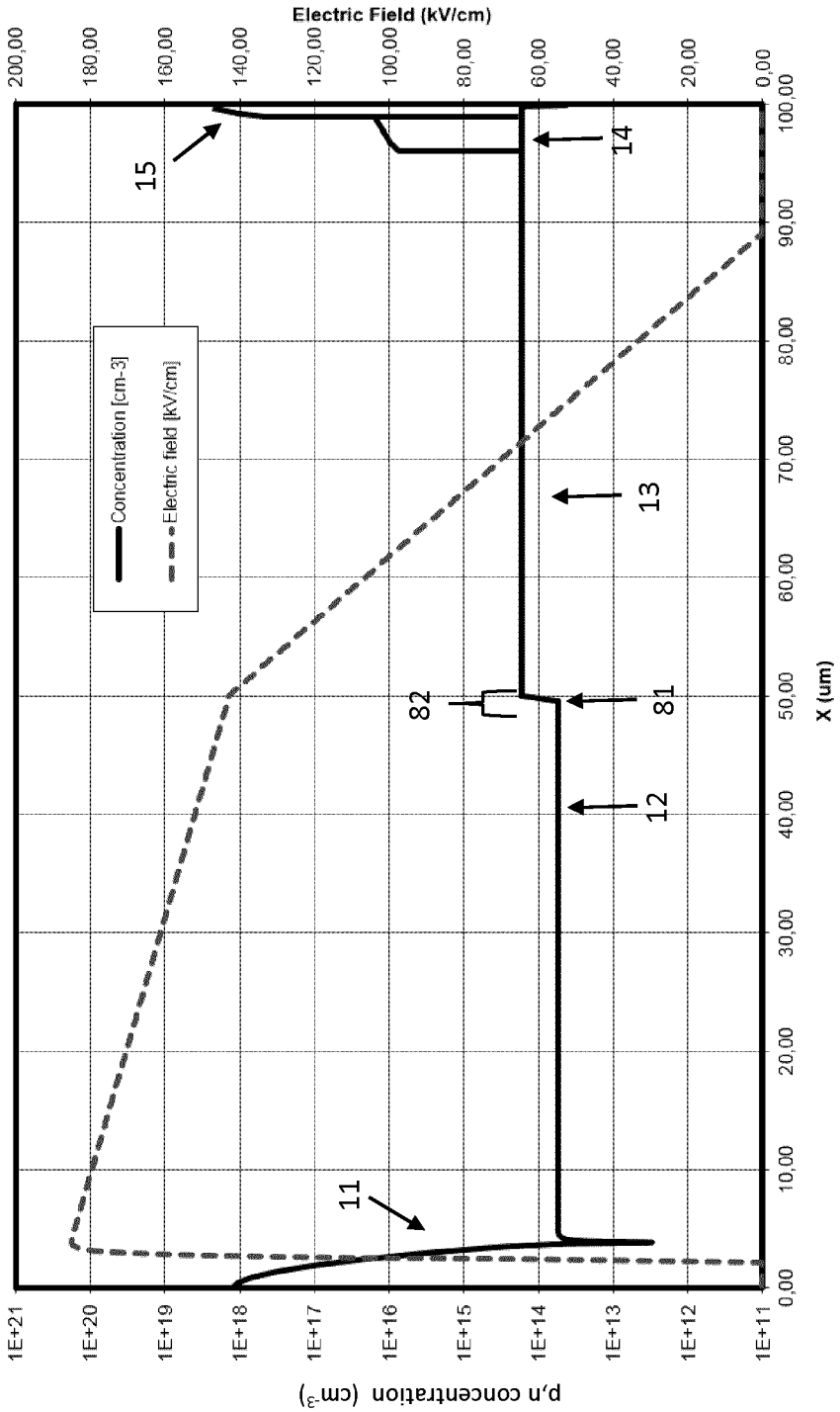

300
21
16
23
41
11
18
12
n+
p
n-
13
1
L'
n
14
15
n+
d5
p
19
22

Fig. 5


Electric Field (kV/cm)
200,00
180,00
160,00
140,00
120,00
100,00
80,00
60,00
40,00
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0,00
100,00
90,00
80,00
70,00
60,00
50,00
40,00
30,00
20,00
10,00
0,00
X (um)
Concentration [cm-3]
Electric field [kV/cm]
15
14
13
82
81
12
11
1E+21
1E+20
1E+19
1E+18
1E+17
1E+16
1E+15
1E+14
1E+13
1E+12
1E+11
p,n concentration (cm-3)

Fig. 6A

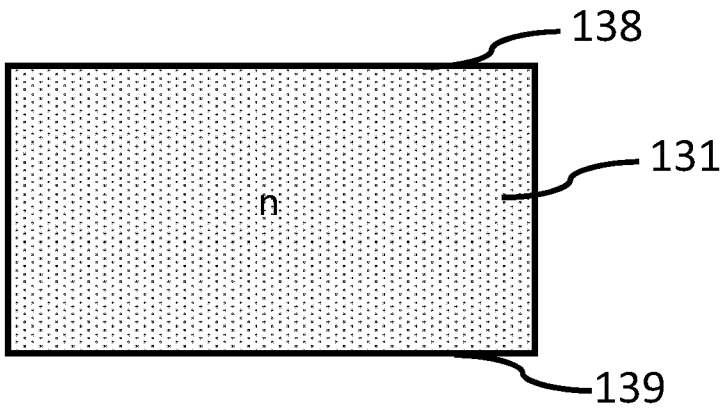


Fig. 6B

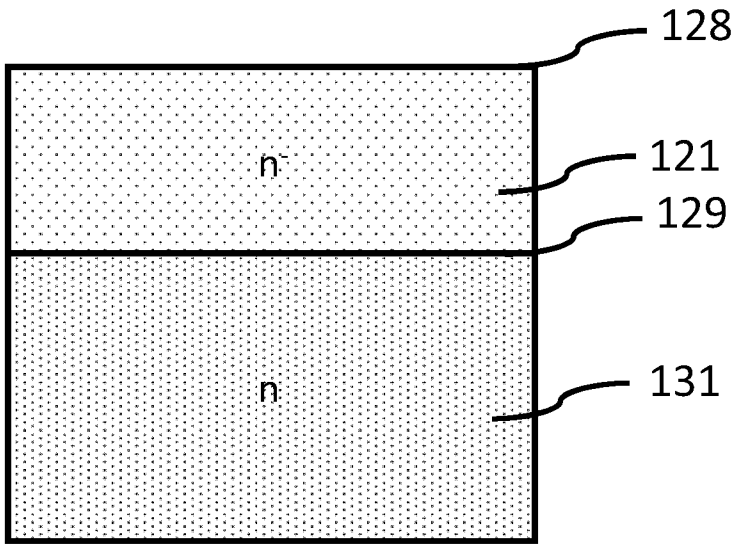


Fig. 6C

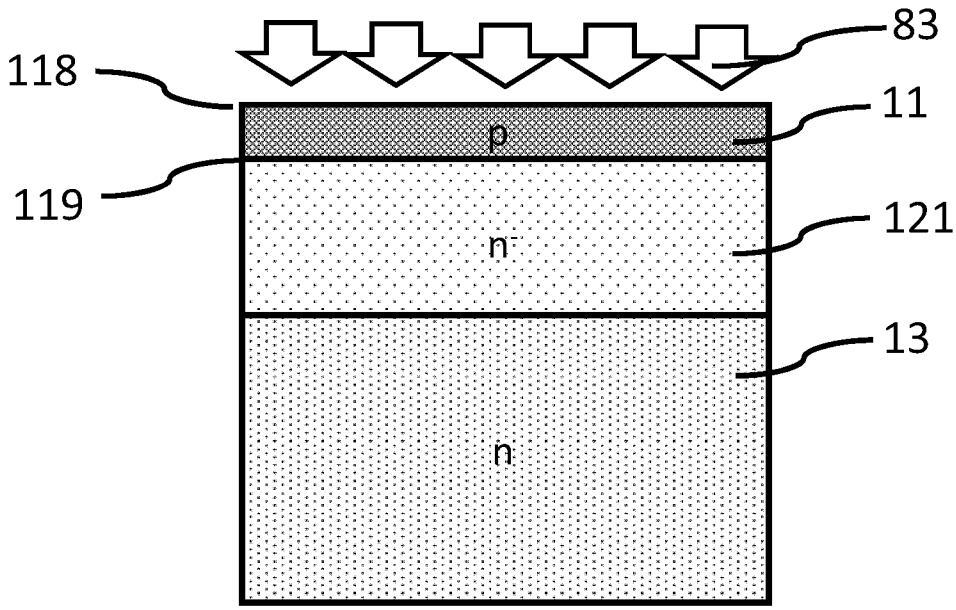


Fig. 6D

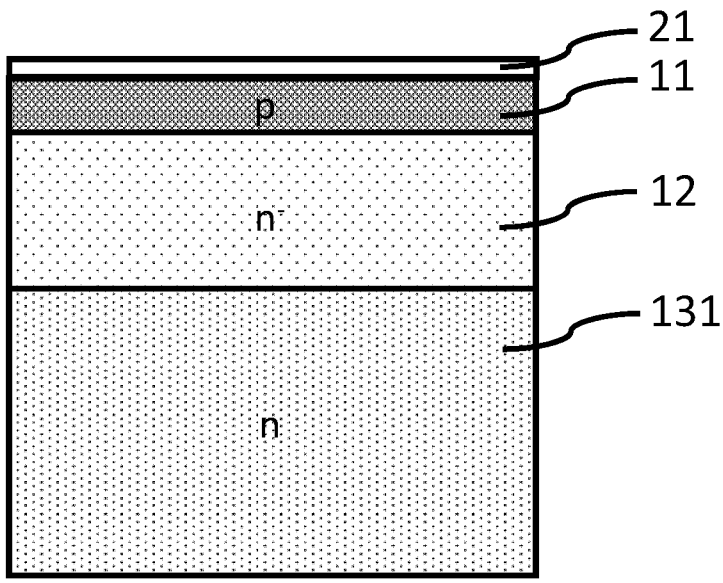


Fig. 6E

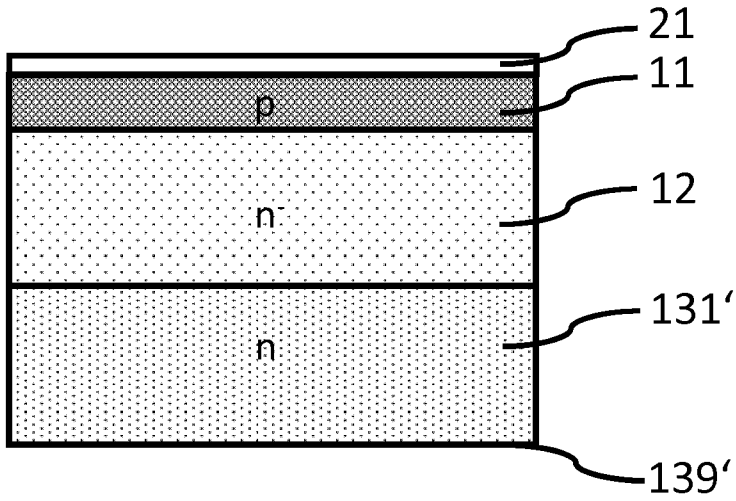


Fig. 6F

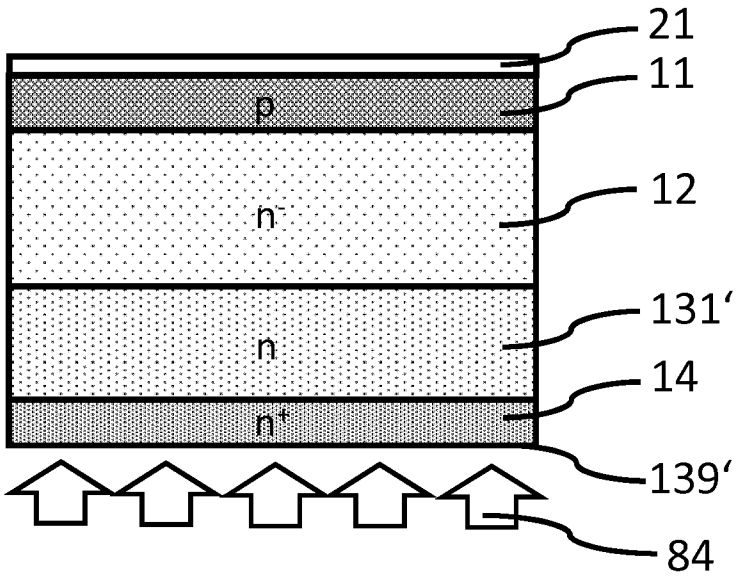


Fig. 6G

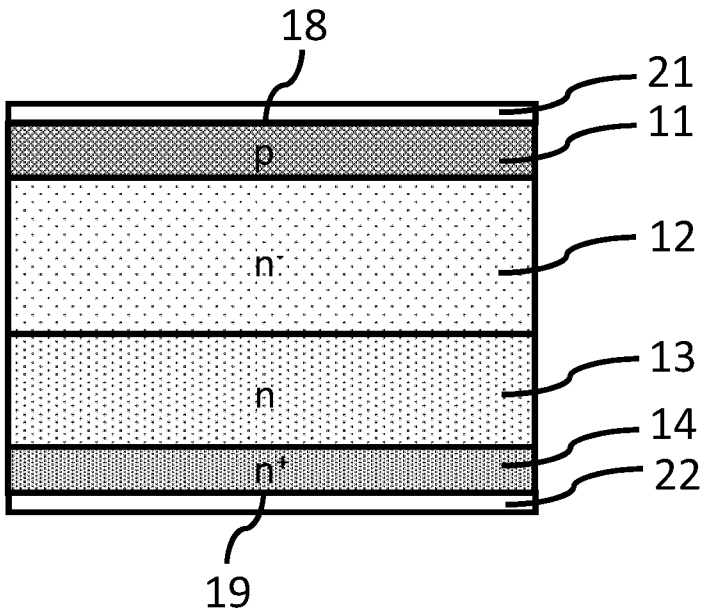


Fig. 7A

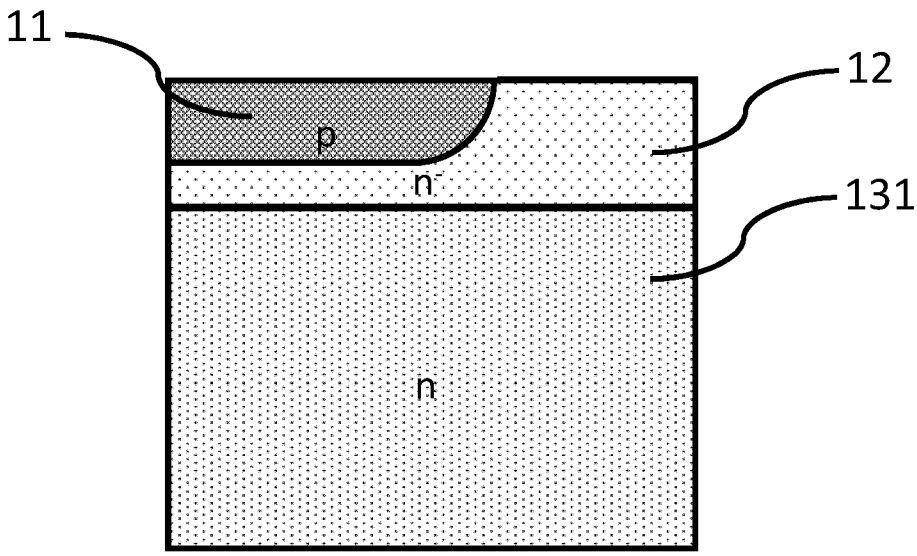


Fig. 7B

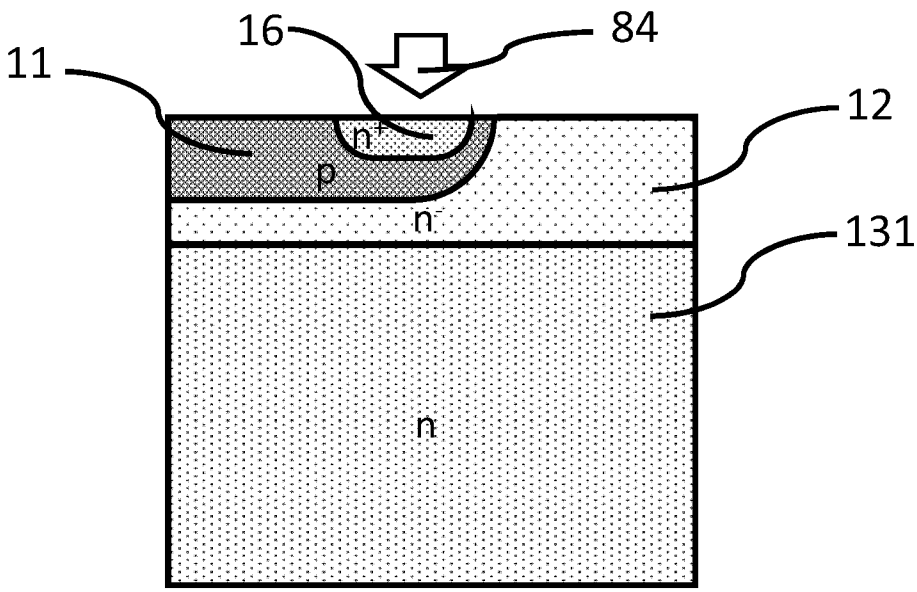


Fig. 7C

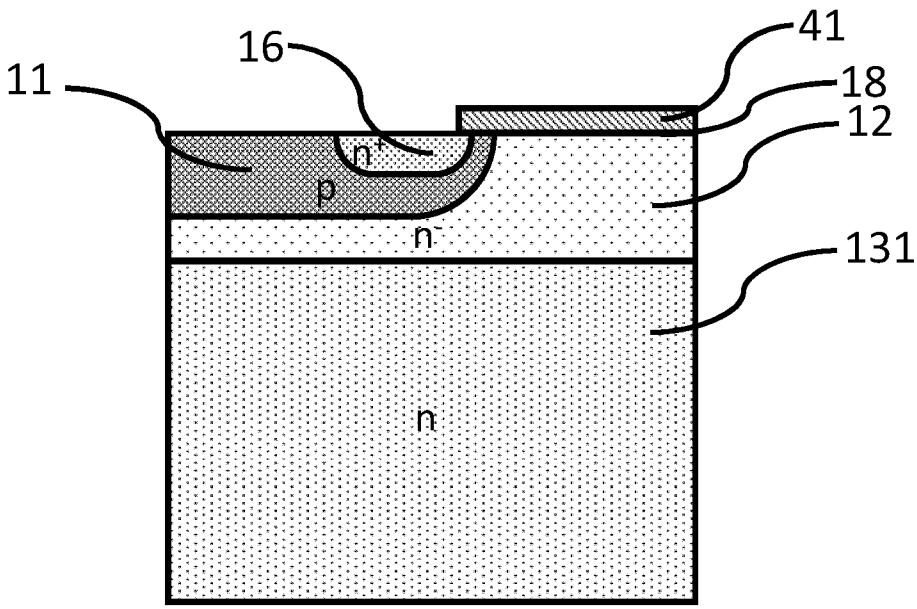


Fig. 7D

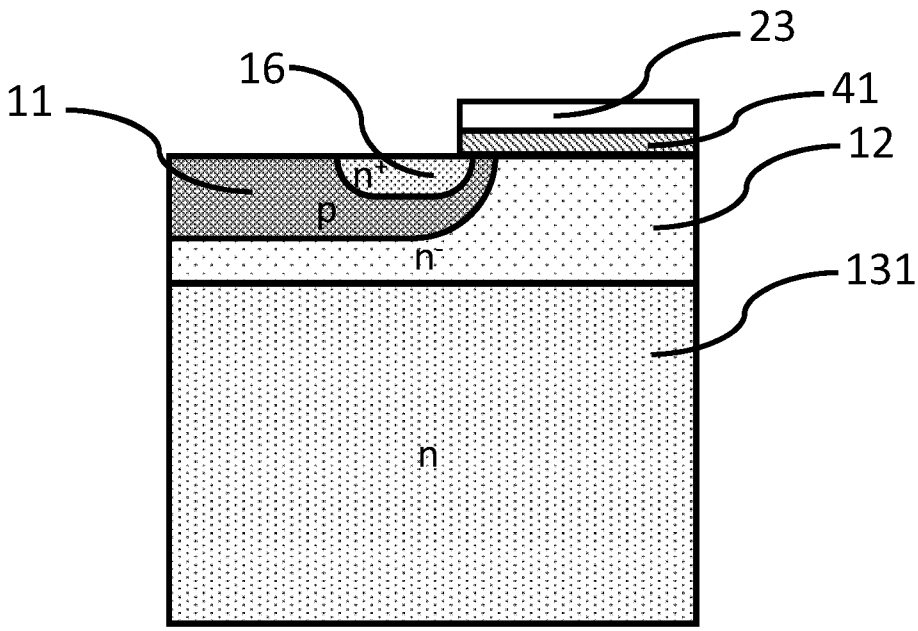


Fig. 7E

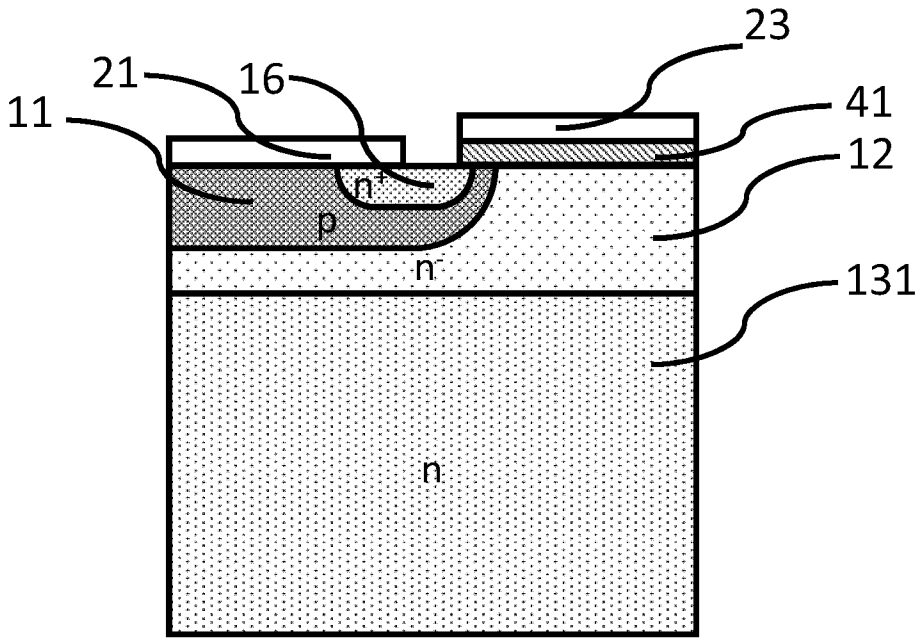


Fig. 7F

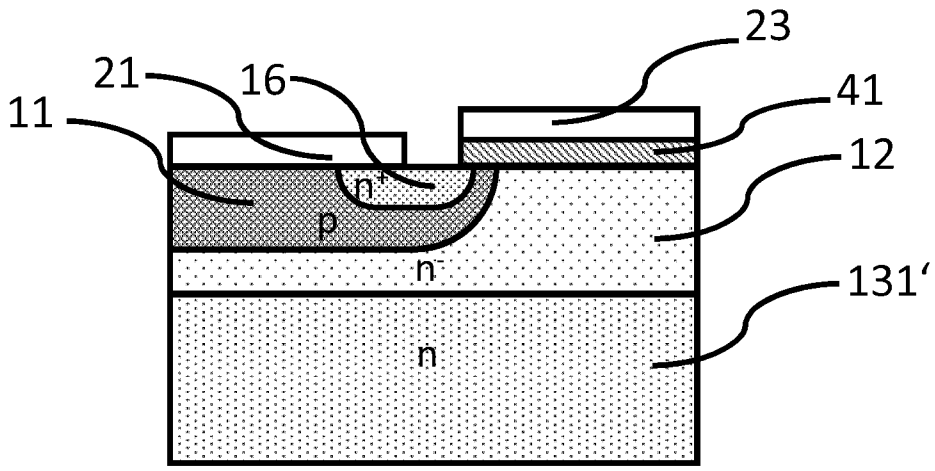


Fig. 7G

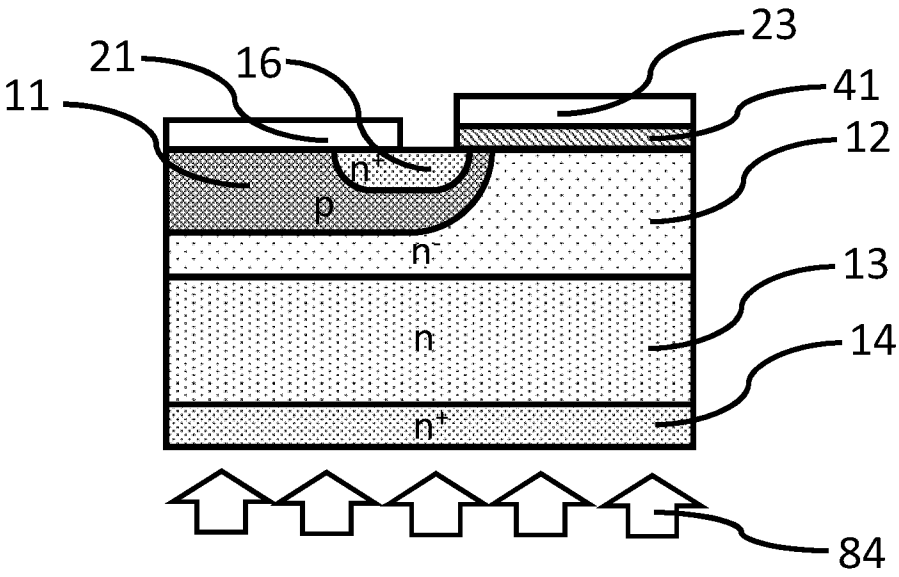


Fig. 7H

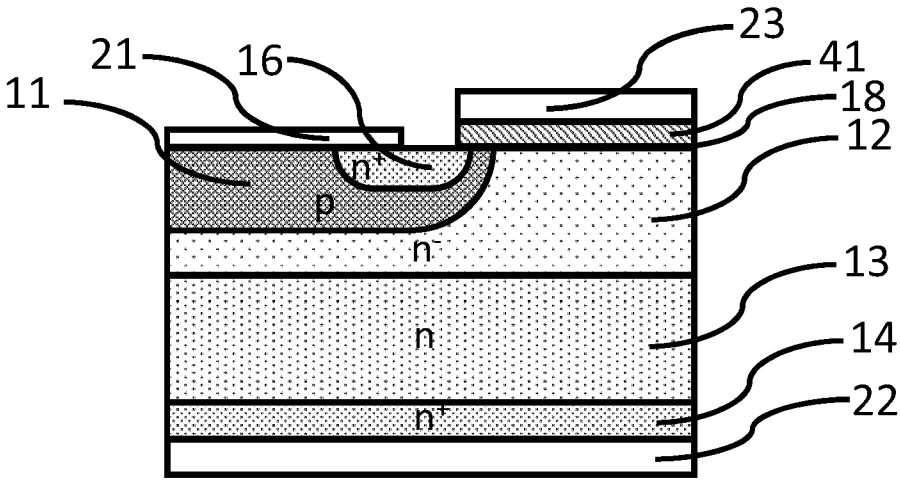


Fig. 8A

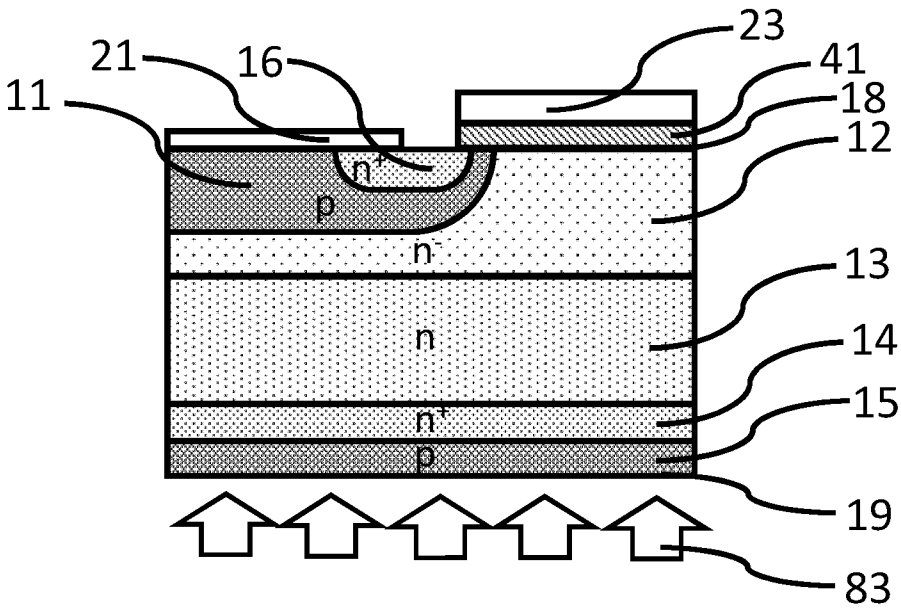

23
21
16
41
11
18
12
n+
p
n-
13
n
14
n+
15
p
19
83

Fig. 8B

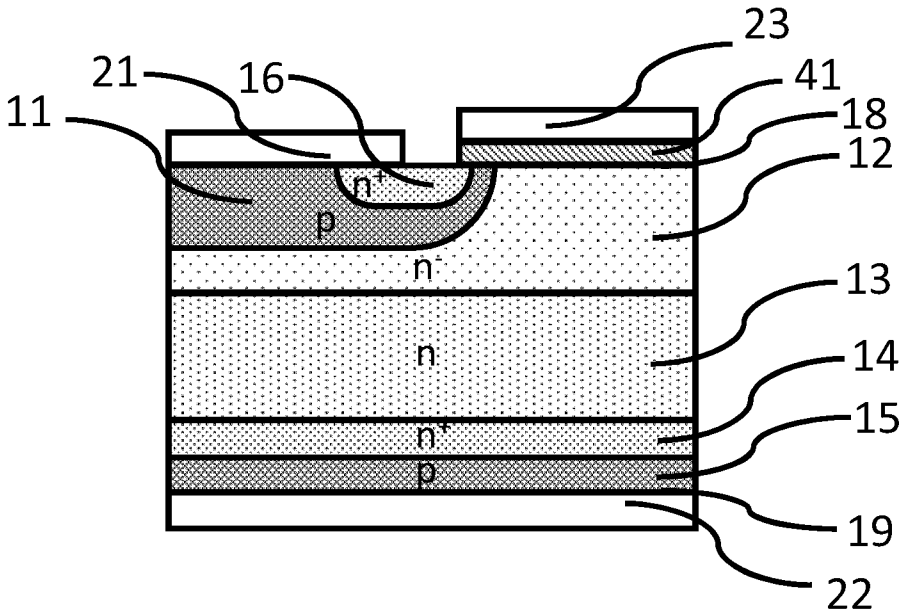

23
21
16
41
11
18
12
n+
p
n-
13
n
14
n+
15
p
19
22

Fig. 9

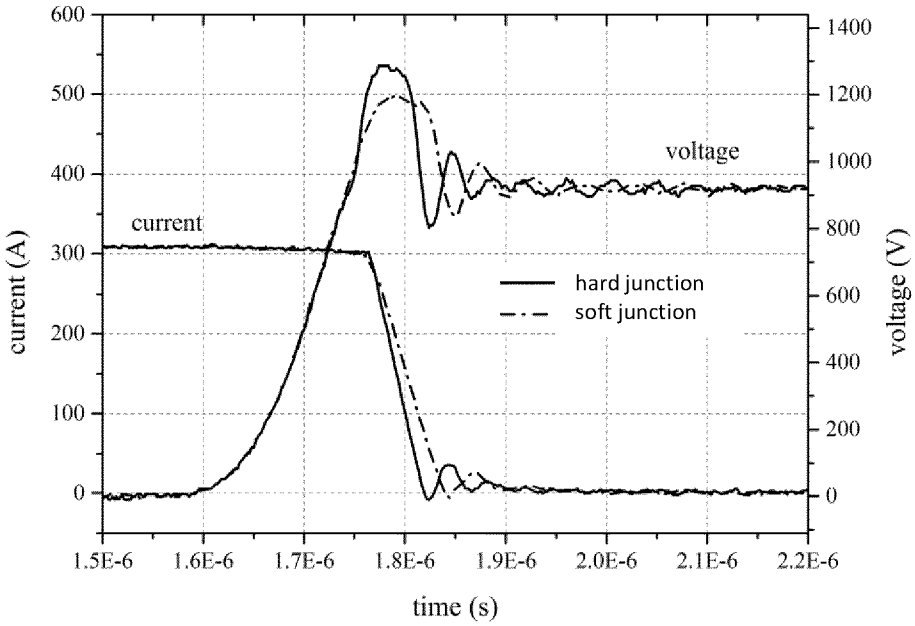

current (A)
voltage (V)
time (s)
current
voltage
hard junction
soft junction
600
500
400
300
200
100
0
1400
1200
1000
800
600
400
200
0
1.5E-6
1.6E-6
1.7E-6
1.8E-6
1.9E-6
2.0E-6
2.1E-6
2.2E-6

Fig. 10

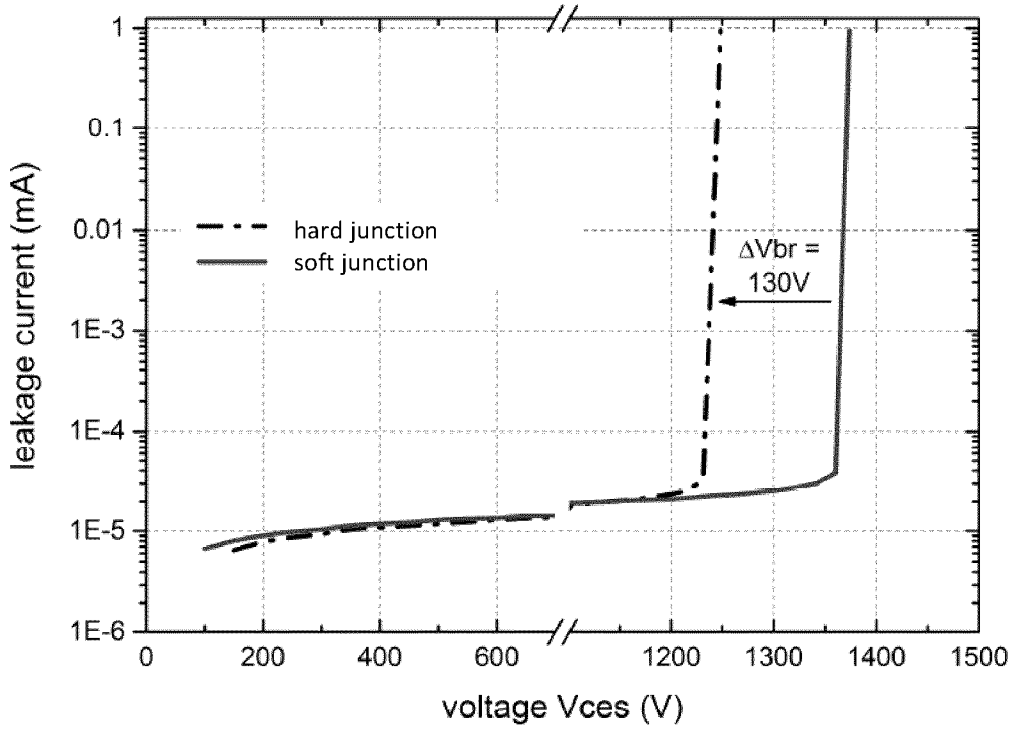

leakage current (mA)
voltage Vces (V)
hard junction
soft junction
ΔVbr =
130V
1
0.1
0.01
1E-3
1E-4
1E-5
1E-6
0
200
400
600
1200
1300
1400
1500

Fig. 11

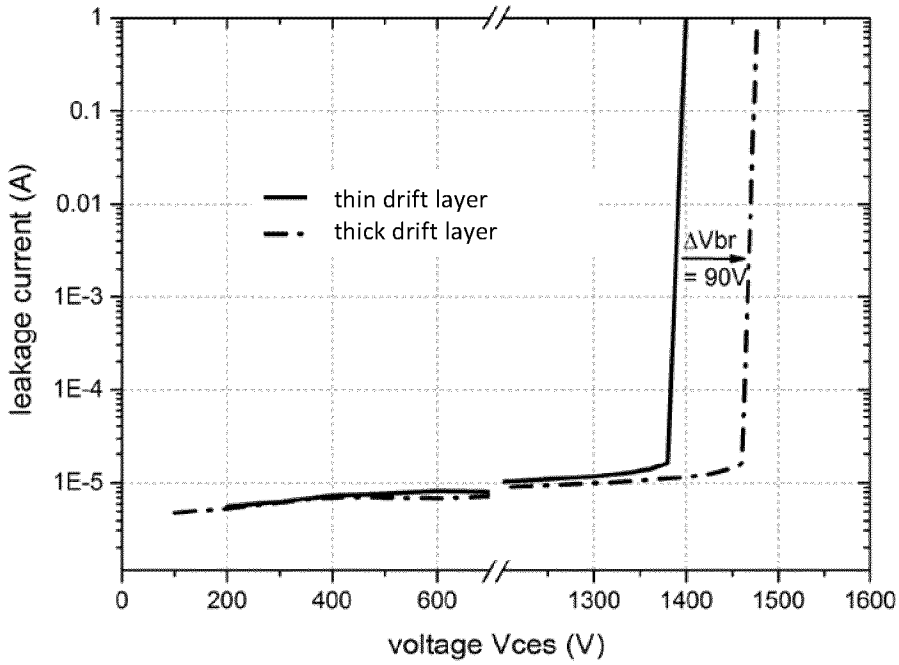
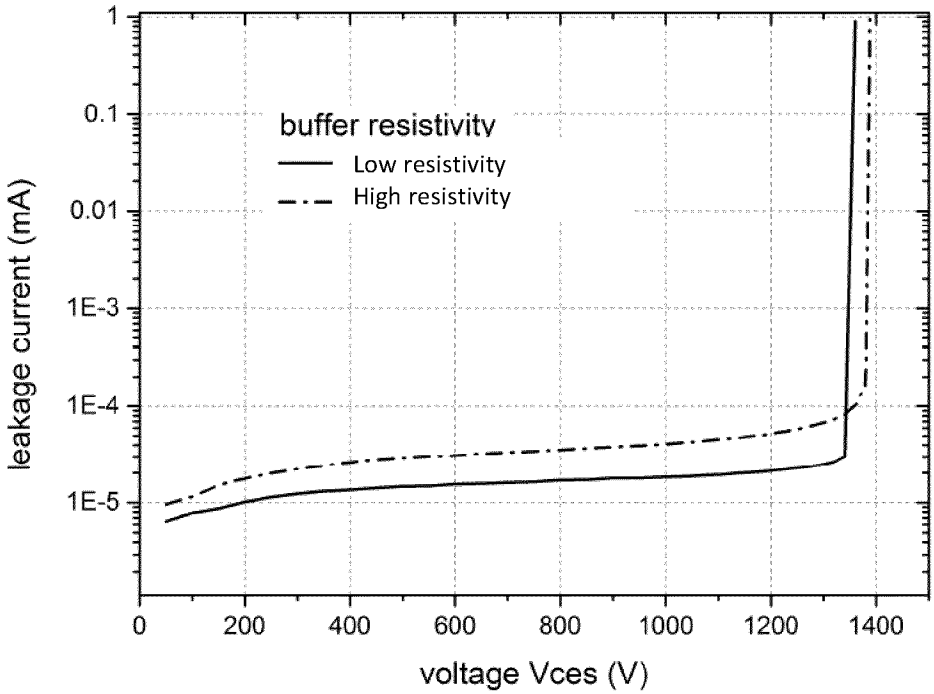

leakage current (A)
1
0.1
0.01
1E-3
1E-4
1E-5
thin drift layer
thick drift layer
ΔVbr
= 90V
0
200
400
600
1300
1400
1500
1600
voltage Vces (V)

Fig. 12


leakage current (mA)
1
0.1
0.01
1E-3
1E-4
1E-5
buffer resistivity
Low resistivity
High resistivity
0
200
400
600
800
1000
1200
1400
voltage Vces (V)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2020/063030

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/331 H01L21/336 H01L21/329 H01L29/78 H01L29/739
H01L29/861 H01L29/36
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 237 200 A2 (TOSHIBA KK [JP]) 4 September 2002 (2002-09-04) paragraph [0016] - paragraph [0037] figures 1-6	1-15

X	US 8 084 814 B2 (NEMOTO MICHIO [JP]; NAKAZAWA HARUO [JP]; FUJI ELECTRIC CO LTD [JP]) 27 December 2011 (2011-12-27)	1-10
A	column 10, line 4 - column 11, line 8 column 20, line 49 - column 21, line 21 figures 1,14	11-15

X	US 2004/041225 A1 (NEMOTO MICHIO [JP]) 4 March 2004 (2004-03-04)	1-10
A	paragraph [0016] figures 3A,3B,8	11-15

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 June 2020	23/06/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kostrzewa, Marek

1

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2020/063030

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2012/007222 A1 (MISUMI TADASHI [JP] ET AL) 12 January 2012 (2012-01-12) paragraph [0029] - paragraph [0040] figures 1-6 -----	1-8,11, 14,15 9,10,12, 13

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2020/063030

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2012007222 A1	12-01-2012
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