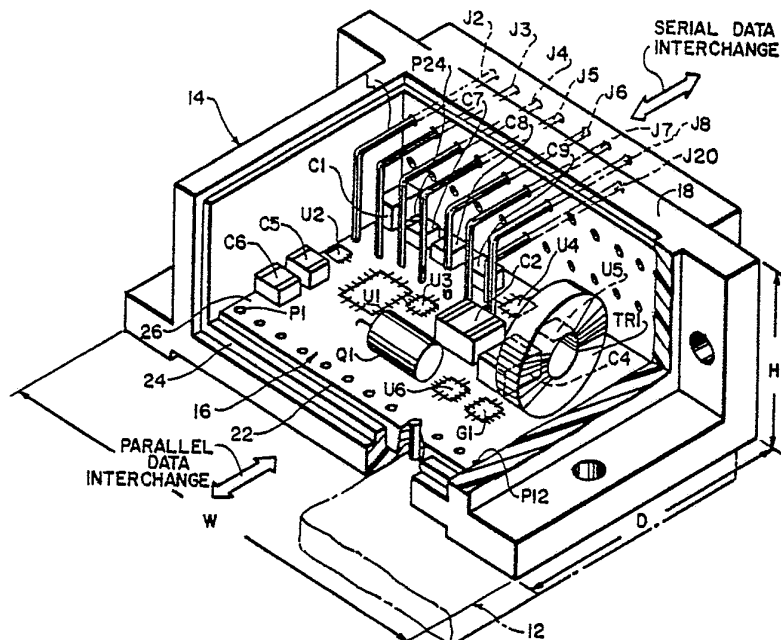




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(54) Title: CONNECTOR INTERFACE



(57) Abstract

A connector interface (10) for enabling communications between first and second data handling systems wherein the data in the first system is arranged in a first type of format and the data in the second system is arranged in a second type of format, includes a connector housing (14) with first and second sets of electrical contact elements exposed at different portions of the housing. Circuitry contained entirely within the housing operates to convert data transmitted to the first set of contact elements from the first data handling system into corresponding data in the second type of format for transmission to the second data handling system through the second set of contact elements, and to convert data transmitted to the second set of contact elements from the second data handling system into corresponding data in the first format for transmission to the first data handling system.

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CONNECTOR INTERFACEBACKGROUND OF THE INVENTION1. Field of the Invention

5 The present invention relates generally to electrical connectors, and particularly to a connector having internal circuitry capable of providing a specified electrical interface between various types of data handling equipment.

2. Description of the Prior Art

10 The proliferation of digital data processing equipment, first in business and now into the home, has created an ongoing demand for such equipment with ever increased capabilities but at an affordable price. The modern trend to integrate numerous discrete electrical components within
15 single semiconductor integrated circuits or "chips", has provided for greater economies in the manufacture of digital electronic equipment. Not only is the overall physical size and weight of the equipment reduced through use of integrated circuit technology, but manufacturing costs also
20 are alleviated in that the price of each integrated circuit used is but a fraction of the total cost represented by all the components it contains.

 Digital data processing systems which are in common use today include portions arranged to allow the user to communicate with the system by way of, for example, a terminal or a printer. The user "talks" or provides
25 information to the system through the terminal, and this information is converted into digital data which the system is capable of understanding. After the data is processed by the system which may include some form of computer, a suitable response is transmitted back to the user in digital form and then properly converted into visibly recognizable words or symbols
30 on the screen of the terminal or on a sheet generated by a printer.

 Accordingly, it is often necessary to provide cable interconnections between differently located units of a data processing system to allow the units to transmit and receive digital data to and from one another.

 Certain types of digital equipment, e.g. a terminal or a printer, transmit or receive digital data in serial bit format. That is, each
35 character (i.e., letter or numeral) of the data is sent or received one bit at a time. It will be appreciated that in a typical system where each character occupies multiple bits, communicating the characters as serial bits between separately located pieces of equipment reduces significantly the number of separate conductors which must be provided in the connecting
40 cables, allows for the communicating equipments to operate in time

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synchronism with one another with regard to the data exchanged between them, as well as for the use of parity bits and other common error detecting techniques to be applied for each data character communicated. Other kinds of equipment in data handling systems operate in a parallel bit format. For example, computers operate on data which is loaded in internal registers one full character (i.e, eight bits) at a time, and likewise provide output information a character at a time to internal output registers.

In order to insure compatability between terminals, printers and other input/output data handling equipment which operate in a serial bit format, and computer mainframes and related equipment, the Electronic Industries Association promulgated in 1969 a now widely accepted interface standard known as EIA RS-232-C, the provisions of which are incorporated by reference herein. The RS-232-C Standard, entitled "Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange", ensures that serial bit format equipment produced by one manufacturer will operate properly with serial bit format equipment of another manufacturer. The RS-232-C Standard applies not only to the interchange of information data signals between data handling equipment, but also to the interchange of timing and control data signals between such equipment (Sec. 1.4 of the Standard).

In order to ensure satisfactory noise immunity of the data signals to be communicated over connecting cables, the RS-232-C Standard provides that the data signals transmitted over the cables have magnitudes of at least ± 6 volts (See Sec. 2.3 of the Standard). Since most data handling equipment today operate at five-volt levels, the Standard makes necessary additional power supplies for enabling a voltage level conversion of the data signals to be interchanged over the connecting cable.

With regard to mechanical characteristics of the interface, the RS-232-C Standard states that the interface is "located at a pluggable connector signal interface point between the two equipments. The female connector ... should be mounted in a fixed position near the data terminal equipment".(Sec. 3.1). Figure 3.1 within the RS-232-C Standard assigns certain circuit functions to each of 25 connector pins associated with the pluggable connector at the signal interface point. While the Standard does not specify a particular type of multiple pin connector (See Appendix I to the Standard), the "D-type" 25 pin connector (for example, AMP type 206584-1) has essentially become an industry standard.

A printed circuit board together with circuit components and software necessary to achieve an RS-232-C interface between a computer terminal on

one side, and modems or serial line printers on the other side, is available from a variety of manufacturers. Such boards are mountable inside the computer, and a separate cable is provided. These boards are compatible from the RS-232-C side but they differ on the computer side from computer
5 to computer.

The known RS-232-C interfaces which include a printed circuit board are arranged physically as shown in FIG. 1. The board B can be a "stand alone card" and be connected via a card cage connector (not shown) to various parallel signal bus lines associated with a microprocessor in a
10 computer or other terminal equipment (also not shown). Alternatively, it can be a part of a more complex board. The RS-232-C Standard 25-pin connector CON may be mounted along one edge of the board B as shown, and the pins directly connected electrically to printed conductors on the board by soldering as at points S on the underside of the board B. This leaves a
15 female connector part F fixedly mounted near the data terminal equipment as required by the Standard. The various conductors to which the pins of the connector CON are connected lead to electrical circuitry arranged over other portions of the board B, including, for example, a main logic element chip IC 1, line driver IC 3, line receiver IC 4, crystal oscillator OSC,
20 frequency divider IC 2, and a number of discrete components C.

It will be appreciated that the known RS-232-C interface board arrangements require that a certain amount of space be allocated in existing equipment for their insertion, such space often being at a premium in units intended to be portable and of small overall dimensions. As far
25 as is known, there has been no attempt to integrate any electrical interface circuitry including those components required to implement the RS-232-C interface as shown in FIG. 1, within the prescribed interface connector itself such as the 25-pin connector CON.

A connector is known from U.S. Patent 3,790,858 to Brancalone et al within which RF filter elements are connected to a number of parallel
30 pin-like contact elements which are supported inside and extend axially through a cylindrical shell. The filter elements are connected internally between the contact elements and a common cylindrical metal ground plate.

35 SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a connector which exhibits simultaneously both the electrical characteristics and the connector requirements of a specified interface between two different data handling systems or equipments.

40 Another object of the invention is to provide a method wherein

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electrical circuitry for carrying out a specified function between two different data handling systems is integrated within a connector housing so as to reduce significantly spatial requirements within equipment associated with the systems.

5 According to one aspect of the invention, a connector includes a housing having a first set and a second set of terminals extending at least partly through wall parts of the housing to engage corresponding terminals of first and second outside connection means associated with first and second data handling systems, respectively. Logic interface circuit means is arranged within the connector housing and coupled between the first and second set of terminals. The circuit means operates to convert data signals transmitted to the first set of terminals from the first data handling system in a first type of format into corresponding data signals in a second type of format, and to provide the corresponding data signals in the second type of format to the second set of terminals for transmission to the second data handling system. The circuit means also operates to convert data signals transmitted to the second set of terminals from the second data handling system in a second type of format into corresponding data signals in a first type of format, and to provide the corresponding data signals in the first type of format to the first set of terminals for transmission to the first data handling system.

10 According to another aspect of the invention, a method of implementing a logical interface to enable communications between a first data handling system in which data signals are arranged in a first type of format, and a second data handling system in which data signals are arranged in a second type of format, includes the steps of providing a connector housing; supporting first and second sets of electrical contact elements on the housing; containing electrical circuitry within the connector housing and connecting the circuitry with the first and the second sets of contact elements by arranging conductors inside the housing; converting by way of the electrical circuitry data signals transmitted to the first set of electrical contact elements in a first type of format from a first data handling system outside the connector housing into corresponding data signals in a second type of format and providing same to the second set of electrical contact elements through the conductors inside the connector housing; and converting by way of the electrical circuitry data signals transmitted to the second set of electrical contact elements in the second type of format from a second data handling system outside the connector housing into corresponding data signals in the first type of format and providing same to the first set of electrical contact elements

through the conductors inside the connector housing.

The invention will be more clearly understood upon reading the following detailed description of preferred embodiments thereof in conjunction with the accompanying drawing.

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BRIEF DESCRIPTION OF THE DRAWING

In the drawing:

FIG. 1 is a perspective view of a conventional serial interface arranged on a portion of a printed circuit board;

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FIG. 2 is a perspective view, with parts broken away, showing a first embodiment of a connector according to the present invention mounted on a printed circuit board;

FIG. 3 is a schematic diagram representing electrical circuitry contained in the housing of the connector in FIG. 2;

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FIG. 4 is a perspective view of a second embodiment of a connector according to the present invention;

FIG. 5 is a perspective view of a third embodiment of a connector according to the present invention;

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FIG. 6A is a top plan view of a printed circuit layout, and the phantom outline of the components, of the electrical circuitry seen in the schematic diagram of FIG. 3; and

FIG. 6B is a bottom plan view of the printed circuit board illustrating the interconnection among the various components.

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DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a first embodiment of a connector 10 according to the invention, the connector 10 being mounted on a printed circuit board 12 associated with a data handling system or equipment (not shown) in which data is interchanged in a parallel format. The connector 10 includes a connector housing 14, portions of which are omitted in FIG. 2 for the purpose of illustrating electrical circuitry 16 mounted in the interior space of the housing 14. It is preferable that walls of the housing 14 substantially enclose the interior space so as to protect the circuitry 16 contained therein.

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As shown in FIG. 2, the housing 14 is in the form of a generally rectangular hollow block and includes a front wall 18, a part of which projects outwardly to define a first outside connection surface 20 parallel to the inside surface of wall 18. Housing 14 also includes a bottom wall 22 the outside surface of which defines a second outside connection surface 24. The outside dimensions of the housing 14, particularly those of the front

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wall 18 together with the first outside connection surface 20, preferably conform to those of a standard socket connector, thereby being adapted to mate with a standard plug connector or corresponding or complementary configuration. For applications in the RS-232-C interface, the housing 14 should conform to the dimensions of the known 25-pin "D type" subminiature connector mentioned earlier. Typical dimensions for the housing 14 thus may be a height H of about 0.5 inches (12.70 mm.), a depth D of about 1.2 inches (30.48 mm.) and a width W of about 2.0 inches (50.80 mm.).

The electrical circuitry 16 includes, in the embodiment of FIG. 2, a carrier in the form of a single printed circuit board or substrate 26 mounted closely adjacent and parallel to the inside surface of the bottom wall 22. Various integrated circuits and discrete components are mounted on the board 26, and are electrically connected by soldering, or by other technology, to conductors on one or both sides of the board 26.

The various "chips" and components shown in FIG. 2 as contained within the connector housing 14 on the board 26, and represented schematically in FIG. 3, include integrated circuits U1 - U6; four tantalum chip capacitors C1 - C4; a set of five chip capacitors C5 - C9; a quartz crystal Q1; a toroid core transformer TR1 having bifilar wound primary and secondary windings T1 - T2 and T4 - T6; and a Graetz diode bridge G1. Each of eight conductors L extends from a different one of eight connection points on the printed circuit board 26 (FIG. 2), to corresponding female electrical contact elements or terminals J2 - J8 and J20 which extend partly through and are supported in openings in the wall 18. The outside ends of the female contact elements are exposed at the first outside connection surface 20 to engage corresponding pins of an outside plug connector (not shown). The numbers assigned to the female contact elements J2 - J8 and J20 correspond to the pin number-circuit function assignments prescribed in the RS-232-C Standard, mentioned earlier. Further, 24 male electrical contact elements or pins P1 - P24 extend in two parallel rows of 12 pins each, downwardly from connection points near the long edges of the board 26 (FIG. 2), to engage openings in printed conductors or a conventional dual in line socket on the outside printed circuit board 12, at the second outside connection surface 24.

In accordance with a preferred technique of manufacture, the housing 14, except for the bottom wall 22, is molded in one piece; the elements or terminals J2 - J8 and J20, as well as the conductors L, being included in the molding operation. Then, the bottom wall 22 and abutting printed circuit board 26 are snapped into position in the housing. By means of localized heating, the bottom wall is fused to the housing so that a

completely unitary structure is achieved.

FIG. 3 shows the interconnections between the chips and other electrical components on the printed circuit board 26 contained within the connector housing 14, together with the female and the male contact elements arranged on the first and the second outside connection surfaces 20, 24 of the connector 10, respectively. The circuitry of FIG. 3 is one example of circuitry which functions to provide the electrical characteristics of an RS-232-C interface, but it will be appreciated that different circuitry may be integrated within the connector housing 14 to carry out the same function or other commonly used interfaces including 8-bit Parallel, GPIB (general purpose interface bus- IEEE 488), and Ethernet.

The integrated circuit U1 may be, for example, National Semiconductor type INS 8250A. The circuit U1 serves as a main logic element which handles all data signal interchanges between, e.g., a microprocessor (not shown) which handles data in a parallel bit format and communications equipment (not shown) which sends and receives serial bit data. Circuit U1 contains several programmable registers which determine the communications format and all the necessary information data to perform successfully a two-way data interchange between two data systems of different data formats. Specifically, before sending or receiving any data via an RS-232-C line, a controlling microprocessor (not shown) must load the internal registers with the required commands. The system software contains the following load functions which, when programmed within circuit U1, enable the latter to be used for data communications. The preprogrammed functions are:

1. Baud rate and baud rate factor;
2. Character length;
3. Number of stop bits;
4. Parity enable/disable and parity polarity;
5. Modem control functions; and
6. Additional operational conditions.

Instructions representing the above load functions are transmitted to the circuit U1 from an outside microprocessor (not shown) over data bus lines D0-D7 corresponding to the male contact elements or pins P1 - P8 on the second outside connector surface 24 of the connector housing 14 (FIG. 2). The appropriate registers within circuit U1 are selected by the address bus lines A, A1 and A2 (pins P23, P22 and P21), and a write signal (\overline{WR} , pin P19) validates the register loadings.

When data characters are transmitted by the outside microprocessor

after the foregoing initialization procedure, the circuit U1 performs a parallel-to-serial data conversion. First, the eight-bit parallel data is placed into a transmitter register within circuit U1 which then automatically adds a start bit, followed by the data character bits themselves (least significant first) and the programmed number of stop bits for each character. Also, an even or odd parity bit is inserted prior to the stop bit(s) as defined previously by the system. The character is then transmitted as a serial data stream on a data output line Sout at terminal 11 of the circuit U1. The rate at which the data is shifted out is determined by another previously programmed register within circuit U1. The quartz crystal Q1 coupled to the circuit U1 operates together with a programmable divider within circuit U1 to generate a signal of the appropriate frequency for shifting out the data bits.

The strength or voltage levels of the data bits or signals shifted out from the circuit U1, typically TTL compatible (zero to +5 volts). As mentioned earlier, the RS-232-C Standard requires a stronger signal level so that data can be transmitted over a long cable with the capacity of noise suppression. Accordingly, a line driver circuit U3, e.g., Motorola type MC 1488, is coupled to data output Sout and supplementary handshake signals as $\overline{\text{RTS}}$ (Request to Send) and DTR (Data Terminal Ready) of the circuit U1. When powered by an appropriate power supply, the line driver circuit U3 converts the TTL compatible level (zero to +5 volt) of the serial output from the circuit U1, to a +12 volt level sufficient to satisfy the RS-232-C Standard. The integral power supply is constructed of a push-pull mode switching scheme, performed by high frequency oscillator derived from U4 (e.g. 4516B RCA), 74C86 exclusive OR gates (U6 e.g. Nat. Semiconductor), high current power transistors within U5 (75951 e.g. Texas Instruments) Tr1 transformer, G1 diode bridge and C2,C3 tantalum capacitors.

When a serial data bit stream is transmitted to the connector 10 from an outside data handling system, specifically to the female contact elements J3 at the first outside connection surface 20 of the housing 14, the higher voltage level of the bit streams is converted to a TTL compatible (0 to 5 volt) logic level by way of buffer-inverters within circuit U2 (e.g., Motorola type MC 1489A). Also, high level complementary signals (J5, J6 and J8 are converted down). The serial data is then shifted into a receiver register within the main logic element circuit U1 where the data is converted into a parallel format; however, the start and stop bits and the parity bit are subtracted. Thus, the data is then ready to be sent to the microprocessor or other outside parallel format data

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system over the data bus lines D0-D7.

The circuit U1 is selected for operation by the microprocessor or other outside parallel data system connected to the pins P1-P24 of the connector 10 by way of a chip select signal (\overline{CS} , pin P18). The receiver register within the circuit U1 is selected by a preset combination of the address bus lines (A0, A1, A2; pins P23, P22, P21), and the parallel data is placed on the data bus lines (D0-D7; pins P1-P8) for transmission to the outside microprocessor. A read signal (\overline{RD} , pin P20) activates the data reading from the circuit U1 to the microprocessor. Likewise, status information reading procedure can be performed similarly.

There are several control signals, and control and status registers in circuit U1 that determine the bidirectional serial communication procedure. All the necessary signals, including "handshaking", status and command bits, and modem control are included in communications following the preprogrammed functions from the outside microprocessor software.

Those components on the board 16 (FIG.2) which have not been discussed above in detail but appear in the circuitry of FIG. 3 will be recognized and understood by those skilled in the art. A preferred quartz crystal Q1 is Seiko type DS-MGQ, 1.8432 MHz, series resonant. The chip capacitors C1-C4 may be Arco type ACT, tantalum, and the chip capacitors C5-C9 may be Murata type GR40 Y5V. Chip resistors R1-R3 can be Panasonic type ERJ-86CSJ, or alternatively can be thick film resistors deposited on the board 16.

The toroid transformer TR1 preferably is made from a Ferroxcube core type 266CT125, material 4C4. The primary winding is 2X10 turns and the secondary is 2X25 turns, both bifilar.

FIG. 4 shows a second embodiment of a connector 10' according to the invention. The outside dimensions and overall appearance of the connector 10' are generally similar to those of the connector 10 of FIG. 2. Two printed circuit boards or substrates 26'A and 26'B are, however, provided in housing 14' instead of the single board 26 in FIG. 2. Board 26'A extends at the top of the housing 14' parallel to the board 26'B which extends across the bottom of housing 14'. Board 26'B carries 24 pins P1'-P24' on its bottom outside surface 24' for connection directly to an outside circuit board or into a dual-in-line socket. The board 26'A is coupled by leads L' to female contact elements J2'-J8' and J20' which engage an outside plug connector at connection surface 20' of the connector 10'.

FIG. 5 shows a third embodiment of a connector 10" according to the invention. A single, flexible printed circuit board 26" is contained

within the connector housing 14". Conductors at one end of the board 26" are directly to the inside ends of female contact elements J2"-J8" and J20" which are arranged to engage an outside plug connector at contact surface 20". Conductors at an opposite end of the flexible board 26" are connected directly to the inside ends of insulation displacement type pins P1"-P24". A cap CP is constructed and arranged to clamp a flat insulated cable (not shown) over pointed ends of pins P1"-P24" so that the pins pierce through the cable insulation to electrically contact corresponding conductors of the flat cable.

It will be appreciated that the connector of the present invention provides a completely self-contained interface unit which eliminates all the inconveniences of designing and realizing a data interface such as the RS-232-C Standard. Particular components no longer need be selected to meet the requirements of the Standard, voltage level conversions are provided for, and time consuming test procedures and debugging are eliminated. The present connector thus saves engineering effort, development and production time as well as labor costs. Importantly, a considerable space savings is achieved in terminal equipment which would otherwise require means to accommodate a separate interface board.

In order to enable the man skilled in the art to practice this invention in some detail, a complete printed circuit layout is shown in FIG. 6. This layout conforms with the circuitry previously illustrated in schematic form in FIG. 3. The contact areas J2-J8 and J20, which correspond with the respective female contact elements so designated, will be seen in FIG. 6A. Likewise, contact areas P1-P12 (at the near longitudinal edge) and P13-P24 (at the far edge), which correspond with the respective male contact elements bearing the same designation. Capacitors C1-C9, oscillator Q1, and transformer TR1, are seen in phantom outline while resistors R1, R2 and R3 are represented by means of hatch lines. All the other principal elements are shown by means of rectangles suitably labeled. Appropriate wire bonding from the several integrated circuits U1-U6, as well as from the Graetz bridge G1, is shown in FIG. 6A connected to the conductors 30A on the printed circuit board.

It will be noted by the skilled worker that suitably correlated conductors 30B are provided on the lower surface of the printed circuit board 26 (FIG. 6B) so as to make the requisite interconnections among components. The dots 32 represent so-called "vias" between the upper and lower surfaces of board 26.

It will be appreciated that, for the sake of clarity, the depiction of a printed circuit layout for a circuit board 26 to be housed in

connector 10 of FIG. 2 is greatly enlarged (approximately 7 times).

While specific embodiments of the invention have been shown and described in detail to illustrate the application of the inventive principles, it will be understood that the invention may be embodied
5 otherwise without departing from such principles.

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CLAIMS:

1. An electrical connector for implementing a predetermined logical interface between a first data handling system wherein data signals are arranged in a first type of format, and a second data handling system wherein data signals are arranged in a second type of format, comprising:
- 5 a connector housing including a first wall part forming a first outside connection surface and a second wall part forming a second outside connection surface;
- a first set of terminals arranged to extend at least partly through said first wall part from inside said connector housing in a given configuration for engaging in electrical contact with corresponding terminals of first outside connection means associated with the first data handling system;
- 10 a second set of terminals arranged to extend at least partly through said second wall part from inside said connector housing in a given configuration for engaging in electrical contact with corresponding terminals of second outside connection means associated with the second data handling system; and
- 15 logic interface circuit means arranged within said connector housing and coupled between said first set of terminals and said second set of terminals for converting data signals transmitted to at least some of said first set of terminals from the first data handling system in the first type of format into corresponding data signals in the second type of format and providing said corresponding data signals in the second type of format to at least some of said second set of terminals for subsequent transmission to the second data handling system, and for converting data signals transmitted to at least some of said second set of terminals from the second data handling system in the second type of format into corresponding data signals in the first type of format and providing said corresponding data signals in the first type of format to at least some of said first set of terminals for subsequent transmission to the first data handling system.
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2. A connector according to claim 1, wherein said logic interface circuit means comprises means for converting data signals transmitted to at least some of said first set of terminals in a serial format into corresponding data signals in a parallel format and providing the corresponding parallel data signals to at least some of said second set of terminals, and for converting data signals transmitted to at least some of said second set of terminals in a parallel format into corresponding data signals in a serial format and providing the corresponding serial data
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signals to at least some of said first set of terminals.

5 3. A connector according to claim 1, wherein said logic interface circuit means comprises means for converting the voltage level of the data signals transmitted to at least some of said first set of terminals from a first voltage level into a second voltage level and providing the corresponding data signals at the second voltage level to at least some of said second set of terminals, and for converting the voltage level of the data signals transmitted to at least some of said second set of terminals from the second voltage level into the first voltage level and providing
10 the corresponding data signals at the first voltage level to at least some of said first set of terminals.

4. A connector according to claim 1, wherein said logic interface circuit means comprises a printed circuit substrate mounted within said connector housing.

15 5. A connector according to claim 1, wherein said logic interface circuit means comprises an integrated circuit mounted within said connector housing.

6. A connector according to claim 4, comprising an integrated circuit mounted on said printed circuit substrate.

20 7. A connector according to claim 1, wherein said first set of terminals comprises a number of female contact elements arranged to mate with corresponding male contact elements of the first outside connection means, said first wall part of said connector housing having a number of openings in said first connection surface within which openings said female
25 contact elements are fixedly supported, and said second set of terminals comprises a number of male contact elements arranged to mate with corresponding female contact elements of the second outside connection means, said second wall part of said connector housing having a number of openings in said second connection surface within which openings said male
30 contact elements are fixedly supported.

8. A connector according to claim 7, wherein said first connection surface extends generally within a first plane, and said second connection surface extends generally within a second plane.

35 9. A connector according to claim 8, wherein said second plane is perpendicular to said first plane.

10. A connector according to claim 8, wherein said second plane is parallel to said first plane.

40 11. A connector according to claim 8, wherein said male contact elements are arranged in two parallel rows for engaging corresponding openings formed in the female contact elements of the second outside

connection means.

12. A method of implementing a logical interface to enable communications between first and second data handling systems wherein data signals are arranged in a first type of format on the first system and in a second type of format in the second system, comprising the steps of:

providing a connector housing and supporting first and second sets of electrical contact elements on the connector housing;

exposing the first set of electrical contact elements on one portion of the outside surface of the connector housing and exposing the second set of electrical contact elements on another portion of the outside surface of the connector housing;

arranging the first set of electrical contact elements for connection with the first data handling system outside of the connector housing and arranging the second set of electrical contact elements for connection with the second data handling system outside of the connector housing;

containing electrical circuitry substantially within the connector housing and connecting the electrical circuitry with the first and the second sets of electrical contact elements by arranging conductors inside the connector housing;

converting by way of the electrical circuitry data signals transmitted to at least some of the second set of electrical contact elements in the second type of format from the second data handling system into corresponding data signals in the first type of format; and

providing the corresponding data signals in the first type of format from the electrical circuitry through the conductors inside the connector housing to at least some of the first set of electrical contact elements.

13. The method of claim 12, including arranging one of the first and second sets of electrical contact elements for connection to corresponding terminals on an outside printed circuit board associated with one of the first and the second data handling systems.

14. The method of claim 12, including arranging one of the first and second sets of electrical contact elements for connection to an outside cable connector associated with one of the first and the second data handling systems.

15. The method of claim 12, including arranging a selected one of the first and second sets of electrical contact elements in the form of insulation displacement elements, piercing an insulated cable associated with one of the data handling systems with the displacement elements and electrically contacting the displacement elements with corresponding conductors inside the cable.

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16. The method of claim 12, wherein one of said converting steps includes converting serial data into corresponding parallel data, and the other one of said converting steps includes converting parallel data into corresponding serial data.

5 17. The method of claim 12, including converting by way of the electrical circuitry the voltage level of the data signals transmitted to at least some of the first set of electrical contact elements from a first voltage level into a second voltage level and providing the corresponding data signals at the second voltage level to at least some of the second set
10 of electrical contact elements through the conductors inside the connector housing, and converting by way of the electrical circuitry the voltage level of the data signals transmitted to at least some of the second set of electrical contact elements from the second voltage level into the first voltage level and providing the corresponding data signals at the first
15 voltage level to at least some of the first set of electrical contact elements through the conductors inside the connector housing.

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AMENDED CLAIMS

[received by the International Bureau on 4 Mars 1987 (04.03.87);
original claims 1-17 replaced by new claims 1-23 (5 pages)]

1. A connector for implementing a direct predetermined logical interface between a first data handling system wherein data signals are arranged in a first type of format, and a second data handling system wherein data signals are arranged in a second type of format, comprising:

5 a connector housing including a first wall part forming a first outside connection surface and a second wall part forming a second outside connection surface;

10 a first set of terminals arranged to extend at least partly through said first wall part from inside said connector housing in a given configuration for engaging in contact with corresponding terminals of first outside connection means associated with the first data handling system, with said first set of terminals forming a logical interface member for matingly engaging a corresponding logical interface member formed by said corresponding terminals associated with the first data handling system;

15 a second set of terminals arranged to extend at least partly through said second wall part from inside said connector housing in a given configuration for engaging in contact with corresponding terminals of second outside connection means associated with the second data handling system, with said second set of terminals forming a logical interface member for matingly engaging a corresponding logical interface member formed by said corresponding terminals associated with the second data handling system; and

20 logic interface circuit means arranged within said connector housing and coupled between said first set of terminals and said second set of terminals for converting data signals transmitted to at least some of said first set of terminals from the first data handling system in the first type of format into corresponding data signals in the second type of format and providing said corresponding data signals in the second type of format to at least some of said second set of terminals for subsequent transmission to the second data handling system, and for converting data signals transmitted to at least some of said second set of terminals from the second data handling system in the second type of format into corresponding data signals in the first type of format and providing said corresponding data signals in the first type of format to at least some of said first set of terminals for subsequent transmission to the first data handling system.

2. A connector according to claim 1, wherein said logic interface

least some of said first set of terminals in a serial format into corresponding data signals in a parallel format and providing the corresponding parallel data signals to at least some of said second set of terminals, and for converting data signals transmitted to at least some of said second set of terminals in a parallel format into corresponding data signals in a serial format and providing the corresponding serial data signals to at least some of said first set of terminals.

3. A connector according to claim 1, wherein said logic interface circuit means comprises means for converting the voltage level of the data signals transmitted to at least some of said first set of terminals from a first voltage level into a second voltage level and providing the corresponding data signals at the second voltage level to at least some of said second set of terminals, and for converting the voltage level of the data signals transmitted to at least some of said second set of terminals from the second voltage level into the first voltage level and providing the corresponding data signals at the first voltage level to at least some of said first set of terminals.

4. A connector according to claim 1, wherein said logic interface circuit means comprises a printed circuit substrate mounted within said connector housing.

5. A connector according to claim 1, wherein said logic interface circuit means comprises an integrated circuit mounted within said connector housing.

6. A connector according to claim 4, comprising an integrated circuit mounted on said printed circuit substrate.

7. A connector according to claim 1, wherein said first set of terminals comprises a number of female contact elements arranged to mate with corresponding male contact elements of the first outside connection means, said first wall part of said connector housing having a number of openings in said first connection surface within which openings said female contact elements are fixedly supported, and said second set of terminals comprises a number of male contact elements arranged to mate with corresponding female contact elements of the second outside connection means, said second wall part of said connector housing having a number of openings in said second connection surface within which openings said male contact elements are fixedly supported.

8. A connector according to claim 7, wherein said first connection surface extends generally within a first plane, and said second connection

surface extends generally within a second plane.

9. A connector according to claim 8, wherein said second plane is circuit means comprises means for converting data signals transmitted to at perpendicular to said first plane.

5 10. A connector according to claim 8, wherein said second plane is parallel to said first plane.

11. A connector according to claim 8, wherein said male contact elements are arranged in two parallel rows for engaging corresponding openings formed in the female contact elements of the second outside
10 connection means.

12. A method of implementing a logical interface to enable communications between first and second data handling systems wherein data signals are arranged in a first type of format in the first system and in a second type of format in the second system, comprising the steps of:

15 providing a connector housing and supporting first and second sets of contact elements on the connector housing;

exposing the first set of contact elements on one portion of the outside surface of the connector housing and exposing the second set of contact elements on another portion of the outside surface of the connector
20 housing;

arranging the first set of contact elements for connection with the first data handling system outside of the connector housing and arranging the second set of contact elements for connection with the second data handling system outside of the connector housing, wherein each of said
25 first and second set of contact elements comprises a logical interface member, and wherein said interface members of said first and second set of contact elements are matingly connected to a corresponding logical interface member of said first and second data handling systems respectively;

30 containing electrical circuitry substantially within the connector housing and connecting the electrical circuitry with the first and second sets of contact elements by arranging conductors inside the connector housing;

35 converting by way of the electrical circuitry data signals transmitted to at least some of the second set of contact elements in the second type of format from the second data handling system into corresponding data signals in the first type of format; and

providing the corresponding data signals in the first type of format

from the electrical circuitry through the conductors inside the connector housing to at least some of the first set of contact elements.

5 13. The method of claim 12, including arranging one of the first and second sets of contact elements for connection to corresponding terminals on an outside printed circuit board associated with one of the first and the second data handling systems.

10 14. The method of claim 12, including arranging one of the first and second sets of contact elements for connection to an outside cable connector associated with one of the first and the second data handling systems.

15 15. The method of claim 12, including arranging a selected one of the first and second sets of contact elements in the form of insulation displacement elements, piercing an insulated cable associated with one of the data handling systems with the displacement elements and electrically contacting the displacement elements with corresponding conductors inside the cable.

20 16. The method of claim 12, wherein one of said converting steps includes converting serial data into corresponding parallel data, and the other one of said converting steps includes converting parallel data into corresponding serial data.

25 17. The method of claim 12, including converting by way of the electrical circuitry the voltage level of the data signals transmitted to at least some of the first set of contact elements from a first voltage level into a second voltage level and providing the corresponding data signals at the second voltage level to at least some of the second set of contact elements through the conductors inside the connector housing, and converting by way of the electrical circuitry the voltage level of the data signals transmitted to at least some of the second set of contact elements from the second voltage level into the first voltage level and providing
30 the corresponding data signals at the first voltage level to at least some of the first set of contact elements through the conductors inside the connector housing.

35 18. A connector according to claim 1 wherein said connector housing has structural dimensions of a height of no more than about 0.5 inches (12.70 mm), a depth of no more than about 1.2 inches (30.48 mm), and a width of no more than about 2.0 inches (50.80 mm).

19. A connector according to claim 1 wherein said connector housing comprises walls forming an enclosure member and wherein said logic

interface circuit means are completely enclosed within the walls of said connector housing.

5 20. The connector of claim 1 wherein said first set of terminals comprises a number of male contact elements adapted for direct integrated electrical mating with a printed circuit board member which handles data in said first type of format and wherein said housing is adapted to be physically supported by said printed circuit board.

10 21. The connector of claim 1 wherein said first set of terminals comprises a number of male contact pins adapted for direct integrated electrical mating with an insulated ribbon cable connector member, with said pins being adapted to pierce the insulation of said cable to electrically contact conductors of said cable whereby said electrical mating is effected, said cable connector member being adapted to be electrically connected to a printed circuit board which handles data in a first format and wherein said connector comprises means to physically
15 enclose a portion of said ribbon cable connector.

22. The connector of claim 19 wherein said logic interface circuit means further comprises a power supply, with said power supply being contained within said walls of said connector housing.

20 23. A "D-type" 25 pin RS-232-C connector having a male connection interface adapted for direct integrated electrical mating with a printed circuit board member which handles data in a parallel format, said connector further having a female connection interface for mating connection with an external male connection interface member from a device
25 which handles data in a serial format, characterized in that means for converting data from said parallel format to said serial format and means for converting data from said serial format to said parallel format are electrically positioned between said male connection interface and said female connection interface within said connector, and wherein said
30 connector is adapted to be physically supported by said printed circuit board.

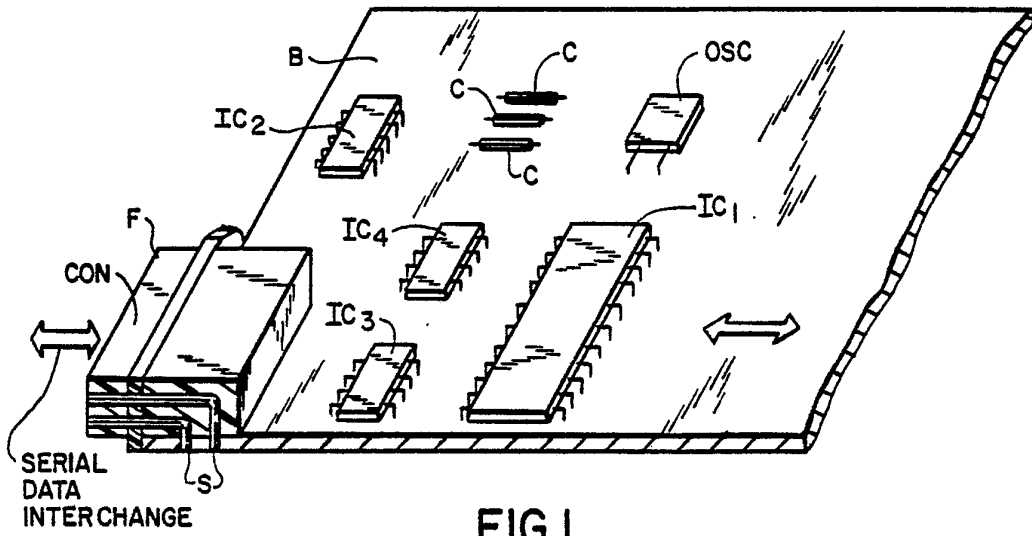
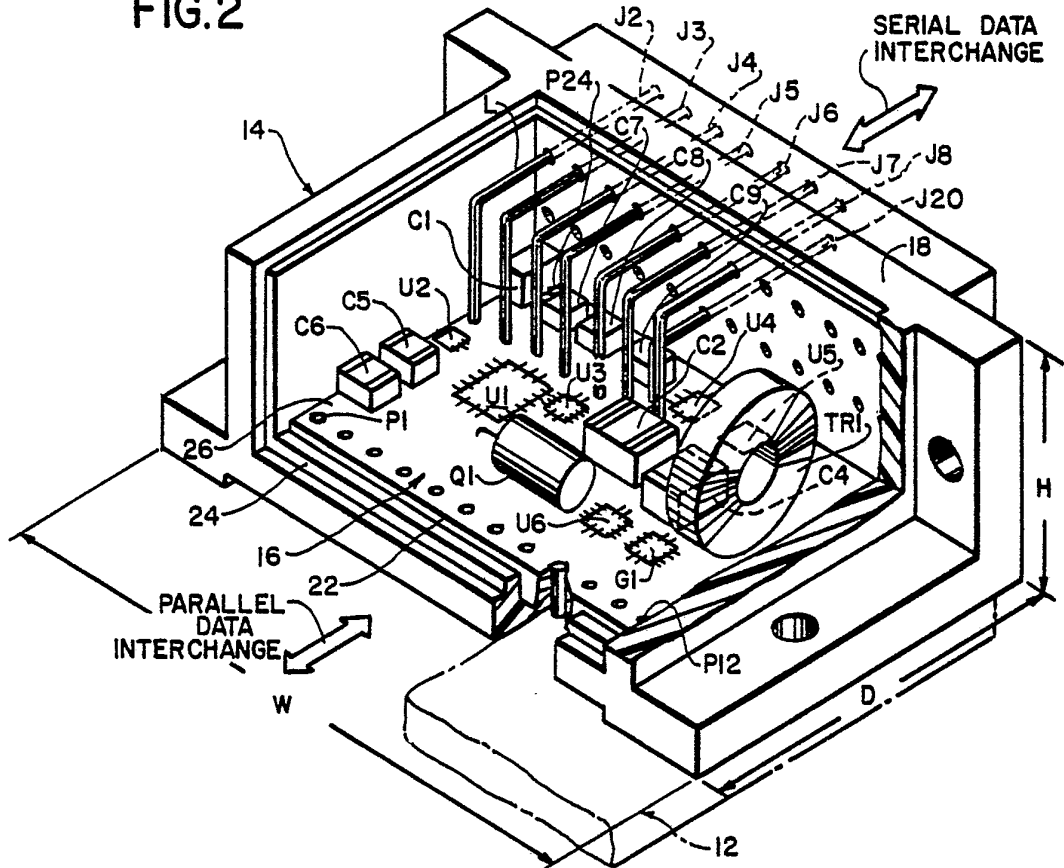


FIG. 1
PRIOR ART

FIG. 2



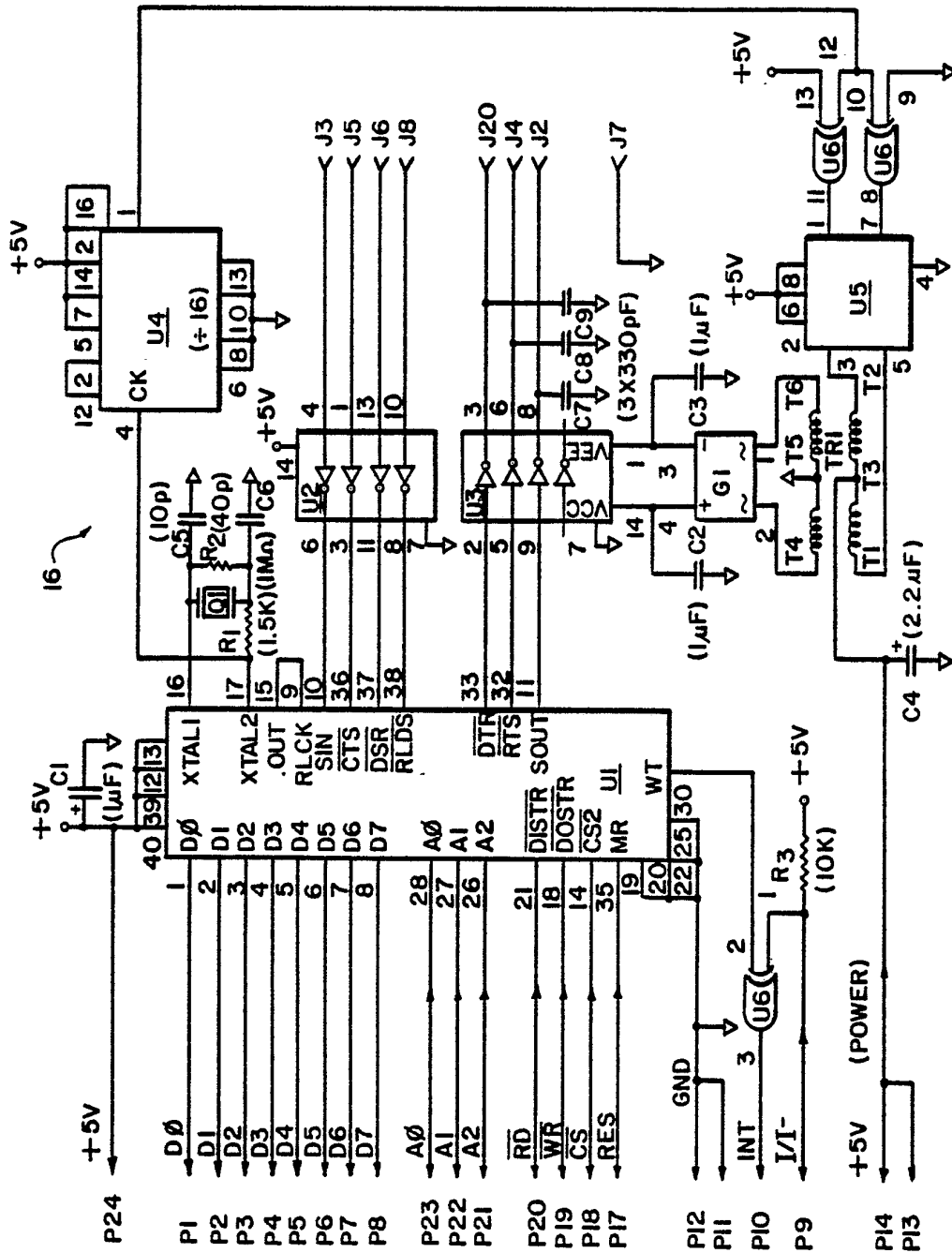


FIG.3

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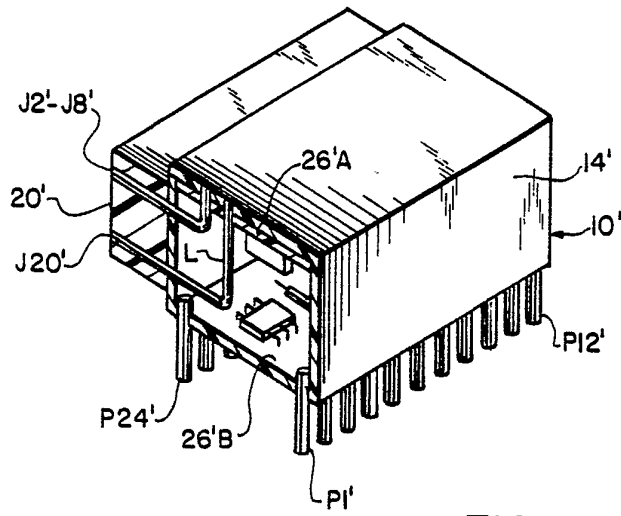


FIG. 4

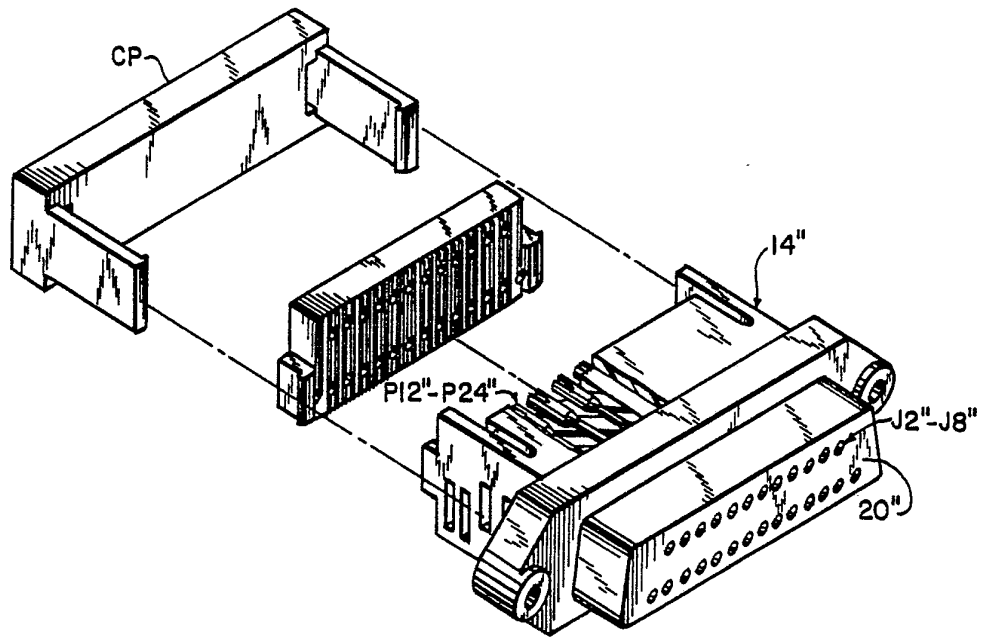


FIG. 5

FIG.6A

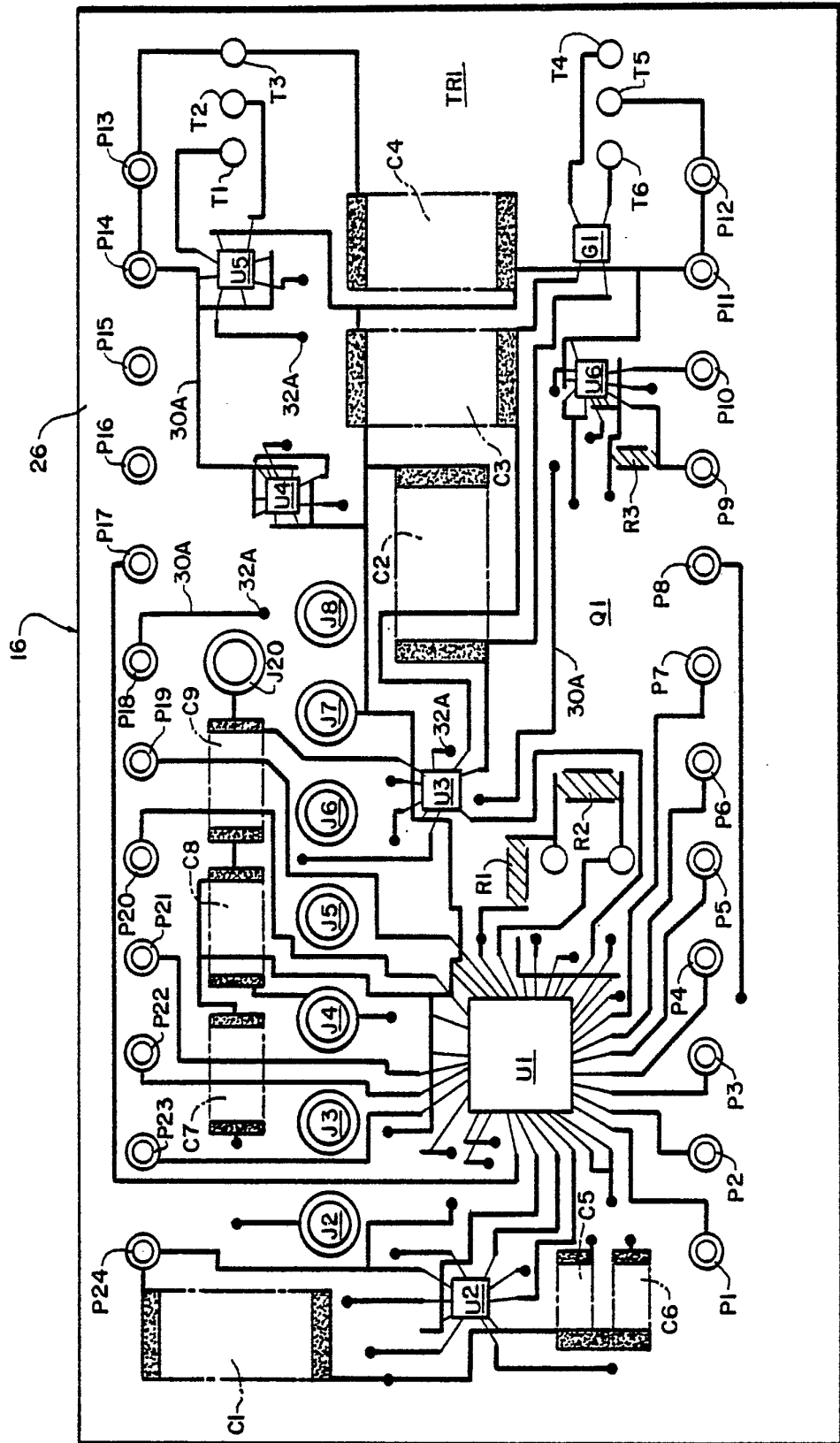
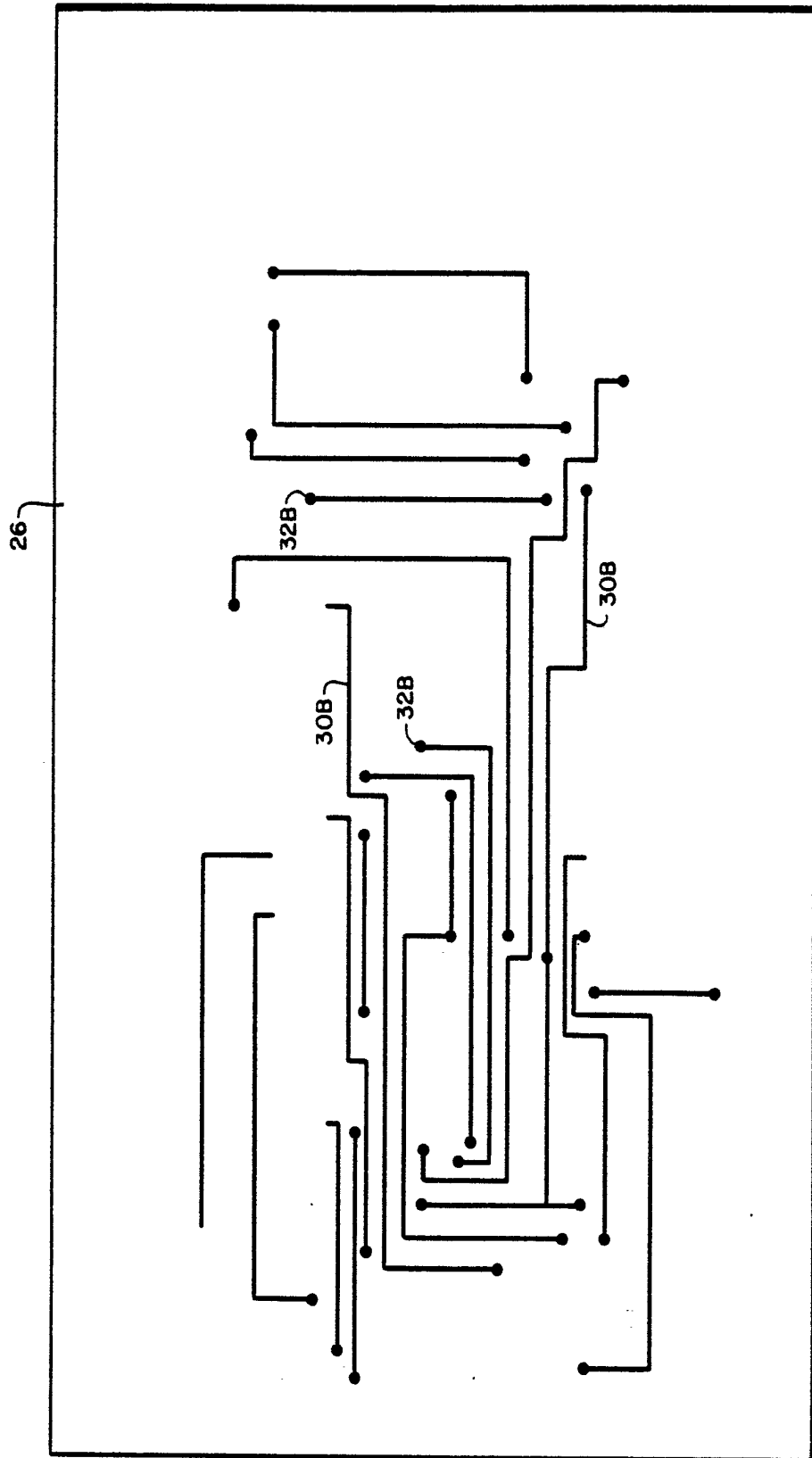


FIG. 6B



INTERNATIONAL SEARCH REPORT

PCT/US85/02107

International Application No

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ³		
According to International Patent Classification (IPC) or to both National Classification and IPC		
INT. CL. H01R 13/50; H05K 7/00;		
US. CL. 339/176; 361/392; 340/347DD		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁴		
Classification System	Classification Symbols	
U.S.	340/347DD 339/17R, 17C, 17F, 17M, 17LC, 176R, 176MP, 176M 361/392-395, 412, 415	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁵		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴		
Category *	Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸
X	US, A, 4,027,941 Published 07 June 1977, NAROZNY	15
X	US, A, 4,124,888 Published 07 November 1978, WASHBURN.	1-4, 16, 17
X	US, A, 4,217,624 Published 12 August 1980, TUCK.	1-4, 16 17
A	US, A, 4,487,464 Published 11 December 1984, KIRSCHENBAUM.	-----
<p>* Special categories of cited documents: ¹⁵</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search ²	Date of Mailing of this International Search Report ³	
08 January 1986	22 JAN 1986	
International Searching Authority ¹	Signature of Authorized Officer ²⁰	
ISA/US	Vit W. Miska <i>Vit W. Miska</i>	