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(54) Title: PHOTOVOLTAIC SYSTEM POWER TRACKING METHOD

(57) Abstract: A photovoltaic system including a photovoltaic cell, and an electronic module connected to the photovoltaic cell. The electronic module is adapted to produce at least one control signal indicative of electrical power being generated by the photovoltaic cells. A tracking controller is adapted to receive the control signal(s) and based on the control signal(s), the controller is adapted to control a tracking motor for adjusting the system so that electrical power generated by the photovoltaic cells is increased. The photovoltaic system may include an optical element, adapted for concentrating solar light onto the photovoltaic cells. The electronic module preferably performs direct current (DC) to direct current (DC) power conversion and maximum power point tracking by electrical power, current, or voltage at either their inputs or their outputs. Alternatively, the tracking controller is configured to also perform maximum power point tracking by increasing to a local maximum electrical power by varying at least one of (i) current or voltage output from the photovoltaic cell or (ii) current or voltage output from the electronic module.



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PHOTOVOLTAIC SYSTEM POWER TRACKING METHOD

CROSS REFERENCE TO RELATED APPLICATIONS

The present invention benefits from US application 60/992,589 filed 5-Dec-2007 and hereby incorporated by reference in its entirety.

5 TECHNICAL FIELD

The present invention relates to current sensing in electronic circuitry and specifically to a device and method for current sensing in a switching power converter.

DESCRIPTION OF RELATED ART

Reference is made to Figure 1 which illustrates the conventional current sensing circuit
10 of US 2008/0246460. US 2008/0246460 illustrates a conventional current sensing circuit
202 coupled to switching field-effect-transistors (FET) high side FET **210**, and low side
FET **206** within a switching regulator. The current-sensing-circuitry **202** is configured to
bypass a small sense current **208** from the conducting current **209** of the switching-FET
according to a sense ratio. The conducting current for the switching regulator is
15 controlled by a control signal. Current sensing circuit **202** includes a sensing FET **204**
which is coupled in parallel with low-side FET **206**. Control logic **306** provides control
signals to low-side FET **206**, high side FET **210** and current sensing FET **204**. More
specifically, the drains and gates of both sensing FET **204** and low-side FET **206** are tied
together. Hence, the same control signal that controls low-side FET **206** also controls
20 sensing FET **204**. The source of low-side FET **206** is connected to the ground while the
source of sensing FET **204** is used as the output node. Although the sources of the two
FETs are not tied together, it is desirable that they have the same voltage. US
2008/0246460 describes a technique that sets the source voltage of sensing FET **204** to
be the same as the source voltage of low-side FET **206** below. Sensing FET **204**
25 conducts a sense current **208** , which is a small fraction of a main switching regulator
current **209** conducted by low-side FET **206** . The ratio between main switching
regulator current **209** and sense current **208** is proportionate to a predetermined large
number, *e.g.* greater than 500.

A characteristic of conventional current sensing circuit 202 is that sense current 208 is supplied by main current 209 of the switched power circuit. Similarly, another well established technique to sense current is to place a small sense resistor in series with the power train (for example on the ground rail) and measure the voltage drop across the sense resistor and thus estimate the current. The current sense resistor method draws current from the
5 switched power circuit.

Thus there is a need for and it would be advantageous to have a current sensing device and method which does not draw current from the switched power circuit.

BRIEF SUMMARY

10 According to a feature of the present invention there is provided a device having a switch with a voltage applied across the switch. A current sensing circuit is connected to one terminal of the switch. The current sensing circuit receives power independently of the voltage applied across the switch. The power supply shares the other terminal of the switch with the current sensing circuit. The switch is adapted for opening and
15 closing. When the switch closes, the current sensing circuit senses current through the switch and when said switch is open the high voltage of the switch is blocked from the current sensing circuit. The sense current is preferably caused to flow from the current sensing circuit to the other terminal when the switch is closed. The flow of the sense current produces a voltage which is compared differentially to another voltage
20 referenced by the other terminal. The current sensing circuit may include an operational amplifier which outputs a voltage sense signal which is proportional to the current flowing through the switch. The current sensing circuit may include a switched power converter which includes the switch. The current sensing circuit senses the current while the voltage output of the switched power converter is switched to a common rail. The
25 current sensing circuit draws power independently and not from the switched power converter. The switch is preferably a MOSFET, but may be one of many other switch types – such as, by way of example, insulated-gate bipolar transistor (IGBT), bipolar junction transistor(BJT) or other transistors or similar devices. The switched power converter may be a buck converter or a boost converter or a buck and boost converter.
30 Additionally an inductor is connected to the terminal of the switch and the current sensing circuit senses current through the inductor and does not integrate voltage across the inductor.

According to a feature of the present invention there is provided a method in a device including a switch. A voltage is applied across the switch. A current sensing circuit is connected to one terminal of the switch. The current sensing circuit receives power
5 independently of the voltage. the power derived independently, shares the other terminal of the switch, with the current sensing circuit. The switch is adapted for opening and closing. Upon closing the switch, the current sensing circuit senses the current through the switch. Upon opening the switch, the high voltage of the switch is blocked from the current sensing circuit.

10 According to a feature of the present invention there is provided a circuit for sensing current flowing through an inductor. The circuit includes: a cathode of a first diode connected to a first side of the inductor. A cathode of a second diode connected to a second side of the inductor. A first node connecting the anode of the first diode with the anode of the second diode. A first voltage divider with a first and second resistor
15 connected between the first node and a power supply. The connection between the first and second resistor forms a second node. A second voltage divider is formed by a third and fourth resistor. A third diode is disposed between the power supply and a ground. The connection between the third and fourth resistor forms a third node. A capacitor is disposed between the ground and the third node. An operational amplifier with a non-
20 inverting input is connected to the second node and an inverting input is connected to the third node. A fifth resistor is connected between the output of the amplifier and the third node. Power is supplied to the operational amplifier and significant current is not drawn from the inductor.

The foregoing and/ or other aspects will become apparent from the following detailed
25 description when considered in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is herein described, by way of example only, with reference to the accompanying drawings, wherein:

Fig. 1 is a conventional circuit for sensing the output current of a switching regulator.

Fig 1a is block diagram of high voltage switch connected to a current sensing circuit according to an embodiment of the present invention.

Fig. 1b is a circuit diagram of the current sensing circuit with a single input according to an embodiment of the present invention.

5 Fig 1c illustrates a method according to a feature of the present invention.

Fig. 2 is a block diagram of a buck and boost converter connected to a current sensing circuit in an embodiment of the present invention.

Fig. 3 is a block diagram showing circuit details of the buck and boost converter according to an embodiment of the present invention.

10 Fig. 3a is graph showing the variation of current in the inductor of a buck and boost circuit according to an embodiment of the present invention.

Fig. 4 is circuit diagram of the current sensing circuit according to an embodiment of the present invention; and

Fig. 5 illustrates a method according to a feature of the present invention.

15

DETAILED DESCRIPTION

Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below to explain

20 the present invention by referring to the figures.

Reference is now made to Figure 1a which is block diagram of high voltage switch G_X connected to a current sensing circuit **26a**, according to an embodiment of the present invention. High voltage switch G_X is connected across a high voltage V_X with respect to ground. A current sensing circuit **26a** is connected to the high voltage side (VA) of

25 switch G_X . In an embodiment of the present invention, switch G_X is a MOSFET.

Alternatively switch G_X can, in different embodiments of the invention, be a silicon controlled rectifier (SCR), insulated gate bipolar junction transistor (IGBT), bipolar junction transistor (BJT), field effect transistor (FET), junction field effect transistor (JFET), switching diode, mechanically operated single pole double pole switch (SPDT),

30 SPDT electrical relay, SPDT reed relay, SPDT solid state relay, insulated gate field effect transistor (IGFET), DIAC, and TRIAC.

Some embodiments of the present invention are applicable for use in a "switched power converter. The terms "switched power converter" and "switching power converter" are used herein interchangeably and refers to a switching regulator as used for example in a switched-mode power supply (SMPS). While a linear regulator maintains the desired output voltage by dissipating excess power in a pass power transistor, the switched-mode power converter rapidly switches a power transistor between saturation (full on) and cutoff (completely off) with a variable duty cycle whose average is the desired output voltage. The resulting rectangular waveform is typically low-pass filtered with an inductor and capacitor. The "switched power converter" as used herein may perform any type of power conversion or inversion including: alternating current (AC) to direct current (DC) or rectifier operation: DC in to DC out: voltage converter, or current converter, or DC to DC converter; AC in to AC out: frequency changer, cycloconverter, and/or DC in, AC out: inverter.

Reference is now also made to Figure 1b which is a circuit diagram of the current sensing circuit **26a** with a single input (VA) according to an embodiment of the present invention. Current sensing circuit **26a** has a power supply VCC **42** which is separate from the high voltage V_X across switch G_X as shown in Figure 1a. Amplifier **40** in an embodiment of the present invention is an operational amplifier (for example OPA2359, Texas Instruments, Dallas, Texas). It may be noted that other methods for measuring the voltage, such as an Analog to Digital converter (ADC), may also be used. The use of an operational amplifier for this purpose is given here only by way of example. A DC supply VCC **42** and a ground **44** is connected to the power supply inputs of amplifier **40**. A voltage divider chain (VDC) **402** is connected between one end of supply VCC and ground **44**. VDC **402** has a resistor RA1 with one end connected to supply VCC **42** and the other end connected in series with resistor RB1. The other end of resistor RB1 is connected in series to the anode of diode D_3 . The cathode of diode D_3 is connected to ground **44**. The point in VDC **402** where resistors RA1 and RB1 are connected is the non-inverting input to amplifier **40**. A capacitor C is connected in parallel across RB1 and D_3 and performs function of decoupling the non-inverting input of amplifier **40** and protecting circuit **26a** from high voltages on the ground rail. A second VDC **400** is connected between one end of supply VCC and the connection across inductor **28** shown in Figure 3. VDC **400** has a resistor RA2 with one end connected to supply VCC **42** and the other end connected in series with resistor RB2. The other end of resistor RB2 is

connected in to the anode of diode D_1 . The point in VDC **400** connecting resistors RA_2 and RB_2 is attached to the inverting input of amplifier **40**. The cathode of D_1 is connected to the high voltage side of switch G_X as shown in Figure 1a. A feedback resistor RC is connected between the output of amplifier **40** (V_{SENSE}) and the inverting

5 input of amplifier **40**. Resistor RC is used to set the gain of amplifier **40**. In an embodiment of the present invention, diodes D_1 and D_3 (for example diode MMSD4148, Fairchild Semiconductor, ME U.S.A.) have a typical maximum repetitive reverse voltage of 100 volts which correspond with the typical voltage values V_X found across MOSFET G_X . Diodes D_1 and D_3 are also preferably matched diodes.

10 Referring back to Figure 1a when MOSFET G_X is closed V_A is brought low *i.e.* near in value to the zero volts of the ground connection of MOSFET G_X . Current sensing circuit **26a** senses the current I_X which flows through MOSFET G_X . With voltage V_A low, diode D_1 is forward biased and a measure of the current I_X flowing through MOSFET G_X is given by Eq.1a when $RA_1 = RA_2 = RA$ and $RB_1 = RB_2 = RB$:

$$15 \quad V_{SENSE} = \left[\frac{V_{CC} \cdot RB + VD_3 \cdot RA}{RA + RB} \cdot \frac{RC}{RB} (VD_3 - VD_1 - V_A) \right] \quad \text{Eq. 1a}$$

where VD_3 is the voltage of diode D_3 . Diode D_3 is used to match the voltage drop of D_1 so that the amplifier **40** won't reach it's saturation point when switch G_X is conducting. the current measurement will be accurate when MOSFET G_X is conducting. Diode D_1 in current sensing circuit **26a** is in reverse bias when MOSFET G_X is off and protects

20 current sensing circuit **26a** from high voltage V_A (typically 100 volts).

Reference is now made to Figure 1c which illustrates a method according to a feature of the present invention. In decision box **600**, it is determined whether either switch G_X is open or closed, if MOSFET G_X is open the voltage V_X is blocked by current sensing circuit **26a** (step **604**), if MOSFET G_X is closed the voltage V_X is sensed by current

25 sensing circuit **26a** (step **602**) as V_{SENSE} proportional to the current I_X flows through MOSFET G_X .

Reference is now made to Figure 2 which illustrates schematically a buck boost converter **24** and current sensing circuit **26** according to an embodiment of the present

invention. Buck and boost converter **24** has a buck circuit **20** which receives an input voltage V_{IN} to buck and boost converter **24**. The output voltage of buck circuit **20** V_A is with respect to common rail **29**. An inductor **28** and common rail **29** connect the output of buck circuit **20** to the input of boost circuit **22**. The input voltage V_B of boost circuit **22** is with respect to common rail **29**. The output of boost circuit **22** is the output voltage V_{OUT} of buck and boost converter **24**. Current sensing circuit **26** is connected across inductor **28** and V_{SENSE} is the output of current sensing circuit **26**.

Reference is now made to Figure 3 which is a block diagram showing circuit details of buck and boost converter **24** according to an embodiment of the present invention. Buck and boost converter **24** has buck circuit **20** which receives the input voltage V_{IN} to buck and boost converter **24**. Buck circuit **20** has a low side buck MOSFET G_A , shunt connected across the output of buck circuit **20** and a high side buck MOSFET G_C , connected in series between the output and input of buck circuit **20**. A capacitor C_1 is shunt connected across the input of buck circuit **20**. The output voltage of buck circuit **20** V_A is with respect to common rail **29**. Inductor **28** and common rail **29** connects the output of buck circuit **20** to the input of boost circuit **22**. Boost circuit **22** has a low side boost MOSFET G_B , shunt connected across the input of boost circuit **22** and a high side boost MOSFET G_D , connected in series between the output and input of boost circuit **22**. A capacitor C_2 is shunt connected across the output of boost circuit **22**. Current sensing circuit **26** is connected across inductor **28** and V_{SENSE} is the output of current sensing circuit **26**.

Reference is now also made to Figure 3a, a graph showing the variation of current I_L in inductor **28** according to an embodiment of the present invention. The working operation of buck and boost converter **24** is in two time phases T1 and T2. Referring back to Figure 3, in time phase T2 buck and boost converter **24** operates with MOSFETS G_A off, G_B on, G_D off and G_C on. During phase T1 the output voltage of buck circuit **20** V_A is approximately the input voltage V_{IN} of buck and boost converter **24** and the input voltage of boost circuit **22** V_B is brought low *i.e.* near in value to the zero volts of common rail **29**. In time phase T1, buck and boost converter **24** operates with MOSFETS G_A on, G_B off, G_D on and G_C off. During phase T2 the output voltage of buck circuit **20** V_A is brought low *i.e.* near in value to the zero volts of common rail **29** and the input voltage of boost circuit **22** V_B is initially approximately equal to the output voltage V_{OUT} of buck

and boost converter **24**. During phase T1, current sensing circuit **26** is sensing the current I_S which flows through MOSFET G_A .

Reference is now also made to Figure 4, which is a circuit diagram of current sensing circuit **26** according to an embodiment of the present invention. Amplifier **40** in an embodiment of the present invention is an operational amplifier (for example OPA2359, Texas Instruments, Dallas, Texas). It may be noted that other methods for measuring the voltage, such as an Analog to Digital converter (ADC), may also be used. The use of an Op-Amp for this purpose is given here only by way of example. A DC supply V_{CC} **42** and a ground **44** is connected to the power supply inputs of amplifier **40**. A voltage divider chain (VDC) **402** is connected between one end of supply V_{CC} and ground **44**. VDC **402** has a resistor RA1 with one end connected to supply V_{CC} **42** and the other end connected in series with resistor RB1. The other end of resistor RB1 is connected in series to the anode of diode D_3 . The cathode of diode D_3 is connected to ground **44**. The point in VDC **402** where resistors RA1 and RB1 are connected is the non-inverting input to amplifier **40**. A capacitor C is connected in parallel across RB1 and D_3 and performs function of decoupling the non-inverting input of amplifier **40**. A second VDC **400** is connected between one end of supply V_{CC} and the connection across inductor **28** shown in Figure 3. VDC **400** has a resistor RA2 with one end connected to supply V_{CC} **42** and the other end connected in series with resistor RB2. The other end of resistor RB2 is connected in to the anodes of diodes D_1 and D_2 . The point in VDC **400** connecting resistors RA2 and RB2 is attached to the inverting input of amplifier **40**. The cathodes of D_1 and D_2 are connected across inductor **28** as shown in Figure 3. A feedback resistor RC is connected between the output of amplifier **40** (V_{SENSE}) and the inverting input of amplifier **40**. Resistor RC is used to set the gain of amplifier **40**. In an embodiment of the present invention, diodes D_1 , D_2 and D_3 (for example diode MMSD4148, Fairchild Semiconductor, ME U.S.A.) have a typical maximum repetitive reverse voltage of 100 volts which correspond with typical voltages VA and VB found in buck and boost converter **24**.

Referring back to Figure 3a, during phase T1 the output voltage of buck circuit **20** VA is brought low *i.e.* near in value to the zero volts of common rail **29**, and the input voltage of boost circuit **22** VB is initially approximately equal to the output voltage V_{OUT} of buck and boost converter **24**. During phase T1, current sensing circuit **26** senses the current I_S

which flows through MOSFET G_A . Diode D_2 in current sensing circuit **26** is in reverse bias and protects current sensing circuit **26** from high voltage V_B which is typically 100 volts. During phase T1 with voltage V_A low, diode D_1 is forward biased and a measure of the current I_S flowing through MOSFET G_A is given by Eq.1 when $RA1 = RA2 = RA$ and $RB1 = RB2 = RB$:

$$V_{SENSE} = \left[\frac{V_{CC} RB}{RA + RB} + VD_3 - I_S R_{ds} \frac{RC}{RB} \right] \quad \text{Eq. 1}$$

where R_{ds} is the resistance between drain and source of MOSFET G_A and VD_3 is the voltage of diode D_3 . Diode D_3 is used to match the voltage drop across D_1 so that the current measurement will be accurate when MOSFET G_A is conducting. During phase T2, current sensing circuit **26** is sensing the current I_S which flows through MOSFET G_B . Diode D_1 in current sensing circuit **26** is in reverse bias and is protecting current sensing circuit **26** from high voltage V_A which is typically 100 volts. During phase T2 with voltage V_B low, diode D_2 is forward biased and a measure of the current I_S flowing through MOSFET G_B is given by Eq.2 when $RA1 = RA2 = RA$ and $RB1 = RB2 = RB$.

$$V_{SENSE} = \left[\frac{V_{CC} RB}{RA + RB} + VD_3 - I_S R_{ds} \frac{RC}{RB} \right] \quad \text{Eq. 2}$$

where R_{ds} is the resistance between drain and source of MOSFET G_B and VD_3 is the voltage of diode D_3 . Diode D_3 is used to match the voltage drop across D_2 so that the current measurement will be accurate when MOSFET G_B is conducting.

Reference is now made to Figure 5 which illustrates a method according to a feature of the present invention. In decision box **500**, it is determined whether either of high voltages V_A or V_B are low (i.e. switched to common rail **29**) and if so, the voltage differential between V_A and V_B is sensed (step **502**) as V_{SENSE} proportional to the current I_S flowing through MOSFETS G_A or G_B .

The articles "a", "an", as used hereinafter are intended to mean and be equivalent to "one or more" or "at least one", For instance, "a switch e " means "one or more switches".

While the invention has been described with respect to a limited number of embodiments, it will be appreciated that many variations, modifications and other applications of the invention may be made.

CLAIMS

1. A photovoltaic system comprising:
 - a photovoltaic cell;
 - an electronic module adapted for connection to said photovoltaic cell, said electronic module configured to produce a control signal indicative of electrical power generated by said photovoltaic cell;
 - a tracking controller adapted to receive said control signal and based on said control signal, said tracking controller is configured to control a tracking motor for adjusting the system so that electrical power generated by said photovoltaic cell is increased.
2. The photovoltaic system according to claim 1, further comprising an optical element adapted for concentrating solar light intensity onto said photovoltaic cell.
3. The photovoltaic system according to claim 1, wherein said electronic module performs direct current (DC) to direct current (DC) power conversion.
4. The photovoltaic system according to claim 1, wherein said electronic module performs maximum power point tracking by increasing to a local maximum electrical power by varying at least one of (i) current or voltage output from said photovoltaic cell or (ii) current or voltage output from said electronic module.
5. The photovoltaic system according to claim 1, wherein said tracking controller is further configured to perform maximum power point tracking by increasing to a local maximum electrical power by varying at least one of (i) current or voltage output from said photovoltaic cell or (ii) current or voltage output from said electronic module.
6. The photovoltaic system according to claim 1, whereby current from said photovoltaic cell varies due to at least one factor other than variations of said solar light intensity, said at least one factor selected from the group consisting of: distribution of

said solar intensity over said photovoltaic cell, varying temperature of said photovoltaic cell, and varying electrical impedance of a load receiving said electrical power.

7. A method for controlling a photovoltaic system including a photovoltaic cell; an electronic module connected respectively to the photovoltaic cell; the method comprising the steps of:

producing a control signal indicative of electrical power being generated by the photovoltaic cell,

receiving said a control signal and based on said a control signal, controlling a tracking motor for adjusting the system thereby increasing electrical power generated by said the photovoltaic cell.

8. The method according to claim 7, further comprising the step of:

performing maximum power point power tracking by maximizing electrical power individually from said photovoltaic cells by varying at least one of (i) current or voltage output from the photovoltaic cell or (ii) current or voltage output from the electronic module.

9. The method according to claim 8, wherein said maximum power point tracking is performed independently from said controlling said tracking motor by performing said maximum power point tracking and said controlling in selectably either different time domains or different frequency domains.

10. The method according to claim 7, wherein said adjusting includes orienting at least one optical component within the system in at least one of two angles.

11. The method according to claim 7, wherein said adjusting includes varying at least one distance of at least one optical component within the system.

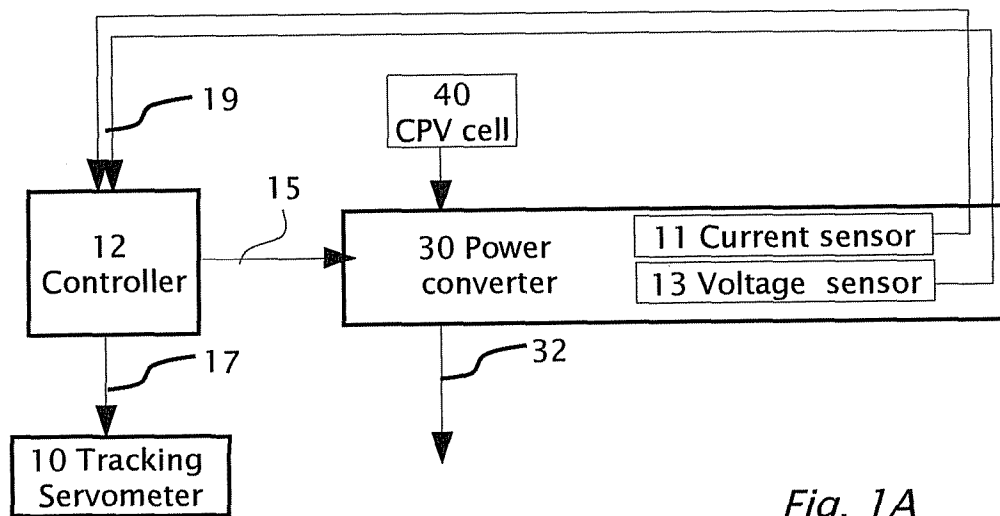
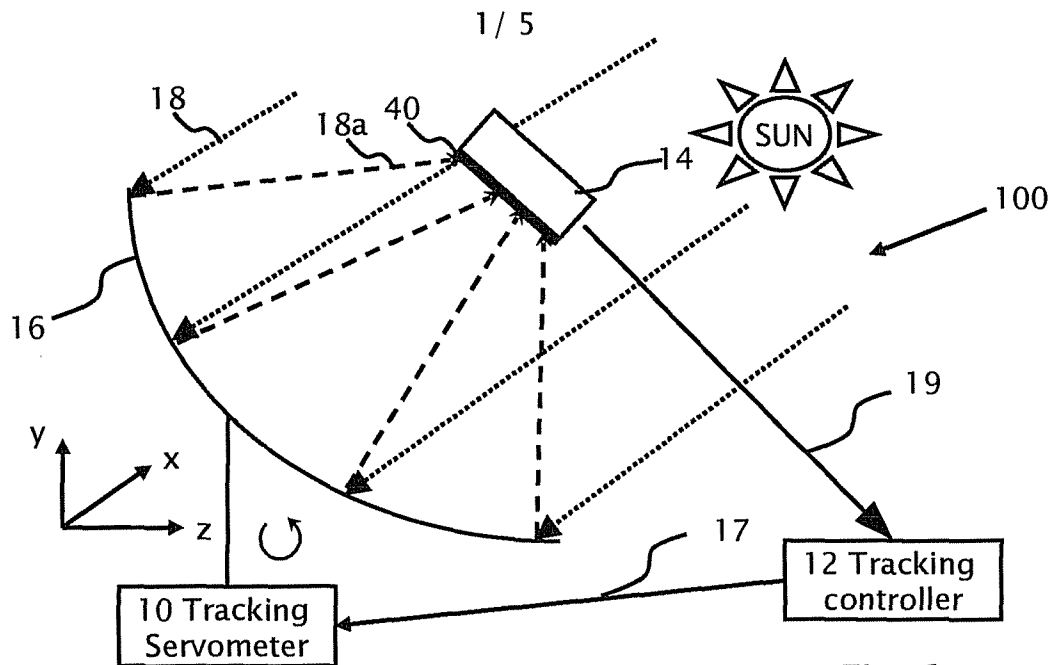
12. The method according to claim 11, wherein said adjusting includes defocusing the system.

13. The method according to claim 11, wherein said adjusting includes changing a distance of a light diffuser in the system.

14. The method according to claim 7, wherein the system includes a plurality of photovoltaic cells connected to respective electronic modules with control signals indicative of electrical power being generated by the photovoltaic cells, further comprising the step of, prior to said producing at least one control signal:

selecting a portion of said photovoltaic cells and corresponding control signals for use in said controlling.

15. The method according to claim 14, further comprising the step of:
reselecting periodically different photovoltaic cells thereby maximizing power on said different photovoltaic cell and thereby increasing reliability of the system.



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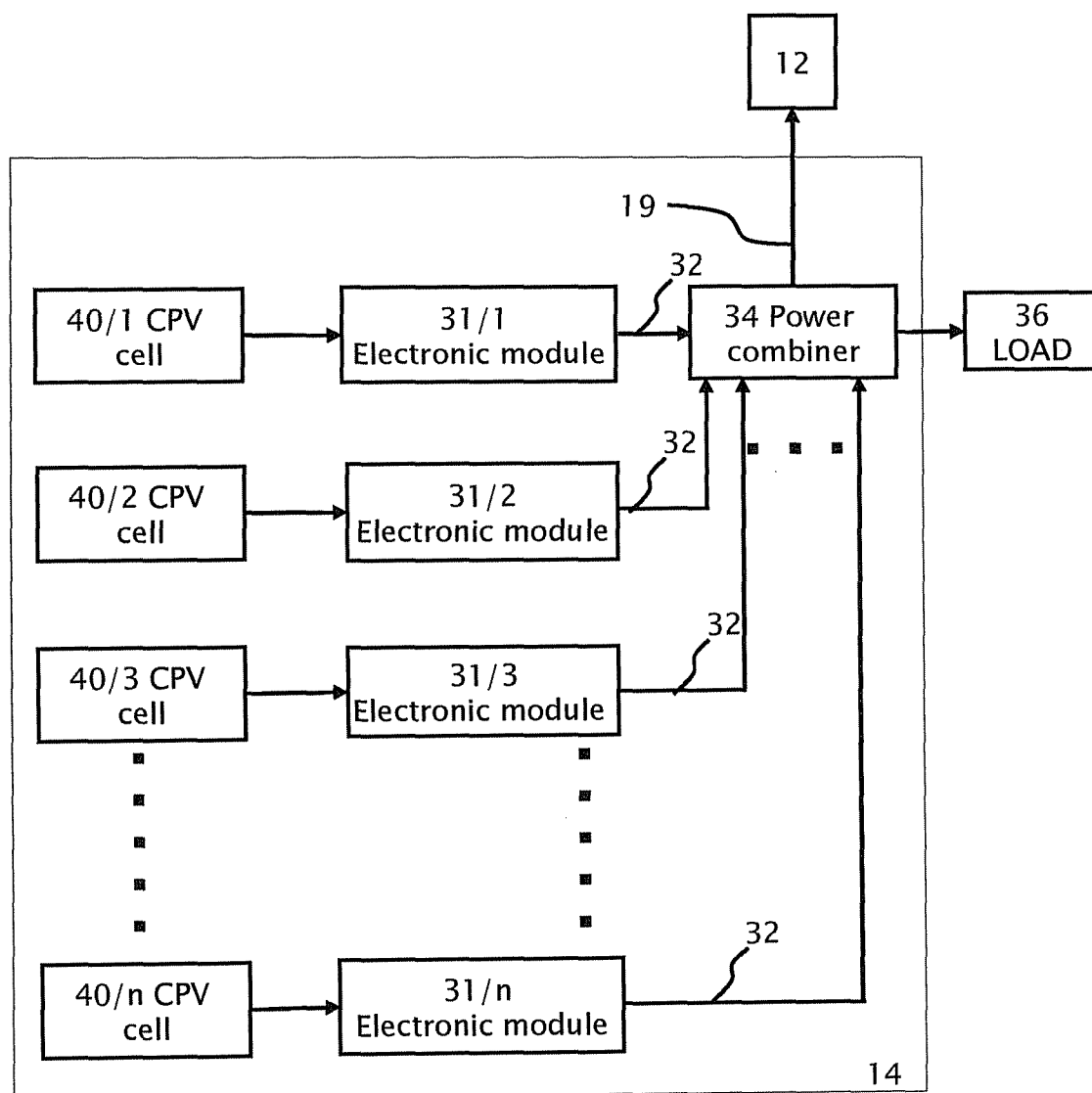


Fig. 2

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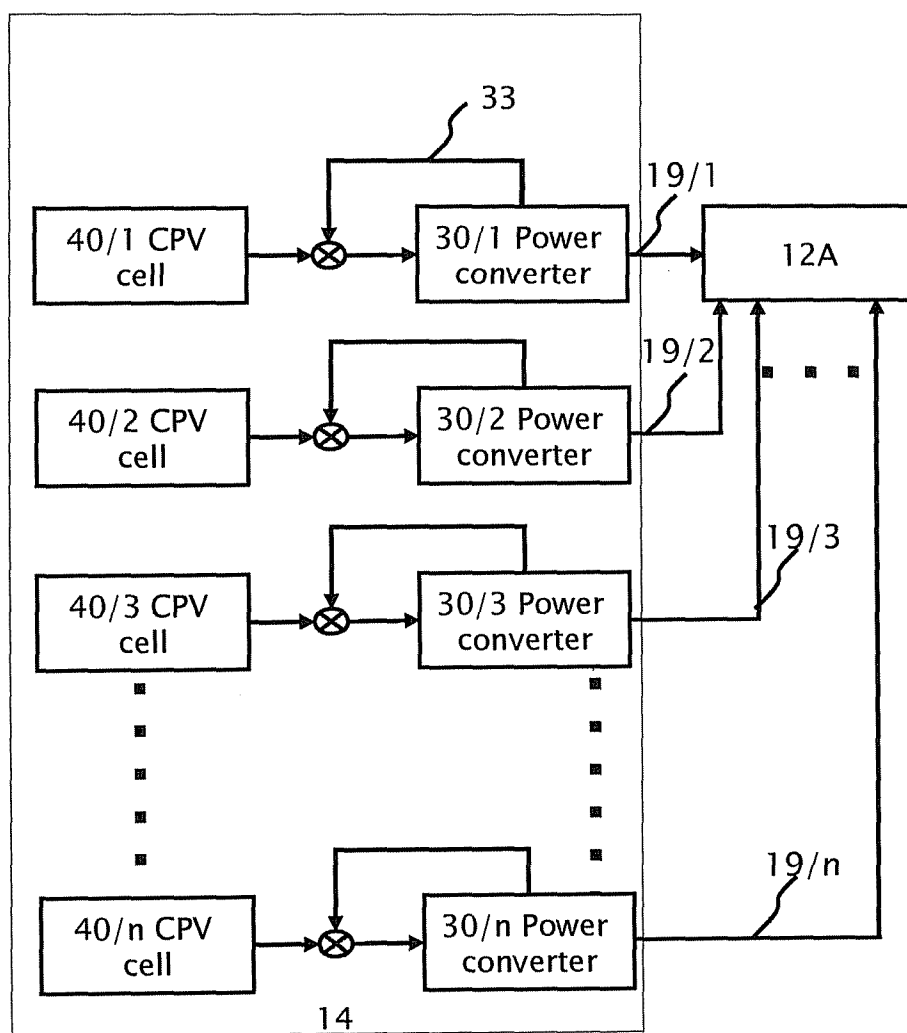


Fig. 3

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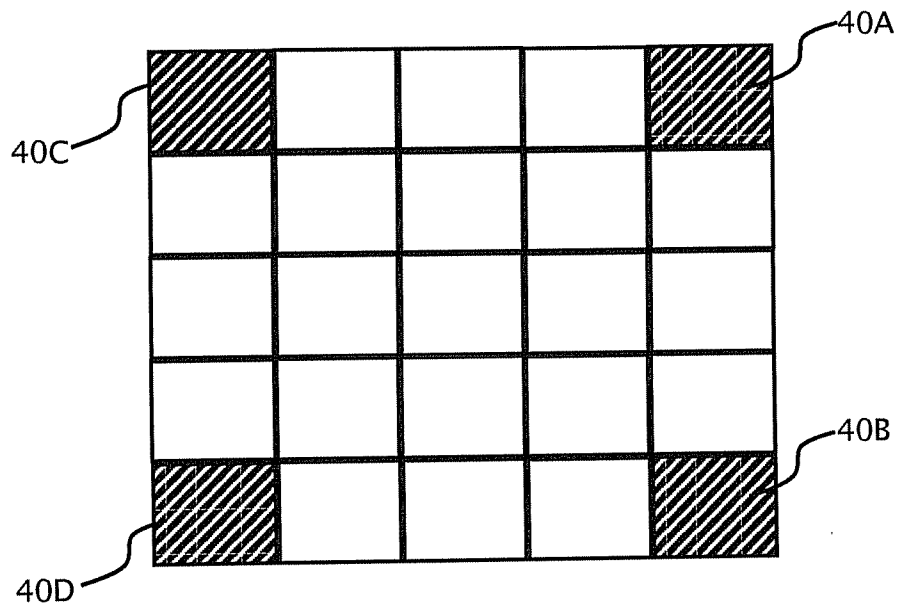


Fig. 4

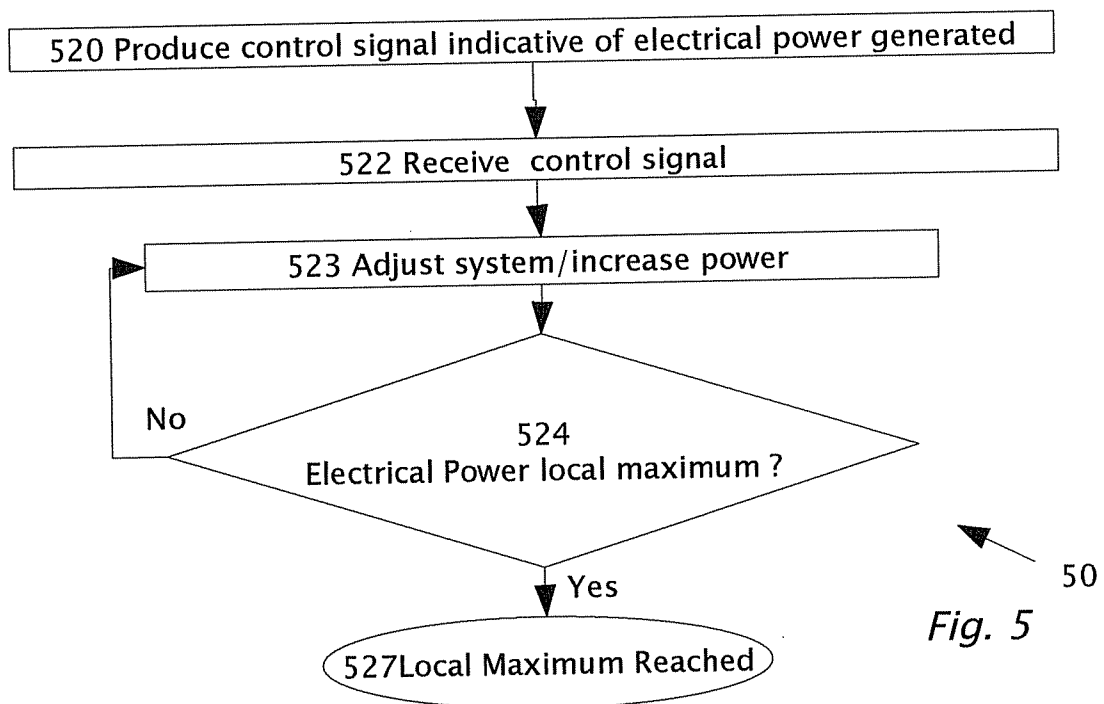


Fig. 5

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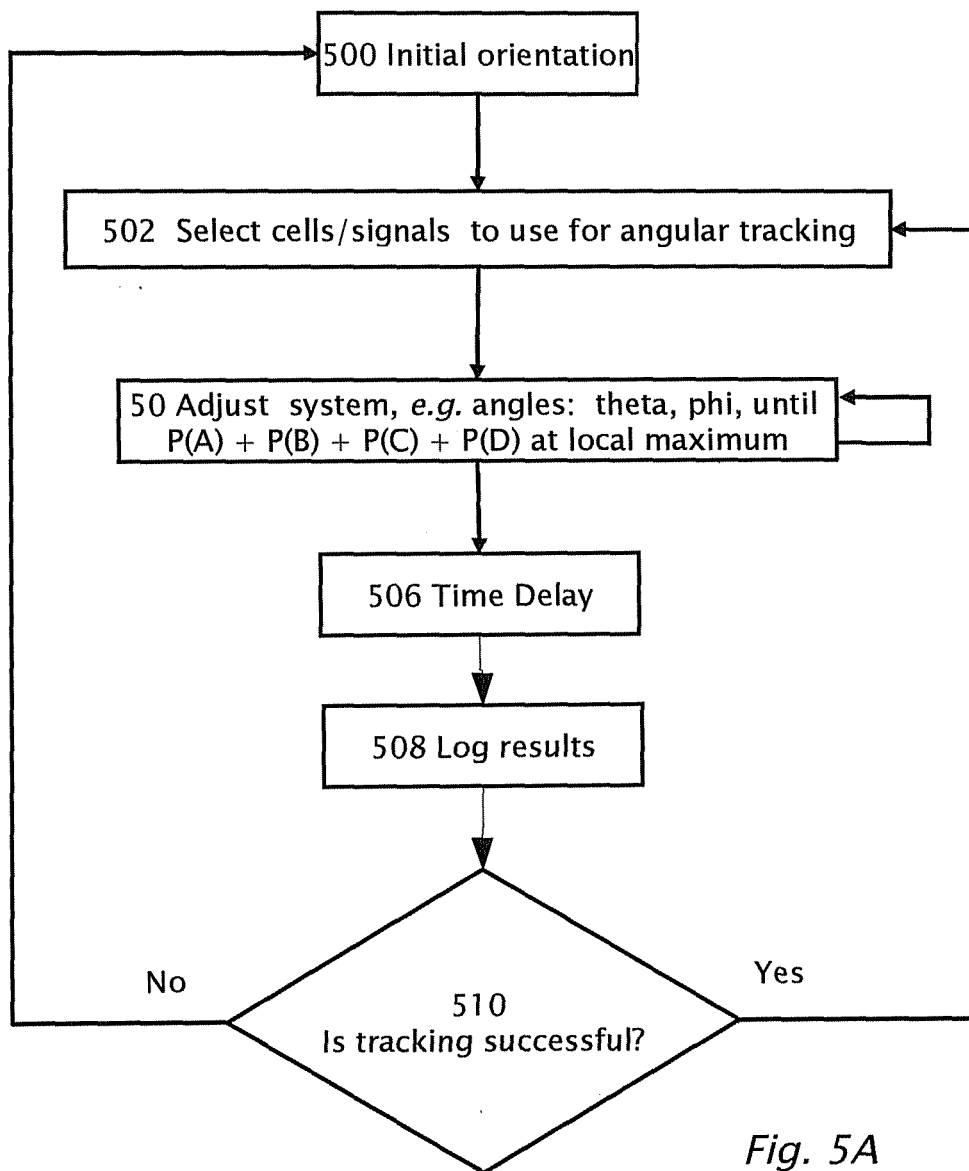


Fig. 5A