Title: MODULE AND CAPACITANCE DETECTING METHOD

Abstract: A module (5) includes a capacitance detecting circuit (10). The capacitance detecting circuit (10) includes a constant current source (20) supplying a constant current to a voltage detection point (P), a time measuring unit (28) measuring time of charge until the voltage of the voltage detection point (P) attains to a prescribed voltage, a storage unit (30) and an operation unit (32). The storage unit (30) stores a first data obtained in advance as the time of charge of a capacitance element having a known capacitance value, and a second data obtained in advance as the time of charge of a capacitance component (Cp). The operation unit (32) generates a third data representing the time of charge of an object of detection (Cs) from a difference between the first measurement value of the time measuring unit (28) when the capacitance component (Cp) is connected to the voltage detection point (P) and the second data, and based on the ratio between the third data and the first data and on the known capacitance value, calculates the capacitance value of the object of detection (Cs).
Module and Capacitance Detecting Method

DESCRIPTION

TECHNICAL FIELD

[0001]
The present invention relates to a module for detecting capacitance value of an object of detection, as well as to a method of detecting capacitance value of an object of detection.

BACKGROUND ART

[0002]
Devices for measuring electrostatic capacitance of a capacitor are disclosed, for example, in Japanese Patent Laying-Open Nos. 56-107170 (Patent Literature 1) and 2-271266 (Patent Literature 2). The device disclosed in Japanese Patent Laying-Open No. 56-107170 includes a power supply and a DC current measuring device. The power supply increases voltage with time at a known constant rate. The power supply and the DC current measuring device are connected in series to terminals of a capacitor. From the measured current value, electrostatic capacitance of the capacitor is calculated.

[0003]
The device disclosed in Japanese Patent Laying-Open No. 2-271266 includes a DC power supply, a resistor connected between the DC power supply and a capacitor, a current detecting circuit for detecting a current flowing through the resistor, an integrating circuit for integrating charging current detected by the current detecting circuit, and an operation output unit. The operation output unit calculates electrostatic capacitance of the capacitor based on the integrated value obtained by the integrating circuit and the voltage across the capacitor terminals.

CITATION LIST

PATENT LITERATURE

[0004]
A capacitance component having a large capacitance value often exists on a path from a detection terminal to an object of detection. The capacitance value of the capacitance component may vary device by device. If variation of capacitance component is comparable to the variation width of capacitance value of the object of detection, it becomes difficult to detect the variation in capacitance value of the object of detection.

An object of the present invention is to provide a technique for detecting capacitance value of an object of detection with high accuracy.

According to an aspect, the present invention provides a module including a current path and a capacitance detecting circuit. The current path is connected to an object of detection and includes a capacitance component. The capacitance detecting circuit supplies a constant current to the object of detection through the current path, and thereby detects a capacitance value of the object of detection. The capacitance value detecting circuit includes: a constant current source supplying the constant current to a voltage detection point; a charge/discharge circuit connecting the current path to the voltage detection point to charge the object of detection and the capacitance component, and disconnecting the current path from the voltage detection point to discharge the object of detection and the capacitance component; a time measuring circuit measuring time of charge until voltage at the voltage detection point attains to a prescribed voltage; a storage unit storing first data obtained in advance as the time of charge of a capacitance element having a known capacitance value, and second data
obtained in advance as the time of charge of the capacitance component; and an operation unit. The operation unit generates third data representing the time of charge of the object of detection from a difference between a first measurement value of the time measuring unit when the current path is connected to the voltage detection point and the second data, and based on a ratio between the third data and the first data and on the known capacitance value, calculates capacitance value of the object of detection.

[0008] Preferably, the time measuring unit includes an oscillator and a counter. The counter generates a count value as data indicating the time of charge, in response to an output signal from the oscillator. The storage unit stores in advance an initial value of oscillation frequency of the oscillator and an initial value of the first data. The operation unit corrects the initial value of the first data in accordance with a ratio between the initial value of the oscillation frequency and a measured value of the oscillation frequency, to update the first data.

[0009] Preferably, the module further includes a reference capacitance element. The charge/discharge circuit connects the reference capacitance element to the voltage detection point to charge the reference capacitance element. The charge/discharge circuit disconnects the reference capacitance element from the voltage detection point to discharge the reference capacitance element. The time measuring unit measures the time of charge of the reference capacitance element to output a second measurement value. The storage unit stores in advance fourth data obtained in advance as the time of charge of the reference capacitance element. The operation unit corrects the first measurement value based on a ratio between the second measurement value and the fourth data.

[0010] Preferably, the storage unit stores relation between information indicating types of control signals and the capacitance value of the object of detection. The operation unit generates a control signal based on a calculated capacitance value and the relation
stored in the storage unit. The capacitance detecting circuit further includes an
interface circuit for outputting the calculated capacitance value and the control signal.

[0011]

According to another aspect, the present invention provides a capacitance
detecting method of detecting a capacitance value of an object of detection connected
to a current path including a capacitance component, including the steps of: supplying a
constant current to a voltage detection point to charge the object of detection and the
capacitance component; measuring time of charge until voltage of the voltage detection
point attains to a prescribed voltage; storing in advance first data obtained in advance
as the time of charge of a capacitance element having a known capacitance value, and
second data obtained in advance as the time of charge of the capacitance component;
generating third data indicating the time of charge of the object of detection, from a
difference between a first measurement value measured as the time of charge of the
object of detection and the capacitance component, and the second data; and calculating
capacitance value of the object of detection, based on a ratio between the third data and
the first data and on the known capacitance value.

[0012]

Preferably, at the step of measuring, the time of charge is measured by an
oscillator and a counter generating a count value in response to an output signal from
the oscillator. The capacitance detecting method further includes the steps of: storing
in advance an initial value of an oscillation frequency of the oscillator and an initial
value of the first data; and correcting the initial value of the first data in accordance
with a ratio between the initial value of the oscillation frequency and a measured value
of the oscillation frequency.

[0013]

Preferably, the capacitance detecting method further includes the steps of:
storing in advance fourth data obtained in advance as the time of charge of a reference
capacitance element; supplying the constant current to the voltage detection point to
charge the reference capacitance element; and measuring the time of charge of the
reference capacitance element to generate a second measurement value. The step of generating the third data includes the step of correcting the first measurement value based on a ratio between the second measurement value and the fourth data.

ADVANTAGEOUS EFFECTS OF INVENTION

The present invention enables highly accurate detection of a capacitance value of an object of detection.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a block diagram showing a schematic configuration of electronic equipment mounting a module in accordance with a first embodiment of the present invention.

Fig. 2 is a block diagram showing a configuration of a capacitance detecting circuit in accordance with the first embodiment of the present invention.

Fig. 3 shows a specific example of a capacitance component Cp.

Fig. 4 shows another example of the module configuration.

Fig. 5 shows a basic method of detecting capacitance in accordance with an embodiment of the present invention.

Fig. 6 is a circuit diagram related to adjustment of the capacitance detecting circuit.

Fig. 7 is a flowchart representing adjustment of the capacitance detecting circuit.

Fig. 8 shows data stored in a storage unit of the capacitance detecting circuit.

Fig. 9 is a circuit diagram related to adjustment of the module.

Fig. 10 is a flowchart representing adjustment of the module.

Fig. 11 shows data stored in the storage unit of the capacitance detecting circuit after adjustment of the module.

Fig. 12 is a flowchart representing detection of a capacitance value of an object of detection Cs.

Fig. 13 is a block diagram showing a schematic configuration of electronic equipment mounting a module in accordance with a second embodiment of the present
Fig. 14 shows a configuration of a storage unit of the capacitance detecting circuit in accordance with the second embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[0016]
In the following, embodiments of the present invention will be described in detail with reference to the figures. In the figures, the same or corresponding portions are denoted by the same reference characters and description thereof will not be repeated.

[0017]
[Embodiment 1]

Fig. 1 is a block diagram showing a schematic configuration of electronic equipment mounting a module in accordance with a first embodiment of the present invention. Referring to Fig. 1, electronic equipment 1 includes a high-frequency power supply 4 and a module 5.

[0018]
Module 5 includes a capacitance detecting circuit 10, a reference capacitance element Cref, a signal line 2, and a matching circuit 12. Reference capacitance element Cref is electrically connected to capacitance detecting circuit 10.

[0019]
Signal line 2 is connected between high frequency power supply 4 and capacitance detecting circuit 10. Signal line 2 includes a capacitance component Cp and an inductor Lb. Capacitance component Cp and inductor Lb are connected in series. Capacitance component Cp passes a high-frequency signal, while it shuts-off DC flow. Inductor Lb passes DC component, while it blocks entrance of high-frequency component to capacitance detecting circuit 10.

[0020]
Object of detection Cs is connected to signal line 2. Therefore, object of detection Cs and capacitance component Cp are electrically connected in parallel with
Capacitance detecting circuit 10 supplies a constant current to object of detection Cs through signal line 2, and detects the capacitance value of object of detection Cs. In the present embodiment, signal line 2 is a current path supplying constant current to object of detection Cs. Object of detection Cs has its capacitance value changed. It is noted, however, that the capacitance value of object of detection Cs may be fixed.

Matching circuit 12 is formed by a combination of an inductor, a fixed capacitance element and a variable capacitance element. In the present embodiment, in order to detect the capacitance value of object of detection Cs, a constant current is supplied to capacitance component Cp and object of detection Cs, so that object of detection Cs and capacitance component Cp are charged. The inductor serves to apply the ground potential to capacitance component Cp when capacitance component Cp and object of detection Cs are charged. In Fig. 1 and in the following figures described later, only the inductor among the components of matching circuit 12 is shown as an element related to detection of capacitance value of object of detection Cs.

Fig. 2 is a block diagram showing a configuration of a capacitance detecting circuit in accordance with the first embodiment of the present invention. Referring to Fig. 2, capacitance detecting circuit 10 includes a constant current source 20, terminals CREF, CIN, 23, 25 and 27, a charge/discharge circuit 24, a band-gap voltage source 26, a time measuring circuit 28, a storage unit 30, a control unit 32, an an interface circuit 34.

Capacitance component Cp and object of detection Cs are electrically connected in parallel with terminal CIN. Reference capacitance element Cref is electrically connected to terminal CREF.
Charge/discharge circuit 24 connects capacitance component \( C_p \) and object of detection \( C_s \) to a voltage detection point \( P \). Thus, capacitance component \( C_p \) and object of detection \( C_s \) are charged. At this time, charge/discharge circuit 24 discharges reference capacitance element \( C_{\text{ref}} \). Further, charge/discharge circuit 24 connects reference capacitance element \( C_{\text{ref}} \) to voltage detection point \( P \), to charge reference capacitance element \( C_{\text{ref}} \). At this time, charge/discharge circuit 24 discharges capacitance component \( C_p \) and object of detection \( C_s \).

Specifically, charge/discharge circuit 24 includes switches SW1 to SW4. Each of switches SW1 to SW4 is controlled by control unit 32.

Switch SW1 has a first end connected to terminal CIN. Switch SW1 has a second end connected to voltage detection point \( P \). Switch SW2 has a first end connected to terminal CIN. Switch SW2 has a second end grounded. Switch SW3 has a first end connected to terminal CREF. Switch SW3 has a second end connected to voltage detection point \( P \). Switch SW4 has a first end connected to terminal CREF. Switch SW4 has a second end grounded.

Switches SW1 and SW4 turn on/off at the same timing. Switches SW2 and SW3 turn on/off at the same timing. Here, when switches SW1 and SW4 are on, switches SW2 and SW3 are off. In this case, a current \( I_{\text{ref}} \) from constant current source 20 is output from terminal CIN through voltage detection point \( P \) and switch SW1. By the current output from terminal CIN, capacitance component \( C_p \) and object of detection \( C_s \) are charged. Further, reference capacitance element \( C_{\text{ref}} \) is discharged. The current from reference capacitance element \( C_{\text{ref}} \) flows through terminal CREF and switch SW4 to the ground node.

When switches SW1 and SW4 are off, switches SW2 and SW3 are on. In this
case, the current Iref from constant current source 20 is output from terminal CREF through voltage detection point P and switch SW3. By the current output from terminal CREF, reference capacitance element Cref is charged. Further, capacitance component Cp and object of detection Cs are discharged. The current from capacitance component Cp and object of detection Cs flows through terminal CIN and switch SW2 to the ground node.

[0030]

Time measuring circuit 28 measures the time of charge of a capacitance element or a capacitance component connected to voltage detection point P. In the present embodiment, the time of charge is defined to be the time period necessary for the voltage Vs of voltage detection point P to reach from 0 to the reference voltage Vref.

[0031]

Time measuring circuit 28 includes an oscillator 42, a counter 44, and a comparator 46. Oscillator 42 generates a clock signal having a constant period. Oscillator 42 is formed, for example of a CR oscillating circuit including a capacitor and a resistor.

[0032]

In response to a signal input to oscillator 42, oscillator 42 can adjust its oscillation frequency. Terminal 25 is for measuring the oscillation frequency of oscillator 42 from the outside.

[0033]

In response to the clock signal CLK from oscillator 42, counter 44 changes its count value. In order to turn on one of the switches SW1 and SW4, control unit 32 outputs a start signal. Counter 44 starts counting when the start signal becomes active.

[0034]

Comparator 46 compares the voltage Vs with the reference voltage Vref. At a time point when voltage Vs attains to the reference voltage Vref, comparator 46 applies a stop signal to counter 44. Counter 44 stops counting when the stop signal becomes active.
[0035]

Band-gap voltage source 26 generates a band-gap voltage, that is, a voltage stable against temperature change. Band-gap voltage source 26 supplies reference voltage Vref to comparator 46. Further, band-gap voltage source 26 supplies a voltage to constant current source 20 and oscillator 42.

[0036]

Storage unit 30 includes a non-volatile memory (NVM) 48 and a data storage unit 50. Non-volatile memory 48 stores trimming codes. The trimming codes represent data for adjusting each of the oscillation frequency of oscillator 42 and the constant current Iref from constant current source 20 to a desired value. Terminal 27 is for adjusting the oscillation frequency and the constant current Iref from the outside.

[0037]

Here, it is noted that input of trimming codes to terminal 27 is not limiting. By way of example, the trimming codes may be stored in non-volatile memory (NVM) 48 through interface circuit 34. In that case, it is possible for control unit 32 to read the trimming codes from non-volatile memory (NVM) 48 and to execute trimming.

[0038]

Data storage unit 50 stores first data obtained in advance as the time of charge of capacitance element having a known capacitance value. Data storage unit 50 stores the first data in association with the oscillation frequency of oscillator 42.

[0039]

Data storage unit 50 further stores data obtained in advance as the time of charge of capacitance component Cp, and data obtained in advance as the time of charge of reference capacitance element Cref. These data are represented as count values of counter 44.

[0040]

The count values stored in data storage unit 50 are obtained before module 5 is mounted on electronic equipment 1. The state in which module 5 is not yet mounted on electronic equipment 1 corresponds to the state in which object of detection Cs is
not connected to signal line 2.

[0041]

Control unit 32 calculates the capacitance value of object of detection Cs based on the data stored in data storage unit 50 and the measurements (count values) obtained by time measuring circuit 28. Specifically, control unit 32 realizes the "operation unit" of the capacitance detecting circuit in accordance with the present invention. The operation for calculating the capacitance value of object of detection Cs will be described in detail later.

[0042]

Interface circuit 34 outputs a signal to the outside of capacitance detecting circuit 10, or receives a signal from the outside of capacitance detecting circuit 10. By way of example, a capacitance value calculated by control unit 32 is output from interface circuit 34. Further, terminal 23 outputs the clock signal CLK generated by oscillator 42 to the outside of capacitance detecting circuit 10.

[0043]

Capacitance component Cp represents a capacitance element, a capacitance component or a combination thereof. Fig. 3 shows a specific example of capacitance component Cp.

[0044]

Referring to Fig. 3, capacitance component Cp is formed, for example, by a plurality of parasitic capacitances. In the example shown in Fig. 3, capacitance component Cp includes capacitance components Ca, Cb and Cc. Capacitance component Ca represents parasitic capacitance of signal line 2. Capacitance component Cb represents capacitance element included in noise filter 3. Capacitance component Cc represents a capacitance component included in capacitance detecting circuit 10.

[0045]

The configuration of module 5 is not limited to those shown in Figs. 1 and 2. Fig. 4 shows another example of the configuration of module 5. Referring to Fig. 4,
object of detection Cs is included in module 5. Object of detection Cs is an element having correlation between the change in its characteristics and fluctuation of capacitance, such as a resonator. Further, matching circuit 12 is provided outside of module 5. As long as module 5 includes capacitance detecting circuit 10, module 5 may have a still different configuration.

[0046]
In order to avoid complicated description, in Figs. 3 and 4, reference capacitance element Cref is not shown.

[0047]
Next, the method of detecting capacitance in accordance with an embodiment of the present invention will be described.

[0048]
Generally, charges Q stored in a capacitance element, capacitance value C of the capacitance element and the voltage V of the capacitance element satisfy the relation of \( Q = CV \). By differentiating both sides of this equation by time \( t \), the following equation is obtained, where I represents current.

\[
dQ/dt = I = C \times (dV/dt)
\]

[0049]
The equation above represents that the voltage increases in proportion to time, when the capacitance element is charged with a constant current.

[0050]
Fig. 5 shows a basic method of detecting capacitance in accordance with an embodiment of the present invention. Referring to Fig. 5, \( C_p \) and \( C_s \) represent the capacitance value of capacitance component \( C_p \) and capacitance value of object of detection Cs. When \( C = (C_p + C_s) \) and when \( C = C_p \), count value until the voltage \( V_s \) of voltage detection point P attains to the voltage \( V_{ref} \) is obtained. The count value changes in a prescribed period in proportion to the period of clock signal CLK. Therefore, the time of charge is represented by a product of the count value and the prescribed period.
The count value when the voltage $V_s$ attains to the voltage $V_{ref}$ depends on the magnitude of the capacitance value. When $C = (C_p + C_s)$, the count value is $N_{ps}$, and when $C = C_p$, the count value is $N_p$. The value $\Delta N$ represents a difference between the count values $N_{ps}$ and $N_p$. The value $\Delta N$ represents the time of charge corresponding to object of detection $C_s$.

A count value $N_O$ of a capacitance element having a known capacitance value $C_k$ is obtained in advance. From the relation $C_s = \Delta N \cdot N_O$, the capacitance value of object of detection $C_s$ can be calculated. In the present embodiment, the capacitance of the object of detection $C_s$ can be detected through the following steps.

1. Adjustment of capacitance detecting circuit;
2. Adjustment of the module; and

In the following, processes of respective steps will be described in greater detail.

(Adjustment of Capacitance Detecting Circuit)

Fig. 6 is a circuit diagram related to adjustment of the capacitance detecting circuit. Referring to Fig. 6, capacitance detecting circuit 10 is connected to a test board 60. Test board 60 includes capacitance elements $C_{ref}$, $C_{p'}$ and $C_k$, a counter 62, and a frequency measuring circuit 64. Capacitance elements $C_{p'}$ and $C_k$ are connected in parallel with terminal $C_{IN}$ of capacitance detecting circuit 10. Capacitance element $C_{ref}$ is connected to terminal $C_{REF}$ of capacitance detecting circuit 10.

Capacitance values of capacitance elements $C_k$, $C_{p'}$ and $C_{ref}$ are measured in advance. Elements having mutually equal capacitance are selected as capacitance components $C_{p'}$ and $C_{ref}$. By way of example, if the capacitance value of...
capacitance element \( C_{\text{ref}} \) is determined in advance, a capacitance element having the capacitance value substantially equal to the capacitance value may be selected as capacitance element \( C_p' \).

[0056]

Capacitance detecting circuit 10 has terminals 23, 25 and 27. Terminal 23 outputs the clock signal CLK. Clock signal CLK is input to counter 62. Counter 62 starts counting in response to a start signal, and stops counting in response to a stop signal. Terminal 25 is connected to frequency measuring circuit 64. Terminal 27 receives the timing codes for adjusting the oscillation frequency.

[0057]

Fig. 7 is a flowchart representing adjustment of the capacitance detecting circuit. Referring to Figs. 6 and 7, at step S1, frequency measuring circuit 64 measures the oscillation frequency of the oscillator provided inside capacitance detecting circuit 10. At step S2, based on the measured oscillation frequency, trimming of current \( I_{\text{ref}} \) from constant current source 20 (see Fig. 2) and of oscillation frequency \( f_{\text{osc}} \) is executed. By the trimming, the value of current \( I_{\text{ref}} \) is adjusted to a desired value and the oscillation frequency is adjusted to the initial frequency \( f_{\text{osc}0} \).

[0058]

Referring to Figs. 2 and 7, at step S3, control unit 32 stores the oscillation frequency \( f_{\text{osc}0} \) and the trimming codes in storage unit 30 (non-volatile memory 48).

[0059]

At step S4, capacitance detecting circuit 10 supplies the current \( I_{\text{ref}} \) from terminal CIN to charge capacitance elements \( C_p' \) and \( C_k \). Specifically, control unit 32 controls charge/discharge circuit 24 to turn on switches SW1 and SW4, and turns off switches SW2 and SW3. Time measuring circuit 28 generates a count value \( N_{01} \) until the voltage \( V_s \) reaches the reference voltage \( V_{\text{ref}} \). Control unit 32 obtains the count value \( N_{01} \) from time measuring circuit 28.

[0060]

At step S5, capacitance detecting circuit 10 supplies the current \( I_{\text{ref}} \) from
terminal CREF to charge capacitance element Cref. Specifically, control unit 32 controls charge/discharge circuit 24 to turn on switches SW2 and SW3, and turns off switches SW1 and SW4. Capacitance element Cref is charged, and capacitance elements Cp' and Ck are discharged. Time measuring circuit 28 generates a count value N02 until the voltage Vs reaches the reference voltage Vref. Control unit 32 obtains the count value N02 from time measuring circuit 28. The processes of steps S4 and S5 may be executed in reverse order.

[0061]
At step S6, control unit 32 calculates a difference ΔN0 between the two count values N01 and N02. The difference count value ΔN0 is calculated as ΔN0 = N01 - N02.

[0062]
At step S7, control unit 32 stores the capacitance value of capacitance element Ck and the difference ΔN0 of the count value in storage unit 30 (data storage unit 50).

In the following description, the capacitance value of capacitance element Ck is denoted as capacitance value Ck.

[0063]
Capacitance elements Cp' and Cref have capacitance values equal to each other. Therefore, the difference between the sum of capacitance values Ck and Cp' and the capacitance value Cref is equal to the capacitance value Ck. By a separate measurement, the capacitance value Ck can be obtained precisely in advance. The difference count value ΔN0 is a count value representing the time of charge of capacitance element Ck.

[0064]
By the process of steps S6 and S7, capacitance detecting circuit 10 stores the capacitance value Ck and the difference count value ΔN0 in association with each other.

[0065]
Fig. 8 shows data stored in the storage unit of the capacitance detecting circuit. Referring to Fig. 8, non-volatile memory 48 of storage unit 30 stores a frequency foscO
in association with a trimming code D. Data storage unit 50 of storage unit 30 stores capacitance value Ck and difference count value ΔN0 in association with each other. The frequency fosc0 is the initial value of oscillation frequency.

(Adjustment of the Module)

Fig. 9 is a circuit diagram related to adjustment of the module. Referring to Fig. 9, the module is connected to a test board 70. Test board 70 includes a counter 72 and a frequency measuring circuit 74. Clock signal CLK is output from terminal 23 of capacitance detecting circuit 10 and input to counter 72. Counter 72 starts counting in response to a start signal, and ends counting in response to a stop signal. Terminal 25 is connected to frequency measuring circuit 74. The oscillation frequency and constant current Iref have already been adjusted. Therefore, in Fig. 9, terminal 27 is not shown.

It is unnecessary that the capacitance values of capacitance component Cp and reference capacitance element Cref are known. Further, it is unnecessary that the capacitance value of capacitance component Cp is equal to the capacitance value of reference capacitance element Cref.

Fig. 10 is a flowchart representing adjustment of the module. Referring to Figs. 9 and 10, at step S11, frequency measuring circuit 74 measures the oscillation frequency of the oscillator provided in capacitance detecting circuit 10.

Referring to Figs. 2 and 10, at step S12, control unit 32 corrects the difference count value ΔN0 stored in storage unit 30 (data storage unit 50) based on the measured oscillation frequency. Control unit 32 corrects the difference count value ΔN0 and generates a difference count value ΔNO' in accordance with Equation (1) below.

\[
\Delta N_{O'} = \Delta N_0 \times \frac{f_{osc}}{f_{osc0}} 
\]

[0070]
Control unit 32 updates the difference count value ΔN0 stored in data storage unit 50 to ΔΝ0'.

At step S13, capacitance detecting circuit 10 supplies the current Iref from terminal CIN to charge capacitance component Cp. Time measuring circuit 28 generates count value N1 until the voltage Vs reaches the reference voltage Vref. Control unit 32 obtains the count value N1 from time measuring circuit 28.

At step S14, capacitance detecting circuit 10 supplies the current Iref from terminal CREF to charge reference capacitance element Cref. Time measuring circuit 28 generates count value N2 until the voltage Vs reaches the reference voltage Vref. Control unit 32 obtains the count value N2 from time measuring circuit 28.

The processes of steps S13 and S14 are the same as those of steps S4 and S5, respectively, and, therefore, detailed description will not be repeated. The processes of steps S13 and S14 may be executed in reverse order.

At step S15, control unit 32 stores the count value N1 in association with terminal CIN, in storage unit 30 (data storage unit 50). Further, control unit 32 stores the count value N2 in association with terminal CREF in storage unit 30 (data storage unit 50).

Fig. 11 shows data stored in the storage unit of the capacitance detecting circuit after adjustment of the module. Referring to Fig. 11, data storage unit 50 of storage unit 30 stores capacitance value Ck and difference count value ΔΝ0' in association with each other. Further, data storage unit 50 stores count values N1 and N2 in association with terminals CIN and CREF, respectively.

When capacitance detecting circuit 10 is mounted on module 5, the oscillation
frequency of the oscillator may change. Therefore, at step S11, the oscillation frequency is measured.

[0077]

The time of charge of capacitance element Ck does not change before and after the change of oscillation frequency of the oscillator. Therefore, the following relation is satisfied.

\[ \Delta N_0^'/f_{osc} = \Delta N_0/f_{iscO} \]

[0078]

By modifying the equation above, Equation (1) is derived.

[0079]

Count values N1 and N2 are used for detecting the capacitance value of object of detection Cs. The magnitude of parasitic capacitance may differ module by module. Therefore, capacitance component Cp may also differ module by module. The processes of steps S13 and S14 correspond to calibration of the module in consideration of variation in capacitance value of capacitance component Cp.

[0080]

(Mounting of the Module on Electronic Equipment)

Fig. 12 is a flowchart representing detection of the capacitance value of object of detection Cs. The process shown in Fig. 12 is executed at arbitrary timing (for example, at a constant period). Referring to Figs. 2 and 12, at step S21, capacitance detecting circuit 10 supplies current Iref from terminal CIN to charge capacitance component Cp and object of detection Cs. Time measuring circuit 28 generates a count value N11 until the voltage Vs reaches the reference voltage Vref. Control unit 32 obtains the count value N11 from time measuring circuit 28.

[0081]

At step S22, capacitance detecting circuit 10 supplies the current Iref from terminal CREF to charge reference capacitance element Cref. Time measuring circuit 28 generates a count value N12 until the voltage Vs reaches the reference voltage Vref. Control unit 32 obtains the count value N12 from time measuring circuit 28.
The processes of steps S21 and S22 are the same as those of steps S4 and S5, respectively, and, therefore, detailed description thereof will not be repeated. The processes of steps S21 and S22 may be executed in reverse order.

At step S23, control unit 32 calculates the ratio of count value N2 to count value N12, that is, N2/N12.

At step S24, control unit 32 calculates a count value N1' by multiplying count value N1 by the ratio (N2/N12). Specifically, count value N1' is calculated in accordance with Equation (2) below.

\[ N_{1}' = N_{1} \times (N_{2}/N_{12}) \ldots (2) \]

At step S25, control unit 32 calculates the capacitance value Cs in accordance with Equation (3) below.

\[ \Delta N \text{O}: (N_{1}' - N_{1}) = C_{k}: C_{s} \ldots (3) \]

Basically, the capacitance of capacitance component Cp does not change even when module 5 is mounted on electronic equipment 1. Count value N1 represents the time of charge of capacitance component Cp and object of detection Cs, and count value N1' represents the time of charge of capacitance component Cp. Provided that the oscillation frequency fosc does not fluctuate before and after module 5 is mounted on electronic equipment 1, the count value that indicates the time of charge of object of detection Cs will be (N1' - N1). Count value corresponding to the known capacitance value Ck is obtained in advance (difference count value \( \Delta N \text{O} \)) in data storage unit 50. Therefore, if oscillation frequency fosc does not fluctuate, the capacitance value of object of detection Cs can be calculated from the relation Ck: Cs = \( \Delta N \text{O}: (N_{1}' - N_{1}) \).

Oscillation frequency fosc, however, may possibly fluctuate depending on
temperature or other factors. Therefore, in the embodiment of the present invention, the count value $N_{11}$ is corrected in consideration of the fluctuation of oscillation frequency.

[0088] The capacitance value of reference capacitance element $C_{ref}$ does not change before and after module 5 is mounted on electronic equipment 1. Therefore, if the oscillation frequency fluctuates, the count value representing the time of charge of reference capacitance element $C_{ref}$ changes.

[0089] The ratio $N_2/N_{12}$ between count values $N_{12}$ and $N_2$ represents $(\text{oscillation frequency before module 5 is mounted on electronic equipment 1})/ (\text{oscillation frequency after module 5 is mounted on electronic equipment 1})$.

[0090] Difference count value $(N_{1f} - N_l)$ and count value $\Delta N_O'$ are both obtained based on the oscillation frequency before module 5 is mounted on electronic equipment 1. Therefore, capacitance value $C_s$ is detected from the relation represented by Equation (3).

[0091] If the oscillation frequency is stable, the ratio between the count values $N_{12}$ and $N_2$ becomes closer to 1. In such a state, the processes of steps S14 and S22 to S24 may be omitted. In such a case, capacitance value $C_s$ may be detected in accordance with Equation (4) below, at step S25.

$$\Delta N_O': (N_{1f} - N_l) = C_k: C_s \ldots (4)$$

[0092] As described above, in accordance with the first embodiment, before the module is mounted on the electronic equipment, the count value corresponding to the capacitance component $C_p$ of the module is obtained and the count value is stored.

[0093] As shown as an example in Fig. 3, capacitance component $C_p$ may include the
parasitic capacitance of the module. Therefore, the capacitance value of capacitance component C_p may differ module by module. Specifically, the capacitance value of capacitance component C_p may vary significantly module by module. Basically, however, the capacitance value of a capacitance component C_p of a certain module does not change before and after the module is mounted on electronic equipment. By the first embodiment, even if the capacitance value of capacitance component C_p differs module by module, the capacitance value of object of detection C_s can be detected with high accuracy.

[0094]

Further, by the first embodiment, the count value (N_i 1) corresponding to the time of charge of the capacitance component C_p and object of detection C_s is corrected. It is possible that the oscillation frequency fluctuates depending on temperature or other factors. By the first embodiment, the capacitance value of object of detection C_s can be detected with high accuracy regardless of the fluctuation in oscillation frequency.

[0095]

[Embodiment 2]

Fig. 13 is a block diagram showing a schematic configuration of electronic equipment mounting a module in accordance with a second embodiment of the present invention. Referring to Fig. 13, capacitance detecting circuit 10 detects the capacitance value C_s and applies a control signal in accordance with the detected capacitance value C_s to matching circuit 12. Thus, capacitance detecting circuit 10 controls matching circuit 12. As described above, matching circuit 12 includes a variable capacitance element. By way of example, the control signal is used for changing the capacitance value of a variable capacitance element.

[0096]

The second embodiment is not limited the configuration in which capacitance detecting circuit 10 directly controls matching circuit 12. For example, module 5 may include a control circuit for controlling matching circuit 12 in accordance with a control signal output from capacitance detecting circuit 10.
The configuration of capacitance detecting circuit 10 is basically the same as that shown in Fig. 2. Storage unit 3 stores a table defining the relation between the detected capacitance value and the types of control signals. Except for this point, the configuration of other portions of capacitance detecting circuit 10 is the same as that shown in Fig. 2, and therefore, detailed description will not be repeated.

Fig. 14 shows a configuration of a storage unit of capacitance detecting circuit 10 in accordance with the second embodiment of the present invention. Referring to Figs. 11 and 14, in the second embodiment, tables 48a and 48b are stored in non-volatile memory 48 in storage unit 30. The number of tables is not specifically limited.

In table 48a, the range of capacitance value C_s and the types of control signals correspond to each other. For example, capacitance detecting circuit 10 has two channels for outputting control signals. If capacitance value C_s is smaller than C_O, for instance, the first and second channels (channel 1, channel 2) correspond to control signals SPI1a and SPI2a, respectively.

Control unit 32 shown in Fig. 2 specifies the type of control signal corresponding to the detected capacitance value C_s, by looking up the table. Control unit 32 generates a control signal of the specified type. The generated control signal is output from interface circuit 34 (see Fig. 2). An external device may access to interface circuit 34 to read the control signal.

As described above, according to the second embodiment, control in accordance with the detected capacitance becomes possible. This improves convenience for the user.
In the embodiments described above, the difference count value $\Delta N_0$ corresponds to first data obtained in advance as the time of charge of a capacitance element having a known capacitance value (Ck). The count value $N_1$ corresponds to the second data obtained in advance as the time of charge of capacitance component Cp. The difference count value $(N_0 - N_1)$ corresponds to the third data indicating the time of charge of object of detection Cs. Count value $N_2$ corresponds to the fourth data obtained in advance as the time of charge of reference capacitance element Cref. Count value $N_{12}$ corresponds to the first measurement value of time measuring circuit 28. Count value $N_{12}$ corresponds to the second measurement value of time measuring circuit 28.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being interpreted by the terms of the appended claims.

REFERENCE SIGNS LIST

2 signal line, 3 noise filter, 4 high frequency power supply, 5 module, 10 capacitance detecting circuit, 12 matching circuit, 20 constant current source, 23, 25, 27, CIN, CREF terminals, 24 charge/discharge circuit, 26 band-gap voltage source, 28 time measuring circuit, 30 storage unit, 32 control unit, 34 interface circuit, 42 oscillator, 44, 62, 72 counters, 46 comparator, 48 non-volatile memory, 50 data storage unit, 60, 70 test boards, 64, 74 frequency measuring circuits, Ck capacitance element, Cref reference capacitance element, Cs object of detection, Lb inductor, P voltage detection point.
CLAIMS

1. A module, comprising:
   
a current path connected to an object of detection (Cs) and including a
   capacitance component (Cp); and
   
a capacitance detecting circuit (10) supplying a constant current to said object
   of detection (Cs) through said current path, for detecting a capacitance value of said
   object of detection (Cs),
   
said capacitance value detecting circuit (10) including
   
a constant current source (20) supplying said constant current to a voltage
   detection point (P),
   
a charge/discharge circuit (24) connecting said current path to said voltage
   detection point (P) to charge said object of detection (Cs) and said capacitance
   component (Cp), and disconnecting said current path from said voltage detection point
   
a time measuring circuit (28) measuring time of charge until voltage at said
   voltage detection point (P) attains to a prescribed voltage,
   
a storage unit (30) storing first data (ΔΝ₀) obtained in advance as said time of
   charge of a capacitance element (Ck) having a known capacitance value, and second
   
data (Ν₁) obtained in advance as said time of charge of said capacitance component
   (Cp), and
   
an operation unit (32) generating third data representing said time of charge of
   said object of detection (Cs) from a difference between a first measurement value
   (Ν₁₁) of said time measuring unit (28) when said current path is connected to said
   
voltage detection point (P) and said second data (Ν₁), and based on a ratio between
   
said third data and said first data (ΔΝ₀) and on said known capacitance value,
   calculating capacitance value of said object of detection (Cs).

2. The module according to claim 1, wherein
said time measuring unit (28) includes
an oscillator (42), and
a counter (44) responsive to an output signal from said oscillator, for generating
a count value as data indicating said time of charge;
said storage unit (30) stores in advance an initial value of oscillation frequency
of said oscillator and an initial value of said first data ($\Delta N_0$); and
said operation unit (32) corrects the initial value of said first data ($\Delta N_0$) in
accordance with a ratio between the initial value of said oscillation frequency and a
measured value of said oscillation frequency, to update said first data ($\Delta N_0$).

3. The module according to claim 1, further comprising
a reference capacitance element (Cref); wherein
said charge/discharge circuit (24) connects said reference capacitance element
(Cref) to said voltage detection point (P) to charge said reference capacitance element
(Cref);
said charge/discharge circuit (24) disconnects said reference capacitance
element (Cref) from said voltage detection point (P) to discharge said reference
capacitance element (Cref);
said time measuring unit (28) measures said time of charge of said reference
capacitance element (Cref) to output a second measurement value (N12);
said storage unit (30) stores in advance fourth data (N2) obtained in advance as
said time of charge of said reference capacitance element (Cref); and
said operation unit (32) corrects said first measurement value (Ni 1) based on a
ratio between said second measurement value (N12) and said fourth data (N2).

4. The module according to claim 1, wherein
said storage unit (30) stores relation between information indicating types of
control signals and the capacitance value of said object of detection (Cs);
said operation unit (32) generates a control signal based on a calculated
capacitance value and said relation stored in said storage unit (30); and
said capacitance detecting circuit further includes
an interface circuit (34) for outputting the calculated capacitance value and said control signal.

5. A capacitance detecting method of detecting a capacitance value of an object of detection (Cs) connected to a current path including a capacitance component (Cp), comprising the steps of:
supplying a constant current to a voltage detection point (P) to charge said object of detection (Cs) and said capacitance component (Cp);
measuring time of charge until voltage of said voltage detection point (P) attains to a prescribed voltage;
storing in advance first data (ΔΝ0) obtained in advance as the time of charge of a capacitance element (Ck) having a known capacitance value, and second data (Nl) obtained in advance as the time of charge of said capacitance component (Cp);
generating third data indicating said time of charge of said object of detection (Cs), from a difference between a first measurement value (Nl 1) measured as said time of charge of said object of detection (Cs) and said capacitance component (Cp) and, said second data (Nl); and
calculating capacitance value of said object of detection (Cs), based on a ratio between said third data and said first data (ΔΝ0) and on said known capacitance value.

6. The capacitance detecting method according to claim 5, wherein
at said step of measuring,
said time of charge is measured by an oscillator (42) and a counter (44)
generating a count value in response to an output signal from said oscillator;
said capacitance detecting method further comprising the steps of:
storing in advance an initial value of an oscillation frequency of said oscillator (42) and an initial value of said first data (ΔΝ0); and
correcting the initial value of said first data ($\Delta N_0$) in accordance with a ratio between the initial value of said oscillation frequency and a measured value of said oscillation frequency.

7. The capacitance detecting method according to claim 5, further comprising the steps of:
   - storing in advance fourth data ($N_2$) obtained in advance as said time of charge of a reference capacitance element ($C_{ref}$);
   - supplying said constant current to said voltage detection point (P) to charge said reference capacitance element ($C_{ref}$); and
   - measuring said time of charge of said reference capacitance element ($C_{ref}$) to generate a second measurement value ($N_{12}$); wherein said step of generating said third data includes the step of correcting said first measurement value ($N_i\_1$) based on a ratio between said second measurement value ($N_{12}$) and said fourth data ($N_2$).
FIG. 7

START

S1

MEASURE OSCILLATION FREQUENCY OF OSCILLATOR

S2

TRIM CONSTANT CURRENT AND OSCILLATION FREQUENCY

S3

STORE OSCILLATION FREQUENCY \((f_{osc0})\) AND TRIMMING CODE IN STORAGE UNIT

S4

SUPPLY CURRENT FROM TERMINAL \(C_{in}\) AND OBTAIN COUNT VALUE \(N01\) UNTIL VOLTAGE \(V_s\) ATTAINS TO \(V_{ref}\)

S5

SUPPLY CURRENT FROM TERMINAL \(C_{ref}\) AND OBTAIN COUNT VALUE \(N02\) UNTIL VOLTAGE \(V_s\) ATTAINS TO \(V_{ref}\)

S6

CALCULATE DIFFERENCE BETWEEN TWO COUNT VALUES \((\Delta N0 = N01 - N02)\)

S7

STORE CAPACITANCE VALUE \(C_k\) AND DIFFERENCE COUNT VALUE \((\Delta N0)\) IN STORAGE UNIT

END
**FIG. 8**

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FIG. 10

START

S11

MEASURE OSCILLATION FREQUENCY OF OSCILLATOR

S12

CORRECT DIFFERENCE OF COUNT VALUE STORED IN MEMORY
($\Delta N_0 \rightarrow \Delta N_0'$)

S13

SUPPLY CURRENT FROM TERMINAL CIN AND OBTAIN COUNT VALUE N1 UNTIL VOLTAGE Vs ATTAINS TO Vref

S14

SUPPLY CURRENT FROM TERMINAL CREF AND OBTAIN COUNT VALUE N2 UNTIL VOLTAGE Vs ATTAINS TO Vref

S15

STORE COUNT VALUES N1 AND N2 IN ASSOCIATION WITH TERMINALS CIN AND CREF, RESPECTIVELY, IN STORAGE UNIT

END
### FIG. 11

#### Frequency Trimming Code Table

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#### Capacitance Value Count Value Table

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#### Terminal Count Value Table

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FIG. 12

START

S21
SUPPLY CURRENT FROM TERMINAL CIN AND
OBTAIN COUNT VALUE N11 UNTIL VOLTAGE
Vs ATTAINS TO Vref

S22
SUPPLY CURRENT FROM TERMINAL CREF
AND OBTAIN COUNT VALUE N12 UNTIL
VOLTAGE Vs ATTAINS TO Vref

S23
CALCULATE RATIO OF COUNT VALUE N2 TO
COUNT VALUE N12
(N2/N12)

S24
CALCULATE N11' BY MULTIPLYING COUNT
VALUE N11 BY THE RATIO
(N11' = N1 \times N2/N12)

S25
CALCULATE Cs FROM THE RELATION
\( \Delta N0' : (N11' - N1) = Ck : Cs \)

END
### FIG.14

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# INTERNATIONAL SEARCH REPORT

**International application No.**
PCT/CN2012/076262

**A. CLASSIFICATION OF SUBJECT MATTER**

According to International Patent Classification (IPC) or to both national classification and IPC

G01R27/26 (2006.01) i

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC: G01R27/1-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPLSIP0ABS, CNABS, CNKI, capacitor, capacitance, time+, count+, current, source, constant, stray, parasitic, detect+, measure+, sens+

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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<th>Category</th>
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<td>JP6-2421 59A(JAPAN RADIO CO., LTD.) 02 September 1994 (02.09.1994) the specification: paragraphs 0011-0021, figure 1</td>
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<tr>
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<td>CN101082644A(WANG, Yue et.al.) 05 December 2007 (05.12.2007) the whole document</td>
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<tr>
<td>A</td>
<td>CN101578526A(MICROCHIP TECHNOLOGY INC.) 11 November 2009 (11.11.2009) the whole document</td>
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<td>A</td>
<td>CN101910850A(3M INNOVATIVE PROPERTIES CO.) 08 December 2010(08.12.2010) the whole document</td>
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<tr>
<td>A</td>
<td>US2011/0050255A1(ANALOG DEVICES INC.) 03 March 2011(03.03.2011) the whole document</td>
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1-7 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:
  ‘A’ document defining the general state of the art which is not considered to be of particular relevance
  ‘E’ earlier application or patent but published on or after the international filing date
  ‘L’ document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)
  ‘O’ document referring to an oral disclosure, use, exhibition or other means
  ‘P’ document published prior to the international filing date but later than the priority date claimed

‘T’ later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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‘Y’ document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

‘&’ member of the same patent family

Date of the actual completion of the international search
25 January 2013 (25.01.2013)

Date of mailing of the international search report
07 Mar. 2013 (07.03.2013)

Name and mailing address of the ISA/CN
The State Intellectual Property Office, the P.R.China
6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088
Facsimile No. 86-10-62019451

Form PCT/ISA /210 (second sheet) (July 2009)

Authorized officer
MA, Yujie
Telephone No. (86-10) 624 14 15 1
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<td>JP6-242159A</td>
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<td>WO2008088986A2</td>
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