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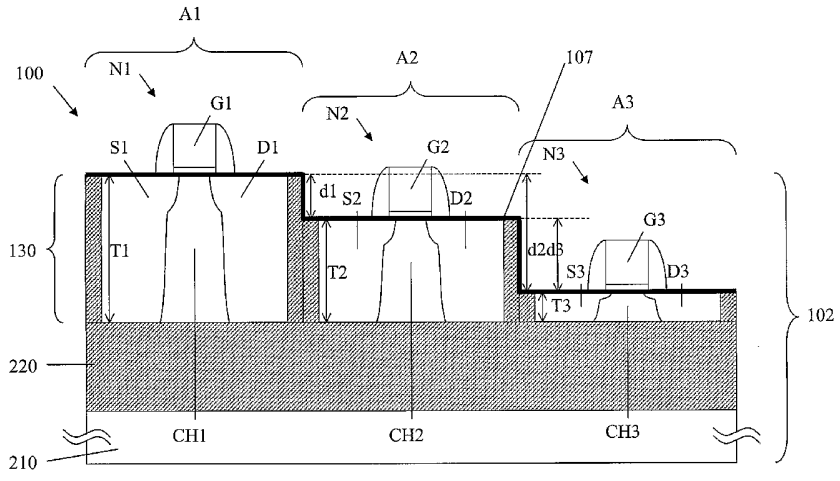
(54) **Title:** SEMICONDUCTOR DEVICE HAVING SUBSTRATE COMPRISING LAYER WITH DIFFERENT THICKNESSES AND METHOD OF MANUFACTURING THE SAME



(57) **Abstract:** This invention relates to a semiconductor device and a method of manufacturing this device. An embodiment of the semiconductor device (100) according to the invention comprises a semiconductor body (102) with a surface (107), the semiconductor body (102) further comprising an active part (130) positioned at the surface (107), a substrate part (210) and an insulating layer (220) located between the active part (130) and the substrate part (210). The active part (130) comprises three parts (A1,A2,A3), each part having a thickness (Tl,T2,T3), the thickness (TI,T2,T3) being measured at right angles to the surface (107), and the thickness within each area (A1,A2,A3) being substantially uniform. In each area (A1,A2,A3) a transistor (Nl,N2,N3) is present. Each transistor (N1,N2,N3) comprises a source (Sl,S2,S3), a drain (Dl,D2,D3) and a channel region which extends between the source (Sl,S2,S3) and the drain (Dl,D2,D3), wherein the source (S1,S2,S3), the drain (D,D2,D3) and the channel region (CH1,CH2,CH3) are located under the surface (107) of the semiconductor body (102). Each transistor (N1,N2,N3) further comprises a gate (G1,G2,G3) located above the surface (107) of the semiconductor body (102).

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SEMICONDUCTOR DEVICE HAVING SUBSTRATE COMPRISING LAYER WITH DIFFERENT THICKNESSES AND METHOD OF MANUFACTURING THE SAME

The invention relates to a semiconductor device comprising a semiconductor body with a surface, which semiconductor body comprises an active part situated at the surface, a substrate part and an insulating part situated between the active part and the substrate part, wherein the active part comprises a first region having a first thickness and a second region having a second thickness, which deviates from the first thickness, wherein the first thickness and the second thickness are measured in the direction perpendicular to the surface, and wherein the thickness of the active part within the first region as well as within the second region is substantially uniform.

The invention further relates to a method of manufacturing such a semiconductor device.

A semiconductor device of the type mentioned in the opening paragraph is known from United States Patent Publication US 2003/0183877 A1. The known semiconductor device comprises: a semiconductor substrate; an insulating layer on the semiconductor substrate; a silicon layer formed on the insulating layer and further comprising a first and a second source, a first and a second drain, and a first and a second channel region formed between the first source and the first drain, and between the second source and the second drain, respectively, wherein at least one of the channel regions has a thickness smaller than or equal to 10 nanometers. The semiconductor device further comprises a first gate-insulating layer and a second gate-insulating layer formed on, respectively, the first and the second channel region, and a first and a second gate electrode formed on, respectively, the first and the second gate-insulating layer.

A drawback of the known semiconductor device is that the electrical characteristics of transistors arranged therein, which are each composed of a source, a drain, an interposed channel, a gate-insulating layer and a gate electrode, are not optimal in the semiconductor device.

It is an object of the invention to provide a semiconductor device of the type mentioned in the opening paragraph, which has improved electrical characteristics of the transistors.

To achieve this object, the semiconductor device mentioned in the opening paragraph is characterized according to the invention in that the active part comprises, within each of the regions, a source, a drain and a channel region extending between the source and the drain.

The invention is based on the recognition that, in the known semiconductor device, the parasitic capacitances and resistances of transistors, which are formed by a source, a drain, a channel region and a gate, are large and, in addition, dependent upon the thickness of the channel region. The parasitic capacitances from the gate to the source and from the gate to the drain are large, because in the known semiconductor device the gate has a comparatively large common boundary with the source and the drain. This results in substantial overlap capacitances. The parasitic capacitances from the gate to the source and from the gate to the drain are dependent upon the thickness of the channel region, because a thinner channel region leads to a greater thickness of the gate. After all, the sum of both thicknesses is constant. Analogously, this implies that a larger thickness of the channel region leads to a smaller thickness of the gate.

In the semiconductor device in accordance with the invention, the source, the channel region and the drain are situated in the active part, said active part having a substantially uniform thickness within each of the regions. This means that a gate provided at a later stage will be situated either above the active part (and hence above the surface) of the semiconductor device and/or below the active part (for example in the case of a double-gate transistor architecture). The overlap between the gate on the one hand and the source and the drain on the other hand is smaller. Consequently, a reduction rather than an increase of the parasitic capacitances from the gate to the source and from the gate to the drain is achieved as compared to the buried-gate architecture of the known semiconductor device.

In addition, the thickness of the gate in the semiconductor device in accordance with the invention no longer necessarily depends on the channel thickness. After all, the gate (or gates) is (are) situated completely outside the active part and hence exhibit(s) a uniform thickness, viewed across the semiconductor device. Consequently, both the series

resistance of the gate and the gate capacitances vary less throughout the semiconductor device.

An embodiment of the semiconductor device in accordance with the invention is characterized in that the active part comprises a third region having a third thickness that deviates from the thickness of the first region and the thickness of the second region, wherein the active part comprises also, within the third region, a source, a drain and a channel region extending between the source and the drain. This measure is very attractive because it enables the threshold voltages of transistors, formed by a source, a drain, a channel region and a gate, to be varied more in the semiconductor device.

An embodiment of the semiconductor device in accordance with the invention is characterized in that the thickness of one of the regions of the active part is less than 10 nanometers. This embodiment has the advantage that it is more suitable for use in future generations of CMOS technologies. The scaling down of the technologies also leads to scaling down of the gate length. Consequently, the channel thickness will also have to scale down. To obtain a properly functioning transistor, the channel thickness should be approximately one third of the length of the gate.

Preferably, the semiconductor body comprises silicon, and, preferably, the insulating layer comprises an oxide.

A method of manufacturing the inventive semiconductor device of the type mentioned in the opening paragraph comprises the following steps:

providing a first semiconductor body having a first surface and an opposite second surface, which semiconductor body comprises an active part at the first surface and a substrate part at the second surface,

providing a patterned masking layer on the first surface of the first semiconductor body; and

carrying out an implantation process in the direction of the first surface of the first semiconductor body, wherein the location of implanted regions with respect to the first surface is determined also by the masking layer, and wherein the nature of the implantation is chosen to be such that the implanted regions in at least the active part of the first semiconductor body will distinguish themselves from surrounding regions in the active part in such a manner that the implanted regions can be subjected to a treatment intended to create regions of different thickness in the active part.

The advantage of the method in accordance with the invention resides in that the thicknesses of the regions of the active part can be defined very accurately. The position

of the implanted regions is determined particularly by the thickness of the masking layer, the implantation energy, the implantation dose and the type of implantation ions. These all are quantities that can be controlled very accurately in a production environment.

The treatment can be chosen from a group of treatment methods comprising:

selectively removing the implanted regions; and

converting the implanted regions to electrically insulating regions.

An advantage of this measure is that for the further manufacture of the semiconductor device use can be made of conventional techniques. Consequently, the buried-gate architecture with all concomitant drawbacks, as is known from the semiconductor device according to the prior art, will not be applied.

A further embodiment of the method in accordance with the invention comprises, after the implementation step has been carried out, the following further steps:

removing the masking layer;

bonding together, at the first surface, the first semiconductor body and a second semiconductor body using a further insulating layer between the first semiconductor body and the second semiconductor body, and

removing the substrate part from the first semiconductor body.

An advantage of this embodiment resides in that it can be applied to inexpensive semiconductor bodies, such as bulk substrates. After all, in the eventual semiconductor device only the active part of the first semiconductor body will remain. The use of inexpensive semiconductor bodies results in a lower cost price of the final semiconductor device.

In a further development of the last-mentioned embodiment, the method in accordance with the invention is characterized in that the implantation process comprises at least a doped implantation, and said method comprising, after the removal of the substrate part from the first semiconductor body, a step in which the implanted regions are converted to oxide regions by means of dopant-enhanced oxidation. This embodiment has the advantage that the oxide regions can be readily selectively removed at a later stage of the method. The conversion to oxide regions preferably takes place by dopant-enhanced low-temperature oxidation.

In an embodiment related to the last-mentioned embodiment, the method in accordance with the invention is characterized in that the implantation process comprises at least an amorphisation implantation, as a result of which the implanted regions are formed so

as to be amorphous regions. This embodiment has the advantage that the low-temperature oxidation step is not necessary. As a result, one step can be saved in the method.

In an extension to the last-mentioned embodiment, the method is characterized in that, after the step of removing the substrate part from the first semiconductor body, the method comprises a step in which the amorphous regions are converted to oxide regions by means of oxidation. This embodiment has the advantage that it enables the oxide regions to be more readily selectively removed at a later stage of the method. Preferably, the conversion to oxide regions takes place by means of low-temperature oxidation.

In an embodiment of the method in accordance with the invention, after the step of conversion into oxide regions, these oxide regions are selectively removed in the active part, as a result of which the active part comprises a first region having a first thickness and a second region having a second thickness which deviates from the first thickness, wherein the first thickness and the second thickness are measured in the direction perpendicular to the first surface of the first semiconductor body, and wherein the thickness within the first region as well as within the second region is substantially uniform. This measure has the advantage that it enables all regions of the active part to be accessed from the upper side of the semiconductor device.

In an embodiment related to the last-mentioned embodiment of the method in accordance with the invention, after the step of removing the substrate part from the first semiconductor body, the amorphous regions in the active part are selectively removed, as a result of which the active part comprises a first region having a first thickness and a second region with a second thickness that deviates from the first thickness, wherein the first thickness and the second thickness are measured in the direction perpendicular to the first surface of the first semiconductor body, and wherein the thickness within the first region as well as within the second region is substantially uniform. This measure is necessary to create regions having different thicknesses in the active part. In addition, this measure also enables all regions of the active part to be accessed from the upper side of the semiconductor device.

In a very advantageous modification of the second embodiment of the method in accordance with the invention, the first semiconductor body comprises an insulating layer which extends between the active part and the substrate part, and the implantation process at least comprises an implantation with oxygen ions, and the method, after said implantation, comprises a step in which the oxygen ions in the implanted regions are activated, so that oxide regions are formed at the locations of the implanted regions. The important advantage of this embodiment is that it comprises fewer steps. The oxide regions are situated under the

first surface of the semiconductor body and hence all regions of the active part can be accessed from the upper side of the semiconductor device.

In an extension to the last-mentioned embodiment, the method comprises, after the step of carrying out the activation, the following further steps:

removing the masking layer;

bonding together, at the first surface, the first semiconductor body and a second semiconductor body using a further insulating layer between the first semiconductor body and the second semiconductor body,

removing the substrate part from the first semiconductor body;

removing the insulating layer from the first semiconductor body; and

selectively removing the oxide regions, as a result of which the active part comprises a first region having a first thickness and a second region having a second thickness that deviates from the first thickness, wherein the first thickness and the second thickness are measured in the direction perpendicular to the first surface of the first semiconductor body, and wherein the thickness within the first region as well as within the second region is substantially uniform.

This embodiment has the advantage that the insulating layer of the eventual semiconductor device extends substantially in one plane and, in addition, has a substantially uniform thickness within said plane.

In a further improvement of the last-mentioned embodiment of the method, the insulating layer of the first semiconductor body comprises substantially the same material as oxide regions to be formed at a later stage, so as to enable the insulating layer and the oxide regions to be selectively removed in one step. This has the advantage that one step is saved in the method.

In a modification of above-mentioned embodiments of the method, the first semiconductor body comprises an insulating layer which is situated between the active part and the substrate part of the first semiconductor body, and, after the step of removing the substrate part from the first semiconductor body, the insulating layer is removed.
This embodiment has the advantage that the step of removing the substrate part from the first semiconductor body is simplified. That is to say, this embodiment enables said substrate part to be selectively removed, after which also the insulating layer can be selectively removed.

In another modification of above-mentioned embodiments of the method in accordance with the invention, the first semiconductor body comprises a germanium-containing layer which is situated between the active part and the substrate part of the first

semiconductor body, and, after the step of removing the substrate part from the first semiconductor body, the germanium-containing layer is removed. This embodiment has the additional advantage that the step of removing the substrate part from the first semiconductor body is simplified. That is to say, this embodiment enables said substrate part to be removed selectively, after which also the germanium-containing layer can be selectively removed.

In an embodiment of the method, the process of bonding together the first and the second semiconductor body includes the following sub-steps:

providing the further insulating layer on the first surface of the first semiconductor body;

providing the second semiconductor body with a second surface;

bringing the first surface of the first semiconductor body into contact with the second surface of the second semiconductor body; and

bonding together the first semiconductor body and the second semiconductor body by means of "fusion bonding".

An advantage of these steps is that the insulating layer can be provided on the first semiconductor body in a highly controlled manner, so that the eventual, active part will exhibit little difference in thickness, viewed across the surface.

In an embodiment related to the last-mentioned embodiment of the method, bonding together the first and the second semiconductor body includes the following sub-steps:

providing the second semiconductor body with a second surface, the further insulating layer being present at the second surface;

bringing the first surface of the first semiconductor body into contact with the second surface of the second semiconductor body; and

bonding together the first semiconductor body and the second semiconductor body by means of "fusion boding".

An advantage of these steps is that the insulating layer can be provided on the second semiconductor body in a highly controlled manner, so that the eventual active part will exhibit little difference in thickness, viewed across the surface.

In an extension to above-mentioned embodiments of the method, the masking layer and the implantation are provided in such a manner that the thickness of one of the regions of the resulting active part is less than 10 nm. The thicknesses of the regions of the active part are very accurately determined by the method, yielding relatively the greatest advantage in this range.

Preferably, the method according to the invention comprises a step in which at the location of each of the regions at least one transistor is provided in the active part. This step has the advantage that it allows the greatest variation of the threshold voltage of the transistors.

In an important modification of all of the above embodiments of the method, the masking layer is provided so as to have a stepped profile. A stepped profile in the masking layer enables the implanted regions to be formed at different depths in the semiconductor body. This means that more than two different thicknesses in the active part can be created, dependent upon the number of different thicknesses in the masking layer. This is advantageous if more than two different threshold voltages have to be formed. Preferably, in an embodiment of the method, more than one mask is used during the application of the masking layer. An advantageous manner of creating a stepped profile in the masking layer consists in providing the masking layer in a number of steps, with each step comprising different masks.

Preferably, at least one of the semiconductor bodies comprises silicon. Preferably, the second semiconductor body comprises silicon, because silicon is a very common material.

The masking layer preferably comprises a photoresist. This is an attractive option, because photoresist is a common material for use as a masking layer.

These and other aspects of the semiconductor device and the method of manufacturing the semiconductor device according to the invention are apparent from and will be elucidated with reference to the embodiment(s) described hereinafter.

In the drawings:

Fig. 1 illustrates the problem in the known semiconductor device,

Fig. 2 shows a graph in which the threshold voltage variation of a single-gate SOI NMOS transistor is plotted as a function of the channel thickness at different doping levels in the channel region.

Fig. 3 shows a graph in which the oxidation enhancement is plotted as a function of the doping concentration and the doping type.

Figs. 4 through 11 show an embodiment of the method by means of diagrammatic cross-sectional views of the semiconductor device in different stages of the manufacturing process.

Fig. 12 shows a first embodiment of the semiconductor device in accordance with the invention; and

Fig. 13 shows a second embodiment of the semiconductor device in accordance with the invention.

The problem of the known semiconductor device will be explained in greater detail with reference to Fig. 1. Said Figure shows the known semiconductor device 1 comprising a semiconductor substrate 2, an insulating layer 3 on the semiconductor substrate 2, a silicon layer 4, formed on the insulating layer 3, and comprising a first source 10 and a second source 10', a first drain 12 and a second drain 12' and a first channel region 14 and a second channel region 14' formed between the first source 10 and the first drain 12, and between the second source 10' and the second drain 12', respectively. The known semiconductor device 1 further comprises a first gate-insulating layer 16 and a second gate-insulating layer 16' formed on the first channel region 14 and the second channel region 14', respectively, and a first gate electrode 18 and a second gate electrode 18' formed on the first gate-insulating layer 16 and the second gate-insulating layer 16', respectively. The first source 10, the first drain 12, the first channel region 14 and the first gate electrode 18 together form a first transistor 20, and the second source 10', the second drain 12', the second channel region 14' and the second gate electrode 18' together form a second transistor 20'.

The invention is based also on the recognition that, in the known semiconductor device 1, certain parasitic capacitances and resistances in both transistors 20, 20' differ due to the difference in thickness between the channel regions 14, 14'. In Fig. 1, the first transistor 20 has a channel region 14 with a thickness h1, which is smaller than the thickness h1' of the channel region 14' of the second transistor 20'. This also implies that the thickness h2 of the gate electrode 18 of the first transistor 20 exceeds the thickness h2' of the gate electrode 18' of the second transistor 20'. After all, the sum of the thicknesses of the channel region and the gate electrode is constant due to the buried-gate architecture. As a result of said differences in thickness, the gate-source capacitances C1 and gate-drain capacitances C2 of the first transistor 20 exceed the gate-source capacitances C1' and gate-drain capacitances C2' of the second transistor 20'.

The invention is further based on the recognition that the gate-source capacitances C1, C1' and gate-drain capacitances C2, C2' in the known semiconductor device

1 are comparatively large, which is caused by the buried-gate architecture of the transistors 20, 20'.

The differences in thickness between the gate electrodes 18, 18' have yet another adverse effect. The series resistances R and R" will also be different. In the illustrated example of Fig. 1, the thickness h2 exceeds the thickness h2', which means that the gate-series resistance R is smaller than R'. Inter alia in analog circuits, such large, non-constant parasitic elements are undesirable, because they influence the transistor characteristics.

The invention is also based on insights illustrated in Fig. 2 and Fig. 3. Fig. 2 shows the dependence of the threshold voltage as a function of the thickness of the channel region at three different doping levels in the channel region: This Figure relates to a single-gate SOI NMOS transistor. A single-gate SOI PMOS transistor has similar characteristics. Arrow 100 illustrates for curve A (doping level in the channel region of $1.10^{e}18.cm^{-3}$) a threshold voltage difference of 550 mV at a difference in channel thickness of 30 nm. Consequently, varying the thickness of the channel region is an attractive option for varying the threshold voltage in a semiconductor device, as long as the doping level is sufficiently high. Preferably, the doping level of the channel region exceeds $1.10^{e}17.cm^{-3}$.

The invention is also based on the recognition that oxidation enhancement is an attractive technique for use in the manufacture of the semiconductor device in accordance with the invention. Fig. 3 shows that the increase in oxidation speed is higher than a factor of 20 if the doping concentration exceeds $2.10^{e}21.cm^{-3}$ for the arsenic (As) dopant type. The temperature chosen in the Figure is 650°C. The fact that the oxidation occurs much more rapidly at the location of the dopant than at dopant-free locations enables selectively implanted regions to be converted into a thicker oxide. This advantage will be used at a later stage in a method in accordance with the invention.

Fig. 4 is a diagrammatic cross-sectional view of the semiconductor device 100 in a stage of its manufacturing process. In this stage, a first semiconductor body (101) is provided comprising a first surface 105, an active layer 130 located at the first surface 105, as well as a substrate layer 110 and an insulating layer 120 which is situated between the active layer 130 and the substrate layer 110. The insulating layer 120 may be made of, for example, silicon oxide or silicon nitride, but other materials are also possible. The thickness of the active layer 130, measured at right angles to the first surface 105, preferably ranges between 5 and 400 nm. In an alternative embodiment, the insulating layer 120 is not present in the first semiconductor body 101. In this case, the semiconductor body may be a bulk substrate,

wherein there is no, or hardly any, difference between the active layer 130 and the substrate layer 110. This embodiment will be described in greater detail later on in the description.

Fig. 5 is a diagrammatic cross-sectional view of the semiconductor device 100 in a stage of its manufacturing process. In this stage, the first surface 105 of the first semiconductor body 101 is provided with a masking layer 140. For this purpose use can be made of conventional photolithography. In an embodiment of the method, the material of the masking layer 140 comprises a photoresist. In the embodiment shown of the method, this masking layer 140 comprises two differently patterned layers 140A, 140B. This results in a stepped profile in the masking layer 140. This stepped profile in the masking layer 140 can be obtained, for example, by using a plurality of masks. The advantage of said stepped profile will be discussed later on in the description. It is to be noted however that the masking layer does not necessarily have to present a stepped profile. In the absence of said stepped profile, the active part may possibly have two different thicknesses instead of three, in a later stage of the method.

Fig. 6 is a diagrammatic cross-sectional view of the semiconductor device 100 in a stage of its manufacturing process. In this stage, an implantation step with doping ions 199 is carried out. These doping ions may be, for example, arsenic (As), boron (B) or phosphor (P) ions. In another embodiment of the method, this implantation may also comprise other ions, as will be discussed later on in the description. The implantation takes place in the direction of the first surface 105 of the first semiconductor body 101 through the masking layer 140. The implantation ions 199 will end up in the first semiconductor body 101 at a certain depth under the first surface 105. The position of the implanted regions I1, I2, I3 thus formed depends on a number of parameters, including: the implantation energy, the pattern and dimensions of the masking layer 140 and of any sublayers 140A, 140B thereof, the material used for the masking layer 140, the type of implantation ions 199, the implantation dose and the structure of the semiconductor body 101.

In the example of Fig. 6, at the location of part A1 of the semiconductor body 101, the ions 199 of region I1 have passed through layer 140A as well as 140B, whereas, at the location of part A2 of the semiconductor body 101, the ions 199 of region I2 have passed through layer 140A only, and at the location of part A3 of the semiconductor body 101, the ions 199 of region I3 have not passed through any masking layer. As a result, the ions 199 in region I1 have been decelerated the most by the masking layer 140 during the implantation process, so that region I1 is closest to the first surface 105 of the semiconductor body 101. Region I2 has been decelerated less by the masking layer 140 and is situated at a greater

depth under the first surface 105 of the semiconductor body 101, and region I3 is situated at the greatest depth under the first surface 105 of the semiconductor body 101. In this example, region I3 demonstrates no overlap with the active layer 130, but this is not required for the invention. The choice of a certain depth also depends on the desired thickness of the active layer 130 at the location of the parts A1, A2, A3 in the semiconductor device 100.

Of course it is also possible to use only one patterned layer or more than two differently patterned layers 140A, 140B, as a result of which the depth of the implanted regions I1, I2, I3 under the first surface 105 can be varied less or more, respectively. If only one patterned layer 140A is used, only two different depths are possible; and if, for example, three patterned layers are used, four different depths are possible. After the implantation step, the masking layer 140 is removed. This can be achieved using conventional techniques.

Fig. 7 shows a diagrammatic cross-sectional view of the semiconductor device 100 in a stage of its manufacturing process. In this stage, a second semiconductor body 201 having a second surface 205 is provided. In this example, the second semiconductor body comprises an insulating layer 220 at the second surface 205. The insulating layer 220 may be made of, for example, silicon oxide, although other materials are also possible. To apply this insulating layer 220 to the second semiconductor body 201, use can be made of conventional growth techniques. In a next step, the second surface 205 of the second semiconductor body 201 is brought into contact with the first surface 105 of the first semiconductor body 101. Subsequently, the two semiconductor bodies 101, 201 are bonded together by means of fusion bonding so as to form a new semiconductor body 102. Fusion bonding is a technique known to those skilled in the art; for more information about this technique, reference is made to, for example, ["*Semiconductor Wafer Bonding: Science and Technology*", by Q.-Y. Tong, U. Gösele, Wiley-Interscience ; (1998), ISBN:0471574813].

In an alternative embodiment of the method in accordance with the invention, the first semiconductor body 101 is provided with a further insulating layer at the first surface 105. In this embodiment it is sufficient to provide a second semiconductor body 201 without an insulating layer. This may be, for example, a bulk substrate. The two semiconductor bodies 101, 201 are bonded together in a manner analogous to that described hereinabove.

Fig. 8 shows a diagrammatic cross-sectional view of the semiconductor device 100 in a stage of its manufacturing process. In this stage, the semiconductor device 100 is inverted, so that the original substrate layer 110 of the original first semiconductor body 101 becomes the topmost layer. As a result of this step, the implanted region I3 is situated closest under the upper surface 106. The step of Fig. 8 is an optional one, but it has been included in

this description in order to explain the invention. Said step can be dispensed with if means are provided for carrying out the method at the original lower side 106 of the semiconductor device 100.

Fig. 9 shows a diagrammatic cross-sectional view of the semiconductor device 100 in a stage of its manufacturing process. In this stage, both the substrate layer 110 and the insulating layer 120 are removed from the original, first semiconductor body 101. This can be achieved using a selective etch method. According to said method, for example, first the substrate layer 110 is selectively removed with respect to the insulating layer 120, after which the insulating 120 can be selectively removed with respect to the active layer 130. The removal of the substrate layer 110 and the insulating layer 120 implies, in the example shown in Fig. 9, that also the implanted region I3 is removed as well as a part of the implanted region I2. An important aspect of this embodiment of the invention lies in the fact that the steps of the method carried out so far provide access to the implanted regions I1, I2. However, in the description of another embodiment of the method, it will become apparent that this aspect is not necessary for the invention.

If the insulating layer 120 were to be absent, however, as described in the description with respect to Fig. 4, only the substrate layer 110 has to be removed. In this case, removal can be achieved, for example, by etching for a certain period of time. Preferably, however, said additional layer 120 is present between the substrate layer 110 and the active layer 130, because this renders the removal of the substrate layer 110 (and, if necessary, the insulating layer 120 itself) simpler and more reliable.

Fig. 10 is a diagrammatic cross-sectional view of the semiconductor device 100 in a stage of its manufacturing process. In this stage the dopant-enhanced oxidation is carried out. This technique is known from, inter alia, [C.P. Ho and J.D. Plummer, *"Si/Sio2 interface oxidation kinetics: a physical model for the influence of high substrate doping levels"*, J. Electrochem Soc., 126, 1979, pp. 1516-1530]. In this step, oxide regions 150 are formed in the active layer 130. Oxidation takes place, preferably, between 600°C and 750°C and is therefore also referred to as dopant-enhanced low-temperature oxidation. The oxidation regions 150 have a step-shaped structure and correspond substantially to the original, implanted regions I1, I2 (Fig. 9).

The basic idea behind this technique is that oxide is grown from the upper side of the semiconductor device. As shown in Fig. 3, the dopant-enhanced oxidation rate is highest at high surface concentrations of the doping. In the regions A2, A3 where implantation took place, the thickest oxide will be grown. However, oxide will also grow at

locations where implantation did not take place (in this example in region A1). This oxide will be much thinner, however, than at locations where doping was implanted, i.e. A2, A3. Any excess thin oxide in region A1 has not been shown for clarity of the Figures.

Fig. 11 is a diagrammatic cross-sectional view of the semiconductor device 100 in a stage of its manufacturing process. In this stage, the oxide regions 150 are selectively removed. This can be achieved using conventional techniques, such as selective etch methods. The result of the step illustrated in Fig. 11 is a semiconductor device 100 comprising an active part 130 with three regions A1,A2,A3 having different thicknesses T1,T2,T3, respectively. As a result of this step, in this example the semiconductor device 100 has a surface 107 with a step profile having a substantially uniform thickness T1,T2,T3 in each of the regions A1,A2,A3, respectively. The thicknesses T1,T2,T3 correspond to the eventual channel thicknesses of transistors to be provided later on in each of the regions A1,A2,A3.

The method as explained with reference to Figs 4 through Fig. 11 has many advantages. A first advantage of the method in accordance with the invention is that the thicknesses T1, T2, T3 of the eventually obtained active part 130 can be very accurately defined. The position of the implanted regions I1, I2, I3 is determined, in particular, by the thickness of the masking layer, the implantation energy, the implantation dose and the type of implantation ions. These all are quantities that can be controlled very accurately in a production environment.

An additional advantage of the method is that it can be applied to inexpensive semiconductor bodies 101, 201. A comparatively inexpensive semiconductor body 101 generally has a greater non-uniformity in the active part. This non-uniformity disappears in the final product when use is made of the method. Moreover, as regards the second semiconductor body, use can be made of an inexpensive bulk substrate onto which a thin oxide layer 220 can subsequently be grown with high accuracy (using conventional techniques), which will serve as an insulating layer in the final semiconductor device 100. As will be described later on in this description, this is very advantageous. The result of the use of comparatively inexpensive semiconductor devices 101, 201 is a reduced cost price of the eventual semiconductor device 100.

A third advantage is that the manufacture of the semiconductor device 100 can be continued using conventional techniques. This continuation includes, inter alia, the provision of transistors, contact holes and metal connections.

Fig. 12 shows a first embodiment of the semiconductor device in accordance with the invention. After carrying out the steps shown in Fig. 4 through Fig. 11, transistors N1,N2,N3 must be provided in the regions A1,A2,A3, respectively, of the active part 130. These are diagrammatically shown in Fig. 12. This Figure shows only one transistor per region A1,A2,A3, but a larger number is also possible. To provide transistors use can be made of conventional techniques.

The semiconductor device 100 shown in Fig. 12 comprises a semiconductor body 102 having a surface 107, said semiconductor body 102 further comprising an active part 130 situated at the surface 107, a substrate part 210 and an insulating part 220 situated between the active part 130 and the substrate part 210. The active part 130 comprises a first region A1 having a first thickness T1, a second region A2 having a second thickness T2 and a third region A3 having a third thickness T3, all thicknesses T1,T2,T3 of the regions A1,A2,A3 being measured at right angles to the surface 107 and being substantially uniform within each region A1,A2,A3. The active part 130 comprises, within each of the regions A1,A2,A3, a source S1,S2,S3, a drain D1,D2,D3 and a channel region CH1,CH2,CH3 extending between the source S1,S2,S3 and the drain D1,D2,D3, and, within each of the regions A1,A2,A3, a gate G1,G2,G3 being situated above the surface 107 at the location of the channel region CH1,CH2,CH3, the gate G1,G2,G3 being arranged so as to control the channel CH1,CH2, CH3. The source S1,S2,S3, the drain D1,D2,D3 and the channel region CH1,CH2,CH3 extending between the source S1,S2,S3 and the drain D1,D2,D3 form, in conjunction with the gate G2,G2,G3, a transistor N1,N2,N3.

After the provision of transistors in the semiconductor device 100, the usual steps are carried out for providing the metal connections, contact holes and vias, as well as any further manufacturing steps that might be required. For this purpose use can also be made of conventional techniques. Differences in thickness d1,d2,d3 in the active part 130 can be bridged by the contact holes (not shown) between the first metal layer (not shown) and the active part 130 and/or between the first metal layer and the gates G1,G2,G3 of the transistors N1,N2,N3. The differences in thickness d1,d2,d3 are shown exaggerated for clarity.

In combination with the appropriate doping in the channel regions CH1,CH2,CH3, the threshold voltages of each of the transistors N1,N2,N3 can be defined, as illustrated in Fig. 2. In each of the regions A1,A2,A3, both P-type and N-type transistors can be manufactured. A region A1,A2,A3 does not have to be uninterrupted, but may instead be spread over the semiconductor device 100. In the examples in the Figures, these regions A1,A2,A3 are depicted uninterrupted for reasons of clarity only.

The thicknesses T1,T2,T3 of the regions A1,A2,A3 of the active part 130 are preferably different. In this example, three regions A1,A2,A3 can be distinguished, but it is alternatively possible to manufacture more or fewer regions, dependent upon the desired spread in threshold voltage of the transistors N1,N2,N3 of the semiconductor device 100. The number of regions A1,A2,A3 having a different thickness T1,T2,T3, respectively, influences the number of possible threshold voltages. In other words, the larger the number of different thicknesses T1,T2,T3, the more the threshold voltage can be varied. The threshold voltage is determined predominantly by the combination of channel thickness T1,T2,T3 and doping level in the channel region CH1,CH2,CH3.

The semiconductor device 100 in accordance with the invention comprises transistors N1,N2,N3 of conventional architecture, and has a number of important advantages in comparison with the known semiconductor device 1 having the buried-gate architecture. Firstly, the thickness T1,T2,T3 of a channel region has less influence on the gate-source capacitances and the gate-drain capacitances. This can be attributed to the fact that not only is the thickness of the gate electrodes G1,G2,G3 independent of the thickness T1,T2,T3 of the channel region, but it even is constant throughout the semiconductor device 100. Secondly, the gate-source capacitances and the gate-drain capacitances are smaller. The third advantage is that, as a result of the constant thickness of the gate electrodes G1,G2,G3, the series resistance of the gate electrodes G1,G2,G3 is also uniform throughout the semiconductor device 100. These three advantages result in improved electrical characteristics of the transistors N1,N2,N3. Particularly in analog circuits these improvements are highly desirable.

There is a large number of parameters in the method according to the invention, and there are many possible parameter combinations to arrive at a properly functioning semiconductor device 100. An example of a possible combination is:

- the first semiconductor body 101 having an n-type or p-type doping (for example As, P, Sb, or B in a concentration of approximately 1^e15cm^{-3});
- the thickness of the active layer of the original semiconductor body 130 ranges between 10 nm and 100 nm,
- the masking layer 140 of a photoresist of the type JSR;
- the thickness of the photoresist layers 140A, 140B ranges between 5nm and 1000 nm;
- the implantation energy ranges preferably between 1keV and 500 keV;
- the type of ions used for the implantation for the dopant-enhanced oxidation is As or P;
- the implantation dose ranges between 1^e16cm^{-3} and 1^e17cm^{-3};

- the second semiconductor body 210 having an n-type or p-type doping (for example As, P, Sb, or B in a concentration of approximately 1^e15cm^{-3}); and
- the thickness of the insulating layer 220 of the second semiconductor body ranges between 5 nm and 1000 nm.

Fig 3 through Fig. 11 shows a first embodiment of the method in accordance with the invention. A second embodiment of the method substantially resembles the first embodiment. In this description only the differences between the second and the first embodiment will be described.

The implantation with doping ions (cf. Fig. 6) is substituted with an amorphisation implantation. For said amorphisation implantation, inter alia, Xenon (Xe), Argon (Ar), Arsenic (As), Antimony (Sb), Indium (In), Silicon (Si) and Germanium (Ge) can be implanted. As a result of this implantation, the implanted regions I1,I2,I3 are rendered amorphous instead of crystalline, and said regions I1,I2,I3 will distinguish themselves from the non-implanted regions, so that these regions can be selectively removed at a later stage (cf. Fig. 11) using, for example, selective etch methods.

The dopant-enhanced oxidation step is dispensed with.

The further manufacture of the semiconductor device 100 is similar to that of the first embodiment of the method. This second embodiment of the method has the advantage that one step in the method is saved, namely the step where the dopant-enhanced oxidation is carried out. In addition, by using amorphisation implantation the advantage is achieved that the amount of dopant necessary for the implantation is reduced, thereby reducing the risk of damage in the active layer. In addition, this embodiment of the method has the advantage that the overall thermal budget is lower than in the first embodiment of the method (the oxidation step is saved).

A third embodiment of the method in accordance with the invention is a combination of the first and the second embodiment. Initially the method is analogous to that of the second embodiment but becomes different after the step of removing the substrate part 110 (and, if necessary, the insulating layer 120, if present) from the first semiconductor body. After this step, an oxidation step is carried out in this embodiment of the method. In this step, use is made of the effect that the oxidation of the amorphous, implanted regions I1,I2,I3 takes place at a higher rate than that of the crystalline regions. Consequently, this effect is comparable to the dopant-enhanced oxidation. The further manufacture of the semiconductor device 100 proceeds in a way similar to that of the first embodiment of the method.

A change of the first embodiment of the method yields a fourth embodiment of the method. In this method the following steps are dispensed with:

the provision of the second semiconductor body 201 (Fig. 7)

the inverting of the semiconductor device (Fig. 8),

the removal of the substrate part 110 (and, if necessary, the insulating layer 120, if present) from the first semiconductor body (Fig. 9),

the selective removal of the implanted regions (Fig. 11).

In this embodiment of the method, the implantation step is carried out using oxygen ions 199 (Fig. 6). Instead of an oxidation process (Fig. 10), the oxygen ions in the semiconductor body are activated (immediately after the implantation step), as a result of which oxidation regions are formed at the location of the implanted regions. Activation of the oxygen ions takes place at a high temperature, preferably between 1000°C and 1400°C, and is well-known to those skilled in the art. The oxide regions do not have to be removed (Fig. 11), because they are situated under the surface 107 of the semiconductor device 100. The further manufacture of the semiconductor device proceeds in a manner similar to that of the first method. This fourth embodiment of the method has the advantage that it is less complex, because it comprises fewer steps.

In the first embodiment of the semiconductor device 100, the surface 107 (Fig. 12) of the active part 130 (Fig. 12) has a stepped profile. The advantage of this semiconductor device 100 resides in that the insulating layer 220 is flat and has a uniform thickness. As a result, all transistors N1, N2, N3 have a comparable parasitic capacitance from the active part to the substrate 210. The insulating layer 220 is preferably manufactured as thin as possible, because this has a favorable effect on the characteristics of transistors N3 with a thin channel region CH3. A comparatively thick insulating layer 220 leads, inter alia, to a comparatively large electrostatic coupling between the source S3 and the drain D3 via the insulating layer 220, which may be undesirable in certain situations.

In other situations, by contrast, a flat surface of the active part 130 may be advantageous. Fig. 13 shows a second embodiment of the semiconductor device 300 in accordance with the invention, which is obtained by means of the above-mentioned fourth embodiment of the method in which use has been made of a masking layer with two differently patterned sub-layers. The second embodiment of the semiconductor device 300 has an active part 330 with a surface 307 which is substantially flat. This has the advantage that, during further manufacture of the semiconductor device 300, bridging of differences in

thickness d1,d2,d3 (Fig. 12) in the surface 307 is not necessary, leading to a simplification of the manufacture of the semiconductor device 300.

The interface 308 between the active part 330 and an insulating region 360, defined by the insulating layer 320 together with the oxide region 350, has a stepped profile. In this example, the lower side 309 of the insulating region 360 also has a stepped profile, but this may alternatively be flat in the case of different parameter settings of the method. This depends, briefly summarized, on the position and the dimensions of the implanted regions I1,I2,I3.

The semiconductor device 300 is also provided with at least one transistor N1, N2, N3 per region A1, A2, A3 in the active part 330. In this example, transistors N3 in region A3 have the smallest thickness T3 of the channel region and, as a result, the insulating region 360 below them is the thickest. A favorable effect thereof is that the transistors N3 are least affected by substrate noise.

Should it nevertheless be deemed necessary that an insulating layer having a substantially uniform thickness is present over the surface of the semiconductor device, then the fourth embodiment of the method can be adapted. As a result, a fifth embodiment of the method according to the invention is obtained, which method, after the steps of the fourth embodiment of the method, proceeds similarly to the first embodiment of the method. After the step of activating oxygen ions, the following further steps are carried out:

removing the masking layer;

bonding together, at the first surface 307, the first semiconductor body 301 and a second semiconductor body, using a further insulating layer (220) between the first semiconductor body (101) and the second semiconductor body (201);

removing the substrate part 310 from the first semiconductor body 301;

removing the insulating layer 320 from the first semiconductor body 301; and

selectively removing the oxide regions 350, as a result of which the active part comprises a first region A1 having a first thickness T1 and a second region A2 having a second thickness T2 which is different from the first thickness T1, wherein the first thickness T1 and the second thickness T2 are measured in the direction perpendicular to the surface, and wherein the thickness within the first region A1 and within the second region A2 is substantially uniform.

The result of this fifth embodiment of the method is a semiconductor device comprising an active part 130 having a surface 107 with a stepped profile, which is identical to the first embodiment of the semiconductor device 100, as shown in Fig. 12. The most

important object of this embodiment of the method is, however, to ensure that the insulating layer 220 has a substantially uniform thickness throughout the surface 107 of the semiconductor device 100.

In this embodiment, like in the other embodiments, it is of course possible to use a masking layer having two differently patterned sub-layers, as a result of which three regions A1,A2,A3 are formed in the active part of the semiconductor device 100.

A further improvement of this embodiment of the method is achieved if the insulating layer 320 of the first semiconductor body 301 comprises substantially the same material as the oxide regions 350 formed (for example, if they both consist of silicon oxide). This makes it possible to selectively remove, in a single step, the insulating layer 320 from the first semiconductor body 310 as well as the oxide regions 350 formed. This leads to a saving of one step in the method.

All Figures in this description are merely diagrammatic and, in addition, not drawn to scale. They are used to illustrate the embodiments in accordance with the invention as well as technical backgrounds. The shapes of interfaces shown in the Figure may be different in reality. Every person skilled in the art will of course be capable of conceiving new embodiments of the invention. These, however, fall within the scope of protection of the claims.

The semiconductor bodies mentioned in the description, which are used in the method according to the invention, may comprise silicon in the substrate layer or in the active layer or in both. In other embodiments, only one of the two semiconductor bodies comprises silicon, and in yet other embodiments neither one of the two semiconductor bodies contains silicon. In the latter case, alternative materials are, for example, gallium-arsenic (GaAs), indium-phosphide (InP) or germanium (Ge).

In the Figures use is made, for illustration purposes, of a SOI substrate as a first semiconductor body; however, the invention can also be applied to, *inter alia*, "bulk" substrates, "strained-silicon" substrates and substrates containing a germanium component.

The description is based on a semiconductor device comprising single-gate transistors. However, the invention also relates to a semiconductor device comprising double-gate transistors. The second gate electrode, also referred to as back-gate, can then be provided, in the method, in, for example, the second semiconductor body.

CLAIMS:

1. A semiconductor device (100, 300) comprising a semiconductor body (102, 301) with a surface (107, 307), which semiconductor body (102, 301) comprises an active part (130, 330) situated at the surface (107, 307), a substrate part (210, 310) and an insulating part (220, 320) situated between the active part (130, 330) and the substrate part (210, 310), wherein the active part (130, 330) comprises a first region (A1) having a first thickness (T1) and a second region (A2) having a second thickness (T2), which deviates from the first thickness (T1), wherein the first thickness (T1) and the second thickness (T2) are measured in the direction perpendicular to the surface (107, 307), and wherein the thickness of the active part (130, 330) within the first region (A1) as well as within the second region (A2) is substantially uniform, characterized in that the active part (130, 330) comprises, within each of the regions (A1, A2), a source (S1, S2), a drain (D1, D2) and a channel region (CH1, CH2) extending between the source (S1, S2) and the drain (D1, D2).

2. A semiconductor device (100, 300) as claimed in Claim 1, characterized in that the active part (130, 330) comprises a third region (A3) having a third thickness (T3) that deviates from the thickness (T1) of the first region (A1) and the thickness (T2) of the second region (A2), wherein the active part (130, 330) comprises also, within the third region (A3), a source (S3), a drain (D3) and a channel region (CH3) extending between the source (S3) and the drain (D3).

3. A semiconductor device (100, 300) as claimed in any one of the preceding Claims, characterized in that the thickness of one of the regions (A1, A2, A3) of the active part (130, 330) is less than 10 nanometers.

4. A method of manufacturing a semiconductor device (100, 300) comprising the following steps:

providing a first semiconductor body (101) having a first surface (105) and an opposite second surface, which semiconductor body (101) comprises an active part (130) at the first surface (105) and a substrate part (110) at the second surface,

providing a patterned masking layer (140) on the first surface (105) of the first semiconductor body (101); and

carrying out an implantation process (199) in the direction of the first surface (105) of the first semiconductor body (101), wherein the location of implanted regions (I1, I2, I3) with respect to the first surface (105) is determined also by the masking layer (140), and wherein the nature of the implantation (199) is chosen to be such that the implanted regions (I1, I2, I3) in at least the active part (130) of the first semiconductor body (101)will distinguish themselves from surrounding regions in the active part (130) in such a manner that the implanted regions (I1, I2, I3) can be subjected to a treatment intended to create regions (A1, A2, A3) of different thickness (T1, T2, T3), respectively, in the active part (130).

5. A method as claimed in Claim 4, wherein the treatment is chosen from a group of treatment methods comprising:

selectively removing the implanted regions (I1, I2, I3); and

converting the implanted regions (I1, I2, I3) into electrically insulating regions (150, 350).

6. A method as claimed in Claim 5, wherein, after the implementation step (199) has been carried out, the method comprises the following further steps:

removing the masking layer (140),

bonding together, at the first surface 105, the first semiconductor body (101) and a second semiconductor body (201) using a further insulating layer (220) between the first semiconductor body (101) and the second semiconductor body (201), and

removing the substrate part (110) from the first semiconductor body (101).

7. A method as claimed in Claim 6, characterized in that the implantation process (199) comprises at least a doped implantation, and said method comprising, after the removal of the substrate part (110) from the first semiconductor body (101), a step in which the implanted regions (I1, I2, I3) are converted to oxide regions (150) by means of dopant-enhanced oxidation.

8. A method as claimed in Claim 6, characterized in that the implementation process (199) comprises at least an amorphisation implantation, as a result of which the implanted regions (I1, I2, I3) are formed so as to be amorphous regions.

9. A method as claimed in Claim 8, characterized in that, after the step of removing the substrate part (110) from the first semiconductor body (101), the method comprises a step in which the amorphous regions are converted to oxide regions (150) by means of oxidation.

10. A method as claimed in Claim 7 or 9, characterized in that, after the step of conversion into oxide regions (150), these oxide regions (150) are selectively removed in the active part (130), as a result of which the active part (130) comprises a first region (A1) having a first thickness (T1) and a second region (A2) having a second thickness (T2) which deviates from the first thickness (T1), wherein the first thickness (T1) and the second thickness (T2) are measured in the direction perpendicular to the first surface (105) of the first semiconductor body (101), and wherein the thickness within the first region (A1) as well as within the second region (A2) is substantially uniform.

11. A method as claimed in Claim 8, characterized in that, after the step of removing the substrate part (110) from the first semiconductor body (101), the amorphous regions in the active part (130) are selectively removed, as a result of which the active part (130) comprises a first region (A1) having a first thickness (T1) and a second region (A2) having a second thickness (T2) that deviates from the first thickness (T1), wherein the first thickness (T1) and the second thickness (T2) are measured in a direction perpendicular to the first surface (105) of the first semiconductor body (101), and wherein the thickness within the first region (A1) as well as within the second region (A2) is substantially uniform.

12. A method as claimed in Claim 5, wherein the first semiconductor body (101) comprises an insulating layer (120) which extends between the active part (130) and the substrate part (110), and wherein the implantation process (199) at least comprises an implantation with oxygen ions, and wherein the method, after said implantation, comprises a step in which the oxygen ions in the implanted regions (I1, I2, I3) are activated, so that oxide regions (350) are formed at the locations of the implanted regions (I1, I2, I3).

13. A method as claimed in Claim 12, wherein, after the step of carrying out the activation, the method comprises the following further steps:

removing the masking layer (140);

bonding together, at the first surface (105), the first semiconductor body (101) and a second semiconductor body (201) using a further insulating layer (220) between the first semiconductor body (101) and the second semiconductor body (201),

removing the substrate part (110) from the first semiconductor body (101);

removing the insulating layer (120) from the first semiconductor body (101); and

selectively removing the oxide regions (350), as a result of which the active part (130) comprises a first region (A1) having a first thickness (T1) and a second region (A2) having a second thickness (T2) that deviates from the first thickness (T1), wherein the first thickness (T1) and the second thickness (T2) are measured in a direction perpendicular to the first surface (105) of the first semiconductor body (101), and wherein the thickness within the first region (A1) as well as within the second region (A2) is substantially uniform.

14. A method as claimed in Claim 13, wherein the insulating layer (320) of the first semiconductor body (101) comprises substantially the same material as the oxide regions (350) to be formed at a later stage, so as to enable the insulating layer (320) and the oxide regions (350) to be selectively removed in one step.

15. A method as claimed in Claim 6, wherein the first semiconductor body (101) comprises an insulating layer (120) which is situated between the active part (130) and the substrate part (110) of the first semiconductor body (101), and wherein, after the step of removing the substrate part (110) from the first semiconductor body (101), the insulating layer (120) is removed.

16. A method as claimed in Claim 6, wherein the first semiconductor body (101) comprises a germanium-containing layer which is situated between the active part (130) and the substrate part (110) of the first semiconductor body (101), and wherein, after the step of removing substrate part (110) from the first semiconductor body (101), the germanium-containing layer is removed.

17. A method as claimed in Claim 6 or 13, characterized in that the process of bonding together the first and the second semiconductor body (201) includes the following sub-steps:

providing the further insulating layer (220) on the first surface (105) of the first semiconductor body (101);

providing the second semiconductor body (201) with a second surface (205);

bringing the first surface (105) of the first semiconductor body (101) into contact with the second surface of the second semiconductor body (201); and

bonding together the first semiconductor body (101) and the second semiconductor body (201) by means of "fusion bonding".

18. A method as claimed in Claim 6 or 13, characterized in that bonding together the first and the second semiconductor body (201) includes the following sub-steps:

providing the second semiconductor body (201) with a second surface, the further insulating layer (220) being present at the second surface;

bringing the first surface (105) of the first semiconductor body (101) into contact with the second surface of the second semiconductor body (201), and

bonding together the first semiconductor body (101) and the second semiconductor body (201) by means of "fusion boding".

19. A method as claimed in any one of Claims 10 through 13, characterized in that the masking layer (140) and the implantation (199) are provided in such a manner that the thickness (T1, T2, T3) of one of the regions (A1, A2, A3) of the resulting active part (130) is less than 10 nanometers.

20. A method as claimed in any one of Claims 10 through 13, characterized in that at the location of each of the regions (A1, A2, A3) at least one transistor (N1, N2, N3) is provided in the active part (130).

21. A method as claimed in Claim 4, characterized in that the masking layer (140A, 140 B) is provided so as to have a stepped profile.

22. A method as claimed 21, characterized in that more than one mask is used during application of the masking layer (140A, 140B).

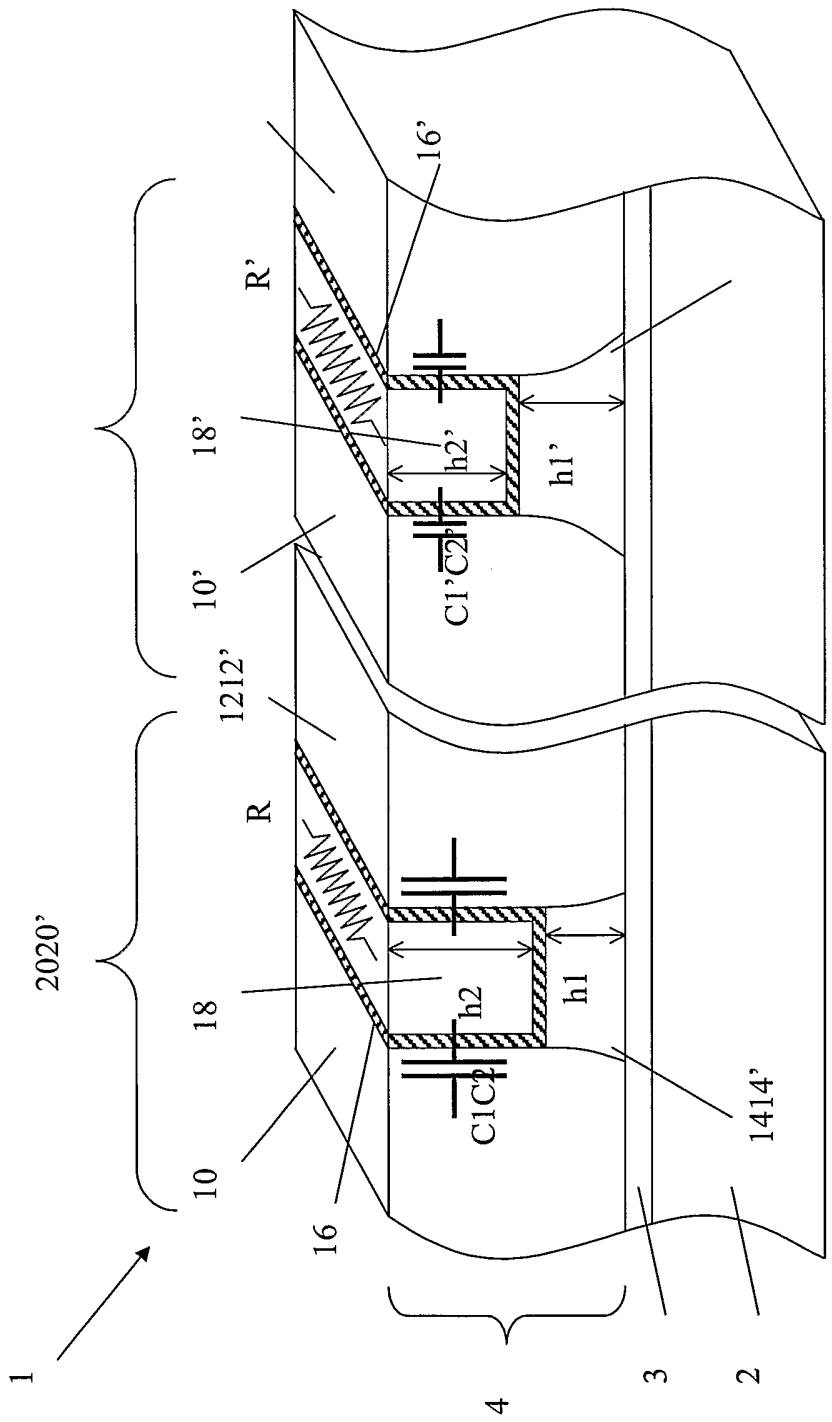
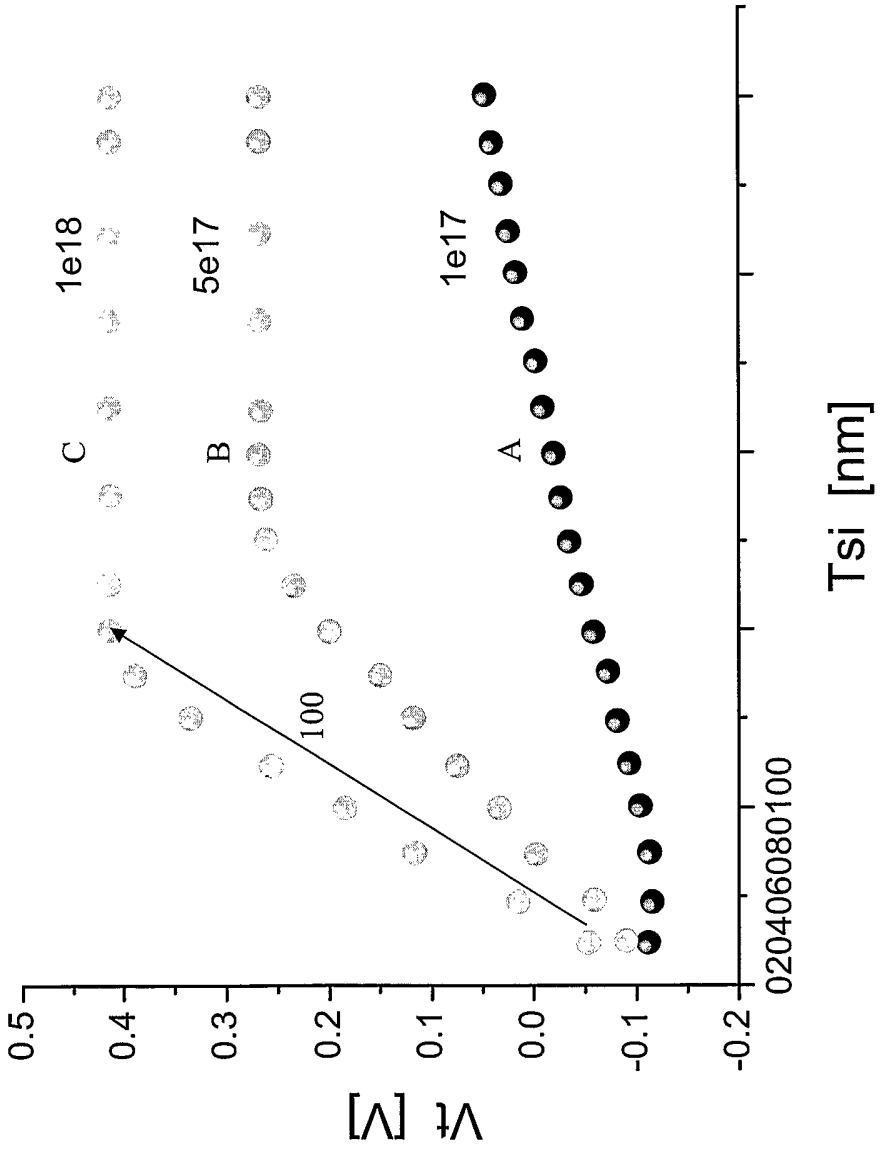


Fig. 1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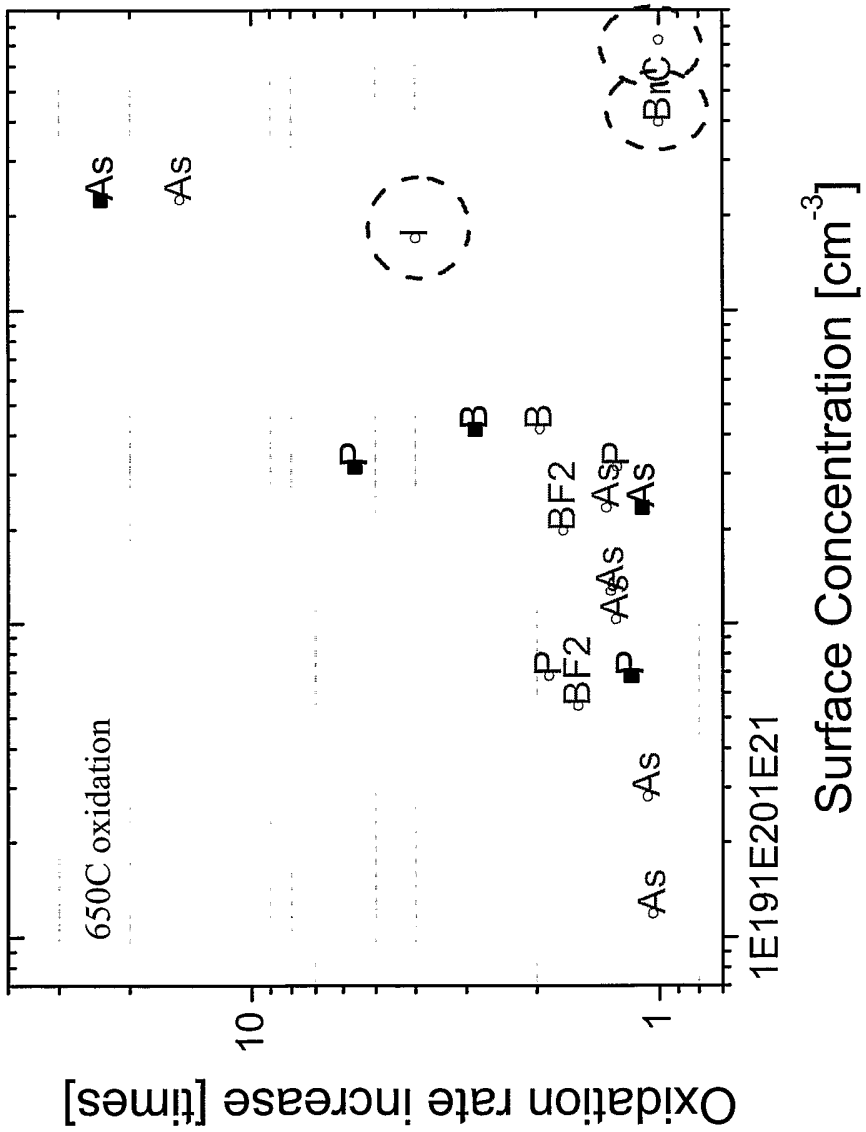
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
0
20
40
60
80
100
Tsi [nm]
1e18
5e17
1e17
C
B
A
100

Fig. 2


650C oxidation
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As
P
B
B
BF2
P
BF2
As
As
P
As
As
As
P
B
C
1E19
1E20
1E21
10
1
Oxidation rate increase [times]
Surface Concentration [cm-3]

Fig. 3

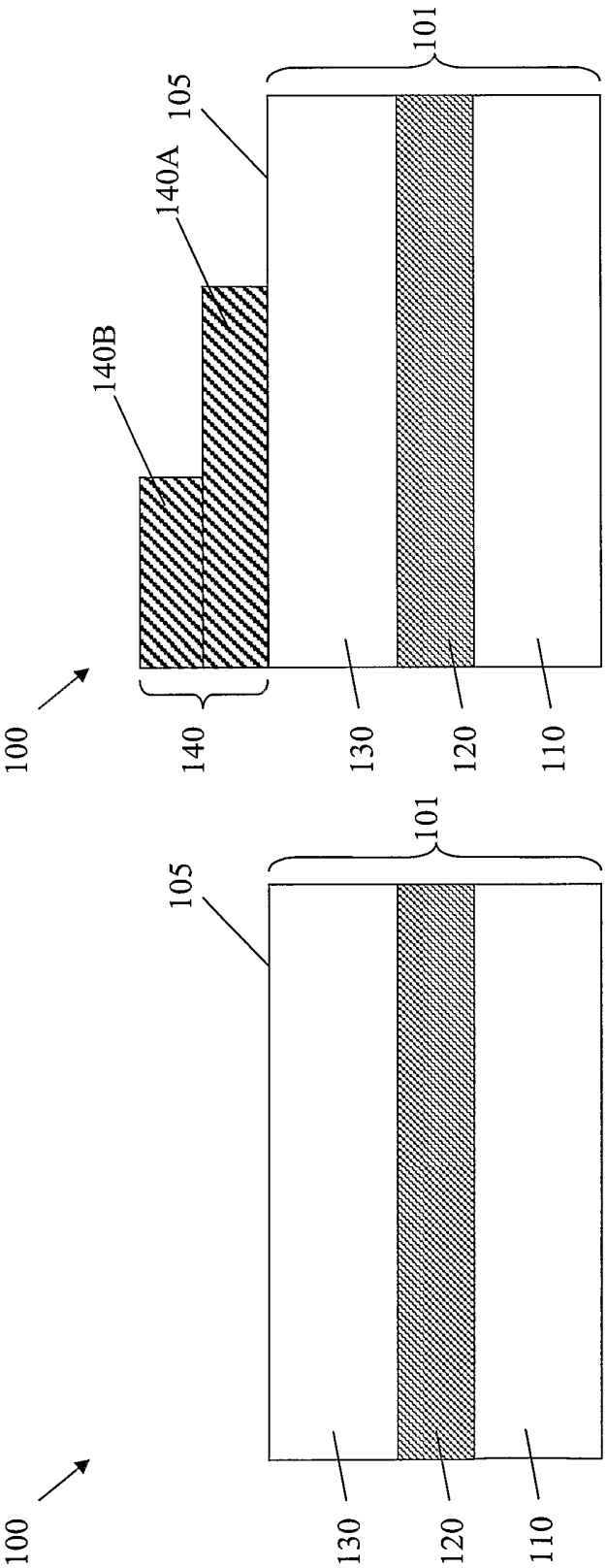


Fig. 5

Fig. 4

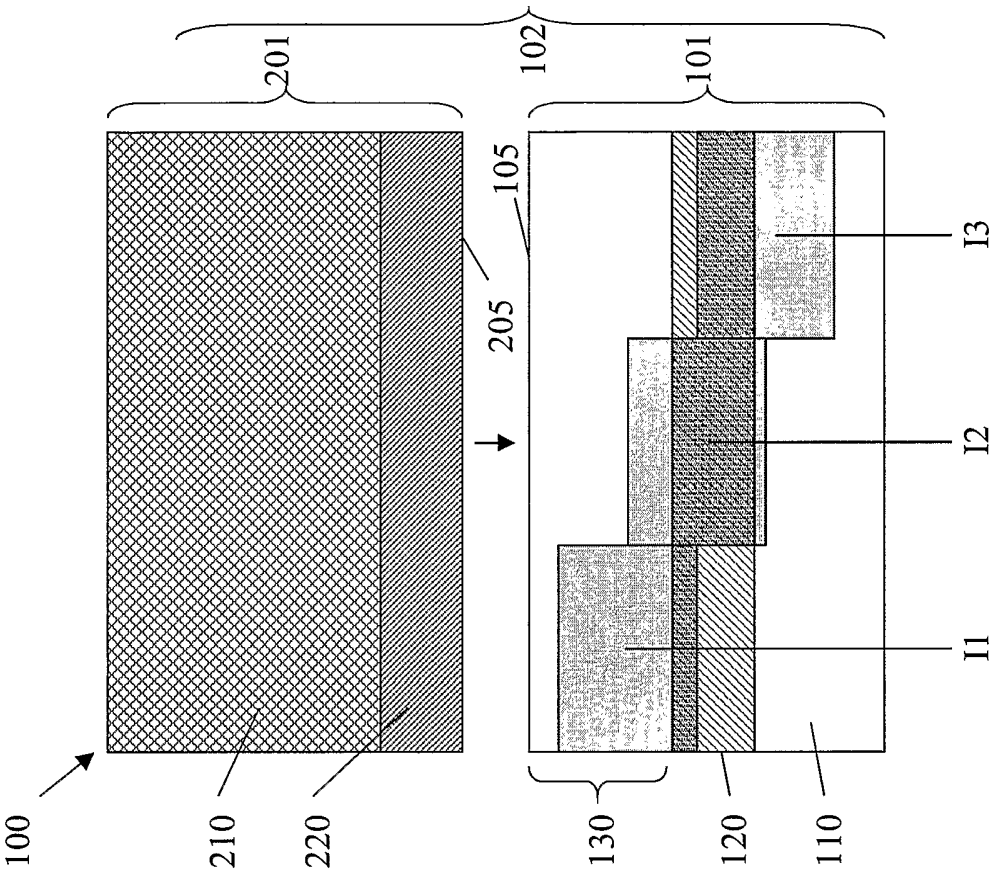

201
102
101
105
205
I3
I2
I1
100
210
220
130
120
110

Fig. 7

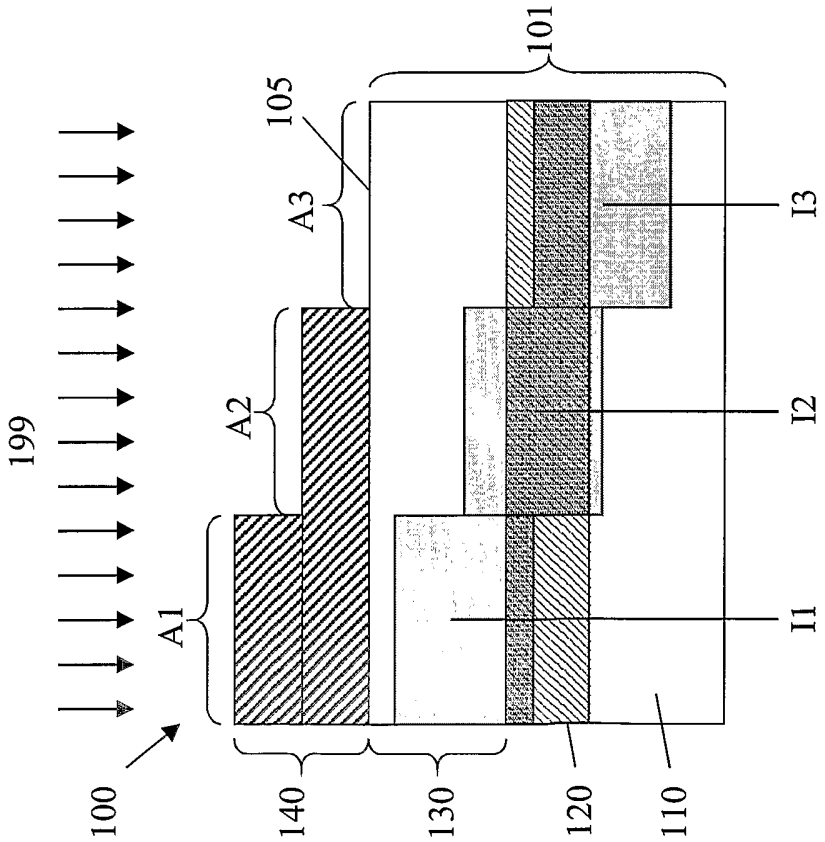

101
105
A3
A2
A1
199
I3
I2
I1
100
140
130
120
110

Fig. 6

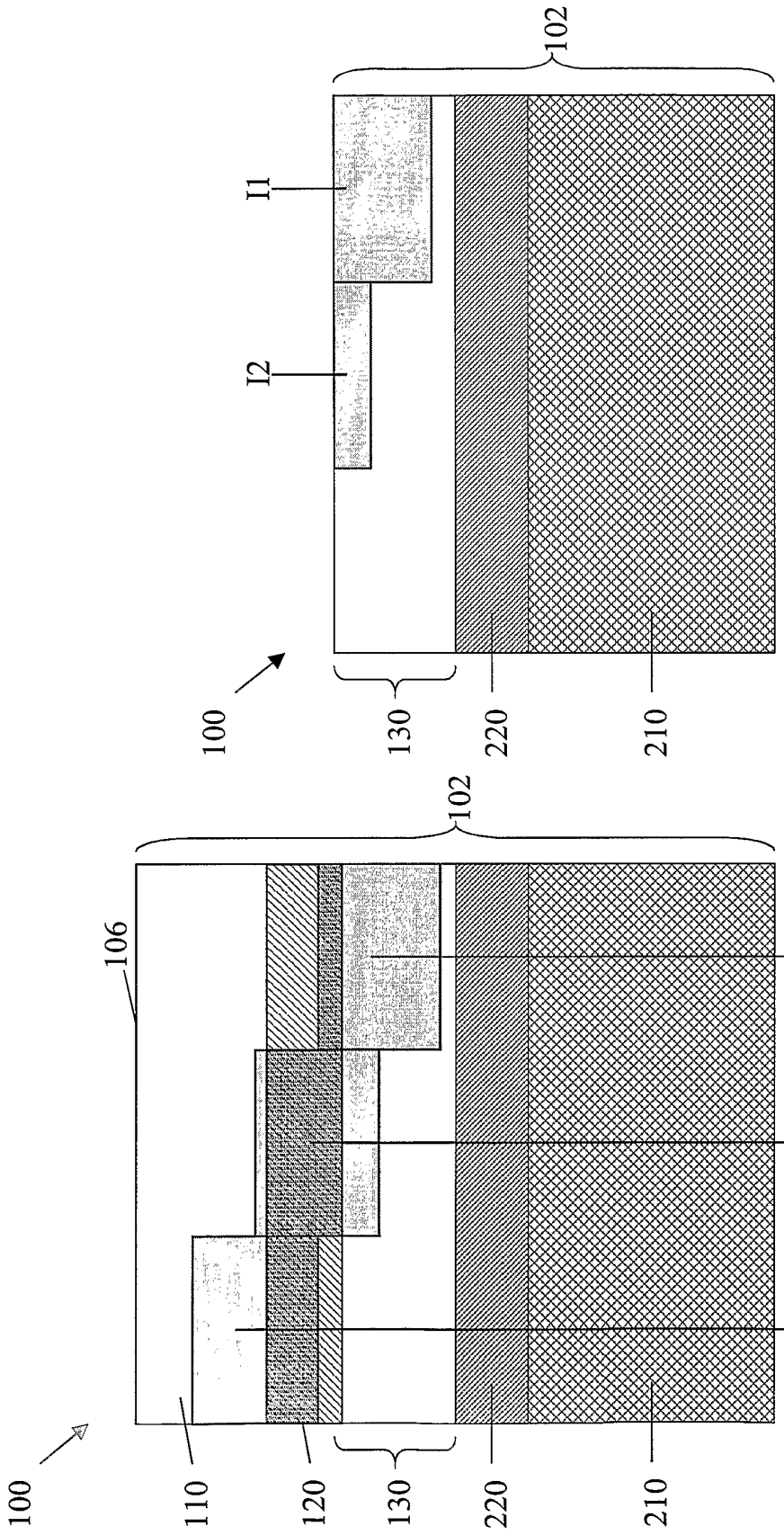


Fig. 9

Fig. 8

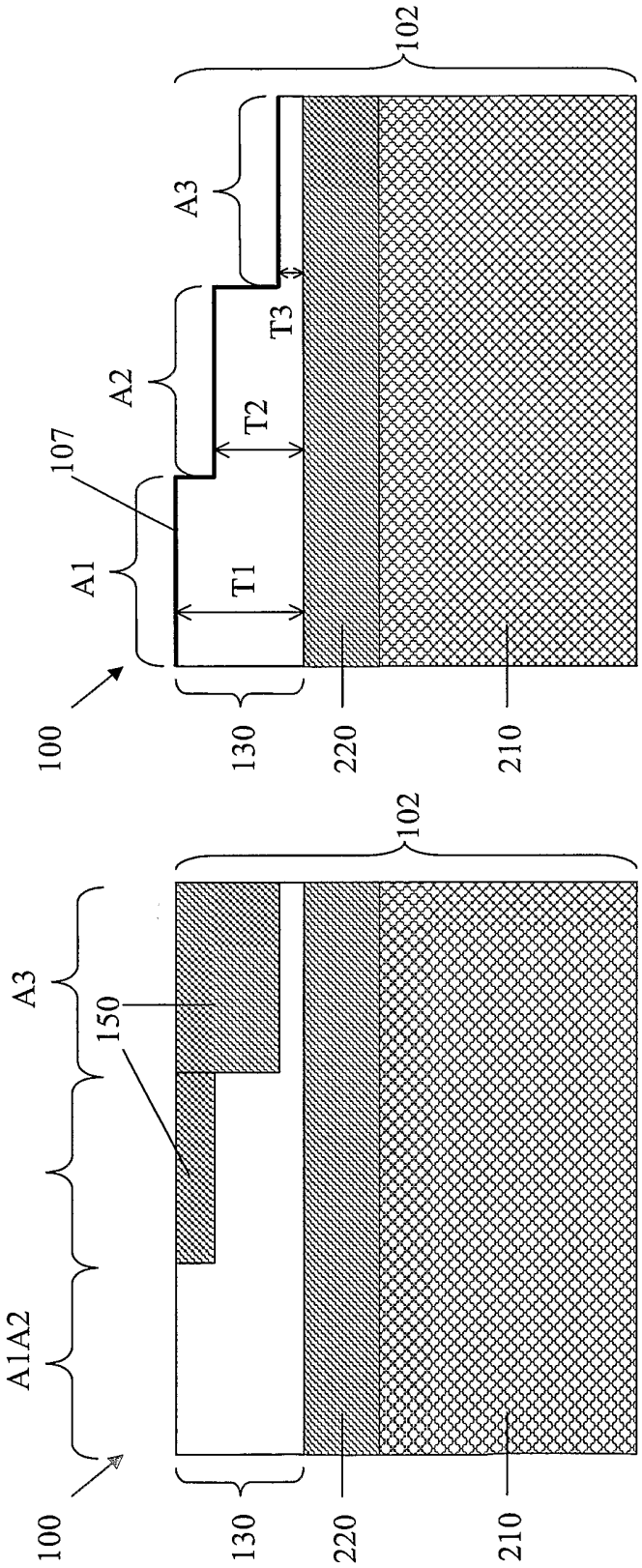
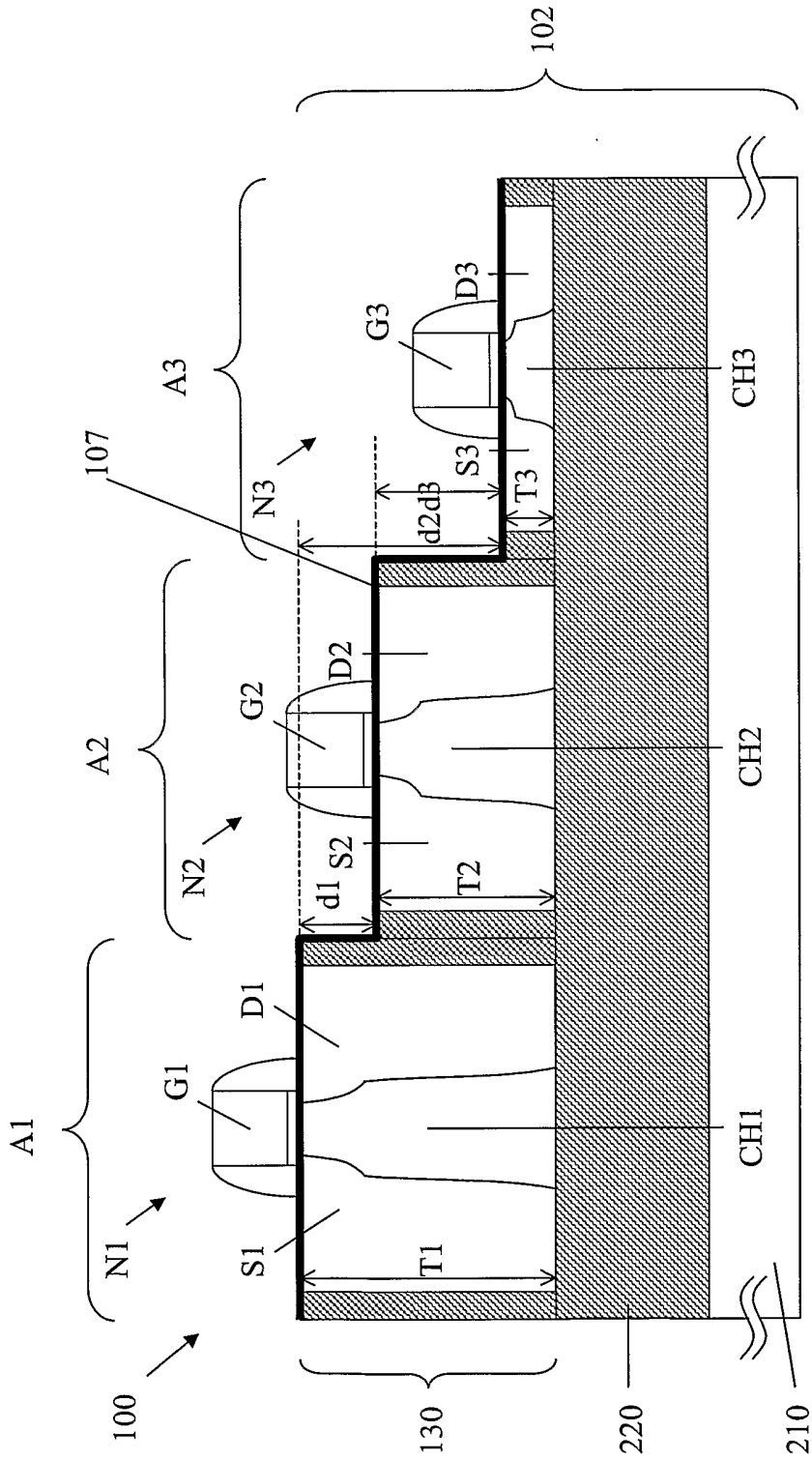

102
A3
150
A1A2
100
130
220
210

Fig. 10

102
A3
T3
A2
T2
107
A1
T1
100
130
220
210

Fig. 11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A2
A1
107
N3
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G3
D3
S3
T3
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G2
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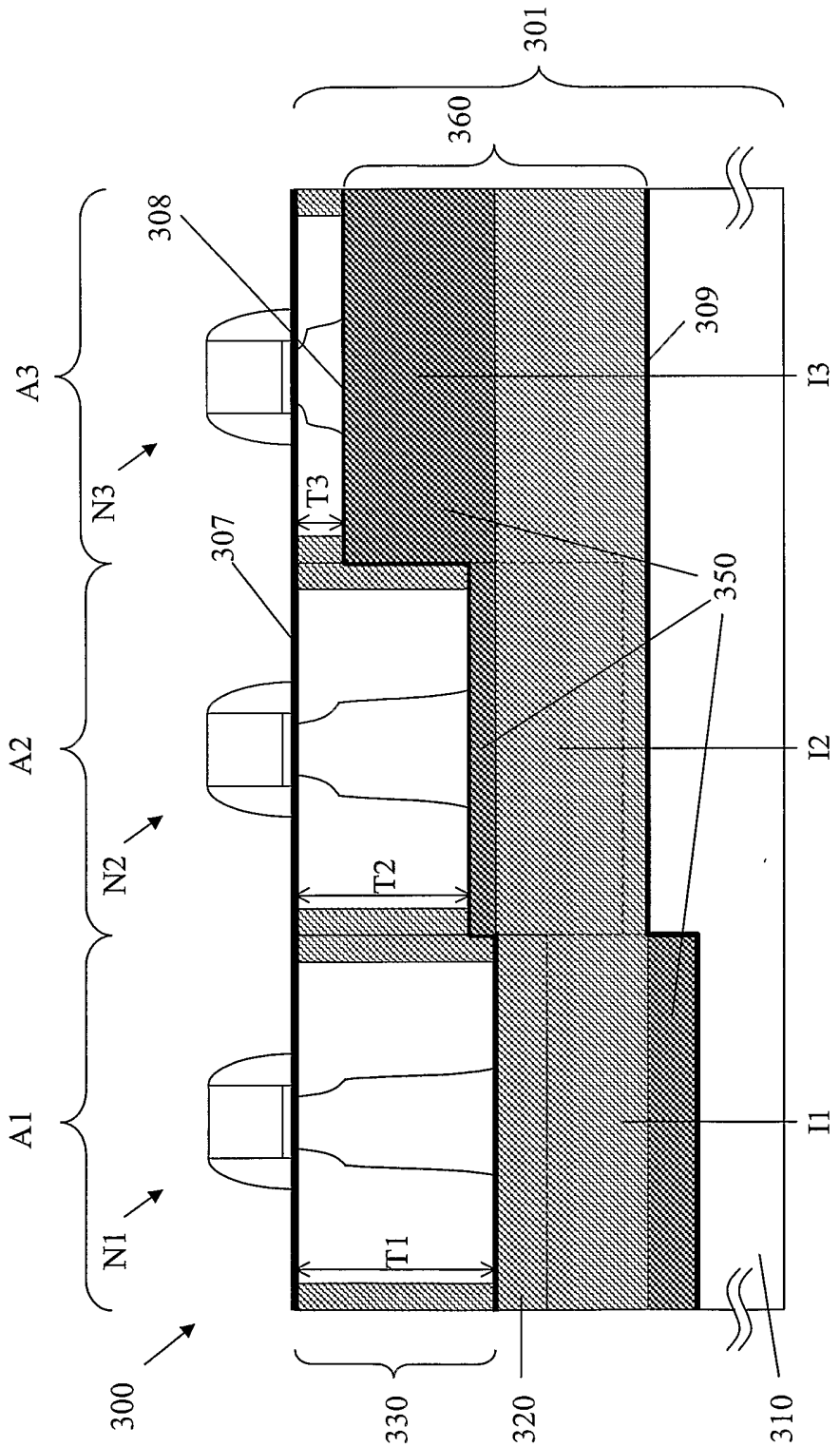
S2
T2
d1
G1
D1
S1
T1
CH3
CH2
CH1
130
220
210

Fig. 12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N3
T3
307
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A2
N2
T2
I3
I2
I1
A1
N1
T1
300
330
320
310

Fig. 13

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2005/053215

A. CLASSIFICATION OF SUBJECT MATTER
H01L29/786 H01L21/336 H01L29/06 H01L27/12 H01L21/84

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/071308 A1 (YOSHIDA MASAHIRO) 17 April 2003 (2003-04-17) page 3, paragraph 45 - page 4, paragraph 52; figures 3A-E	1-5,12, 21,22
Y		6-11, 13-20
Y	EP 1 006 567 A (CANON KABUSHIKI KAISHA) 7 June 2000 (2000-06-07) page 3, paragraph 15 - page 5, paragraph 30	6-11, 13-20
X	US 6 197 697 B1 (SIMPSON TODD WILLIAM ET AL) 6 March 2001 (2001-03-06) figures 1A-E	4,5,8, 11,21,22

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 January 2006	26/01/2006

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Hoffmann, N

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 764 917 B1 (CHAN DARIN A ET AL) 20 July 2004 (2004-07-20) the whole document	1-3
X	US 2001/005030 A1 (IMAI KIYOTAKA) 28 June 2001 (2001-06-28) figures 2E,3F	1-3
X	US 2004/169226 A1 (OYAMATSU HISATO) 2 September 2004 (2004-09-02) figures 4,10,11,13	1-3
X	US 2002/180069 A1 (HOUSTON THEODORE W) 5 December 2002 (2002-12-05) figure 5	1-3
A	US 2001/015256 A1 (YAMAZAKI SHUNPEI ET AL) 23 August 2001 (2001-08-23) page 1, paragraph 10	16
A	EP 0 731 387 A (SAMSUNG ELECTRONICS CO., LTD) 11 September 1996 (1996-09-11) the whole document	4,21,22

1

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2005/053215

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003071308 A1	17-04-2003	JP 2003124345 A	25-04-2003
EP 1006567 A	07-06-2000	CN 1259758 A	12-07-2000
		JP 2000349264 A	15-12-2000
		KR 2000047925 A	25-07-2000
		SG 74757 A1	22-08-2000
		TW 463223 B	11-11-2001
		US 2003159644 A1	28-08-2003
US 6197697 B1	06-03-2001	CA 2246084 A1	28-02-2000
US 6764917 B1	20-07-2004	AU 2002357367 A1	09-07-2003
		CN 1606807 A	13-04-2005
		DE 10297583 T5	11-11-2004
		GB 2407703 A	04-05-2005
		JP 2005514770 T	19-05-2005
		WO 03054966 A1	03-07-2003
US 2001005030 A1	28-06-2001	NONE	
US 2004169226 A1	02-09-2004	NONE	
US 2002180069 A1	05-12-2002	US 6424016 B1	23-07-2002
US 2001015256 A1	23-08-2001	TW 490717 B	11-06-2002
EP 0731387 A	11-09-1996	JP 8250446 A	27-09-1996
		KR 161389 B1	15-01-1999