United States Patent

Wood

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[54] **QUERY AND RESPONSE SYSTEM WITH AUDIO MESSAGE SYNTHESIZING**

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[52] **U.S. Cl.**.....**340/152 R,** 179/1 SA, 179/15 AC

[51] **Int. Cl.**.....**H04m 11/08**

[58] **Field of Search**..179/1 VC, 1 SA, 2 DP, 15 AW, 179/15 AS, 15 AC, 15.55; 178/5.6, 23, 50; 340/152, 153, 154

[56] **References Cited**

UNITED STATES PATENTS

3,534,171	10/1970	Shepard et al.	340/152 X
3,400,392	9/1968	Willcox et al.	340/152 X
3,253,263	5/1966	Lee et al.	340/154 X
3,278,907	10/1966	Barry et al.	179/15 AC

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[57] **ABSTRACT**

A query and response system embodying an audio response generator for synthesizing audio messages responsive to subscriber queries, said audio response generator comprising an audio memory unit for storing data in analog form regarding a plurality of speech words, means for converting audio outputs from the memory to digital form, multiplexer and demultiplexer means controlled by data from a computer for distributing word data to individual subscriber output channels to provide responses to subscriber queries, and means for converting the demultiplexer output from digital back to audio form for supply to subscribers. In one form of the invention means are provided for supplying either audio response or a response capable of actuating a teletype printer to each subscriber output channel as desired.

8 Claims, 11 Drawing Figures

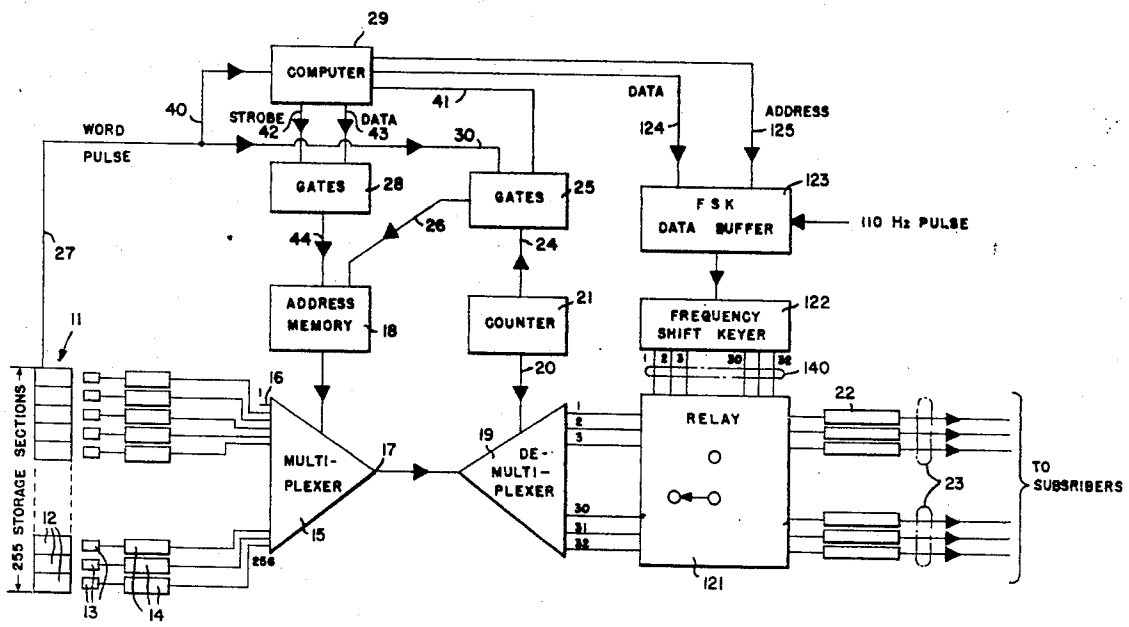
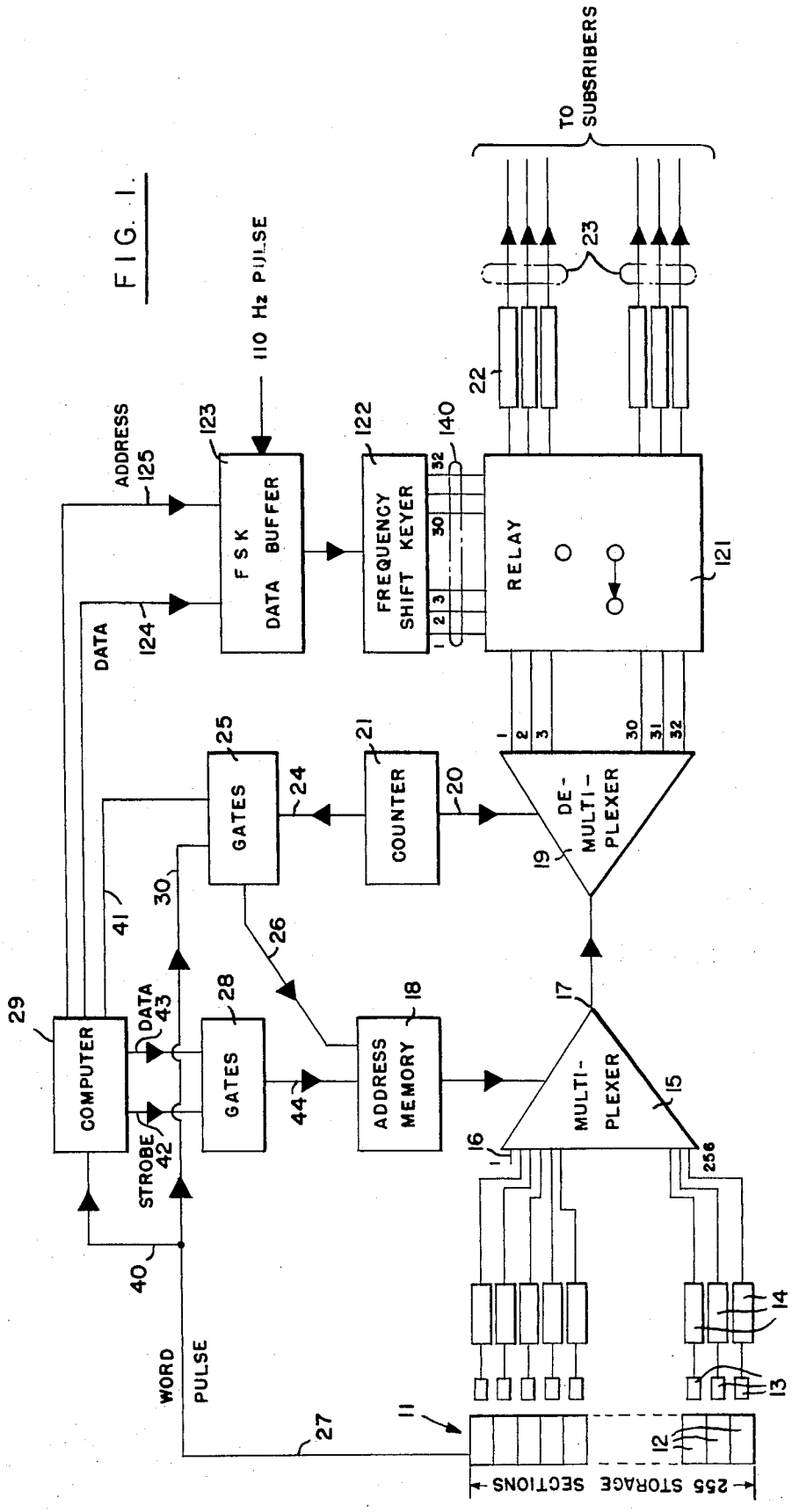


FIG. 1.


TO SUBSCRIBERS
23
22
110 Hz PULSE
ADDRESS
125
123
FSK DATA BUFFER
122
FREQUENCY SHIFT KEYER
140
32
30
3
2
1
RELAY
121
DATA
124
1
2
3
30
31
32
25
GATES
24
21
COUNTER
20
DE-MULTI-PLEXER
19
30
41
26
29
COMPUTER
DATA
43
28
GATES
18
ADDRESS MEMORY
17
MULTI-PLEXER
15
STROBE
42
44
16
1
256
40
WORD PULSE
27
11
12
14
13
255 STORAGE SECTIONS

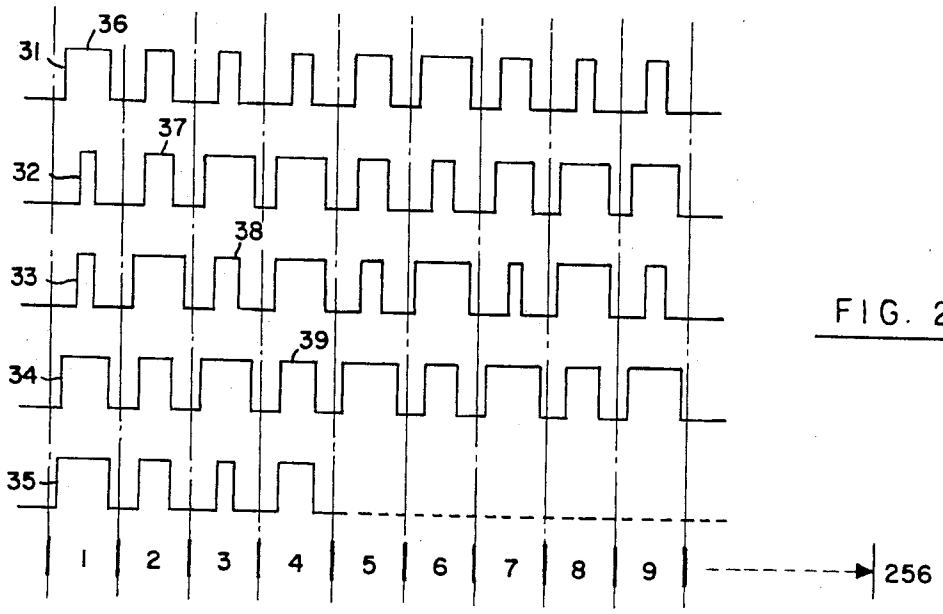


FIG. 2.

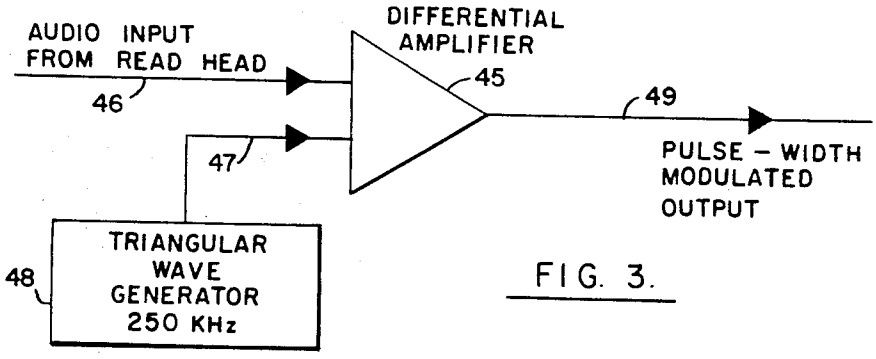


FIG. 3.

FIG.4a

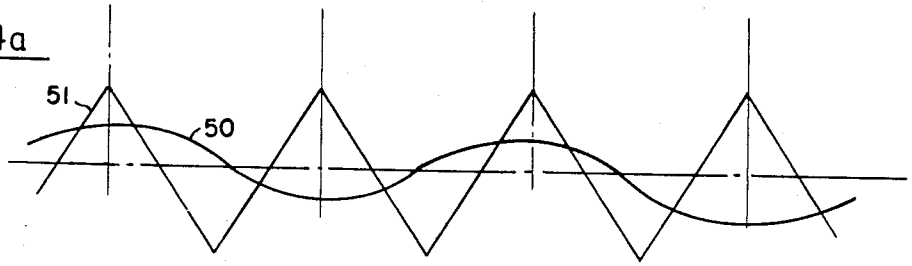
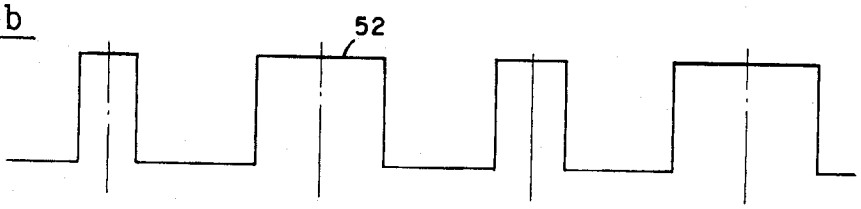


FIG.4b



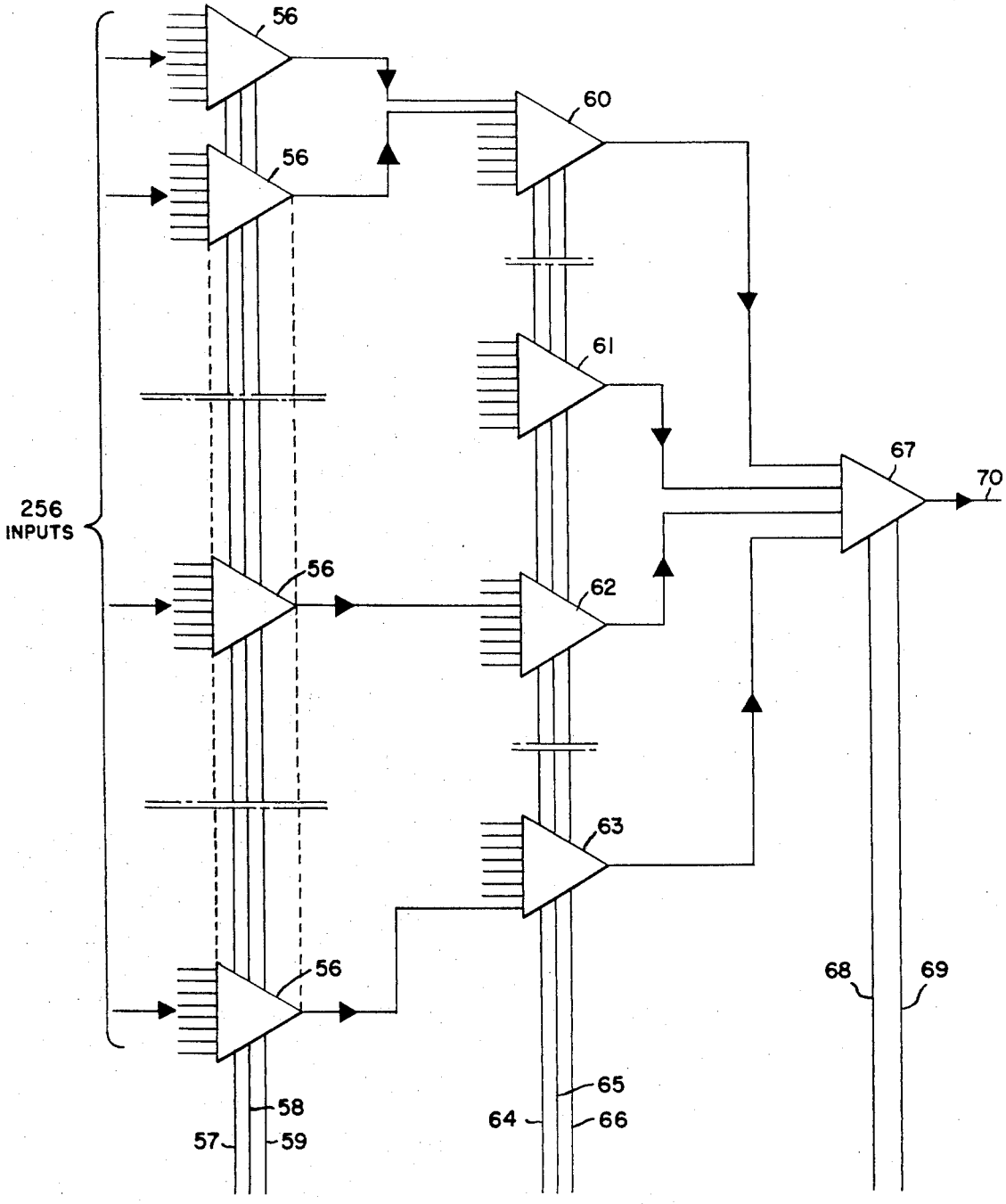


FIG. 5.

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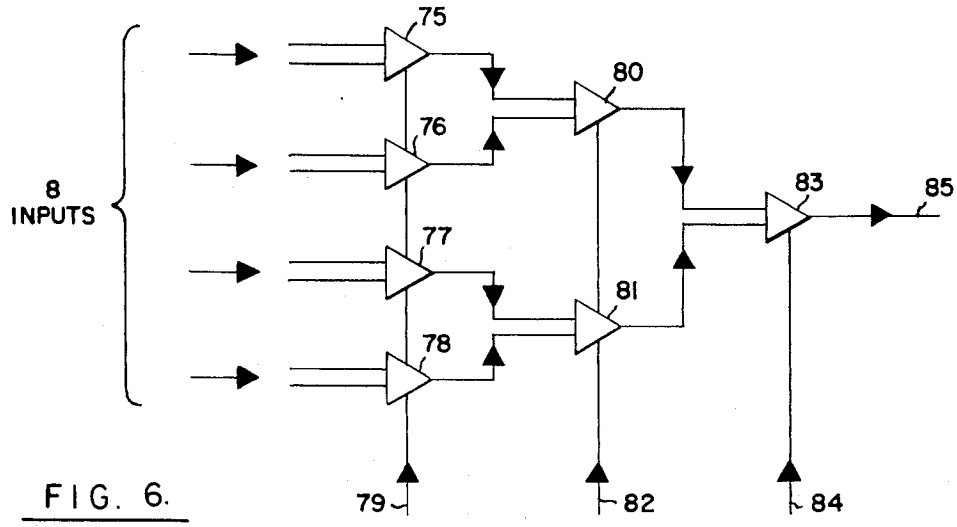


FIG. 6.

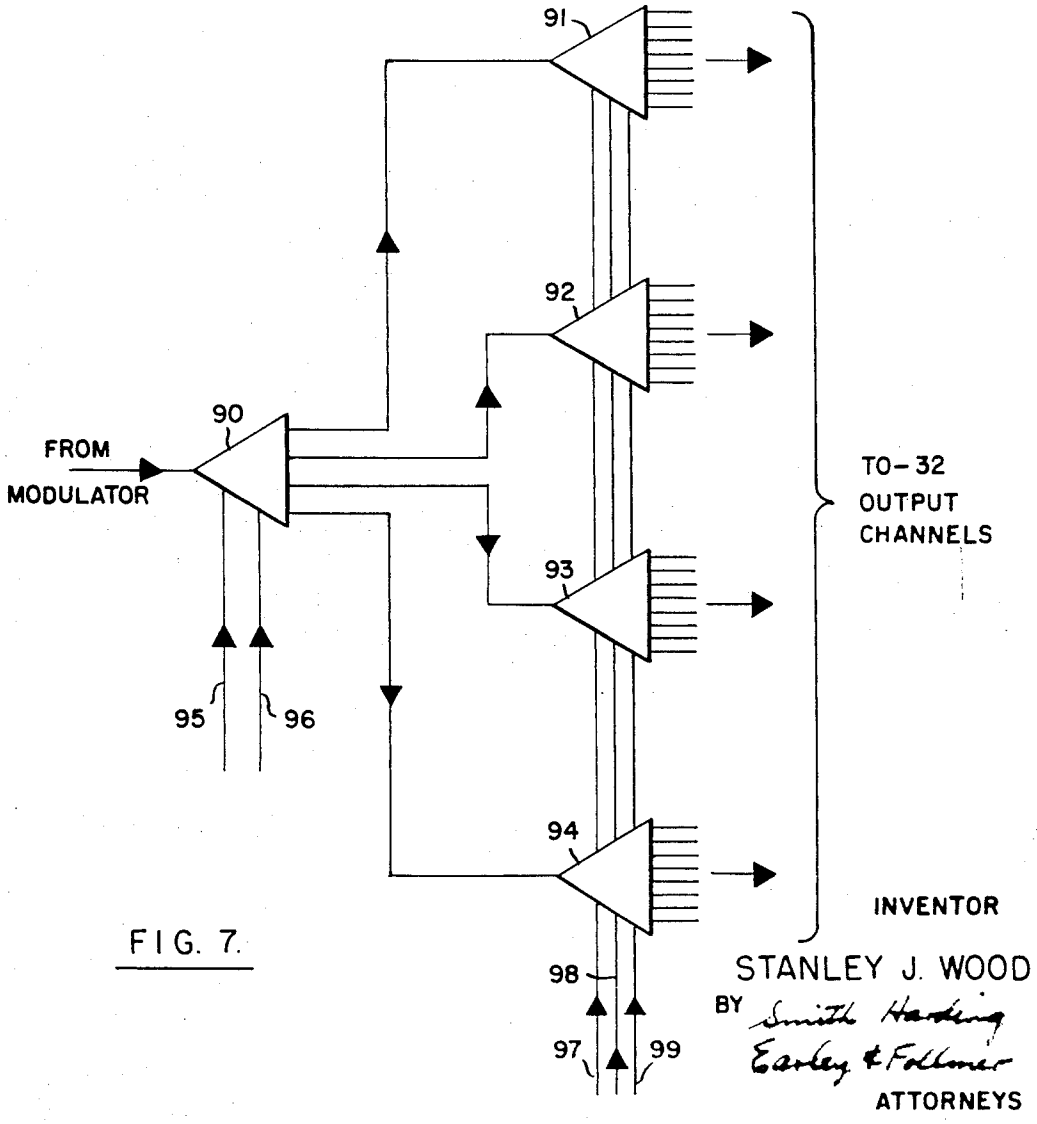


FIG. 7.

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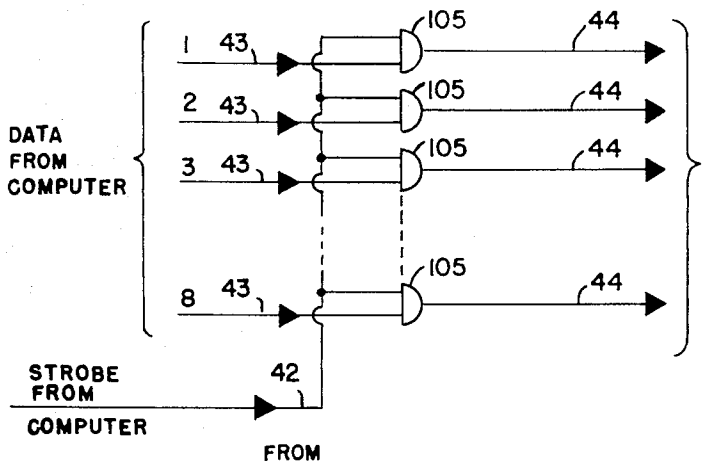


FIG. 8.

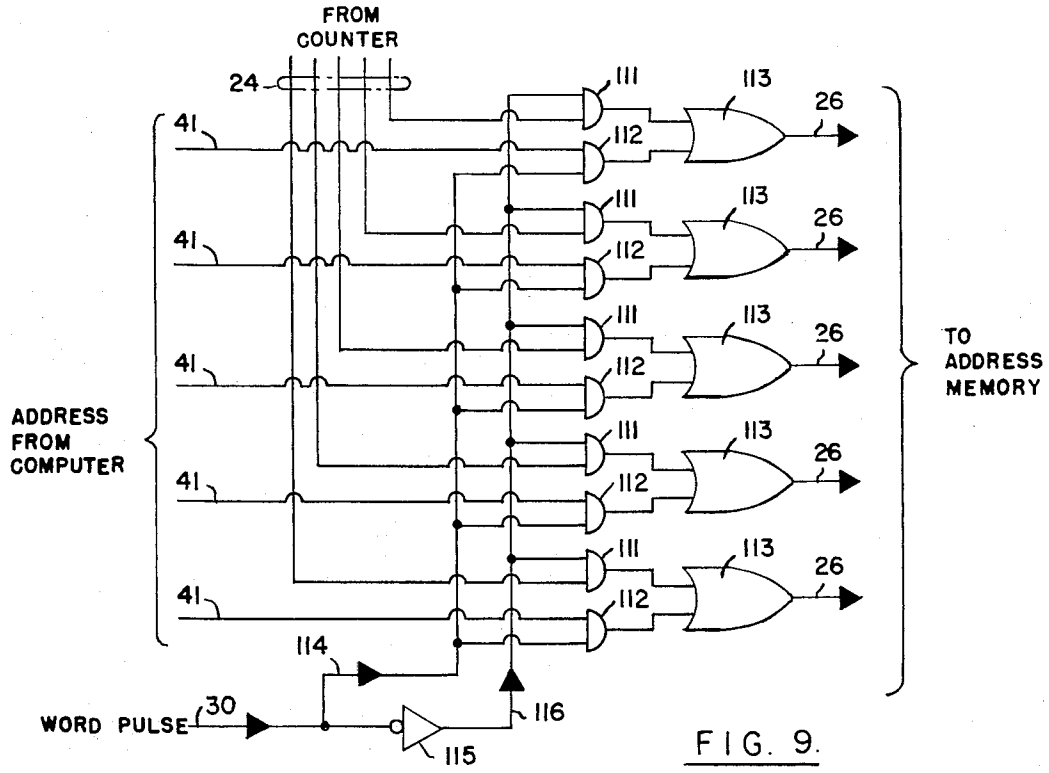


FIG. 9.

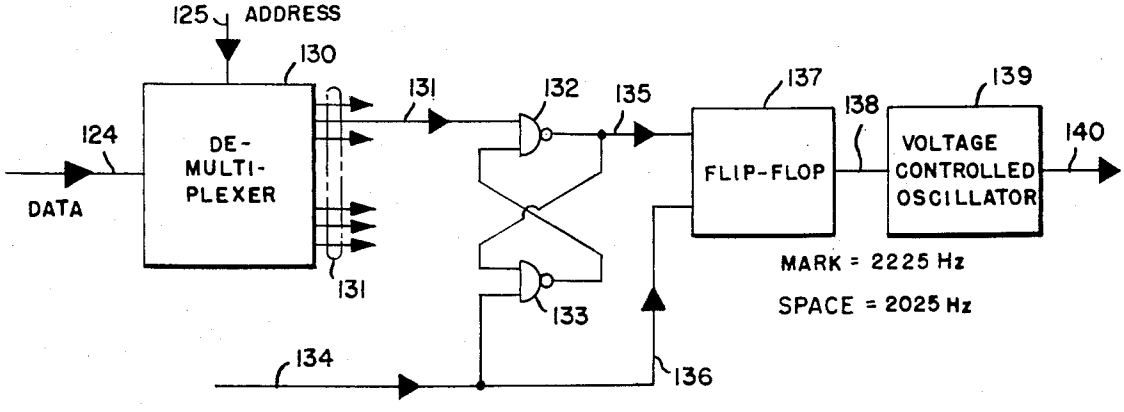


FIG. 10.

QUERY AND RESPONSE SYSTEM WITH AUDIO MESSAGE SYNTHESIZING

This invention relates to an audio response generator for synthesizing audio messages under control of digital data. Systems are known in which a centrally located computer may be interrogated by a remote subscriber to provide answers to questions presented by the subscriber. Specifically, systems are known in which the subscriber uses the push buttons on a touch-tone telephone set to encode his query which is then transmitted to the centrally located computer over the telephone lines. At the computer location, the tone signal produced by the touch-tone telephone set is converted to digital form and used to interrogate the computer. The output from the computer, in digital form, is desirably converted to audio form for transmission to the subscriber by means of a speech synthesizer. Such a synthesizer may comprise a memory for storing a vocabulary of words needed to synthesize replies to questions which are expected to be presented to the computer, together with means responsive to the digital output from the computer for selecting sequentially the desired word data from the memory for synthesizing an audio signal representative of the desired response. In known systems, the word data, which normally is stored in analog form in the audio memory, has been processed in analog form using relays or solid state circuitry. This mode of processing the word data has not been proven entirely satisfactory. The present invention relates to improved means for processing the word data to synthesize audio messages, in which the word data, which is stored in analog form, is first converted to digital form and is then processed, using known forms of multiplexers and demultiplexers controlled in response to digital data from the computer, to produce simultaneously in a plurality of output channels a plurality of messages in digital form, each responsive to a query to the computer from a different subscriber. Each of these digital outputs then may be converted to analog form to provide an audio response for transmission to a subscriber over telephone lines.

According to the invention, audio data representative of a plurality of speech words needed to synthesize replies to queries which are expected to be presented to a computer are individually stored in a memory having a separate output for data regarding each word stored in the memory. For example, the memory may comprise a standard form of magnetic drum memory comprising, for example, **255** storage sections, each having recorded therein data regarding a different word. Each section is provided with a conventional read head for reading out audio data representative of a word stored in that section. The output of each read head is supplied to a separate pulse width modulator for converting the amplitude-modulated audio information into a series of width-modulated pulses recurrent at a frequency of, for example, 250 kilohertz. The outputs of each of the 255 pulse width modulators is supplied to a different input of a time division multiplexer which operates to convert the individual input signals into a single output signal comprising successively occurring width-modulated pulses, each occupying a 4-microsecond time slot and each representative of one of the 255 words stored in the magnetic drum memory. The multiplexer is of a form adapted to be controlled in response to digital address data supplied to it to select

the output from any one of the 255 pulse width modulators and supply it to the output of the multiplexer during any 4-micro=second time interval. Its capacity is such that, during each of a cycle of 256 successive 4-microsecond time slots, the output signal from the multiplexer may contain a width-modulated pulse from a different pulse width modulator, and one slot may contain no pulse — i.e., it may be representative of silence. Alternatively the multiplexer may be controlled so that each of the 256 slots in a cycle is occupied by a pulse from the output of any selected pulse width modulator designated by the digital address information. If desired, all of the slots in a cycle may be occupied by the output from a single pulse width modulator — i.e., the information contained in each slot may be representative of the same word — or the slots may contain output from none of the pulse width modulators, thereby representing silence. Normally, unless address data has been supplied to the multiplexer designating a particular word, no pulse-width-modulated information will be supplied to the output of the multiplexer, and the output will be representative of silence.

The output from the multiplexer is supplied to the input of a demultiplexer having a single input and a plurality of outputs, e.g. 32, for supplying responses to a corresponding number of subscriber output lines. Like the multiplexer, the demultiplexer is of a form adapted to be controlled in response to digital information to effect a connection of its input to any one of a plurality of 32 outputs. In accordance with the invention it may be supplied with digital information from a counter circuit to cause its input to be connected successively and cyclically to each of the 32 outputs in a predetermined sequence during successive intervals of 4 microseconds duration. At the same time, the multiplexer is supplied with correlated digital information such as to cause the pulse-width-modulated data supplied to its output during a given 4-microsecond time slot to be representative of the speech word which it is desired to supply to that output channel of the demultiplexer to which the input of the demultiplexer is at that time connected. The individual outputs of the demultiplexer being in width-modulated form, each output is supplied to a separate demodulator for converting it back into audio form for use by individual subscribers.

Further in accordance with the invention, the digital data for controlling the operation of the multiplexer is supplied to it from a memory unit in which the required data is stored prior to each cycle of operation of the system. The commencement of this storage period, which may occupy **25** milliseconds, is initiated in response to a "word pulse" from the audio memory drum indicating that a new period of rotation of the drum is about to begin. This word pulse actuates gates which control the supply to the memory of data from a computer indicative of the addresses of word information to be supplied to the specific output channels for responding to subscriber's queries. Following this storage period, and during the normal operating cycle of the audio response generator, data from the same counter which controls the operation of the demultiplexer also is supplied through suitable gates to the address data memory to control the supply of address data to the multiplexer and thereby coordinate the

operation of the multiplexer with the operation of the demultiplexer so as to cause the desired word information to be supplied to the various output channels.

The invention will be understood more fully from a consideration of the following detailed description with reference to the accompanying drawings in which:

FIG. 1 is a block diagram of an embodiment of the invention;

FIG. 2 is a series of waveforms which will be referred to in explaining the operation of the arrangement of FIG. 1;

FIG. 3 is a block diagram showing a form of pulse width modulator suitable for use in the arrangement of FIG. 1;

FIGS. 4*a* and 4*b* are a series of waveforms which will be referred to in explaining the operation of the pulse width modulator of FIG. 3;

FIG. 5 is a block diagram showing the details of a multiplexer suitable for use in the arrangement of FIG. 1;

FIG. 6 is a block diagram of a multiplexer suitable for use as a component of the multiplexer shown in FIG. 5;

FIG. 7 is a bock diagram showing the details of a demultiplexer suitable for use in the arrangement of FIG. 1;

FIG. 8 shows the details of the gate 28 in the arrangement of FIG. 1;

FIG. 9 shows the details of gate 25 of the arrangement of FIG. 1;

FIG. 10 shows the details of the FSK data buffer 123 and frequency shift keyer 122 of FIG. 1.

Referring now to FIG. 1, there is shown a magnetic drum memory 11 having 255 storage sections, in each of which is stored data regarding a different speech word which may be required to respond to queries presented to a computer. The data may be stored in standard amplitude-modulated analog form and data regarding the same word may be stored several times (e.g., three times) in each section depending upon the storage capacity thereof. Typically, the drum may rotate at a rate of once every 0.5 to 0.6 seconds. Each section has associated with it a read head 13 for continuously deriving an amplitude modulated signal representative of the word data stored in that section. The read heads may be of more or less conventional form, except that preferably they may be provided with preamplifiers for raising the level of their outputs, for example, to approximately 2 volts peak-to-peak. The output of each read head is supplied to a separate one of a plurality of (255) pulse width modulators 14 which may be of the form described hereinafter with reference to FIG. 3. Each of the pulse width modulators 14 operates to convert the analog output of one of the read heads 13 to a pulse-width-modulated signal comprising pulses recurrent at a frequency of, for example, 250 kilohertz whose widths are varied in response to the amplitude variations of the audio signal supplied from read head 13.

The pulse-width-modulated output from each of the pulse width modulators 14 is supplied to a separate input of multiplexer 15 which is provided with 256 inputs to accommodate the outputs from the 255 pulse width modulators 14 and having one additional input, to which no signal is supplied, and which is therefore representative of silence. Multiplexer 15 is provided with a single output 17 and is adapted to be controlled in response to digital address information supplied to it from address memory 18 to connect selected ones of its inputs to its output 17 as dictated by data from address memory 18. The construction and operation of multiplexer 15 is more fully explained hereinafter with reference to FIGS. 5 and 6. The output 17 of multiplexer 15 is connected to the input of demultiplexer 19 which is adapted to be controlled in response to digital information supplied to it through connection 20 from counter 21 to connect its input to selected ones of its 32 outputs. Each of the 32 outputs of demultiplexer 19 is connected to the input of a relay 121 which may be actuated to connect those outputs to the respective inputs of demodulators 22 for converting the pulse-width-modulated outputs of demultiplexer 19 to amplitude modulated audio signals for supply through separate output lines 23 to individual subscribers. Demodulators 22 comprise merely high pass filters with cut off frequencies at approximately 4 kilohertz for eliminating the fundamental components of the pulse with modulated signals and for passing only the modulation components thereof.

Alternatively, instead of supplying the outputs of demultiplexer 19 to the inputs of demodulators 22, relay 121 may be actuated to supply to output lines 23 a signal suitable for actuating a teletype printer in the event that such capability is preferred to the audio response under certain circumstances. The teletype signal is supplied to the inputs of relay 121 from a frequency shift keyer 122 which operates under control of frequency shift keyer data buffer 123. This data buffer in turn is controlled in response to word data and address data supplied to it from computer 29 through connections 124 and 125 respectively and a 110 hertz pulse signal supplied to it through connection 126 from a suitable source. The operation of the frequency shift keyer data buffer 123 and frequency shift keyer 122 will be explained more fully hereinafter with reference to FIG. 10.

The digital-information supplied to demultiplexer 19 from counter 21 may be such as to cause the input of demultiplexer 19 to be connected successively to its outputs during successive intervals, each of four-microsecond duration. The same digital information is supplied from counter 21 through connection 24, gates 25 and connection 26 to address memory 18 to cause memory 18 to supply to multiplexer 15, during successive time intervals, each of 4-microsecond duration, address information indicative of the particular word stored in audio memory 11 which it is desired to supply to the particular output line of demultiplexer 19 to which its input is then connected.

The operation of multiplexer 15 will be understood more fully by reference to the diagram of FIG. 2. As hereinbefore mentioned, the output from each of the pulse width modulators 14 comprises a train of pulses recurrent at a 250 kilohertz rate and whose widths are modulated in accordance with variations in the amplitude of the audio information supplied to that modulator from its associated read head 13. Thus the waveforms shown at 31, 32, 33 and 34 in FIG. 2 may represent the outputs of four different pulse modulators 14 of FIG. 1, each having the width of its pulses varying in accordance with audio information

representative of a different word, and each successive pulse in each of the signals occupying a portion of a time slot of 4-microseconds' duration. The operation of multiplexer **15**, under control of the address data from memory **18**, will be to select individual pulses successively from the outputs of different ones of pulse width modulators **14** to produce a composite signal, as represented by waveform **35** in FIG. **2**, in which each one of 256 successive 4-microsecond time slots, as designated by the numerals 1–256 at the lower extremity of FIG. **2**, may be occupied by a pulse from the output of any one of the 255 pulse width modulators **14**, or by no pulse if it is desired to indicate a period of silence. Thus, as shown in FIG. **2**, the initial pulse occupying the first time slot in composite waveform **35** may correspond to the initial pulse **36** in waveform **31**, the pulse occupying the second time slot in waveform **35** may correspond to the second pulse **37** in waveform **32**, the third pulse in waveform **35** may correspond to the third pulse **38** in waveform **33**, and the fourth pulse in waveform **35** may correspond to the fourth pulse **39** in waveform **34**. The operation of demultiplexer **19** of FIG. **1** is essentially the reverse of that of multiplexer **14** in that it will operate, under control of the digital data supplied from counter **21**, to supply successive pulses from composite waveform of FIG. **2** to selected outputs of demultiplexer **19**.

Referring again to FIG. **1**, the information stored in address memory **18** for controlling the operation of multiplexer **15** is placed in memory **18** during an interval of 25 milliseconds' duration immediately preceeding the commencement of the audio response cycle. This action is initiated in response to a synchronizing impulse, called a word pulse, produced by the audio memory drum **11** and supplied through connections **27** and **40** to computer **29** to actuate the computer to supply, through connections **42** and **43**, to the inputs of gates **28** a strobe pulse for actuating the gates and data regarding specific words to be selected by multiplexer **15**. When gates **28** are actuated, the word data is supplied through them to address memory **18**. Gates **28** will be described more fully hereinafter with reference to FIG. **8**. The word pulse from audio memory drum **11** also is supplied through connections **27** and **30** to gates **25** which are supplied with address data from computer **29** through connection **41** and, through connection **24**, with output pulses from counter **21**. The word pulse actuates gates **25** to supply the address data under control of the pulses from counter **21** through connection **26** to address memory **18** to determine the storage locations of the word data supplied thereto through connection **44**. Gates **25** will be described more fully hereinafter with reference to FIG. **9**. Counter **21** may be of conventional form for generating successive pulses at a 250 kilohertz rate. Accordingly, no further description thereof is deemed necessary.

Referring now to FIG. **3**, there is shown one suitable form of the pulse width modulators **14** of FIG. **1**. Basically it comprises a differential amplifier **45** of conventional form, to one input **46** of which is supplied the audio input from one of the read heads **13** of FIG. **1**. This input will comprise audio frequencies ranging from 300 hertz to 4,000 hertz and is represented by the waveform **50** in FIG. **4***a*. The other input **47** to differential amplifier **45** is a triangular wave at a frequency of 250 kilohertz supplied from a generator **48** of a conventional form. This waveform is represented at **51** in FIG. **4***a*. The relative amplitudes of the audio waveform **50** and the triangular waveform **51** are so adjusted that the peak level of the audio wave **50** never exceeds the peak level of the triangular wave **51**. In the output **49** of differential amplifier **45** will appear a wave **52**, as represented in FIG. **4**(b) comprising a series of pulses varying width recurrent at the frequency of the triangular wave, 250 kilohertz, these pulses being centered on the peaks of the triangular wave **51** and varying in width in response to variations in the amplitude of the input audio wave. From consideration of FIG. **4**, it will be noted that a positive pulse will appear in the output **49** of differential amplifier **45** whenever the instantaneous magnitude of the triangular wave **51** exceeds the amplitude of the input audio wave **50**.

Referring now to FIG. **5**, there is shown in further detail the construction of multiplexer **15** of FIG. **1**. As will be seen from FIG. **5**, the multiplexer, having 256 inputs and a single output, is made up of a plurality of component multiplexers, all but one of which have eight inputs and a single output, the remaining one having four inputs and a single output. Shown in a vertical array at the left-hand side of FIG. **5** is a series of 32 multiplexers **56**, each having eight inputs and a single output (only representative ones of these 32 multiplexers are shown), thereby providing a total of 256 inputs as required. Each of multiplexers **56** is adapted to be controlled by 3 bits of digital information supplied to it via control busses **57**, **58** and **59** selectively to connect any one of its eight inputs to its output.

The output of each multiplexer **56** in turn is connected to a different input of one of a series of four similar multiplexers **60**, **61**, **62** and **63**, each having eight inputs and a single output as shown. Thus the outputs of the upper two multiplexers **56** in the series of **32** are connected respectively to the first two inputs of multiplexer **60**, the output of the intermediate multiplexer **56** is connected to the third input of multiplexer **62**, and the output of the lower multiplexer **56** is connected to the final input of multiplexer **63**. Like multiplexers **56**, multiplexers **60**, **61**, **62** and **63** each is adapted to be controlled by three bits of digital information supplied to it from control busses **64**, **65** and **66** selectively to connect any one of its eight inputs to its output. The outputs of multiplexers **60**, **61**, **62** and **63** are connected respectively to the four inputs of multiplexer **67**, which is adapted to be controlled by two bits of digital information supplied to it through control busses **68** and **69** to connect any one of its four inputs selectively to its single output **70**.

It readily will be seen that, by applying eight bits of appropriate digital information to the eight control busses **57**, **58**, **59**, **64**, **65**, **66**, **68** and **69**, multiplexers **56**, **60**, **61**, **62**, **63** and **67** can be controlled so as to connect any one of the **256** inputs to the 32 multiplexers **56** to the single output **70** of multiplexer **67**, thus providing a multiplexer suitable for use as the multiplexer **15** in FIG. **1**.

In FIG. **6** is shown the detailed construction of one of the eight-to-one multiplexers of FIG. **5**. Such a multiplexer comprises an arrangement consisting of seven single-pole double-throw electronic switches of conventional form, each adapted to be controlled in

response to a single bit of information supplied to it from a control buss. As shown, four such switches 75, 76, 77 and 78 are arranged to provide eight inputs in pairs of two, each pair being connected to the input terminals of one of the switch circuits 75–78, the switch circuit being controllable through the control buss 79 to connect either one of its two inputs to its single output. The four outputs from switches 75–78 in turn are connected in pairs to the inputs of switches 80 and 81 each of which is controllable through buss 82 to connect either one of its pair of inputs to its single output. The two outputs from switches 80 and 81 in turn are connected to the two inputs of switch 83, which likewise is controllable through buss 84 to connect either input to its single output. Thus there is provided an arrangement which may be controlled by three bits of information supplied to it through control busses 79, 82 and 84 to connect any one of the eight inputs to switches 75, 76, 77 and 78 to the single output 85 of switch 83. Also it will be seen that control busses 79, 82 and 84 may correspond to control busses 57, 58 and 59 in FIG. 5 or to control busses 64, 65 and 66. Also it will be readily apparent that if the switches 75, 76, 77 and 78 are omitted in the arrangement of FIG. 6, the remaining structure, comprising switches 80, 81 and 83, will provide a 4-to-1 multiplexer suitable for use as the multiplexer 67 of FIG. 5.

Referring now to FIG. 7, there is shown the detailed construction of the demultiplexer 19 of FIG. 1. This comprises a single 1-to4 demultiplexer 90 and a series of four 1-to -8 demultiplexers 91, 92, 93 and 94. The four outputs of demultiplexer 90 are connected respectively to the inputs of demultiplexers 91, 92, 93 and 94. Demultiplexer 90 is adapted to be controlled in response to two bits of information supplied to it through busses 95 and 96 to connect its input selectively to any one of its four outputs. Similarly each of demultiplexers 91, 92, 93 and 94 is adapted to be controlled in response to three bits of information supplied to it through busses 97, 98 and 99 to connect its input selectively to any one of its eight outputs. Thus it will be seen that, by controlling demultiplexer 90 through control busses 95 and 96, and demultiplexers 91, 92, 93 and 94 through control busses 97, 98 and 99, the single input to demultiplexer 90 may be selectively connected to any one of the 32 outputs provided by the four demultiplexers 91, 92, 93 and 94. It will be readily apparent that the individual demultiplexers may comprise an arrangement of single pole double throw electronic switches similar to that of FIG. 6 but in an inverse relation proceeding from a single input to plural outputs.

In FIG. 8 is shown in further detail the construction of block 28 labeled "gates" in FIG. 1. The gates comprise a series of eight and-gates 105, of which only representative ones are shown. One input to each of these gates is through connections 43 from the computer and comprises the data in binary form regarding words to be selected from the audio memory drum 11 of FIG. 1 by multiplexer 15. The other input to each gate 105 comprises a strobe pulse from computer 29 of FIG. 1 supplied through connection 42. In response to actuation by the strobe pulse, each gate 105 operates to supply word data from the computer to output connections 44 for supply to the address memory 18 of FIG. 1.

In FIG. 9 is shown the detailed construction of block 25 also labeled "gates" in FIG. 1. There are five gate sections, each section comprising an and-gate 111 and and-gate 112 having their respective outputs connected to the inputs of an or-gate 113. One input to each and-gate 112 comprises address data from the computer supplied through connections 41, and the other input is a word pulse from the audio memory drum 11 of FIG. 1 supplied through connections 30 and 114. When address data and word pulses are supplied simultaneously to an and-gate 112, the and-gate produces an output which is supplied to one of the inputs of the corresponding or-gate 113.

One input to each and-gate 111 comprises pulses from counter 21 of FIG. 1 supplied through connections 24. The other input to each and-gate 111 is an inverted word pulse supplied through connection 116 from the output of inverter 115, to the input of which word pulses are supplied to connection 30. When counter pulses and inverted word pulses are supplied simultaneously to an and-gate 111, (i.e. in the absence of a word pulse) the and-gate produces an output which is supplied to the other input of the corresponding or-gate 113. An input to one of the or-gates 113 from either of its associated and-gates 111 and 112 results in the production of a signal in the output of the or-gate which is supplied through connections 26 to the address memory to determine the storage locations of the word data supplied from gates 28 through connections 44 in FIG. 1, to determine the locations in the memory in which such word data is to be stored.

Reference now is made to FIG. 10 which shows the details of the FSK data buffer 123 and frequency shift keyer 122 of FIG. 1. A demultiplexer 130, having a data input 124 from computer 29 and, in this instance, 32 individual outputs 131, is controlled in response to address data supplied through connection 125 from computer 29 to direct the data, at any given time, to the desired one of the 32 output connections 131. Each of the 32 output connections is supplied to an input of a cross-coupled gate comprising gates 132 and 133 with their inputs and outputs interconnected as shown. Only one such gate, connected to a typical output 131 of demultiplexer 130, is shown, all of the others being similar. Another input to the cross-coupled gate is a 110 hertz timing signal supplied through connection 134 to one of the inputs of gate 133. The output of the cross-coupled gate is supplied through connection 135 to the input of a conventional flipflop 137, which also is supplied with the 110 hertz timing signal through connection 136. The output from flipflop 137 is supplied through connection 138 to control the operation of a voltage-controlled oscillator 139 which, for one output level of flipflop 137, produces an output at 2,225 hertz corresponding to a teletype mark signal and, for the other output level of flipflop 137, produces an output at 2,025 hertz corresponding to a teletype space signal. These outputs from voltage controlled oscillator 140 are supplied through connection 140 to relay 121 of FIG. 1 for selection and supply to demodulators 22 as desired.

In the arrangement just described, the cross-coupled gate 132, 133 and flipflop 137 operate as a buffer for the data supplied thereto from demultiplexer 130. Each successive bit of data supplied to the cross-coupled

gate 132, 133 is effectively stored thereby until the occurrence of one of the 110 hertz timing pulses supplied through connection 134. When such a pulse occurs it first actuates flipflop 137 through connection 136 and causes the flipflop to respond to the output of the cross-coupled gate. It then resets the flipflop to render it responsive to the next bit of data supplied through connection 131 from demultiplexer 130. The output of flipflop 137 will comprise a square wave having either of two voltage levels. Voltage-controlled oscillator 139, which may be a typical multivibrator circuit, responds to the different voltage output levels from flipflop 137 to produce a frequency shift signal corresponding to either a mark or a space, which is capable of operating a conventional teletype printer. The latter signals will be a square waves which will be converted to sine waves by the high-pass filters comprising demodulators 22 in FIG. 1.

While the invention has been described with reference to a system having a capacity of 256 words, and capable of serving 32 subscriber output lines, it will be understood that these figures are merely exemplary and that the system can be adapted to accommodate any number of words and any number of subscriber output lines subject only to the limitations imposed by complexity of the equipment. Further it will be understood that numerous modifications may be made in the apparatus specifically disclosed without departing from the scope of the invention as defined by the appended claims.

I claim:

1. An audio response generator for synthesizing audio messages, comprising:

a. an audio memory unit for storing data in analog form regarding a plurality of speech words and having an output for each word,

b. analog-to-digital converter means connected to each of said audio memory outputs for converting data from said output to digital form,

c. multiplexer means supplied with the outputs from said last means for generating a time-multiplexed signal having a plurality of successive time slots, each occupied by digital information supplied from one of said analog-to-digital converters,

d. demultiplexer means supplied with said time-multiplexed signal from said multiplexer for supplying digital information from the respective time slots of said multiplexed signal to selected ones of a plurality of output channels, and

e. means in each of said output channels for converting said digital information to audio data.

2. In a query and response system, a computer for storing data responsive to queries from subscribers, and an audio response generator supplied with data from said computer for synthesizing audio messages responsive to said queries, said audio response generator comprising:

a. an audio memory unit for storing data in analogue form regarding a plurality of speech words and having an output for each word,

b. pulse width modulator means connected to each of said audio memory outputs for converting data from said output to digital form,

c. multiplexer means supplied with the outputs from said last means for generating a time-multiplexed signal having a plurality of successive time slots, each occupied by a width-modulated pulse from one of said pulse width-modulators,

d. demultiplexer means supplied with said time-multiplexed signal from said multiplexer for supplying said width-modulated pulses to selected ones of a plurality of output channels, and

e. means in each of said output channels for converting said width-modulated pulses to audio data.

3. An audio response generator for synthesizing audio messages, comprising:

a. an audio memory unit for storing data in analog form regarding a plurality of speech words and having an output for each word,

b. pulse width modulator means connected to each of said audio memory outputs for converting data from said output to digital form,

c. multiplexer means supplied with the outputs from said last means for generating a time-multiplexed signal having a plurality of successive time slots, each occupied by a width-modulated pulse from one of said pulse width modulators,

d. demultiplexer means supplied with said time-multiplexed signal from said multiplexer for supplying said width-modulated pulses to selected ones of a plurality of output channels, and

e. means in each of said output channels for converting said width-modulated pulses to audio data.

4. An audio response generator according to claim 3, including means for controlling said demultiplexer to cause it to supply said width-modulated pulses occupying successive time slots in said multiplexed signal to said output channels cyclically and in a predetermined order.

5. An audio response generator according to claim 4, including means for controlling said multiplexer to cause each time slot of said multiplexed signal to be occupied by a width-modulated pulse from a desired one of said pulse width modulators.

6. An audio response generator according to claim 5, in which said multiplexer is responsive to digital address data supplied to it to select the output from a particular one of said pulse width modulators and supply it to the output of said multiplexer.

7. An audio response generator according to claim 3, in which said demultiplexer is responsive to digital address data supplied to it to supply said width-modulated pulses to selected output channels, and including means for successively supplying to said demultiplexer digital address data designating different output channels.

8. An audio response generator according to claim 3, in which said multiplexer is responsive to digital address data supplied to it to select the output from a particular one of said pulse width modulators and supply it to the output of said multiplexer, in which said demultiplexer is responsive to digital address data supplied to it to supply said width-modulated pulses to a selected output channel, and including:

a. a first source of digital data in the form of a plurality of bytes, each indicative of the address in said audio memory unit of data regarding a particular speech word to be supplied to a particular output channel,

b. a second source of digital data in the form of a plurality of bytes, each indicative of the output channel to which data regarding a particular speech word is to be supplied,

c. means for successively applying data bytes from said second source to said demultiplexer in a predetermined sequence, and

d. means for simultaneously successively supplying

data bytes from said first source to said multiplexer, the data supplied to said multiplexer at any given time being indicative of the address of speech word data to be supplied to the output channel indicated by the data from said second source simultaneously supplied to said demultiplexer.

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