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(54) **CAPACITOR WITH 3D NAND MEMORY**

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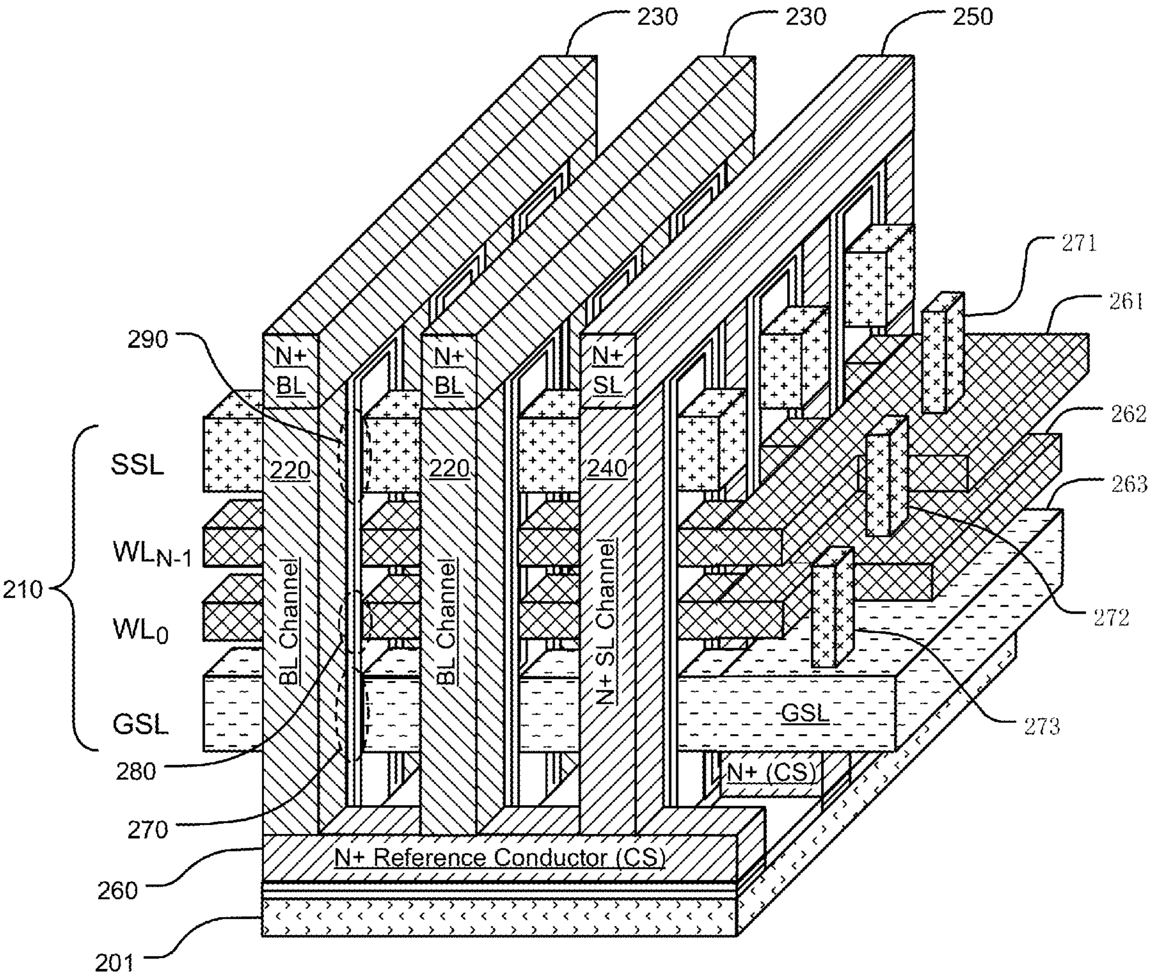
(57) **ABSTRACT**

An integrated circuit includes a 3D NAND memory array with a stack of conductive strips and a capacitor with a stack of capacitor terminal strips. Multiple conductive strips in the stack of conductive strips, and multiple capacitor terminal strips of the stack of capacitor terminal strips, share a same plurality of plane positions relative to the substrate. Different plane positions in the same plurality of plane positions characterize different capacitor terminal strips in the stack of capacitor terminal strips and different conductive strips in the stack of conductive strips, and a same plane position characterizing both a conductive strip in the stack of conductive strips and a capacitor terminal strip in the stack of capacitor terminal strips indicates that the conductive strip and the capacitor terminal strip have a same vertical position relative to each other.



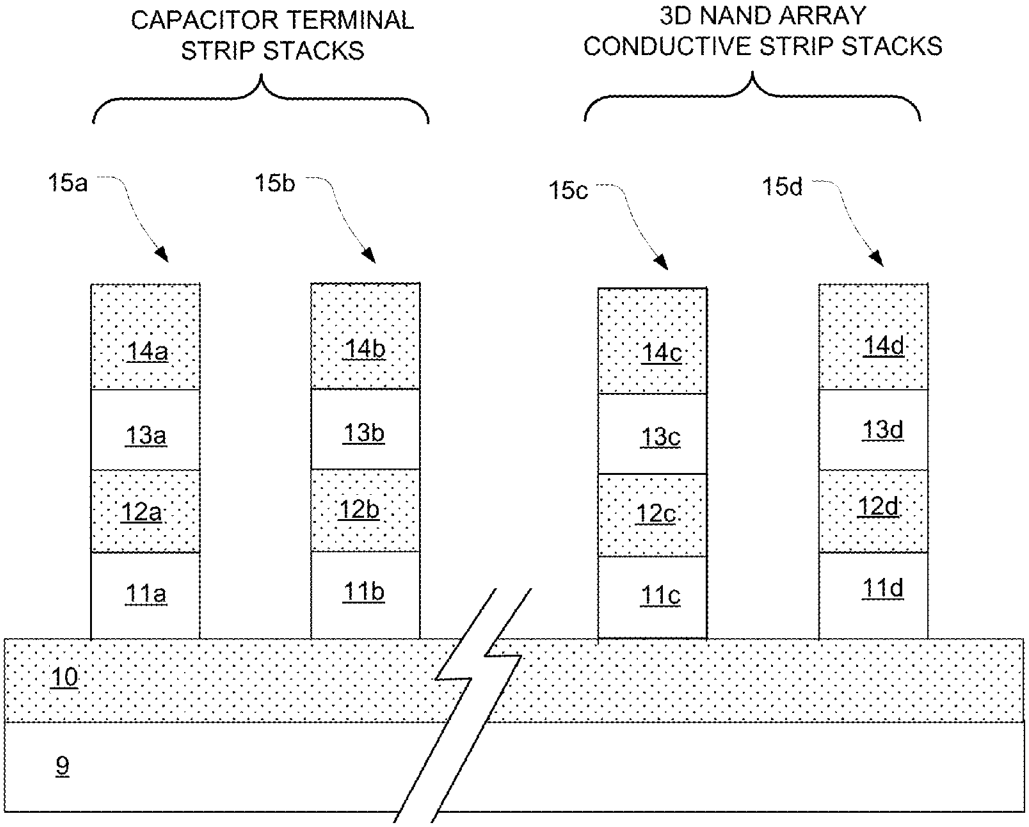

CAPACITOR TERMINAL
STRIP STACKS
3D NAND ARRAY
CONDUCTIVE STRIP STACKS
15a
15b
15c
15d
14a
14b
14c
14d
13a
13b
13c
13d
12a
12b
12c
12d
11a
11b
11c
11d
10
9

FIG. 1

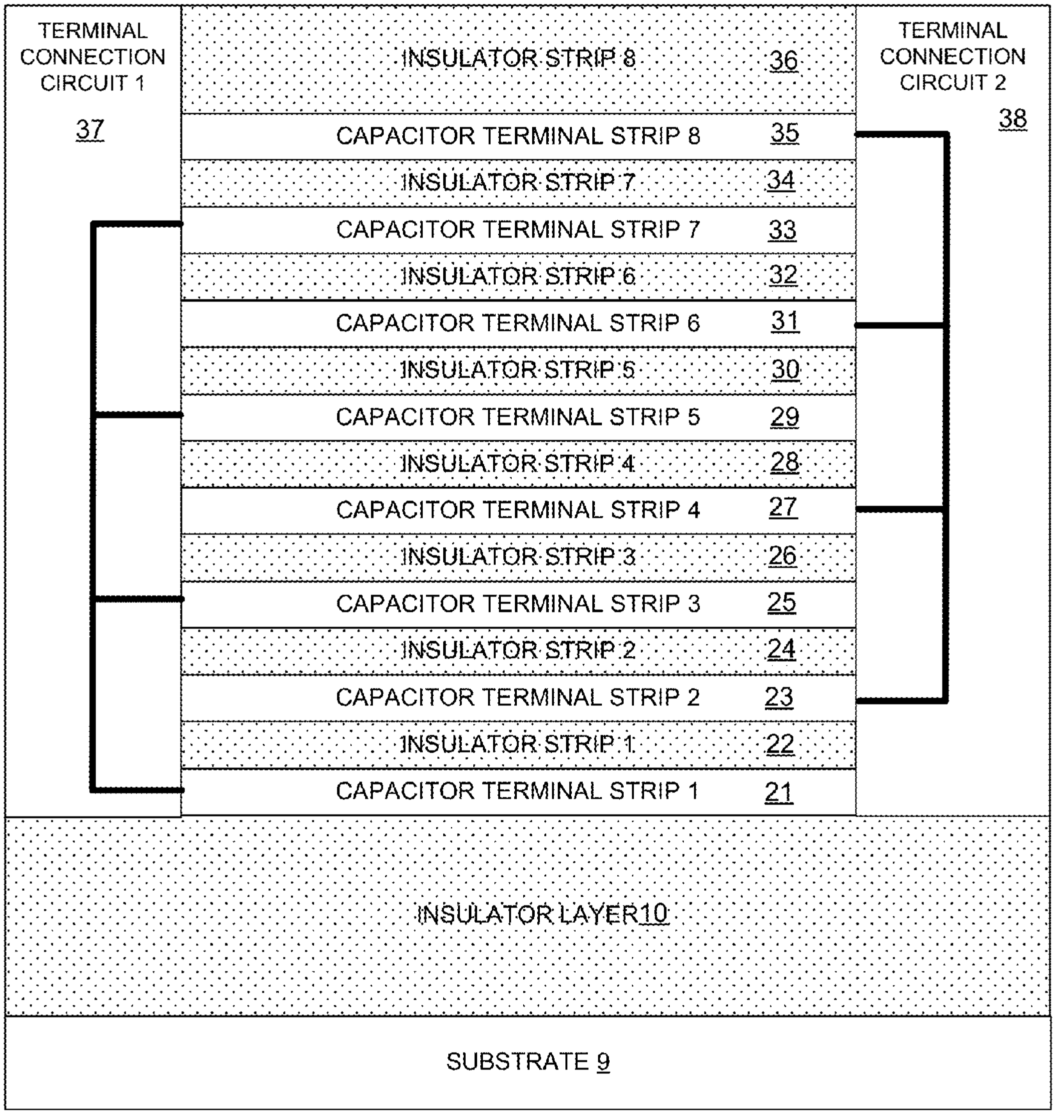
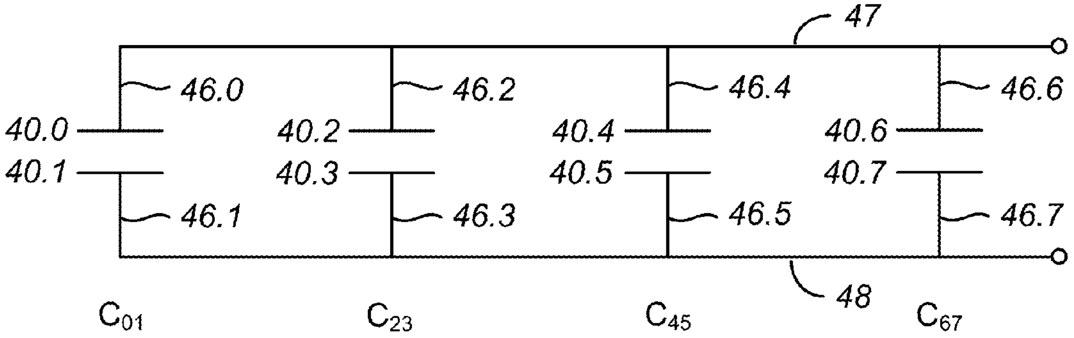
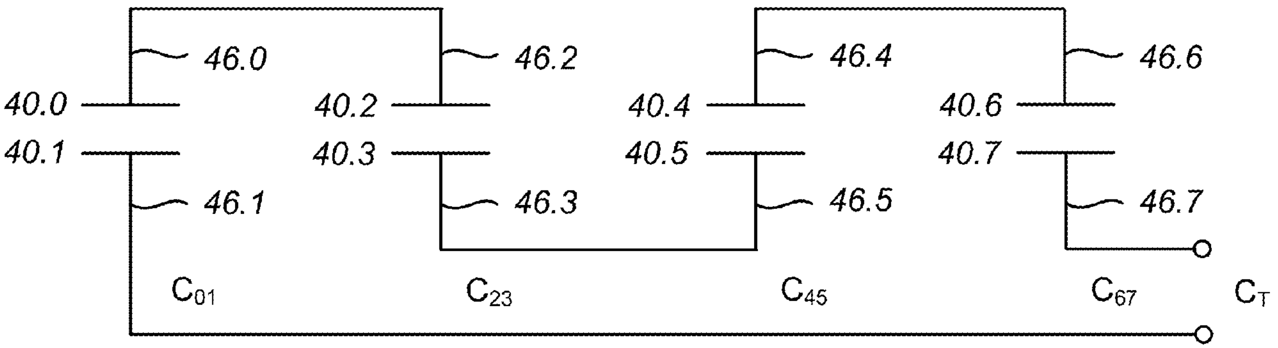

TERMINAL CONNECTION CIRCUIT 1
37
INSULATOR STRIP 8
36
TERMINAL CONNECTION CIRCUIT 2
38
CAPACITOR TERMINAL STRIP 8
35
INSULATOR STRIP 7
34
CAPACITOR TERMINAL STRIP 7
33
INSULATOR STRIP 6
32
CAPACITOR TERMINAL STRIP 6
31
INSULATOR STRIP 5
30
CAPACITOR TERMINAL STRIP 5
29
INSULATOR STRIP 4
28
CAPACITOR TERMINAL STRIP 4
27
INSULATOR STRIP 3
26
CAPACITOR TERMINAL STRIP 3
25
INSULATOR STRIP 2
24
CAPACITOR TERMINAL STRIP 2
23
INSULATOR STRIP 1
22
CAPACITOR TERMINAL STRIP 1
21
INSULATOR LAYER 10
SUBSTRATE 9

FIG. 2



$$C_T = C_{01}+C_{23}+C_{45}+C_{67}$$

FIG. 3



$$\frac{1}{C_T} = \frac{1}{C_{01}} + \frac{1}{C_{23}} + \frac{1}{C_{45}} + \frac{1}{C_{67}}$$

FIG. 4

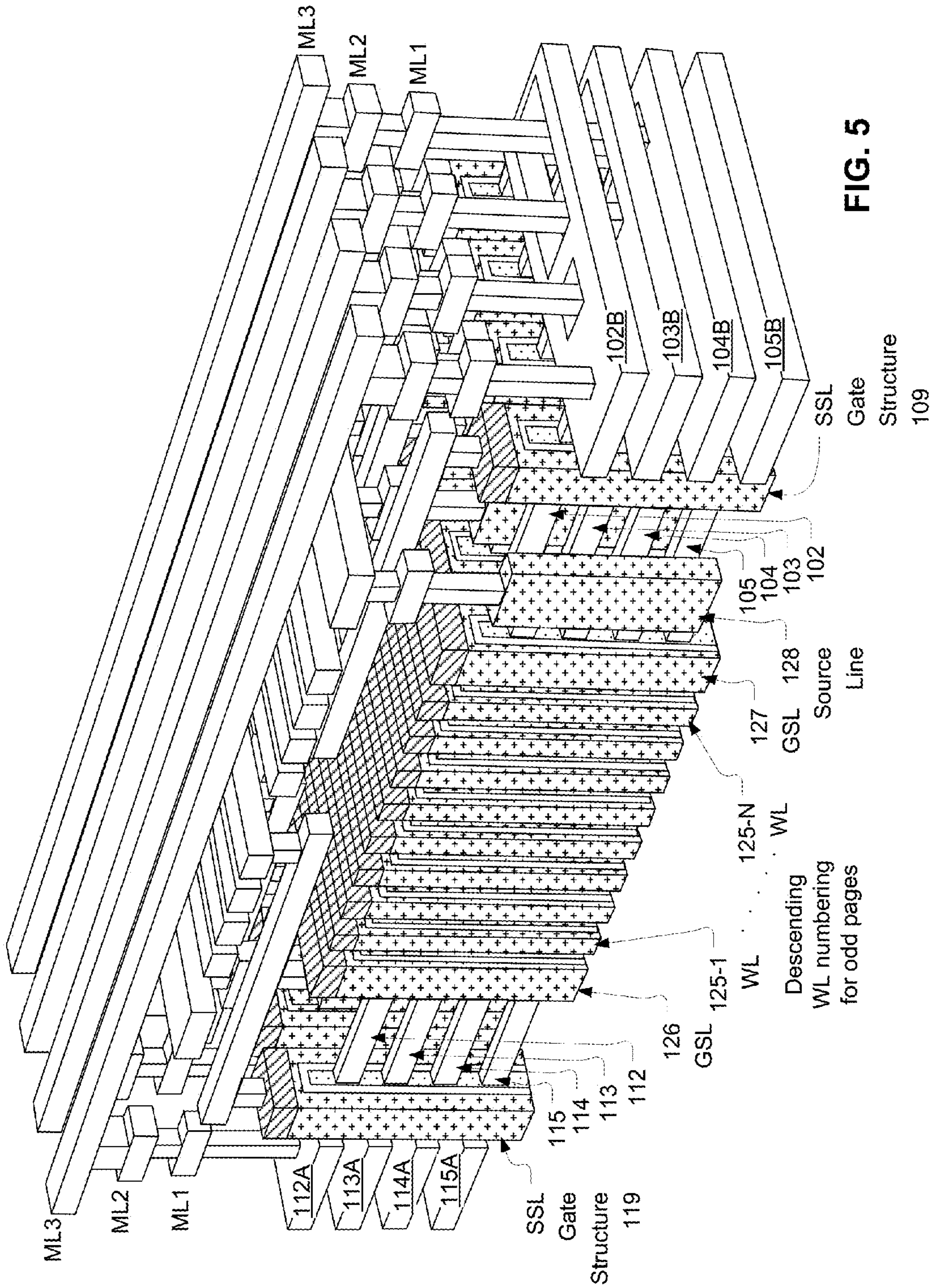

ML3
ML2
ML1
112A
113A
114A
115A
SSL Gate Structure 119
115
114
113
112
126 GSL
125-1 WL
. . .
125-N WL
Descending WL numbering for odd pages
127 GSL
128 Source Line
105
104
103
102
SSL Gate Structure 109
102B
103B
104B
105B
ML3
ML2
ML1

FIG. 5

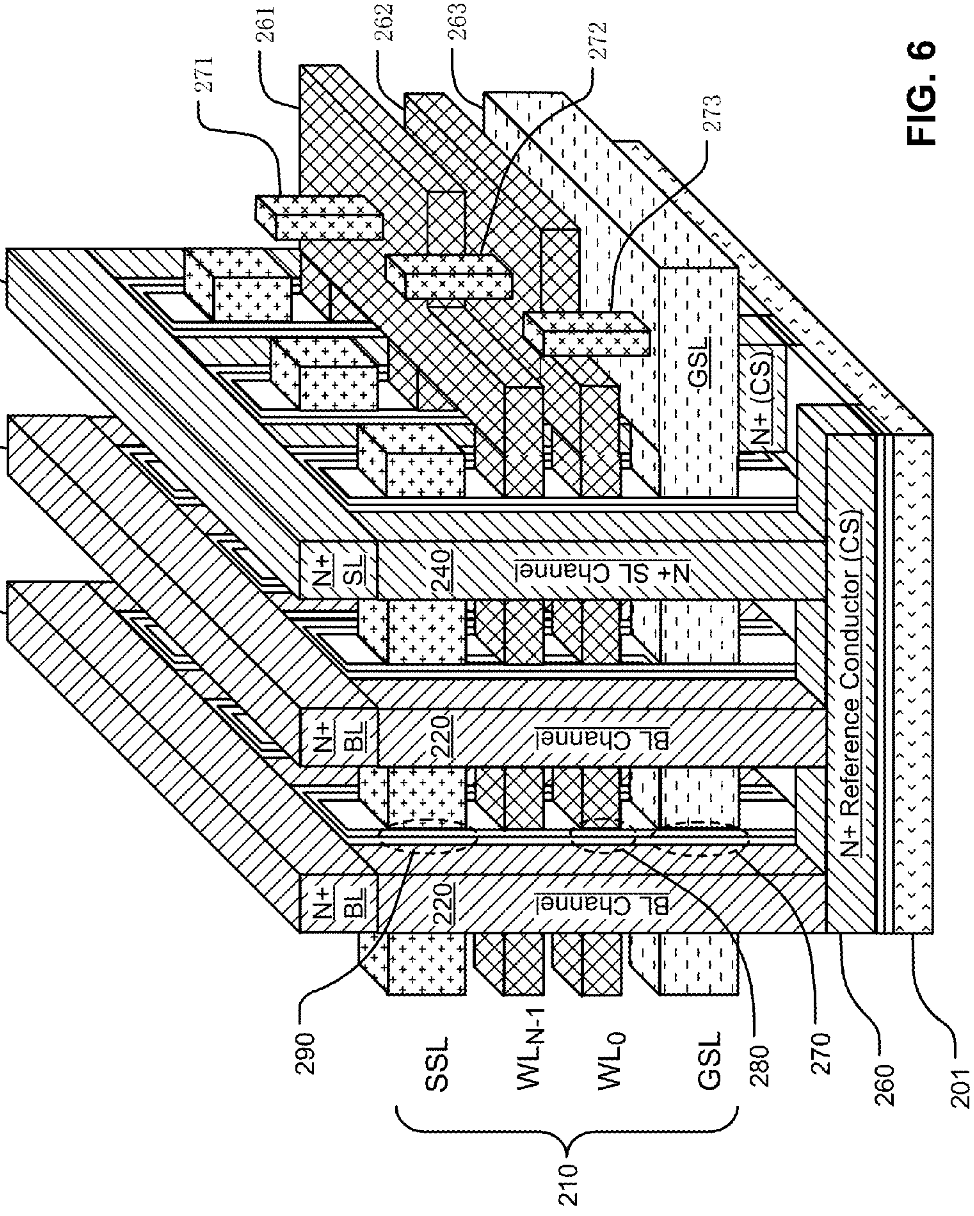

250
230
230
230
271
261
262
263
272
273
N+
SL
240
N+ SL Channel
N+
BL
220
BL Channel
N+
BL
220
BL Channel
N+ Reference Conductor (CS)
GSL
N+ (CS)
290
SSL
WL_{N-1}
WL_0
GSL
280
270
260
201
210

FIG. 6

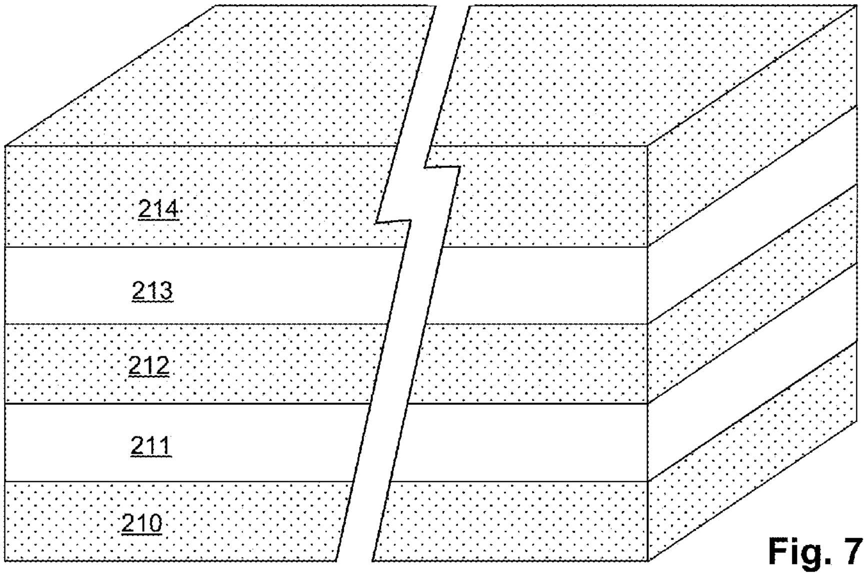

214
213
212
211
210

Fig. 7

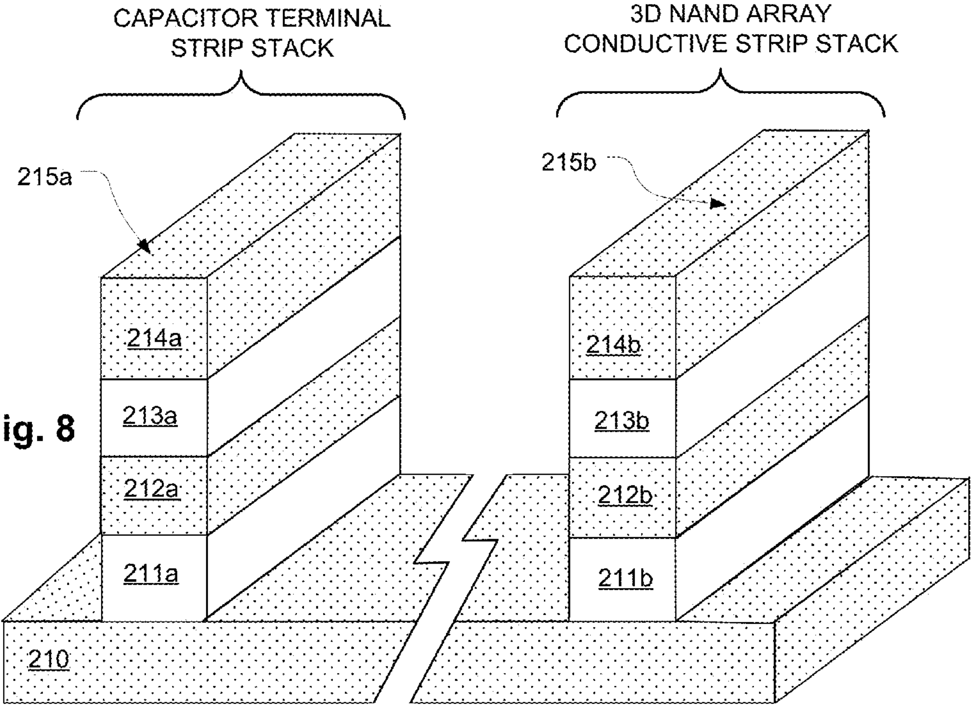

CAPACITOR TERMINAL
STRIP STACK
3D NAND ARRAY
CONDUCTIVE STRIP STACK
215a
215b
214a
213a
212a
211a
214b
213b
212b
211b
210

Fig. 8

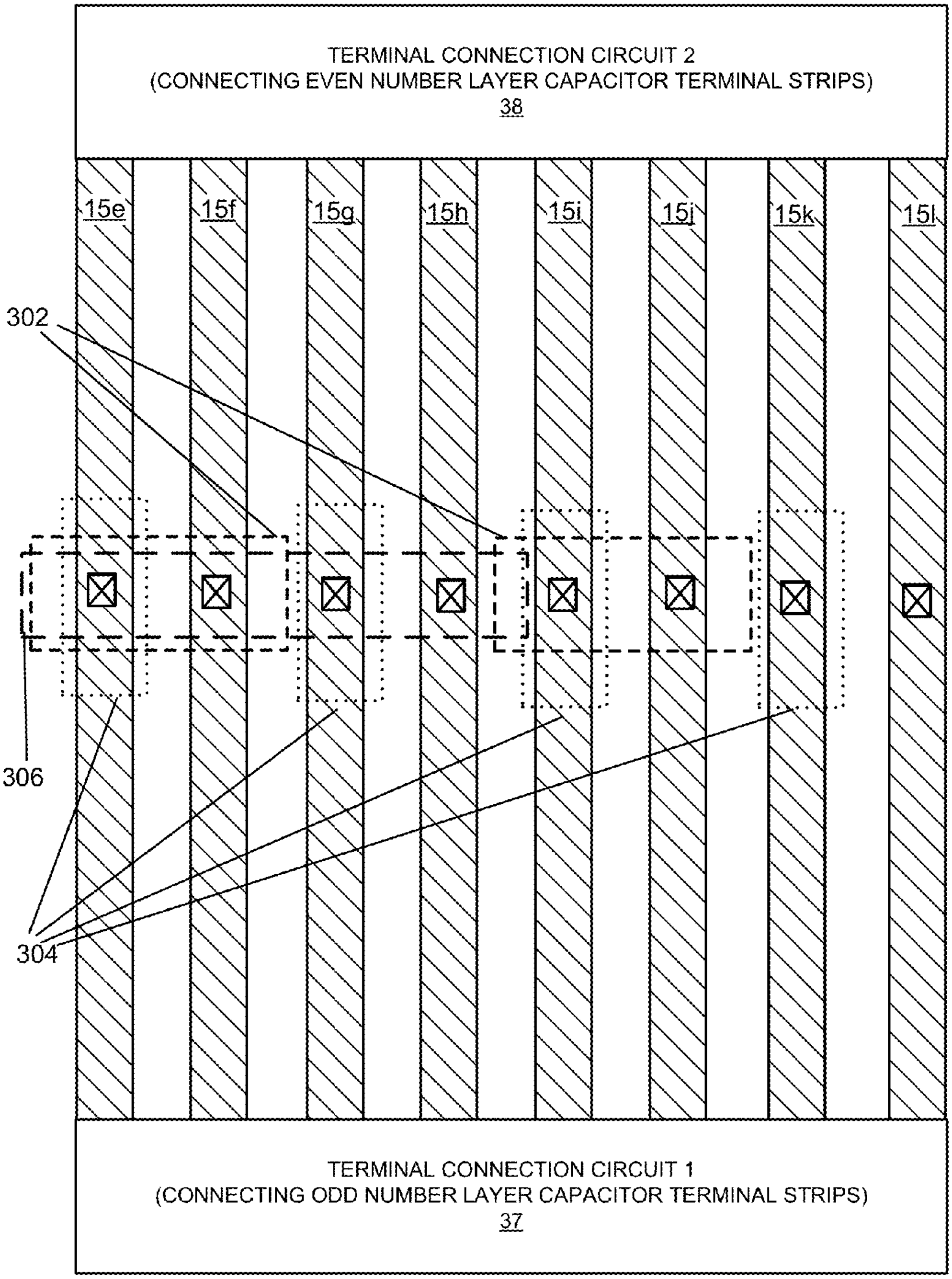

TERMINAL CONNECTION CIRCUIT 2
(CONNECTING EVEN NUMBER LAYER CAPACITOR TERMINAL STRIPS)
38
15e
15f
15g
15h
15i
15j
15k
15l
302
306
304
TERMINAL CONNECTION CIRCUIT 1
(CONNECTING ODD NUMBER LAYER CAPACITOR TERMINAL STRIPS)
37

FIG. 9

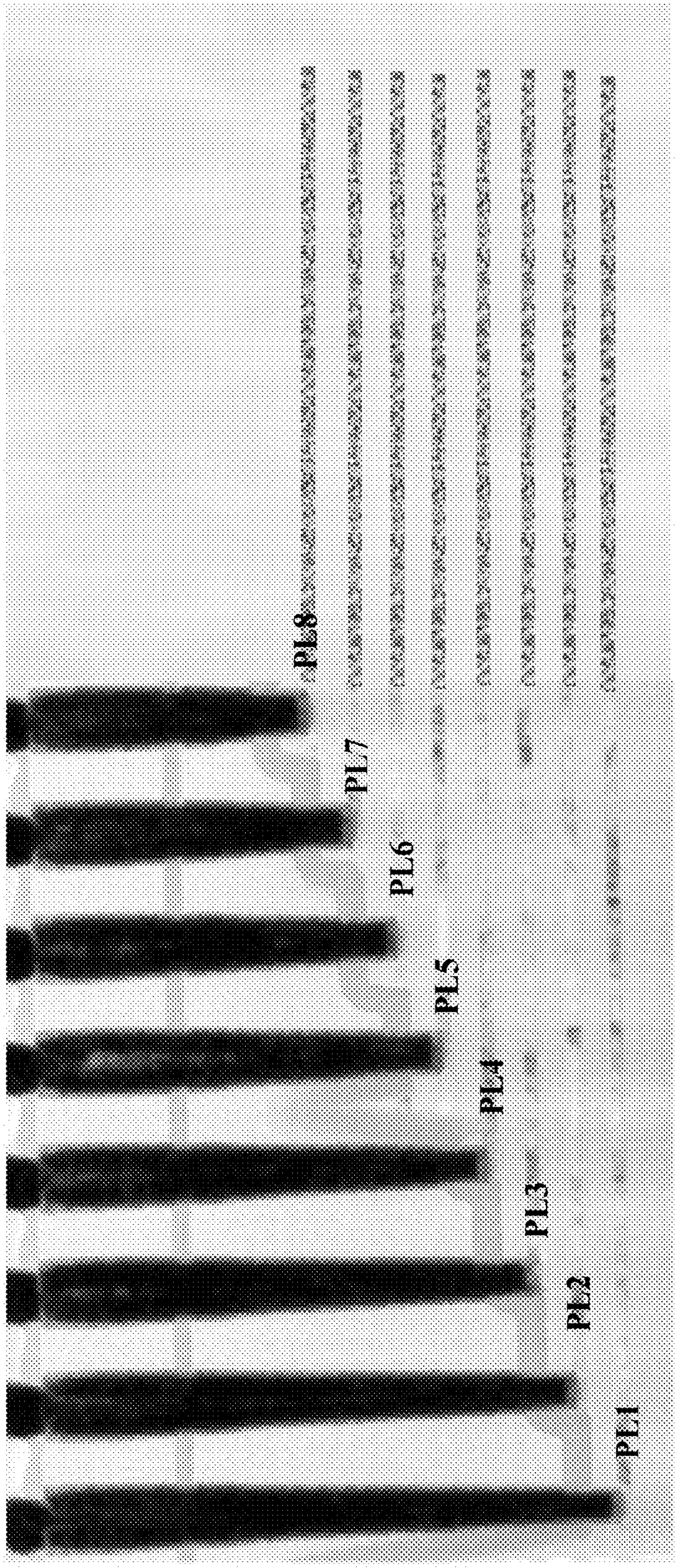


FIG. 10

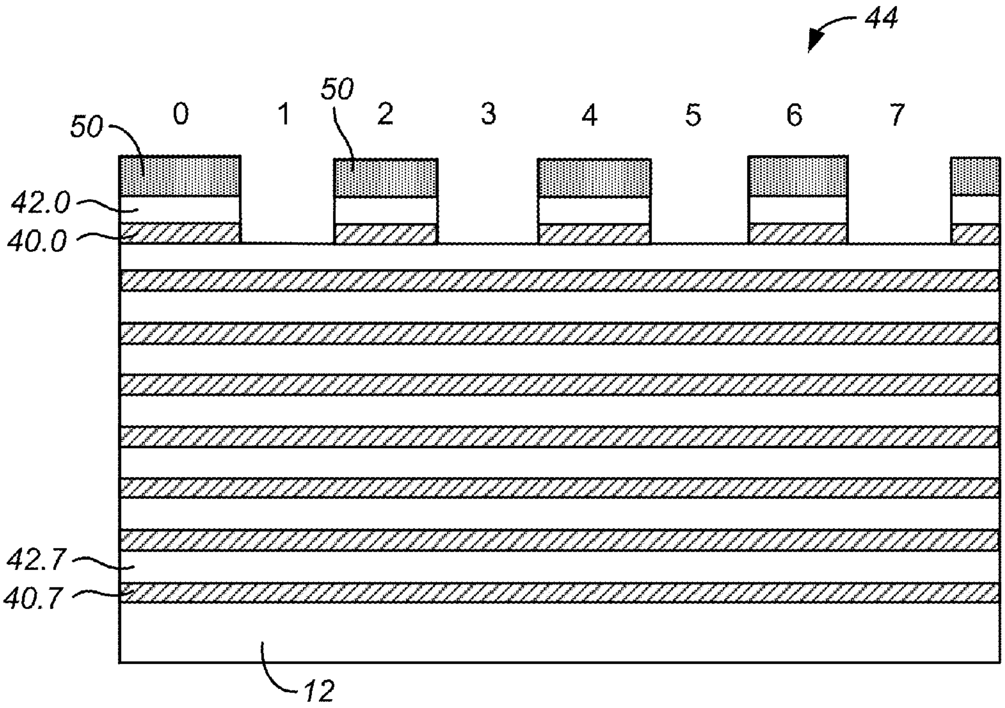


FIG. 11

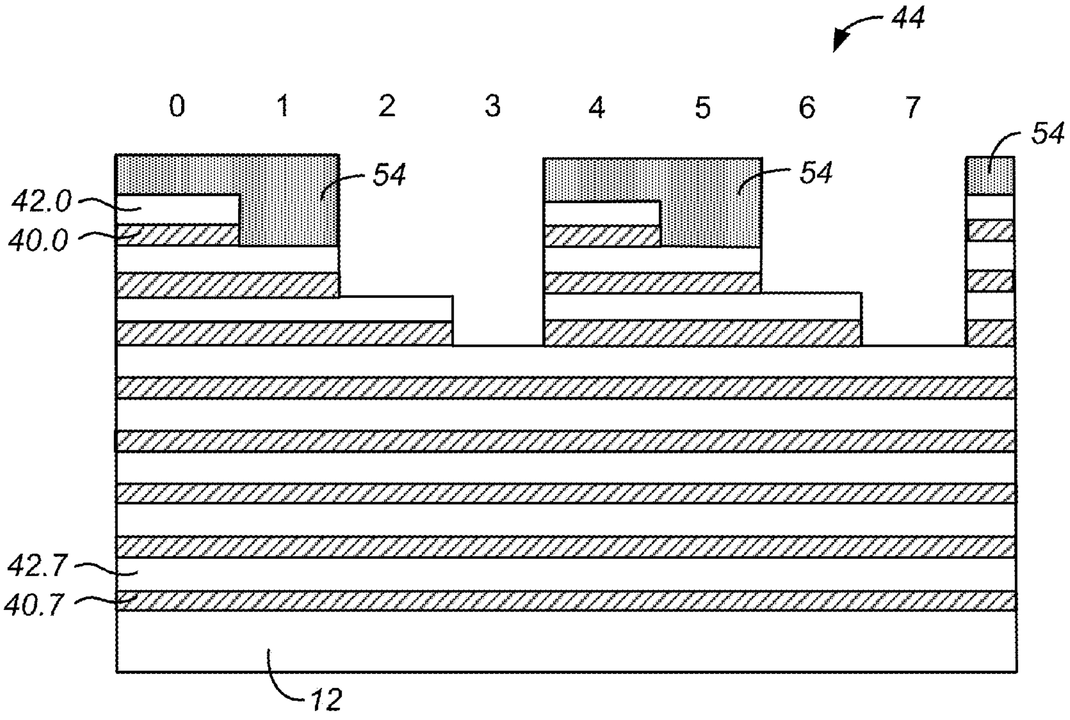


FIG. 12

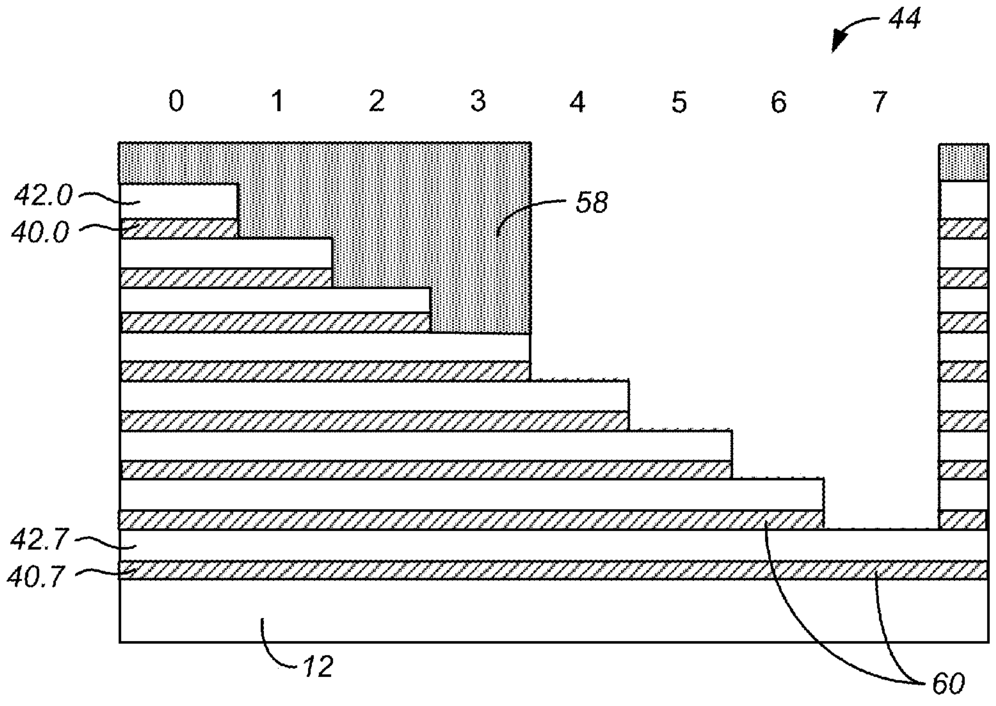


FIG. 13

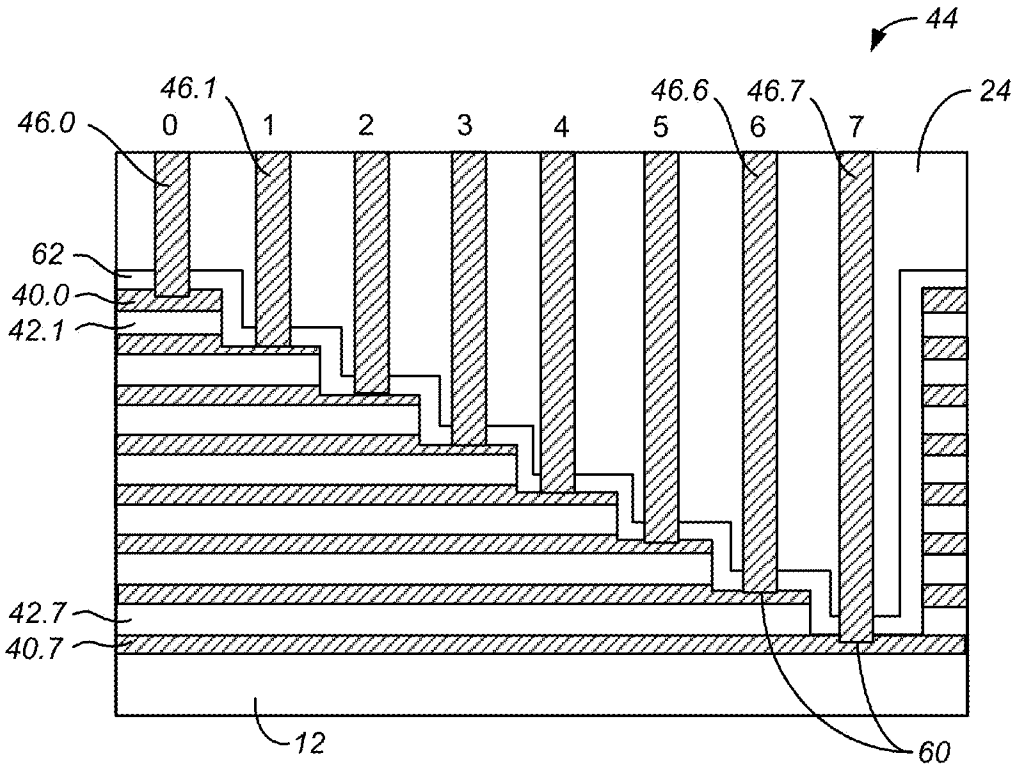


FIG. 14

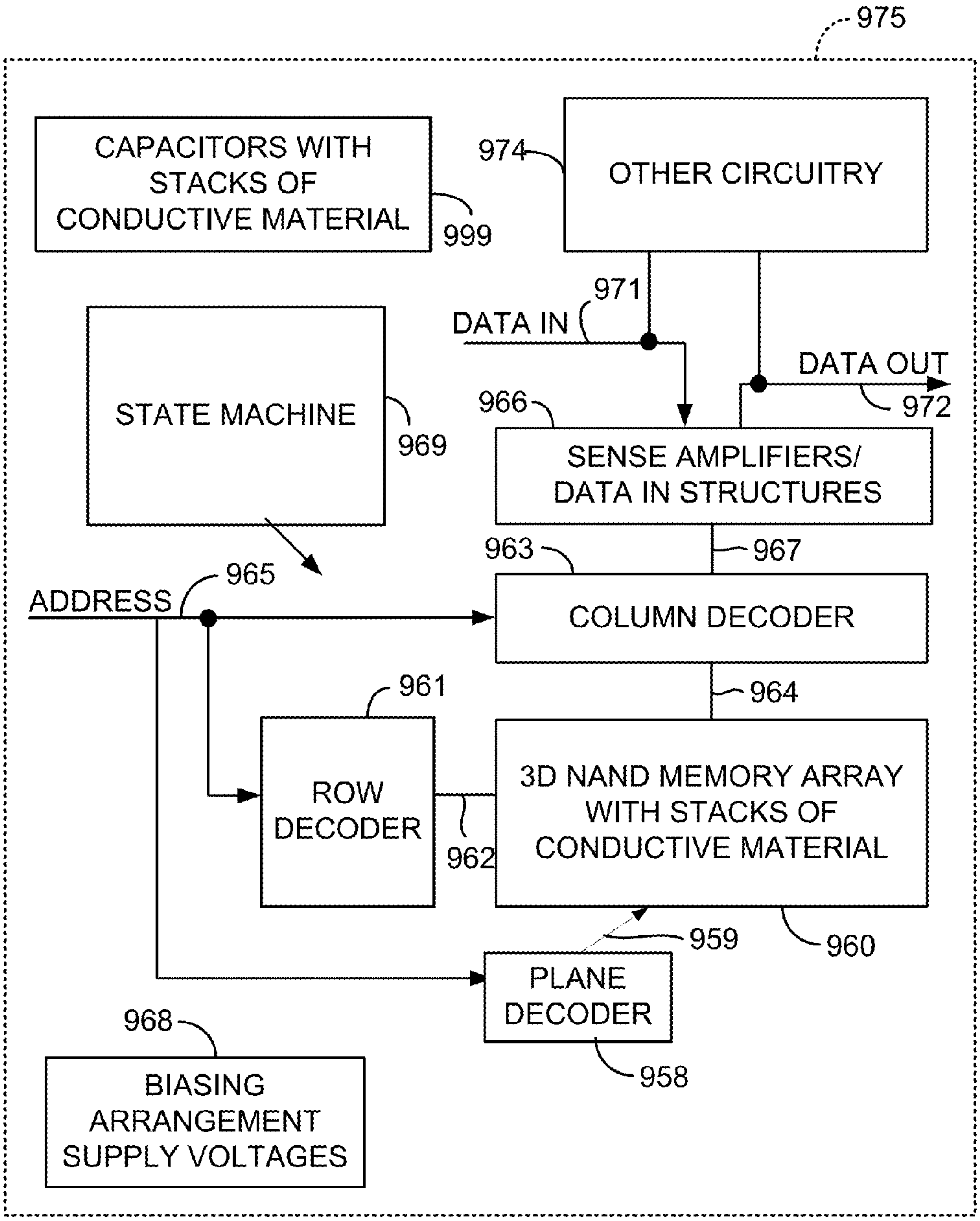

975
CAPACITORS WITH STACKS OF CONDUCTIVE MATERIAL
999
974
OTHER CIRCUITRY
971
DATA IN
DATA OUT
972
STATE MACHINE
969
966
SENSE AMPLIFIERS/ DATA IN STRUCTURES
963
967
ADDRESS
965
COLUMN DECODER
964
961
ROW DECODER
962
3D NAND MEMORY ARRAY WITH STACKS OF CONDUCTIVE MATERIAL
959
960
PLANE DECODER
958
968
BIASING ARRANGEMENT SUPPLY VOLTAGES

FIG. 15

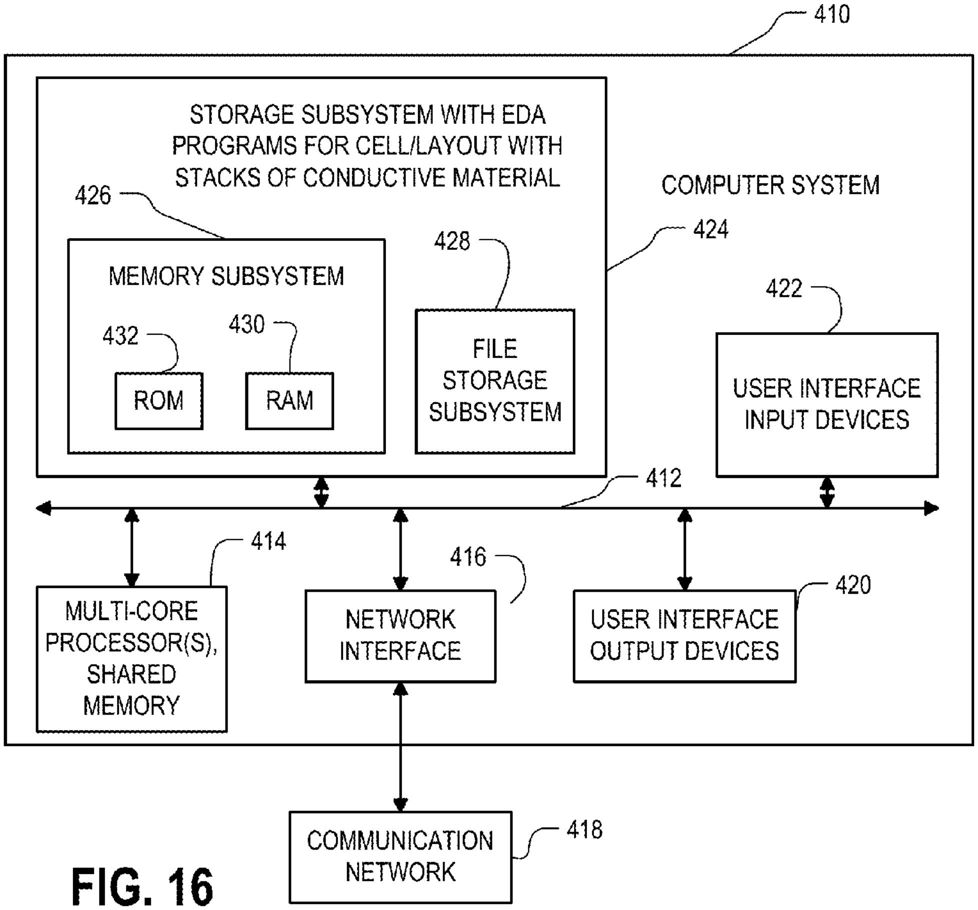


FIG. 16

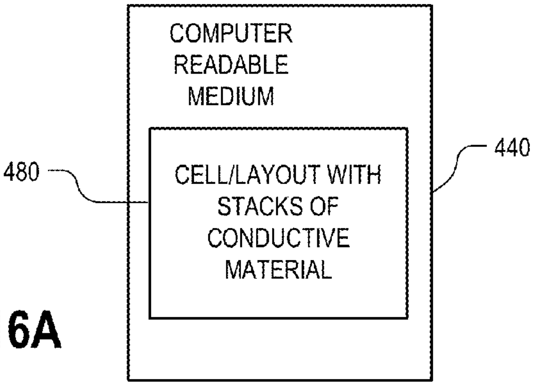


FIG. 16A

CAPACITOR WITH 3D NAND MEMORY

CROSS-REFERENCE TO OTHER APPLICATIONS

[0001] This application is related to the following co-pending U.S. patent applications: U.S. patent application Ser. No. 13/049,303, filed 16 Mar. 2011, entitled REDUCED NUMBER OF MASK FOR IC DEVICE WITH STACKED CONTACT LEVELS, now U.S. Pat. No. 8,598,032; and U.S. patent application Ser. No. 13/114,931, filed 24 May 2011, entitled MULTILAYER CONNECTION STRUCTURE AND MAKING METHOD, now U.S. Patent No. 8,383,512.

BACKGROUND OF THE INVENTION

[0002] Capacitors are electronic devices including two terminals separated by insulating material. When there is a voltage difference between the two terminals, an electric field is created between the two terminals thereby storing electrical energy. The amount of electrical charge that can be stored on a capacitor per volt across the terminals is referred to as capacitance. Terminals are typically in the form of plates of various shapes, surface contours and sizes. The capacitance is generally a function of the dielectric constant κ of the dielectric layer, directly proportional to the area of the opposed terminals and inversely proportional to the distance between the terminals. Placing two or more capacitors in parallel results in a total capacitance of the combination that is equal to the sum of the capacitances of the individual capacitors. Placing two or more capacitors in series results in a total capacitance of the combination that is less than the capacitance of any of the individual capacitors. Series connected capacitors are commonly used in high-voltage situations because the high-voltage is divided among the capacitors. While providing capacitors of various sizes is usually not a problem outside of an integrated circuit, conventional integrated circuits are limited to relatively small capacitors because of size limitations. See, for example, U.S. Pat. No. 5,497,016.

[0003] A stack of capacitors connected in parallel has a low area footprint from the bottom capacitor in the stack of capacitors, and yet a large capacitance from the summed capacitance of the capacitors in the stack connected in parallel. However, the stacked capacitor is fabricated by many steps which results in increased complexity and cost of the overall integrated circuit. It would be desirable to take advantage of the low area footprint, large capacitance of the stacked capacitor, while minimizing additional fabrication complexity and cost resulting from the addition of the stacked capacitor to an integrated circuit.

BRIEF SUMMARY OF THE INVENTION

[0004] Various aspects of the technology involve integrated circuits having both a 3D NAND memory array with a stack of conductive strips, and a stacked capacitor with a stack of capacitor terminal strips. Because the integrated circuit is already being fabricated to include a 3D NAND array, overall complexity is changed little from fabricating stacks of conductive strips for a capacitor in addition to the NAND memory array.

[0005] One aspect of the technology includes an integrated circuit with a substrate, a 3D NAND memory array with a stack of conductive strips, and a stacked capacitor with a stack of capacitor terminal strips. Multiple conductive strips in the stack of conductive strips, and multiple capacitor terminal strips of the stack of capacitor terminal strips, share a same plurality of vertical distances from the substrate.

[0006] In some embodiments of the technology, the stack of conductive strips is at least one of: transistor channels in the 3D NAND memory array, conductors routing signals that select memory cells in the 3D NAND memory array, and conductors routing output from the 3D NAND memory array. In one embodiment of the technology, the 3D NAND memory array is a vertical gate memory array, and the conductive strips in the stack are NAND transistor channels in the vertical gate memory array. In one embodiment of the technology, the 3D NAND memory array is a vertical channel memory array, and the conductive strips in the stack are word lines in the vertical channel memory array.

[0007] In one embodiment of the technology, the stack of capacitor terminal strips includes a first plurality of capacitor terminal strips alternating with a second plurality of capacitor terminal strips. The first plurality of capacitor terminal strips are electrically connected together and the second plurality of capacitor terminal strips are electrically connected together.

[0008] In one embodiment of the technology, the stack of capacitor terminal strips has a first end and a second end. Multiple capacitor terminal strips in the stack of capacitor terminal strips are electrically connected together at the first end, and multiple capacitor terminal strips in the stack of capacitor terminal strips are electrically connected together at the second end. The embodiment further comprises a conductive plug electrically connected to at least one of the capacitor terminal strips at an intermediate point in between the first end and the second end.

[0009] In one embodiment of the technology, the stack of capacitor terminal strips is one of a plurality of stacks of capacitor terminal strips having lengths between first ends and second ends. The plurality of stacks of capacitor terminal strips include the first plurality of capacitor terminal strips alternating with the second plurality of capacitor terminal strips. The first plurality of capacitor terminal strips in the plurality of stacks of capacitor terminal strips are electrically coupled together via the first ends and at intermediate points in between the first ends and second ends.

[0010] Another aspect of the technology is a computer readable medium comprising a layout for an integrated circuit including designs for a plurality of masks. The integrated circuit includes a 3D NAND memory array with a stack of conductive strips as described herein, and a capacitor with a stack of capacitor terminal strips as described herein. Multiple masks in the plurality of masks each define at least one conductive strip in the stack of conductive strips and at least one capacitor terminal strip in the stack of capacitor terminal strips.

[0011] A further aspect of the technology is a method of making an integrated circuit comprises:

> **[0012]** making a 3D NAND memory array with a stack of conductive strips as described herein, and a stacked capacitor with a stack of capacitor terminal strips as described herein, including:
>
> > **[0013]** in a same etch, defining the stack of conductive strips and the stack of capacitor terminal strips.

[0014] Other features, aspects and advantages of the present invention can be seen on review the figures, the detailed description, and the claims which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. **1** is an end view of stacks of conductive material for both a capacitor and a 3D NAND array on a same substrate.

[0016] FIG. **2** is a side view of a capacitor with a stack of conductive material from FIG. **1**.

[0017] FIGS. **3** and **4** are circuit diagrams of different ways to interconnect individual capacitors in a stack of conductive material, resulting in different overall capacitances of the stack of conductive material as a whole.

[0018] FIG. **5** is a perspective illustration of a three-dimensional, vertical gate NAND-flash memory device with stacks of conductive material from FIG. **1**.

[0019] FIG. **6** is a perspective illustration of an alternative three-dimensional, vertical channel NAND-flash memory device with stacks of conductive material from FIG. **1**.

[0020] FIGS. **7-8** are steps in a process for forming the stacks of conductive material for both a capacitor and a 3D NAND array on a same substrate from FIG. **1**.

[0021] FIG. **9** is a top view of a capacitor with stacks of conductive material, with an overlay of mask regions defining varying etch depths for electrical conductors.

[0022] FIG. **10** is a side view of a capacitor with stacks of conductive material.

[0023] FIGS. **11-14** illustrate a sequence of steps creating electrical conductors at an interconnect region in contact with extensions of the terminal layers, such as shown in the example of FIG. **10**, providing electrical access to a serpentine, stacked plate capacitor assembly.

[0024] FIG. **15** is a simplified block diagram of an integrated circuit with stacks of conductive material for both a capacitor and a 3D NAND array on a same substrate.

[0025] FIG. **16** is a simplified block diagram of a computer system that implements software incorporating aspects of the present technology.

[0026] FIG. **16**A shows a nontransitory computer readable medium storing computer readable data with aspects of the present technology.

DETAILED DESCRIPTION OF THE INVENTION

[0027] The following description will typically be with reference to specific structural embodiments and methods. It is to be understood that there is no intention to limit the invention to the specifically disclosed embodiments and methods but that the invention may be practiced using other features, elements, methods and embodiments. Preferred embodiments are described to illustrate the present invention, not to limit its scope, which is defined by the claims. Those of ordinary skill in the art will recognize a variety of equivalent variations on the description that follows. Like elements in various embodiments are commonly referred to with like reference numerals.

[0028] It is widely recognized that capacitance is very useful electronic circuitry, but is expensive and has manufacturing difficulties when manufactured in semiconductors. Capacitance can be used to help reduce voltage variations and can be used to help save data in memory, such as SRAM, DRAM and Flash, either during normal operations or due to unexpected power failures. While there are system-level products for providing such capacitance, there may be advantages to providing it at the semiconductor level, including system cost, power and reliability.

[0029] FIG. **1** is an end view of stacks of conductive material for both a capacitor and a 3D NAND array on a same substrate. In this end view, the strips of conductive material and strips of insulator extend into and out of the page to the extent of the lengths of the strips of conductive material and strips of insulator.

[0030] The same insulator layer **10** is the base for stacks of conductive material that are in both a capacitor and a 3D NAND array. Insulator layer **10** is over a substrate layer **9**. Stacks **15***a* and **15***b* are included in capacitor devices. Stacks **15***c* and **15***d* are included in a 3D NAND array.

[0031] The zigzag lines through the insulator layer **10** indicate that the capacitor and a 3D NAND array are spaced apart on the same insulator layer **10**. In another embodiment, the stacks are spaced apart on a same conductive substrate, and the bottom of each stack is an insulator strip.

[0032] In stacks **15***a,* **15***b,* **15***c,* and **15***d,* strips of conductive material alternate with strips of insulator. For example, in stack **15***a,* an insulator strip **12***a* electrically insulates proximate strips of conductive material **11***a* and **13***a* in the same stack from each other. Insulator strip **14***a* is above top-most conductive material strip **13***a*. A same arrangement of insulator strips and conductive material strips is in stacks **15***b,* **15***c,* and **15***d.*

[0033] Conductive material strips **13***a*, **13***b*, **13***c*, and **13***d* share a same plane position and thus have a same vertical position relative to each other. Conductive material strips **11***a*, **11***b*, **11***c*, and **11***d* also share a same plane position and thus have a same vertical position relative to each other. Conductive material strips **13***a*, **13***b*, **13***c*, and **13***d* have a different plane position relative to conductive material strips **11***a*, **11***b*, **11***c*, and **11***d*; thus conductive material strips **13***a*, **13***b*, **13***c*, and **13***d* have a different vertical position relative to conductive material strips **11** a, **11***b*, **11** c, and **11***d.*

[0034] In an embodiment where the stacks share a common conductive substrate, the bottom insulator strip on the common conductive substrate isolates the conductive substrate shared by multiple stacks from the bottom-most conductive strip in each stack.

[0035] The strips of conductive material in both the capacitor terminal stacks and the 3D NAND array can be implemented using polysilicon or epitaxial single crystal silicon having n-type or p-type doping. The insulator strips can be implemented for example using silicon dioxide, other silicon oxides, or silicon nitride.

[0036] The 3D NAND array of the integrated circuit includes stacks **15***c* and **15***d* of strips of conductive material. So complexity and cost of the integrated circuit is not appreciably increased from the further inclusion of stacks **15***a* and **15***b* of strips of conductive material as capacitors of the integrated circuit.

[0037] FIG. **2** is a side view of a capacitor with a stack of conductive material from FIG. **1**. In this side view, the strips of conductive material and strips of insulator extend into and out of the page to the extent of the widths of the strips of conductive material and strips of insulator.

[0038] Insulator layer **10** is the base for the stack of conductive material that in a capacitor device. Insulator layer **10** is over a substrate layer **9**. Additional stacks of conductive material for additional capacitor device can be elsewhere on the insulator layer **10**. Also, a 3D NAND array with multiple stacks of conductive material is elsewhere on the insulator layer **10**. In another embodiment, the stack is on a conductive substrate, and the bottom of each stack is an insulator strip. The capacitor suppresses parasitic capacitance by omitting the well-to-substrate capacitance of well capacitors, which could be in the range of about tenths of picofarads.

[0039] In the stack, strips of conductive material alternate with strips of insulator. The stack includes capacitor terminal strip **1 21**, capacitor terminal strip **2 23**, capacitor terminal strip **3 25**, capacitor terminal strip **4 27**, capacitor terminal strip **5 29**, capacitor terminal strip **6 31**, capacitor terminal strip **7 33**, and capacitor terminal strip **8 35**. The stack also includes insulator strip **1 22**, insulator strip **2 24**, insulator strip **3 26**, insulator strip **4 28**, insulator strip **5 30**, insulator strip **6 32**, insulator strip **7 34**, and insulator strip **8 36**. Accordingly, the capacitor terminal strips alternate with insulator strips. An insulator strip electrically insulates proximate strips capacitor terminal strips in the same stack from each other.

[0040] The strips of conductive material in both the capacitor terminal stacks and the 3D NAND array can be implemented using polysilicon or epitaxial single crystal silicon having n-type or p-type doping. The insulator strips can be implemented for example using silicon dioxide, other silicon oxides, or silicon nitride.

[0041] Terminal connection circuit **1 37** and terminal connection circuit **2 38** electrically connect together capacitor terminal strips. Such terminal connection circuits electrically connect the multiple capacitors within the stack in parallel. As discussed below, the parallel connection sums the capacitances of the multiple capacitors within the stack, resulting in a high total capacitance of the stack. Terminal connection circuit **1 37** electrically connects the "odd" capacitor terminal strips, including capacitor terminal strip **1 21**, capacitor terminal strip **3 25**, capacitor terminal strip **5 29**, and capacitor terminal strip **7 33**. Terminal connection circuit **2 38** electrically connects the "even" capacitor terminal strips, including capacitor terminal strip **2 23**, capacitor terminal strip **4 27**, capacitor terminal strip **6 31**, and capacitor terminal strip **8 35**. The stack includes seven capacitors each having a respective one of the insulator strips as the capacitor's intermediate dielectric. The seven capacitors each have two terminals, including a first capacitor terminal which is one of the "odd" capacitor terminal strips, and a second capacitor terminal which is one of the "even" capacitor terminal strips.

[0042] Other embodiments have more or fewer capacitors in the stack. Other embodiments connect in parallel only a subset of the capacitors in the stack. Other embodiments connect in series two or more of the capacitors in the stack. Other embodiments connect in series two or more of the capacitors in the stack, and connect in parallel two or more of the capacitors in the stack. Other embodiments allow one or more of the intermediate terminals to float, to allow more leeway in the layout.

[0043] FIGS. **3** and **4** are circuit diagrams of different ways to interconnect individual capacitors in a stack of conductive material, resulting in different overall capacitances of the stack of conductive material as a whole.

[0044] The example of FIG. **3** has four capacitors connected to electrical conductors **46.0** and **46.1**, **46.2** and **46.3**, **46.4** and **46.5**, and **46.6** and **46.7**. To make one large-capacitance capacitor, the individual capacitors, identified as C_{01}, C_{23}, C_{45} and C_{67} in FIG. **3**, can be placed in parallel. To do so, electrical conductors **46.0**, **46.2**, **46.4** and **46.6** are shorted to one another as a first terminal **47** and electrical conductors **46.1**, **46.3**, **46.5** and **46.7** are shorted to one another as a second terminal **48**. Another example, shown in FIG. **4**, shows each of capacitors C_{01}, C_{23}, C_{45} and C_{67} connected in series. While the total capacitance C_T for the FIG. **4** example is less than the capacitance of any of the individual capacitors, placing the capacitors in series is useful when working with high voltages because each capacitor only sees a fraction of the total voltage. Other embodiments can connect series-connected capacitors and parallel-connected capacitors.

[0045] FIG. **5** is a perspective illustration of a three-dimensional, vertical gate NAND-flash memory device with stacks of conductive material from FIG. **1**. The device illustrated in FIG. **1** includes stacks of active lines in active layers of the array, alternating with insulating lines. Insulating material is removed from the drawing to expose additional structure. For example, insulating lines are removed between the semiconductor lines in the stacks, and between the stacks of semiconductor lines.

[0046] In the example shown in FIG. **1**, a multilayer array is formed on an insulating layer, and includes a plurality of word lines **125-1**, . . . , **125**-N conformal with the plurality of stacks. The plurality of stacks includes semiconductor lines **112**, **113**, **114**, and **115** in multiple planes. Semiconductor lines in the same plane are electrically coupled together by bit line contact pads (e.g. **102**B). The plurality of stacks are formed on a same substrate as stacks in capacitors, as shown in FIG. **1**.

[0047] Bit line contact pads **112**A, **113**A, **114**A, and **115**A are on the near end of the figure terminate semiconductor lines, such as semiconductor lines **112**, **113**, **114**, and **115**. As illustrated, these bit line contact pads **112**A, **113**A, **114**A, and **115**A are electrically connected by interlayer connectors to different bit lines in an overlying patterned metal layer, e.g. ML3, for connection to decoding circuitry to select planes within the array. These bit line contact pads **112**A, **113**A, **114**A, and **115**A can be formed over stepped substrate structures as discussed below, and patterned at the same time that the plurality of stacks is defined.

[0048] Bit line contact pads **102**B, **103**B, **104**B, and **105**B on the far end of the figure terminate semiconductor lines, such as semiconductor lines **102**, **103**, **104**, and **105**. As illustrated, these bit line contact pads **102**B, **103**B, **104**B, and **105**B are electrically connected by interlayer connectors to different bit lines in an overlying patterned metal layer, e.g. ML3, for connection to decoding circuitry to select planes within the array. These bit line contact pads **102**B, **103**B, **104**B, and **105**B can be formed over stepped substrate structures as discussed below, and patterned at the same time that the plurality of stacks is defined.

[0049] In this example, any given stack of semiconductor lines is coupled to either the bit line contact pads **112**A, **113**A, **114**A, and **115**A, or the bit line contact pads **102**B, **103**B, **104**B, and **105**B, but not both. A stack of semiconductor bit lines has one of the two opposite orientations of bit line end-to-source line end orientation, or source line end-to-bit line end orientation. For example, the stack of semiconductor lines **112**, **113**, **114**, and **115** has bit line end-to-source line end orientation; and the stack of semiconductor lines **102**, **103**, **104**, and **105** has source line end-to-bit line end orientation.

[0050] The stack of semiconductor lines **112**, **113**, **114**, and **115** terminated by the bit line contact pads **112**A, **113**A, **114**A, and **115**A, passes through SSL gate structure **119**, ground select line GSL **126**, word lines **125-1** WL through **125**-N WL, ground select line GSL **127**, and is terminated at the other end by source line **128**. The stack of semiconductor lines **112**, **113**, **114**, and **115** does not reach the bit line structures **102**B, **103**B, **104**B, and **105**B.

[0051] The stack of semiconductor lines **102**, **103**, **104**, and **105** terminated by the bit line contact pads **102**B, **103**B, **104**B, and **105**B, passes through SSL gate structure **109**, ground select line GSL **127**, word lines **125**-N WL through **125-1** WL, ground select line GSL **126**, and is terminated at the other end by a source line (obscured by other parts of the figure). The stack of semiconductor lines **102**, **103**, **104**, and **105** does not reach the bit line structures **112**A, **113**A, **114**A, and **115**A.

[0052] A layer of memory material is disposed in interface regions at cross-points between surfaces of the semiconductor lines **112-115** and **102-105** and the plurality of word lines **125-1** through **125**-*n*. Ground select lines GSL **126** and GSL **127** are conformal with the plurality of stacks, similar to the word lines.

[0053] Every stack of semiconductor lines is terminated at one end by bit line contact pads and at the other end by a source line. For example, the stack of semiconductor lines **112**, **113**, **114**, and **115** is terminated by bit line contact pads **112**A, **113**A, **114**A, and **115**A, and terminated on the other end by a source line **128**.

[0054] Bit lines and string select lines are formed at the metal layers ML**1**, ML**2**, and ML**3**. Bit lines are coupled to a plane decoder (not shown) in the peripheral area on the circuit. String select lines are coupled to a string select line decoder (not shown) in the peripheral area on the circuit.

[0055] The ground select lines GSL **126** and **127** can be patterned during the same step that the word lines **125-1** through **125**-n are defined. Ground select devices are formed at cross-points between surfaces of the plurality of stacks and ground select lines GSL **126** and **127**. The SSL gate structures **119** and **109** can be patterned during the same step that the word lines **125-1** through **125**-n are defined. String select devices are formed at cross-points between surfaces of the plurality of stacks and string select (SSL) gate structures **119** and **109**. These devices are coupled to decoding circuitry for selecting the strings within particular stacks in the array.

[0056] FIG. **6** is a perspective illustration of an alternative three-dimensional, vertical channel NAND-flash memory device with stacks of conductive material from FIG. **1**.

[0057] The memory device includes an array of NAND strings of memory cells, and can be a double-gate vertical channel memory array (DGVC). The memory device includes an integrated circuit substrate **201**, and a plurality of stacks of conductive strips alternating with insulating material. The stacks include at least a bottom plane of conductive strips (GSL), a plurality of intermediate planes of conductive strips (WLs), and a top plane of conductive strips (SSLs). The stacks are formed on a same substrate as stacks in capacitors, as shown in FIG. **1**.

[0058] For example, a stack **210** includes a bottom plane of conductive strips (GSL), a plurality of intermediate planes of conductive strips (WLs) ranging from WL_0 to WL_{N-1}, and a top plane of conductive strips (SSLs), where N can be 8, 16, 32, 64 and so on. The insulating material is removed from the drawing to expose additional structure. For example, the insulating material is removed between the conductive strips in the stacks, and is removed between the stacks of conductive strips.

[0059] In the example shown in FIG. **6**, a plurality of bit line structures is arranged orthogonally over, having surfaces conformal with, the plurality of stacks, including inter-stack semiconductor body elements **220** between the stacks and linking elements **230** over the stacks connecting the semiconductor body elements **220**.

[0060] The memory device includes memory elements in interface regions at cross-points **280** between side surfaces of the conductive strips in the plurality of intermediate planes (WLs) in the stacks and the inter-stack semiconductor body elements **220** of the plurality of bit line structures.

[0061] A reference conductor **260** is disposed between the bottom plane (GSL) of conductive strips and the integrated circuit substrate **201**. At least one reference line structure is arranged orthogonally over the plurality of stacks, including inter-stack semiconductor elements **240** between the stacks in electrical communication with the reference conductor **260**, and linking elements **250** over the stacks **210** connecting the inter-stack semiconductor elements **240**. The semiconductor elements **240** can have a higher conductivity than the semiconductor body elements **220**.

[0062] The memory device includes string select switches **290** at interface regions with the top plane of conductive strips, and reference select switches **270** at interface regions with the bottom plane (GSL) of conductive strips.

[0063] In the example shown in FIG. **6**, the memory device can further include decoding circuitry coupled to the conductive strips in the plurality of stacks. The decoding circuitry can include word line decoding circuits, and string selection line decoding circuits coupled to the top plane of conductive strips (SSLs) in the plurality of stacks. String selection lines in the top plane of conductive strips are independently coupled to and controlled by the string selection line decoding circuits.

[0064] Conductive strips in the intermediate planes (WLs), and conductive strips in the bottom plane (GSL) are connected together to reduce decoder areas and consequently an overall size of the memory device. Conductive strips in the top plane (SSL) are individually decoded to allow correct bit line decoding.

[0065] The memory device can include contact pads which provide linking elements, such as contact pads **261** and **262**, connecting sets of word lines in the intermediate planes (WL), and interlayer connectors, such as interlayer connectors **271** and **272**, coupled to landing areas in the contact pads **261** and **262**, and to the word line decoding circuits (not shown). The landing areas are at interface regions between bottom surfaces of the interlayer connectors and top surfaces of the contact pads.

[0066] In the example shown in FIG. **6**, interlayer connectors (e.g. **271** and **272**) for sets of word lines at multiple layers in the plurality of intermediate planes are arranged in a staircase structure, and are connected to landing areas at two different layers in the plurality of intermediate planes. The contact pads can be formed over a stepped substrate structure as described below.

[0067] The staircase structure can be formed in a vertical contact region near the boundary of a memory cell region for the array of memory cells and a peripheral region for components of peripheral circuits. The vertical contact region can include contact pads **261** and **262**, and interlayer connectors **271** and **272**.

[0068] The memory device can include ground selection line decoding circuits coupled to the at least one bottom plane (GSL) of conductive strips in the plurality of stacks. The memory device can include contact pads, such as a contact pad **263**, connecting sets of ground selection lines in the bottom plane (GSL) of conductive strips, and interlayer connectors, such as an interlayer connector **273**, coupled to landing areas in the contact pads, and to the ground selection line decoding circuits (not shown).

[0069] In the example shown in FIG. **6**, the memory device includes a first overlying conductive layer (not shown) connected to the plurality of bit line structures, including a plurality of global bit lines coupled to sensing circuits. The memory device also includes a second overlying conductive layer (not shown) connected to the at least one reference conductor structure, coupled to a reference voltage source.

[0070] Insulating layers in the stack can be the same as or different from the other layers. Representative insulating materials that can be used include a silicon oxide, a silicon nitride, a silicon oxynitride, silicate, or other materials. Low dielectric constant (low-k) materials having a dielectric constant smaller than that of silicon dioxide, such as $SiCHO_x$, can be used. High dielectric constant (high-k) materials having a dielectric constant greater than that of silicon dioxide, such as HfO_x, HfON, AlO_x, RuO_x, TiO_x, can be used also.

[0071] Conductor or semiconductor layers in the stack can be the same as or different from the other layers. Representative materials that can be used include semiconductors including undoped and doped polysilicon (using dopants such as As, P, B), combinations of semiconductor structures, silicides including TiSi, CoSi, oxide semiconductors, including InZnO, InGaZnO, and combinations of semiconductors and silicides. Conductive layers in the stack can also be a metal, a conductive compound, or combinations of materials including Al, Cu, W, Ti, Co, Ni, TiN, TaN, TaA1N, and others.

[0072] FIGS. **7**-**8** are steps in a process for forming the stacks of conductive material for both a capacitor and a 3D NAND array on a same substrate from FIG. **1**.

[0073] In FIG. **7**, a structure is shown which results from alternating deposition of insulating layers **210**, **212**, **214** and semiconductor layers **211**, **213** formed using doped semiconductors for example in a blanket deposition in the array area of a chip. Depending on the implementation, the semiconductor layers **211**, **213** can be implemented using polysilicon or epitaxial single crystal silicon having n-type or p-type doping. A typical thickness range of the semiconductor layers is from 200 to 500 angstroms.

[0074] Inter-level insulating layers **210**, **212**, **214** can be implemented for example using silicon dioxide, other silicon oxides, or silicon nitride. These layers can be formed in a variety of ways, including low pressure chemical vapor deposition LPCVD processes available in the art. The zigzag lines through the insulator layer **210** indicate that the capacitor and a 3D NAND array are spaced apart on the same insulator layer **210**. In another embodiment, the stacks are spaced apart on a same conductive substrate, and the bottom of each stack is an insulator strip.

[0075] FIG. **8** shows the result of a first lithographic patterning step used to define a plurality of ridge-shaped stacks **250** of semiconductor strips, where the semiconductor strips are implemented using the material of the semiconductor layers **211**, **213**, and separated by the insulating layers **212**, **214**. Deep, high aspect ratio trenches can be formed in the stack, supporting many layers, using lithography based processes applying a carbon hard mask and reactive ion etching.

[0076] The same insulator layer **210** is the base for stacks of conductive material that are in both a capacitor and a 3D NAND array. Stack **215***a* is included in a capacitor device. Stack **15***b* is included in a 3D NAND array.

[0077] Conductive material strips **213***a* and **213***b* share a same plane position and thus have a same vertical position relative to each other. Conductive material strips **211***a* and **211***b* also share a same plane position and thus have a same vertical position relative to each other. Conductive material strips **213***a* and **213***b* have a different plane position relative to conductive material strips **211***a* and **211***b*; thus conductive material strips **213***a* and **213***b* have a different vertical position relative to conductive material strips **211** a and **211***b*.

[0078] The zigzag lines through the insulator layer **210** indicate that the capacitor and a 3D NAND array are spaced apart on the same insulator layer **210**. In another embodiment, the stacks are spaced apart on a same conductive substrate, and the bottom of each stack is an insulator strip.

[0079] The various methods typically use a series of deposition and etching steps to do so. Different methods are discussed in Xie, Peng and Smith, Bruce W., *Analysis of Higher-Order Pitch Division for Sub*-32 *nm Lithography,* Optical Microlithography XXII, Proc. of SPIE Vol. 7274, 72741Y, © 2009 SPIE. Multiple patterning methods are also described in U.S. patent application Ser. No. 12/981,121, filed 29 Dec. 2010, entitled MULTIPLE PATTERNING METHOD, having a common assignee and a common inventor with this application.

[0080] Other dielectrics can be used, including low dielectric constant (low-k) materials such as silicon nitride or other low-k dielectrics. In some examples, the capacitor structures can be made on what could be called a rough surface conductor so that the upper portion of substrate **12** and ridges **16** would be made of electrical conductors and thus act as an electrically conductive terminal layer. In general, the conductors can be a metal or combination of metals, include Al, Cu, W, Ti, Co, Ni. The conductors can also be metal compounds, such as TiN/TaN/AlCu, or semiconductor compounds, such as heavily doped Si (using dopants such as As, P, B.); silicides including TiSi, CoSi. Also, typical dielectric materials include SiO_2, SiN, SiON. However, high dielectric constant (high-k) materials having a dielectric constant greater than that of silicon dioxide, such as HfO_x, HfON, AlO_x, RuO_x, TiO_x, are generally preferred. The dielectric materials may also be a multi-layer, such as silicon oxide/silicon nitride, silicon oxide (ONO), silicon oxide, high-k dielectric, silicon oxide (O/high-k/O), which provide higher k values and create less concern about capacitance leakage.

[0081] A suitable deposition technique for dielectric layer **22** would be, for example, atomic layer deposition ALD, high density plasma chemical vapor deposition HDCVD, low density plasma chemical vapor deposition LPCVD, etc., depending on the chosen materials. The process of depositing the terminal layers **20** and dielectric layers **22** proceeds until a desired number of serpentine plate capacitors **18** are created. The size of trench width **26** and the ratio between trench width **26** and ridge height **32** typically limits the number of terminal and dielectric layers **20**, **22**. The size of trench width **26** is usually greater than ridge width **30**.

[0082] FIG. **9** is a top view of a capacitor with stacks of conductive material, with an overlay of mask regions defining varying etch depths for electrical conductors. In this top view, the stacks of conductive strips extend into and out of the page to the extent of the heights of the stacks.

[0083] Shown are the stacks of conductive material **15***e*, **15***f*, **15***g*, **15***h*, **15***i*, **15***j*, **15***k*, and **15***l*. Other embodiments have fewer or more stacks of conductive material. The stacks have lengths with a first end and a second end. The first ends are interconnected electrically by terminal connection circuit **1 37** and the second ends are interconnected electrically by terminal connection circuit **2 38**. Terminal connection circuit **1 37** interconnects "odd" numbered layers of capacitor terminal strips. Terminal connection circuit **2 38** interconnects "even" numbered layers of capacitor terminal strips. Such interconnection can be seen in FIG. **2**.

[0084] The dimensions of the capacitor terminal strips can be sufficiently large such that even the minimal resistance of the conductive strips results in unacceptably long RC delay. An example RC delay calculation of the capacitor in FIG. **2** follows:

$$
\begin{aligned}
RC &= (R)*(C)\\
&= (Rs(L/W)/(\#\text{ layers in parallel}))*\\
&\quad ((\epsilon_0\epsilon_r/\text{thickness})(\text{width length})(\#\text{ capacitors in parallel}))\\
&= (10^5(1.8/1.376)/(4))*\\
&\quad ((8.864\ 10^{-14}\ 3.9/(250\ 10^{-8}))(1.8\ 1.376\ 10^{-8})(7))\\
&= 0.8\text{ nanoseconds}
\end{aligned}
$$

[0085] This example is different in other embodiments, as the variables in other embodiments can be changed: the material which changes Rs and ϵ_r, the dimensions of the material which changes thickness, the layout which changes L and W of the resistance, the # layers in parallel, and the # of capacitors in parallel.

[0086] To decrease the resistance and thus shorten the RC delay, the capacitor terminal strips at different layers can be coupled to terminal connection circuit **1 37** or terminal connection circuit **2 38** not just at ends of the stacks, but also at an intermediate position between the first ends and the second ends. Such more frequent terminal connections are called strap connections. Strap connections reduce the resistance L in the example RC delay calculation.

[0087] The strap connections are defined by the overlay of mask regions defining varying etch depths for the strap connections. Mask region **306** defines an etch depth of **4** layers. Mask regions **302** define an etch depth of 2 layers. Mask regions **304** define an etch depth of 1 layer. In combination, the etch depths vary from 0 layers to 7 layers, depending on the combination of mask regions **302**, **304**, and **306** which overlie each other above particular stacks of conductive material. The conductive material stacks have the following combined etch depths for the strap connections. **15***e* has a 7 layer etch depth, **15***f* has a 6 layer etch depth, **15***g* has a 5 layer etch depth, **15***h* has a 4 layer etch depth, **15***i* has a 3 layer etch depth, **15***j* has a 2 layer etch depth, **15***k* has a 1 layer etch depth, and **15***l* has a 0 layer etch depth.

[0088] FIG. **10** is a side view of a capacitor with stacks of conductive material. The different layers of conductive material are contacted by conductive plugs of different depths. Such an array of conductive plugs can be used as the strap contacts or as the terminal connection circuits in FIG. **9**.

[0089] The staircase plugs can have the same pitch as the stacks of conductive material.

[0090] FIGS. **11-14** illustrate a sequence of steps creating electrical conductors at an interconnect region in contact with extensions of the terminal layers, such as shown in the example of FIG. **10**.

[0091] The different terminal layer extensions **40** are identified in the figures as terminal layer extensions **40.0** through **40.7** with the top most being **40.0**. The locations for the electrical conductors **46** for contact with the corresponding terminal layer extensions **40** are labeled **0** through **7** in the figures. Similar numbering occurs with dielectric layer extensions **42**. When an interconnect region **44** is located at the top of one or more dielectric ridges **16** or at the bottom of one or more trenches **15**, then terminal conductors **46** will directly contact the terminal layers **20** with terminal layer extensions **40** being unnecessary.

[0092] A first photoresist mask **50**, shown in FIG. **11**, is created on dielectric layer extension **42.0** at electrical conductor locations **0**, **2**, **4**, **6** and on the far side of location **7**. The regions covered by photoresist masks are sometimes referred to as mask regions. The regions not covered by first photoresist mask **50**, sometimes referred to as etch regions, are then etched one level through dielectric layer extension **42.0** and terminal layer extension **40.0** to create the structure shown in FIG. **11**. Next, as shown in FIG. **12**, first photoresist mask **50** is removed and then a second photoresist mask **54** is formed on the resulting structure of FIG. **12** to cover electrical conductor locations **0**, **1**, **4**, **5**, and on the far side of location **7**. The structure is then etched two levels at the exposed regions to create the structure shown in FIG. **12**. Next, second photoresist mask **54** is removed and a third photoresist mask **58** is formed to cover electrical conductor locations **0**, **1**, **2**, **3** and on the far side of location **7**. The exposed portions of the structure are then etched four levels to create the structure shown in FIG. **13**.

[0093] Thereafter, third photoresist mask **58** is removed and an optional conformal dielectric barrier layer material can be deposited on the exposed surfaces, including over the stair stepped landing pads **60**, to create a dielectric barrier layer **62**. Barrier layer **62** is used as an etching stop and is can be made of silicon nitride. Dielectric fill layer **24** is deposited on the resulting structure. Appropriate vias are then formed through dielectric fill layer **24** and through the dielectric barrier layer **62** covering the landing pad **60** of each of terminal layer extensions **40.0**-**40.7**. Electrical conductors **46** are then formed in the vias to provide electrical connection with landing pads **60** of terminal layer extensions **40** and thus with terminal layers **20** capacitors to create the structure shown in FIG. **14**. Electrical conductors **46** can be made of the same electrical conductor materials discussed above. However, doped Si, W and Cu may be preferred because of the existing knowledge about chemical mechanical polishing of these electrically conductive materials. Electrical conductors **46** are identified as **46.0**-**46.7** corresponding to locations **0**-**7**.

[0094] More than one interconnect region **44** could be used to access the landing pads **60** at the various levels. Some or all of the landing pads **60** at the different levels could be accessed by the same or different interconnect region **44**.

[0095] The process for creating electrical conductors **46** can be referred to as a binary process, based on $2^0 \ldots 2^{n-1}$ withn being the number of etching steps. That is, first photoresist mask **50** alternatingly covers 2^0 landing pads **60** and exposes 2^0 landing pads **60**; second photoresist mask **54** alternatingly covers 2^1 landing pads **60** and exposes 2^1 landing pads **60**; third photoresist mask **58** alternatingly covers 2^2 landing pads **60** and exposes 2^2 landing pads **60**; and so on. Using this binary process, n masks can be used to provide access to 2^n landing pads **60** for 2^n terminalconductors **46**. Thus, using three masks provides access to 8 landing pads **60** for 8 terminal conductors **46**. Using five masks would provide access to 32 landing pads **60** by 32 electrical conductors **46**. The order of etching need not be in the order of $n-1=0, 1, 2, \ldots$. For example, the first etching step could be with $n-1=2$, the second could be with $n-1=0$, and the third could be with $n-1=1$.

[0096] Further information on similar techniques and methods for connecting electrical conductors **46** to landing pads **60** are disclosed in U.S. patent application Ser. No. 13/049,303, filed 16 Mar. 2011, entitled REDUCED NUMBER OF MASK FOR IC DEVICE WITH STACKED CONTACT LEVELS; and in U.S. patent application Ser. No. 13/114,931, filed 24 May 2011, entitled MULTILAYER CONNECTION STRUCTURE AND MAKING METHOD, the disclosures of which are incorporated by reference. These two applications and the present application have a common assignee.

[0097] FIG. **15** is a simplified block diagram of an integrated circuit with stacks of conductive material for both a capacitor and a 3D NAND array on a same substrate.

[0098] The integrated circuit line **975** includes a 3D NAND flash memory array **960**, implemented as described herein, on a semiconductor substrate with stacks of conductive material and with capacitors with stacks of conductive material. A row decoder **961** is coupled to a plurality of word lines **962**, and arranged along rows in the memory array **960**. A column decoder **963** is coupled to a plurality of SSL lines **964** arranged along columns corresponding to stacks in the memory array **960** for reading and programming data from the memory cells in the array **960**. A plane decoder **958** is coupled to a plurality of planes in the memory array **960** via bit lines **959**. Addresses are supplied on bus **965** to column decoder **963**, row decoder **961** and plane decoder **958**. Sense amplifiers and data-in structures in block **966** are coupled to the column decoder **963** in this example via data bus **967**. Data is supplied via the data-in line **971** from input/output ports on the integrated circuit **975** or from other data sources internal or external to the integrated circuit **975**, to the data-in structures in block **966**. In the illustrated embodiment, other circuitry **974** is included on the integrated circuit, such as a general purpose processor or special purpose application circuitry, or a combination of modules providing system-on-a-chip functionality supported by the NAND flash memory cell array. Data is supplied via the data-out line **972** from the sense amplifiers in block **966** to input/output ports on the integrated circuit **975**, or to other data destinations internal or external to the integrated circuit **975**.

[0099] A controller implemented in this example using bias arrangement state machine **969** controls the application of bias arrangement supply voltage generated or provided through the voltage supply or supplies in block **968**, such as read, erase, program, erase verify and program verify voltages. The controller can be implemented using special-purpose logic circuitry as known in the art. In alternative embodiments, the controller comprises a general-purpose processor, which may be implemented on the same integrated circuit, which executes a computer program to control the operations of the device. In yet other embodiments, a combination of special-purpose logic circuitry and a general-purpose processor may be utilized for implementation of the controller.

[0100] The substrate also includes capacitors with stacks of conductive material **999** on the same substrate as the 3D NAND flash memory array **960**.

[0101] The above descriptions may have used terms such as above, below, top, bottom, over, under, et cetera. These terms may be used in the description and claims to aid understanding of the invention and not used in a limiting sense.

[0102] FIG. **16** is a simplified block diagram of a computer system **110** that implements software incorporating aspects of the present invention. While the present paper indicates individual steps carrying out specified operations, it will be appreciated that each step is actually implemented with software instructions that cause the computer system **110** to operate in the specified manner. The group of software instructions and data to implement a particular step, in conjunction with the processing subsystem and other components of the computer system which enable such software instructions to be executed, constitute a module which implements the particular step.

[0103] Computer system **210** typically includes a processor subsystem **214** which communicates with a number of peripheral devices via bus subsystem **212**. These peripheral devices may include a storage subsystem **224**, comprising a memory subsystem **226** and a file storage subsystem **228**, user interface input devices **222**, user interface output devices **220**, and a network interface subsystem **216**. The input and output devices allow user interaction with computer system **210**. Network interface subsystem **216** provides an interface to outside networks, including an interface to communication network **218**, and is coupled via communication network **218** to corresponding interface devices in other computer systems. Communication network **218** may comprise many interconnected computer systems and communication links. These communication links may be wireline links, optical links, wireless links, or any other mechanisms for communication of information. While in one embodiment, communication network **218** is the Internet, in other embodiments, communication network **218** may be any suitable computer network.

[0104] The physical hardware component of network interfaces are sometimes referred to as network interface cards (NICs), although they need not be in the form of cards: for instance they could be in the form of integrated circuits (ICs) and connectors fitted directly onto a motherboard, or in the form of macrocells fabricated on a single integrated circuit chip with other components of the computer system.

[0105] User interface input devices **222** may include a keyboard, pointing devices such as a mouse, trackball, touchpad, or graphics tablet, a scanner, a touch screen incorporated into the display, audio input devices such as voice recognition systems, microphones, and other types of input devices. In general, use of the term "input device" is intended to include all possible types of devices and ways to input information into computer system **210** or onto computer network **218**.

[0106] User interface output devices **220** may include a display subsystem, a printer, a fax machine, or nonvisual displays such as audio output devices. The display subsystem may include a cathode ray tube (CRT), a flat panel device such as a liquid crystal display (LCD), a projection device, or some other mechanism for creating a visible image. The display subsystem may also provide non visual display such as via audio output devices. In general, use of the term "output device" is intended to include all possible types of devices and ways to output information from computer system **110** to the user or to another machine or computer system.

[0107] Non-transitory storage subsystem **224** stores the basic programming and data constructs that provide the functionality of certain embodiments of the present technology. For example, the various modules implementing the functionality of certain embodiments of the invention may be stored in storage subsystem **224**. Some examples are EDA programs for a cell or layout including stacks of conductive material for NAND memory arrays and capacitors on the same substrate as described herein. These software modules are generally executed by processor subsystem **214**. Storage subsystem **224** also represents storage accessible to the computer system on which the various software mentioned herein are stored. In another embodiment some or all of the software is located on storage accessible to the computer system via the network **218**.

[0108] Memory subsystem **226** typically includes a number of memories including a main random access memory (RAM) **230** for storage of instructions and data during program execution and a read only memory (ROM) **232** in which fixed instructions are stored. File storage subsystem **228** provides persistent storage for program and data files, and may include a hard disk drive, a floppy disk drive along with associated removable media, a CD ROM drive, an optical drive, or removable media cartridges. The databases and modules implementing the functionality of certain embodiments of the invention may have been provided on a computer readable medium such as one or more CD-ROMs, and may be stored by file storage subsystem **228**. The host memory **226** contains, among other things, computer instructions which, when executed by the processor subsystem **214**, cause the computer system to operate or perform functions as described herein. As used herein, processes and software that are said to run in or on "the host" or "the computer", execute on the processor subsystem **214** in response to computer instructions and data in the host memory subsystem **226** including any other local or remote storage for such instructions and data.

[0109] Bus subsystem **212** provides a mechanism for letting the various components and subsystems of computer system **210** communicate with each other as intended. Although bus subsystem **212** is shown schematically as a single bus, alternative embodiments of the bus subsystem may use multiple busses.

[0110] Computer system **210** itself can be of varying types including a personal computer, a portable computer, a workstation, a computer terminal, a network computer, a television, a mainframe, a server farm, or any other data processing system or user device. Due to the ever changing nature of computers and networks, the description of computer system **210** is intended only as a specific example for purposes of illustrating certain embodiments of the present invention. Many other configurations of computer system **210** are possible having more or less components than the computer system depicted.

[0111] FIG. **16**A shows a nontransitory computer readable medium **240** which stores a cell or layout **280** with stacks of conductive material in a NAND array and in a capacitor on a same substrate. The nontransitory computer readable medium can be any of the nontransitory memories discussed in connection with the storage subsystem **224**.

[0112] While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims. Any and all patents, patent applications and printed publications referred to above are incorporated by reference.

1. An integrated circuit comprising:

a substrate;

a 3D NAND memory array with a stack of conductive strips; and

a capacitor with a stack of capacitor terminal strips,

wherein multiple conductive strips in the stack of conductive strips and multiple capacitor terminal strips of the stack of capacitor terminal strips share a same plurality of plane positions relative to the substrate, different plane positions in the same plurality of plane positions characterize different capacitor terminal strips in the stack of capacitor terminal strips and different conductive strips in the stack of conductive strips, and a same plane position characterizing both a conductive strip in the stack of conductive strips and a capacitor terminal strip in the stack of capacitor terminal strips indicates that the conductive strip and the capacitor terminal strip have a same vertical position relative to each other.

2. The integrated circuit of claim **1**, wherein the stack of conductive strips is at least one of: transistor channels in the 3D NAND memory array, conductors routing signals that select memory cells in the 3D NAND memory array, and conductors routing output from the 3D NAND memory array.

3. The integrated circuit of claim **1**, wherein the 3D NAND memory array is a vertical gate memory array, and the conductive strips in the stack are NAND transistor channels in the vertical gate memory array.

4. The integrated circuit of claim **1**, wherein the 3D NAND memory array is a vertical channel memory array, and the conductive strips in the stack are word lines in the vertical channel memory array.

5. The integrated circuit of claim **1**, wherein the stack of capacitor terminal strips includes a first plurality of capacitor terminal strips alternating with a second plurality of capacitor terminal strips, the first plurality of capacitor terminal strips electrically connected together and the second plurality of capacitor terminal strips electrically connected together.

6. The integrated circuit of claim **1**, wherein the stack of capacitor terminal strips has a first end and a second end, multiple capacitor terminal strips in the stack of capacitor terminal strips electrically connected together at the first end, multiple capacitor terminal strips in the stack of capacitor terminal strips electrically connected together at the second end, further comprising:

a conductive plug electrically connected to at least one of the capacitor terminal strips at an intermediate point in between the first end and the second end.

7. The integrated circuit of claim **1**, wherein the stack of capacitor terminal strips is one of a plurality of stacks of capacitor terminal strips having lengths between first ends and second ends, the plurality of stacks of capacitor terminal strips including the first plurality of capacitor terminal strips alternating with the second plurality of capacitor terminal strips, the first plurality of capacitor terminal strips in the plurality of stacks of capacitor terminal strips electrically connected together via the first ends and at intermediate points in between the first ends and second ends.

8-14. (canceled)

15. A method of making an integrated circuit, comprising:

making a 3D NAND memory array with a stack of conductive strips and a capacitor with a stack of capacitor terminal strips, including:

in a same etch, defining the stack of conductive strips and the stack of capacitor terminal strips,

wherein multiple conductive strips in the stack of conductive strips and multiple capacitor terminal strips of the stack of capacitor terminal strips share a same plurality of plane positions relative to the substrate, different plane positions in the same plurality of plane positions characterize different capacitor terminal strips in the stack of capacitor terminal strips and different conductive strips in the stack of conductive strips, and a same plane position characterizing both a conductive strip in the stack of conductive strips and a capacitor terminal strip in the stack of capacitor terminal strips indicates that the conductive strip and the capacitor terminal strip have a same vertical position relative to each other. a 3D NAND memory array with a stack of conductive strips.

16. The method of claim **15**, wherein the stack of conductive strips is at least one of:

transistor channels in the 3D NAND memory array, conductors routing signals that select memory cells in the 3D NAND memory array, and conductors routing output from the 3D NAND memory array.

17. The method of claim **15**, wherein the 3D NAND memory array is a vertical gate memory array, and the conductive strips in the stack are NAND transistor channels in the vertical gate memory array.

18. The method of claim **15**, wherein the 3D NAND memory array is a vertical channel memory array, and the conductive strips in the stack are word lines in the vertical channel memory array.

19. The method of claim **15**, wherein the stack of capacitor terminal strips includes a first plurality of capacitor terminal strips alternating with a second plurality of capacitor terminal strips, the first plurality of capacitor terminal strips electrically connected together and the second plurality of capacitor terminal strips electrically connected together.

20. The method of claim **15**, wherein the stack of capacitor terminal strips has a first end and a second end, multiple capacitor terminal strips in the stack of capacitor terminal strips electrically connected together at the first end, multiple capacitor terminal strips in the stack of capacitor terminal strips electrically connected together at the second end, further comprising:

a conductive plug electrically connected to at least one of the capacitor terminal strips at an intermediate point in between the first end and the second end.

21. The method of claim **15**, wherein the stack of capacitor terminal strips is one of a plurality of stacks of capacitor terminal strips having lengths between first ends and second ends, the plurality of stacks of capacitor terminal strips including the first plurality of capacitor terminal strips alternating with the second plurality of capacitor terminal strips, the first plurality of capacitor terminal strips in the plurality of stacks of capacitor terminal strips electrically connected together via the first ends and at intermediate points in between the first ends and second ends.

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