

Sept. 14, 1965

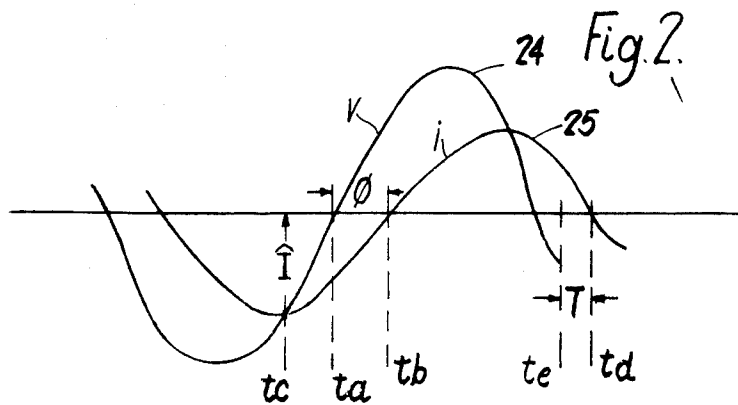
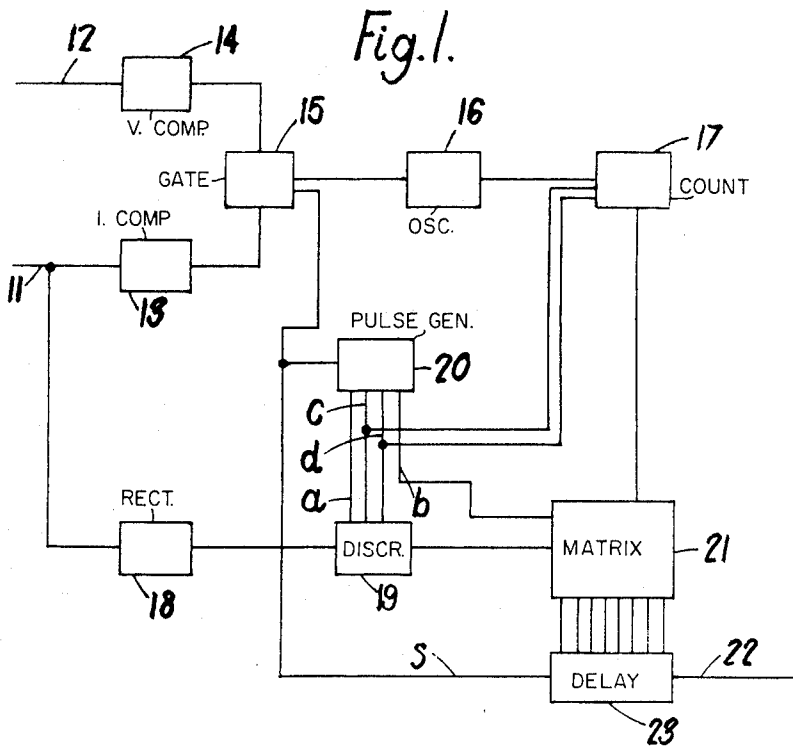
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3,206,642

ELECTRICAL CIRCUIT BREAKERS

Filed July 17, 1962

3 Sheets--Sheet 1



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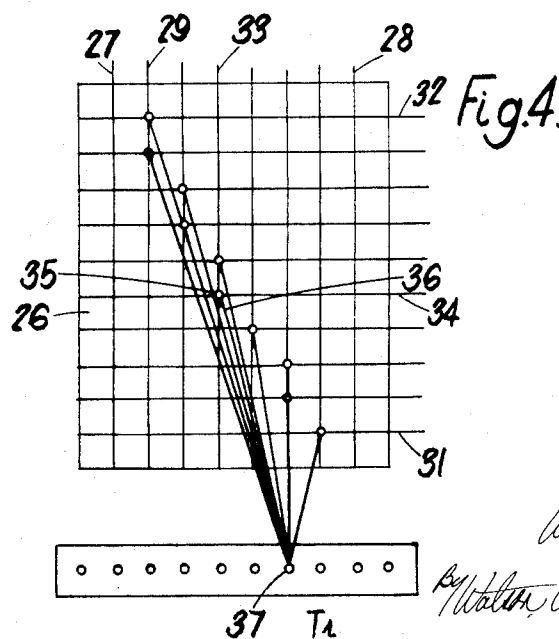
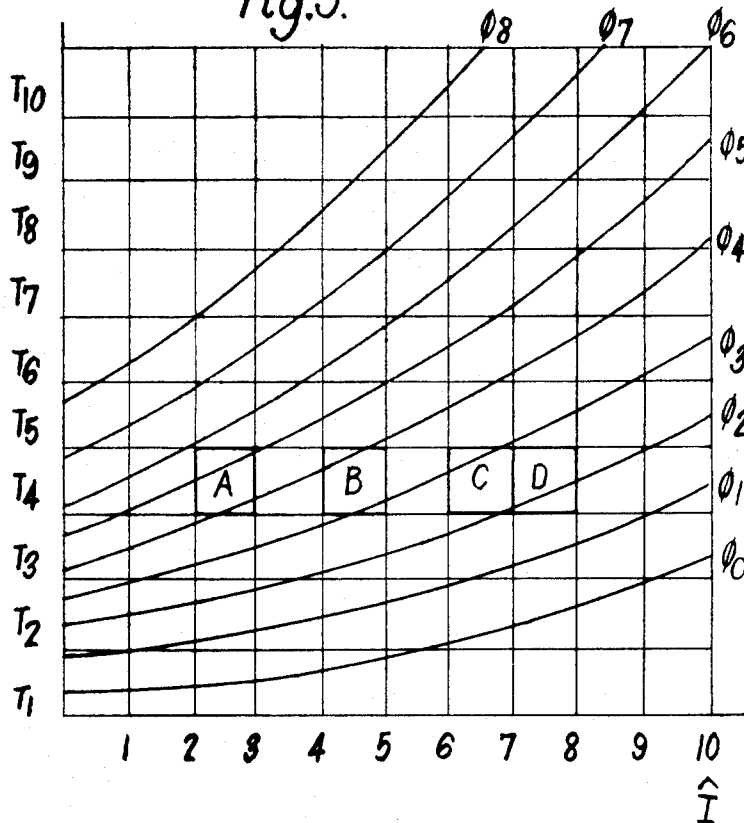
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Fig. 3.



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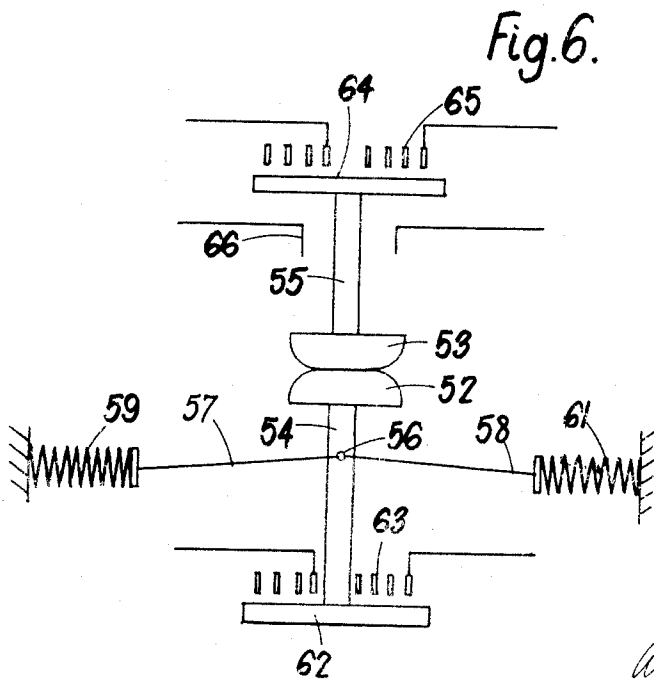
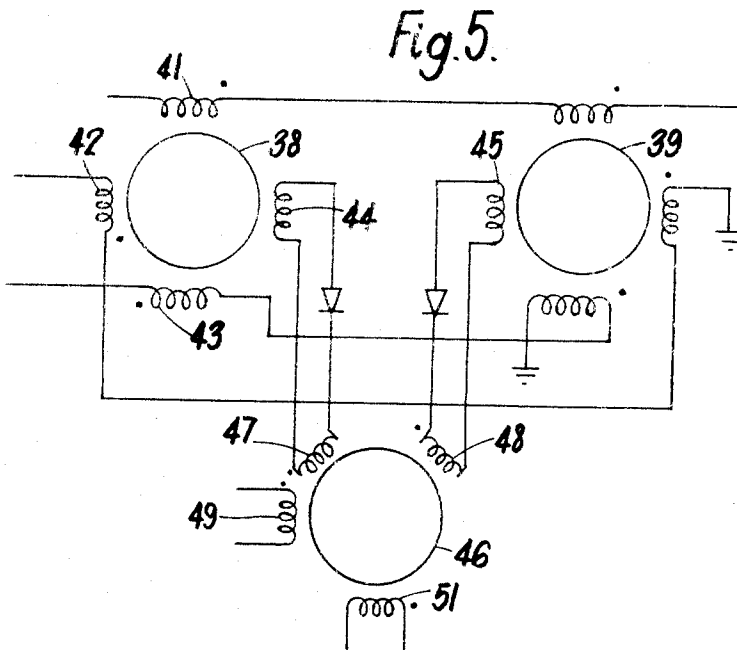
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3 Sheets-Sheet 3



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3,206,642

ELECTRICAL CIRCUIT BREAKERS

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Filed July 17, 1962, Ser. No. 210,457

Claims priority, application Great Britain, July 18, 1961, 26,910/61

9 Claims. (Cl. 317-11)

The invention relates to electrical circuit-breakers for multi-phase or single phase alternating current circuits.

It is one of the objects of the present invention to enable the severity of arcing at circuit-breaker contacts to be reduced. Heretofore it has been the practice to use circuit-breakers which can be operated to open the lines of a single phase or a multi-phase circuit at any instant in the current cycle. However, the degree of arcing at the contacts of a circuit-breaker depends on the timing of the instant of contact separation in the alternating current cycle. If the time interval between contact separation and the subsequent current zero is very short there may not be sufficient arc length at the time of current zero for the gap to withstand the re-striking voltage. The gap insulation will break down and arcing will continue. On the other hand, if the interval is long there is the risk of continued arcing in air-break and oil circuit-breakers, and the risk of current chopping (pre-zero extinction), in air-blast or vacuum types of circuit-breaker.

It would be possible to reduce the severity of arcing by arranging for the various contacts to be opened at fixed times in advance of the current zeroes. However, the optimum time before the current zero for opening the contacts is not constant in a given system and varies with a number of factors, which include the peak value of the sinusoidal current to be interrupted and the phase angle of that current with respect to the line voltage. Thus the optimum time for breaking the alternating current governed by the prevailing circuit conditions may vary with time.

According to one aspect of the invention, there is provided apparatus for controlling the instant of operation of a circuit-breaker operable in response to a control signal to interrupt an alternating current comprising first means for determining a time at which the instantaneous value of the alternating current is zero and computing means responsive to input signals representative of the amplitude of the alternating current and of the phase of the alternating current with respect to the voltage, for determining the optimum time instant at which the circuit breaker should be operated before a current zero and for providing a control signal to operate the circuit breaker at the instantaneous optimum time after the determined current zero.

According to a further aspect of the invention there is provided apparatus for breaking an alternating current carried in a line, comprising a circuit-breaker trippable in response to a control signal to break the alternating current, first means for determining a time at which the instantaneous value of the alternating current is zero and computing means responsive to input signals representative of the amplitude of the alternating current and of the phase of the alternating current with respect to the voltage, for determining the optimum time instant at which the circuit breaker should be operated before a current zero and for providing a control signal to operate the circuit breaker at the instantaneous optimum time after the determined current zero.

Preferably the first means comprises means for measuring the phase angle between the alternating current in the line and the voltage between line and earth or line and neutral.

The arrangement according to the invention enables the switching time of a contact-breaker to be continuously controlled to the optimum value in accordance with such variable factors as the peak current value and the phase angle of the current. Further factors which are preferably taken into account by the computer are concerned with the particular characteristics of the switch employed. The factors which are preferably used to influence timing of the control pulse to the switch are conveniently listed as follows:

(a) The characteristics of the operating mechanism of the circuit breaker;
(b) The acceleration and velocity of the contacts;
(c) The type of arc extinction method which is employed;

(d) The type of circuit-breaker such as air-break, air-blast, oil or vacuum circuit-breaker;

(e) The peak value of sinusoidal current to be interrupted;

(f) The rate of rise of re-striking voltage across the separated contacts at the end of the arcing;

(g) The power factor of the load or fault which is to be disconnected by the operation of the circuit-breaker.

The "law of the circuit breaker," which relates the optimum time of opening the contacts to the factors tested above may be determined empirically by varying some or all of the above factors or it may be predicted.

In accordance with the invention, means are provided whereby the timing of contact separation can be controlled automatically and continuously in service to the optimum value by operating the computing means which is responsive to information on factors such as current amplitude and phase and blend these according to the law of the circuit breaker, so providing correctly delayed impulses to the operating mechanisms. Analogue or digital methods may be employed for the computing means, and although digital methods are described exclusively hereinafter the invention is not restricted thereto.

The apparatus according to the invention may be provided for a single phase or a multi-phase system. In the case of the multi-phase system there is preferably provided a separate single pole circuit-breaker in each line and in breaking the circuit the circuit-breakers are operated in succession. In this case as each circuit-breaker is operated a signal is sent to set the computer for the succeeding circuit-breaker, which is then operated at the appropriate time in the cycle of the alternating current which the circuit-breaker carries.

The invention may provide a complete controlled circuit-breaker unit or a control device which can be arranged to operate an existing circuit-breaker. The type of circuit-breaker which is envisaged for use with the control apparatus according to the invention may be an air-break, air-blast or oil circuit-breaker, or more particularly a vacuum circuit-breaker. However, in either case, in order to take advantage of the automatic control provided by the invention, each circuit-breaker which is controlled must be a high speed circuit-breaker, that is to say a circuit-breaker in which the acceleration and velocity of the moving contact or contacts are sufficiently large that the arc which develops on separating the contacts can be extinguished at the first current zero after contact separation and remain extinguished.

There follows a description of a specific embodiment of the invention in which reference will be made to the accompanying drawings, of which:

FIGURE 1 is a block diagram of a control device according to the invention.

FIGURE 2 is a waveform diagram of line current and reference voltage in the line to be broken,

FIGURE 3 is a graph illustrating the law of the circuit-breaker,

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FIGURE 4 is a schematic diagram of the matrix of FIGURE 1,

FIGURE 5 is a circuit diagram of part of the amplitude discriminator of FIGURE 1, and

FIGURE 6 is a schematic diagram of the mechanism of the circuit-breaker which breaks the circuit.

FIGURE 1 shows a control device for actuating a circuit-breaker at an appropriate time in the cycle of the alternate current to be broken. The pattern of events to be described in the breaking of the circuit is initiated either manually when it is desired to break the circuit or automatically when a fault develops and it is necessary to break the circuit.

With reference to FIGURE 1, there is shown a control device having two inputs 11 and 12. Input 11 carries a sinusoidal signal which is proportional in amplitude and phase to the load or fault current in the line which is to be broken, whereas input 12 carries a sinusoidal signal which is proportional in amplitude and phase to the voltage on the line with respect to neutral or earth. Means for deriving a current which is proportional to the load or fault current may comprise a current transformer or a Hall effect device. The current and voltage signals are applied respectively to comparators 13 and 14 which compare the instantaneous values thereof with reference values of zero and give outputs when the instantaneous values are zero. These outputs are applied to two inputs of a gate circuit 15 which is arranged to give a square output pulse which originates when a pulse is received from comparator 14 and which ceases when a pulse is received from the comparator 13, the length of the output pulse from gate 15 thereby representing the phase-angle difference between the current to be broken and the reference voltage. The output from gate 15 is arranged to trigger a blocking oscillator 16 which gives an output of a number of pulses which is dependent upon the length of the output pulse from gate 15. These pulses are counted and stored in a counter 17.

The signal on input 11 is applied also to a half-wave rectifier 18 and the output thereof to an amplitude discriminator 19. Discriminator 19 is arranged to give an output representative of the peak amplitude of the line current to be broken. The information concerning phase angle and amplitude of the current is fed to a logic matrix 21 which in accordance with a predetermined pattern dependent upon the characteristics of the circuit-breaker uses the information to send a triggering pulse to the operating mechanism over a line 22 at the appropriate time in the current cycle. The timing is effected by feeding an input pulse to a system of delay channels 23 at an appropriate point, the output from the appropriate delay channel being fed to the operating mechanism.

On cessation of the square pulse from the output of gate 15, a pulse is sent to activate a timing pulse generator 20 which generates timing pulses to trigger and re-set the various circuit elements at appropriate times. The timing operation of the pulse generator will be described more fully later.

FIGURE 2 shows the waveform diagram 24 of the voltage applied to input 12 of FIGURE 1 and the waveform 25 of the current signal applied to input 11 of FIGURE 1. With reference to the timing shown in FIGURE 2, the operation of the circuit of FIGURE 1 is as follows. At time t_a the voltage comparator 14 registers that the voltage is zero and a pulse is applied to gate 15 to start the rectangular output pulse therefrom. This rectangular output pulse is stopped at time t_b when the current is zero and an output is obtained from comparator 13. The current had previously reached its maximum value of $\hat{I}$ and this was measured and applied to matrix 21 by discriminator 19. The matrix in accordance with the maximum current value and the characteristics of the circuit-breaker determines the optimum time T at which the circuit-breaker should be triggered before the time t_d of the next

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current zero, and the delay channel system 23 is energized to give a triggering pulse to the circuit-breaker at time t_c .

FIGURE 3 is a graph embodying the law of the circuit-breaker, and comprising plots of maximum current against optimum delay time for various phase angles. The various values are quantized in the matrix 21. It will be seen from the graph that, for instance, should the current amplitude lie between 2 and 3 units and the phase angle between ϕ_4 and ϕ_5 the required time delay for the switch is T_4 . This combination of conditions is represented at square A. This combination is not unique for requiring a time delay of T_4 as is shown at square B where the current amplitude lies between 4 and 5 units and the phase angle between ϕ_3 and ϕ_4 . Further, squares C and D show that a time delay of T_4 is required should the phase angle lie between ϕ_2 and ϕ_3 and the current amplitude between 6 and 8 units. The graph of FIGURE 3 is plotted on the basis of data obtained empirically.

Turning now to FIGURE 4, there is shown in greater detail the logic matrix arrangement of unit 21 of FIGURE 1. The phase angle information is fed into a matrix 26 of AND gates from counter 17 on lines 27 to 28. A phase angle of between ϕ_0 and ϕ_1 (FIGURE 3) is indicated by a signal on line 27, and an angle between ϕ_1 and ϕ_2 by a signal on line 29. The phase angles are represented in order on the successive lines, a signal or line 28 representing an angle between ϕ_7 and ϕ_8 . Similarly, lines 31 to 32 carry information regarding the maximum current in the line, a signal on line 31 representing a current between 0 and 1 unit (FIGURE 3) and a signal on line 32 representing a current lying between 9 and 10 units.

At every junction of the matrix lines there is provided an AND gate, although the only ones shown in FIGURE 3 are those relevant to the time interval T_4 . As an example, let there be simultaneous signals applied to lines 33 and 34 indicating respectively that the phase angle lies between ϕ_3 and ϕ_4 and that the maximum current lies between 4 and 5 units (FIGURE 3). The simultaneous application of signals on these lines will activate the output of the AND gate 35. This output is applied over a line 36 to an OR gate 37 which then gives an output to the delay system 23 of FIGURE 1 and gives rise to a delay in the circuit-breaker operation of appropriate time. In this case, the appropriate time is T_4 , as shown in the graph of FIGURE 3, and the OR gate 37 has its output connected to give only this timing T_4 .

All the other AND gates of the matrix which are shown in FIGURE 3 are connected to gate 37 whereby on activation of any one of these AND gates a time delay of T_4 is effected. No other AND gate of the matrix is connected to the OR gate 37 however, since activation of any of these other AND gates will require a different time delay and they are associated with their respective OR gates, there being 10 OR gates, corresponding to a time delay of T_1 to T_{10} respectively.

Thus it will be seen that the time of operation of the circuit-breaker is governed by the phase angle and the maximum current value taken in conjunction with the characteristics of the switch, these characteristics being set by connections between the AND and OR gates in the matrix to correspond with the empirically determined requirements illustrated in FIGURE 3.

The quantized information regarding the phase angle is derived from the pulse counter 17 (FIGURE 1). This counter comprises a binary counter for counting the pulses, the output of which is fed to a binary to decimal decoding circuit. The decoding circuit has eight outputs corresponding to the eight intervals of phase angle into which the possible range is subdivided for the present purpose. The decoding circuit is arranged to give a signal on one of its eight outputs in accordance with the interval within which the count lies.

FIGURE 5 shows in greater detail part of the ampli-

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tude discriminator shown at 19 in FIGURE 1. The part shown in FIGURE 5 determines whether the maximum current lies between two values I_1 and I_2 . The whole discriminator is built up of like units which determine whether the maximum current lies between two particular values, the particular values being arranged so that the whole range of possible current values is built up in adjacent increments.

In FIGURE 5 there are shown two closed loops 38, 39 of magnetic material having a substantially square loop hysteresis characteristic such as, for example, ferrite. Considering loop 38 there is shown a magnetising winding 41 therefor which is supplied from the half-wave rectifier 18 (FIGURE 1) and carries half-wave rectified current of magnitude proportional to the line current to be interrupted. A re-setting winding 42 is connected so that when supplied with a re-setting pulse the core 38 is magnetised with a flux in a counter-clockwise direction. The core is thus re-set before the half-wave to be measured and on passage of this half-wave the flux induced thereby tends to oppose the flux already established by the re-setting winding. If the half-wave current is sufficiently large the flux in core 38 will be reversed. A testing winding 43 is arranged so that when a testing pulse is applied therein the flux induced is in a clockwise direction and a read-out winding 44 is provided to detect any change in flux direction when the testing pulse is applied. Thus if the half-wave rectified current were sufficiently strong to reverse the flux due to the re-setting winding 42 there will be no output in the read-out winding because the flux in the core 38 will not be changed by the testing pulse. However, if the half-wave current is too weak, that is, the peak amplitude lies below a predetermined value, then there will be such an output on testing, because the flux due to the re-setting winding will not have been reversed by the half-wave current but will have been reversed by the testing pulse.

Similar windings are provided for core 39 with the difference that the sense of the testing winding is opposite to that of the half-wave current winding. Thus an output is given in the read-out coil 45 of this core only if the half-wave rectified current is above a predetermined value. The two predetermined values of half-wave rectified current which effect switching in the two cores are made different by arranging that the number of turns in the respective windings are different, the number of turns for core 39 being greater than the number of turns for core 38. Alternatively the numbers of turns on the cores can be the same but the current differently scaled by separate current transformers or Hall effect devices. The predetermined currents for the cores may be designated I_1 for core 39 and I_2 for core 38. It will be seen that outputs will be obtained simultaneously from read-out coils 44 and 45 only if the peak amplitude of the half-wave rectified current lies between I_1 and I_2 . The output from coils 44 and 45 are fed to an AND gate which gives an output only if these two conditions are simultaneously fulfilled, therefore if the peak amplitude of the half-wave rectified current lies between I_1 and I_2 .

The AND gate comprises a further core of ferrite 46 which is provided with two input windings 47, 48, fed respectively from windings 44 and 45. A re-set winding 49 is provided to re-set the flux in the core 46 in a direction opposite to that which is induced by currents in the windings 47 and 48, which are wound in the same sense. The windings 47 and 48 are arranged so that if, and only if, inputs are applied thereto simultaneously will the re-set flux be reversed in the core 46. In this case, an output is obtained in a read-out coil 51.

The succeeding unit of the amplitude discriminator 19 to that shown in FIGURE 5 would have its lower limit of current as I_2 and its upper limit as say I_3 , an output from its AND gate being obtained when the peak amplitude of half-wave rectified current lies between I_2 and I_3 . In this way the whole range of current amplitude which it is de-

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sired to measure is built up in increments, an output being obtained from a different gate for a different interval. The outputs from the gates are applied respectively to lines 31 to 32 (FIGURE 4) of the matrix.

Referring again to FIGURE 1, the synchronising action of pulse generator 20 is as follows. At the current zero a pulse is fed to the input of generator 20 whereupon an output pulse is applied over line *a* to discriminator 19 to test the comparator cores such as 38 and 39 (FIGURE 5). A pulse is then sent over line *b* to re-set the gates of the matrix. Thirdly a trigger pulse is applied over line *c* to trigger the AND gate cores of the discriminator 19 and to trigger the counter 17 to give its output to the matrix 21. Thus simultaneous signals are applied to the matrix lines of the logic matrix 21, and one of the AND gates thereof is activated, so opening the appropriate OR gate of the delay system 23. The delays are synchronised with the current zeroes by a pulse received at the current zeroes from gate 15 over a synchronising line *s*, and will produce a control pulse to the circuit-breaker mechanism over line 22 before the next current zero with a timing advance dependent upon which OR gate of the matrix is opened. The final pulse in the sequence from generator 20 is applied to line *d* to re-set the counter 17 and the discriminator 19. The pulse generator 20 is a constant-current pulse generator with a silicon-controlled-rectifier switched output to produce the groups of four pulses, the spacing, rise-time and duration of which are controllable.

FIGURE 6 is a schematic diagram of the circuit-breaker used in conjunction with the control apparatus. Contacts 52 and 53 are normally held together by spring pressure and carry the line current. The contacts 52 and 53 are carried at the ends of coaxial shafts 54 and 55 respectively. Shaft 54 is pivotally connected at a pivot 56 with two toggle arms 57 and 58 which bear at the ends remote from pivot 56 against compression springs 59 and 61 respectively. The end of shaft 54 remote from the contact 52 carries an electrically conductive disc 62 arranged parallel to and adjacent a spiral coil 63 of heavy gauge wire. A similar conductive disc 64 and coil 65 is provided for shaft 55.

In order to break the circuit an operating current is passed from the control device through the spirals 63 and 65. Eddy currents are induced in the discs 62 and 64 in such directions as to repel the discs away from their respective coils. The discs, shafts and contacts move bodily downwardly (in the figure) against the compression of springs 59 and 61. With sufficient movement the toggle arms become co-linear and thereafter the springs aid the downward movement of the switch mechanism. During the downward movement the disc 64 is brought to rest against a stop 66, thus bringing contact 53 abruptly to rest. However, contact 52 is not so brought to rest and the combination of magnetic repulsion and spring compression forces it way from contact 53. This arrangement affords a particularly clean and rapid circuit-breaking action. The operating current for the spiral coils is conveniently the discharge current of a charged capacitor, the discharge of which is initiated through a spark gap in response to the output of the delay line.

The invention is not restricted to the details of the above exemplary description of one embodiment thereof.

I claim:

1. Apparatus for controlling the instant of operation of a circuit-breaker operable in response to a control signal to interrupt the current of an alternating signal comprising:

means responsive to the alternating signal for developing a first output signal representative of the phase of the alternating current with respect to the alternating voltage of said alternating signal,
means responsive to said alternating current for developing a second output signal representing the amplitude of the alternating current, and
means responsive to said first and second output sig-

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nals for determining the optimum time instant at which the circuit-breaker should be operable before a current zero and for providing a control signal to operate the circuit-breaker at the instantaneous optimum time after the determined current zero.

2. Apparatus as in claim 1 wherein:

said first output signal developing means includes means for providing a given signal indicating a time at which the instantaneous value of the alternating current is zero, and

said means responsive to said first and second output signals including means for logically determining the said optimum time instant and delay means controlled by said logical determining means and by said given signal for providing said control signal.

3. Apparatus as in claim 1 wherein the said first output signal developing means comprises means for measuring the phase angle between the alternating current in the line and the voltage between line and earth or line and neutral.

4. Apparatus as claimed in claim 3 wherein the said second output signal developing means include means for measuring the peak amplitude value of the alternating current and the said first and second output signal responsive means includes means for correlating the measured value of peak current with the measured phase angle in conjunction with operating characteristics of the circuit-breaker to determine the said instantaneous optimum time at which the circuit-breaker should be operated.

5. Apparatus as claimed in claim 4 wherein the said first and second output signal responsive means employs digital techniques, the said output signals being represented and correlated in quantized form.

6. Apparatus as claimed in claim 5 wherein the said first and second output signal responsive means comprises a matrix of AND gates each gate having two inputs, one input being energised if the phase angle lies in a particular interval in the range of possible values and the other input being energised if the peak current amplitude lies within a particular interval in the range of possible values, any particular combination of phase angle and peak current amplitude giving rise to a response from only one AND gate, the outputs of each AND gate being connected in accordance with the characteristics of the contact-breaker to apply an appropriately timed control signal thereto.

7. Apparatus for breaking the current of an alternating signal carried in a line, comprising:

a circuit-breaker operable in response to a control signal to break the said alternating current,

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means responsive to the alternating signal for developing a first output signal representative of the phase of the alternating current with respect to the alternating voltage of said alternating signal,

means responsive to said alternating current for developing a second output signal representing the amplitude of the alternating current, and

means responsive to said first and second output signals for determining the optimum time instant at which the circuit-breaker should be operable before a current zero and for providing a control signal to operate the circuit-breaker at the instantaneous optimum time after the determined current zero.

8. Apparatus for controlling the instants of operation of a number of circuit-breakers, one for each alternating line signal of a multi-phase system, the line currents of which are broken in succession, each circuit-breaker being operable in response to a control signal to interrupt the current of the associated alternating signal, which apparatus comprises:

means responsive to each said alternating signal for developing first output signals representative of the phase of the alternating current of each line with respect to the alternating voltage thereof,

means responsive to each said alternating current for developing second output signals representing the amplitude of the respective alternating current, and means responsive to said first and second output signals for determining the optimum time instant at which each circuit-breaker should be operated before a current zero of that line and for providing a control signal to operate that circuit-breaker at the instantaneous optimum time after the determined current zero in that line.

9. Apparatus as claimed in claim 8 wherein, upon breaking of one line current, a signal is sent to set the output signal responsive means for operation at the appropriate time of the succeeding circuit-breaker.

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