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STRUCTURE AND METHOD FOR MANUFACTURING THE SAME

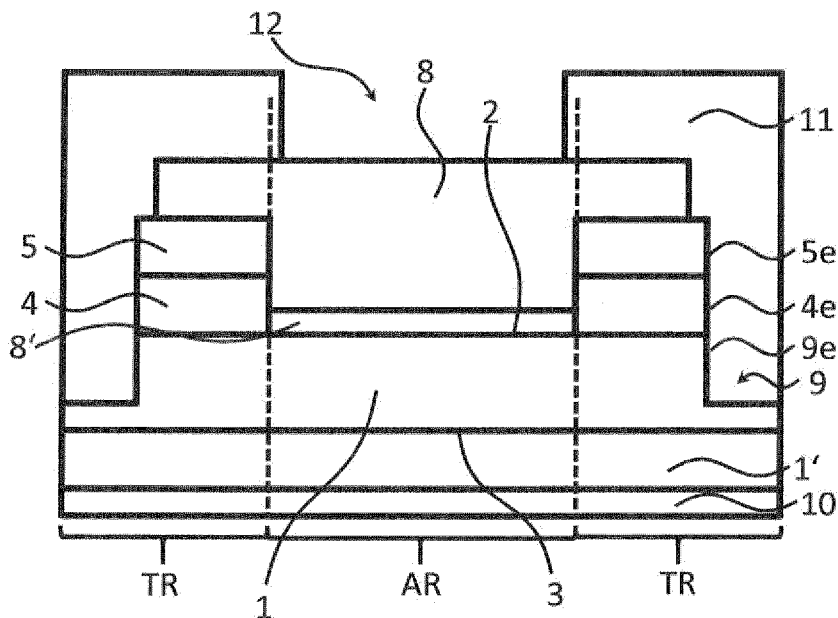


Fig. 1A

(57) Abstract: A power semiconductor device comprises: a wide-bandgap semiconductor layer (1) extending in a lateral direction and comprising an active region (AR) and a termination region (TR) surrounding the active region (AR); a first recess (9) recessed from the first main side (2) in the termination region (TR) and surrounding the active region (AR); a field plate (5) on the first main side (2) of the wide-bandgap semiconductor layer (1) and exposing a first portion of the wide-bandgap semiconductor layer (1) in the termination region (TR); and a sidewall (9e) of the first recess adjacent to the active region (AR) being laterally aligned with a circumferential edge (5e) of the field plate (5).

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Description

5 **High power semiconductor device with self-aligned field plate and mesa termination structure and method for manufacturing the same**

FIELD OF THE INVENTION

10 The present invention relates to a wide-bandgap high power semiconductor device with effective edge termination comprising a field plate and a recess in the termination region (mesa termination structure) and to a method for manufacturing the same.

BACKGROUND OF THE INVENTION

15 Wide-bandgap (WBG) semiconductor materials such as silicon carbide (SiC), gallium nitride, gallium oxide, boron nitride, aluminum nitride, zinc oxide, diamond etc. allow to make semiconductor devices more powerful and energy efficient than those made from conventional semiconductor materials.

20 However, high power semiconductor devices based on wide-bandgap semiconductor materials require an efficient edge termination to avoid electric field crowding at the edge of the main contact resulting in breakdown of the device at a relatively low breakdown voltage VBR.

 Edge termination may be provided in various ways including floating field rings, junction termination extension (JTE), field plates, mesa structures or some combination of these techniques.

25 Floating field rings are produced annularly around the active region of the semiconductor device. The generation of floating field rings can be easily integrated in the manufacturing process since the floating field rings can be formed simultaneously with a main junction in many power semiconductor devices. On the other hand, the design of a high performance floating field ring termination is very challenging given the high number of factors (e.g. ring spacing) affecting the most
30 important trade-off between breakdown voltage and occupied wafer area.

Junction termination extension (JTE) is based on the controlled addition of opposite charges by ion implantation into the surface of the semiconductor layer provided as the drift region. JTE techniques provide good termination efficiencies. However, ion implantation in wide-bandgap materials is more difficult than in conventional semiconductor materials. Moreover, the implantation steps require high temperature implantation facilities and an annealing oven especially designed for activation of such wide-bandgap materials, which makes the fabrication comparably costly. Also the quality of the semiconductor surface and therewith the device yield has been found to be degraded during the activation.

10 Bearing in mind the technologically difficult and expensive processing, besides the processing cost reduction, an implantation free design would enable fabrication of wide-bandgap material based rectifiers in conventional silicon cleanrooms.

The field plating technique provides relative simplicity in process requirements. It is based on a metal layer positioned upon a dielectric layer. The field plate modifies the surface potential at the edge of the main contact (active region). As a result the depletion zone is extended and thus the electrical field as well. The electric field crowding at the edge of the main contact is reduced and shifted towards the edge of the field plate. There however, due to the increasing electric field crowding, the risk of dielectric failure increases, thus limiting the achievable electrical breakdown voltage. In high power devices the problem of dielectric failure is more pronounced than in conventional silicon devices as the critical electric field crowding is almost one order of magnitude larger than in conventional silicon devices.

25 Mesa structure edge termination is another edge termination technique with rather simple process requirements. The technique consists of taking away material and therefore electric charges at the circumferential edge of the main contact by mechanically removal or etching of the semiconductor layer.

From the article "A new edge termination technique for SiC power devices" by Shuntao Hu et al., Solid State Electronics 48 (2004) pp1861-1688, there is known an edge termination technique based on a metal structure overlapping a dielectric filled mesa structure formed in a SiC epilayer. Compared to traditional field plate technique without mesa structure, field crowding at the metal corner can be alleviated by this configuration. Nevertheless premature breakdown occurs before

an ideal breakdown voltage is achieved. This is because field crowding is caused by the difference in dielectric constant between SiC layer and the dielectric layer. To alleviate this effect, it is further proposed in this article to add another dielectric layer on top of the dielectric filled mesa with additional metal field plate extension overlapping the mesa structure. With this modification, in simulation, 80 % of the ideal breakdown voltage is achieved.

From US 2011/0101369 A1 it is known a gallium nitride based semiconductor power device disposed in a semiconductor substrate. The power device comprises a termination area with a mesa shape disposed at a peripheral area of the semiconductor power device, a field plate, and a termination structure having at least a guard ring disposed in a trench filled with doped gallium-based epitaxial layer therein.

SUMMARY OF THE INVENTION

The present invention was made in view of the prior art described above, and the object of the present invention is to provide a wide-bandgap high power semiconductor device with more effective edge termination.

The object of the invention is attained by a power semiconductor device comprising a wide-bandgap semiconductor layer having a first main side and a second main side opposite to the first main side, wherein the first main side and the second main side extend in a lateral direction and wherein the wide-bandgap semiconductor layer comprises an active region and a termination region laterally surrounding the active region, wherein the wide-bandgap semiconductor layer has a first recess, which is recessed from the first main side in the termination region and which surrounds the active region; a field plate on the first main side of the wide-bandgap semiconductor layer exposing a first portion of the wide-bandgap semiconductor layer in the termination region. A sidewall of the first recess adjacent to the active region is laterally aligned with a circumferential edge of the field plate such that in an orthogonal projection onto a plane parallel to the first main side an edge of the recess defined by the upper end of the sidewall is within less than 1 μm from the circumferential edge of the field plate, exemplarily less than 0.5 μm , exemplarily less than 0.2 μm . The power semiconductor device according to the invention is

characterized in that the wide-bandgap semiconductor layer has a second recess in the active region which is recessed from the first main side of the wide-bandgap semiconductor layer and filled with a filling material and a depth of the second recess is the same as a depth of the first recess.

- 5 Throughout the specification a wide-bandgap semiconductor refers to a semiconductor which has a bandgap larger than 2 eV. Moreover, a “lateral direction” refers to a direction parallel to the first main side and “laterally” means relating to a lateral direction. “Upper” means being at a higher level with respect to the second main side in a direction towards the first main side. A sidewall being
10 adjacent to the active region means a sidewall of the first recess closest to the active area and its surface facing away from the active region. A first layer “exposing” a second layer means that the first layer is not formed in areas where the second layer is exposed with respect to the first layer. It does not exclude that one or more additional layers are formed on the second layer.
- 15 The field plate extends the depletion region of the device in lateral direction reducing the magnitude of the electrical field in the active region and shifting the location of the high field region (zone of critical field crowding) away from the periphery of the active region (below the edge of the contact electrode) towards the area below the edge of the field plate. The first recess forms a mesa-type edge
20 termination. By aligning the sidewall of the first recess with the circumferential edge of the field plate, the mesa edge termination efficiently reduces the critical field crowding in the region below the circumferential edge of the field plate for a given voltage. Thus, a higher breakdown voltage can be achieved. As a result, an efficient edge termination is provided. The second recess may reduce leakage currents.
- 25 Further developments of the invention are specified in the dependent claims.
- In an exemplary embodiment the device comprises a dielectric layer interposed between the field plate and the wide-bandgap semiconductor layer to separate the field plate from the wide-bandgap semiconductor layer. The dielectric layer amplifies the effect of the field plate and provides additional electric field relief. The
30 dielectric layer may contain a high field region that exists between the field plate and the wide-bandgap semiconductor layer. The dielectric layer may also reduce the critical field crowding below the circumferential edge of the field plate.

In an exemplary embodiment of the device a thickness of the dielectric layer perpendicular to the lateral direction decreases with increasing lateral distance from the first recess. This feature may further improve the performance of the field plate. A smaller thickness of the dielectric layer increases the field plate's effect on the wide-bandgap semiconductor layer, hence reducing the magnitude of the electrical field in the active region more efficiently; a larger thickness of the dielectric layer provides better protection against voltage breakdown due to dielectric failure. Having a dielectric layer with increasing thickness towards the periphery may provide a higher breakdown voltage by reducing the critical field crowding in the periphery of the active region and shifting it towards the circumferential edge of the field plate, whilst reducing the risk of dielectric failure at this location by means of a thicker dielectric layer.

In an exemplary embodiment the dielectric layer has a thickness adjacent to the first recess which is in a range between 0.02 μm and 1 μm , exemplarily between 0.02 μm and 0.5 μm and more exemplarily between 0.02 μm and 0.3 μm .

The thickness of the dielectric layer may be smaller than in state of the art devices because the field relief due to the mesa structure reduces the risk of voltage breakdown caused by dielectric failure. A thinner dielectric layer is beneficial for reducing the field crowding at the periphery of the active region.

In an exemplary embodiment the field plate comprises at least one of aluminum, nickel, tungsten, and chromium. A field plate comprising one of these materials has beneficial properties in view of a fabrication method detailed later.

In an exemplary embodiment the depth of the first recess may be at least 4 μm , exemplarily at least 6 μm .

The depth of the recess determines the magnitude of the electrical field reduction. The deeper the recess, the more suppressed is the electric field crowding and thus the higher the breakdown voltage which can be achieved.

In an exemplary embodiment, the wide-bandgap semiconductor layer comprises one of silicon carbide (SiC), gallium nitride (GaN) and gallium oxide (Ga_2O_3). These materials are particularly appropriate for forming a wide-bandgap semiconductor layer.

The object of the invention is also attained by a method for manufacturing a power semiconductor device. The method comprising the following steps: providing a wide-bandgap semiconductor layer having a first main side and a second main side opposite to the first main side, wherein the first and the second main side extend in a lateral direction and wherein the wide-bandgap semiconductor layer comprises the active region and the termination region laterally surrounding the active region; forming a field plate on the first main side of the wide-bandgap semiconductor layer, the field plate exposing a first portion of the first main side of the wide-bandgap semiconductor layer in the termination region; and anisotropic etching of the wide-bandgap semiconductor layer in areas where the field plate exposes the first portion of the first main side of the wide-bandgap semiconductor layer in the termination region to form a first recess in the wide-bandgap semiconductor layer in the termination region wherein the first recess surrounds the active region and a sidewall of the first recess adjacent to the active region is laterally aligned with a circumferential edge of the field plate such that in an orthogonal projection onto a plane parallel to the first main side the edge of the recess defined by the upper end of the sidewall is within less than 1 μm from the circumferential edge of the field plate, exemplarily less than 0.5 μm , exemplarily less than 0.2 μm . The method according to the invention is characterized in that the step of forming the field plate comprises: forming a dielectric layer on the first main side of the wide-bandgap semiconductor layer; forming a metal layer on the dielectric layer; and patterning the metal layer and the dielectric layer to expose at least the first portion of the first main side of the wide-bandgap semiconductor layer in the termination region (AR) where the first recess is to be formed in the step of anisotropic etching, wherein in the step of anisotropic etching the patterned metal layer is used at least as a part of an etching mask, and wherein the patterned metal layer in the termination region forms the field plate in the power semiconductor device.

As in the method of the invention areas in the termination region that are exposed by the field plate are etched in the step of anisotropic etching, an outer circumferential edge of the field plate is self-aligned with a sidewall of the first recess formed in the step of anisotropic etching. The recess formed in the step of anisotropic etching forms a mesa edge termination thus an edge termination by a process free of any implantation step. The field plate protects areas of the wide-

bandgap semiconductor layer that shall not be etched during the step of anisotropic etching. Accordingly, a deep SiC etch can be performed more reliably and the sidewall of the first recess and the circumferential edge of the field plate are mutually aligned in lateral direction with high precision. Consequently, as it is
5 discussed above, because of the precise alignment, the electric field crowding below the circumferential edge of the field plate can be efficiently reduced by the mesa edge termination thus resulting in a device providing higher breakdown voltage.

Using a patterned metal layer as the field plate and as an etching mask in the step
10 of anisotropic etching is advantageous compared to using an etching mask made of photoresist because metal is more resistant to etchants, that are used in the step of anisotropic etching of the wide-bandgap semiconductor layer, than photoresist. As discussed above, using the dielectric layer between the wide-bandgap semiconductor layer and the field plate amplifies the effect of the field plate and
15 provides additional electric field relief.

In an exemplary embodiment the dielectric layer is patterned before the step of forming the metal layer to form an opening in the dielectric layer that exposes at least a second portion of the first main side of the wide-bandgap semiconductor layer in the active region.

20 Patterning the dielectric layer before patterning the metal layer enables the formation of advantageous shapes of the dielectric layer. For example, the dielectric layer may be formed such that its thickness decreases with increasing lateral distance from the first recess. As discussed above, a dielectric layer with such a shape may yield beneficial electric field characteristics.

25 In addition, in an exemplary embodiment, a metal layer is formed to be in direct contact with the first main side of the wide-bandgap semiconductor layer through the opening in the dielectric layer.

This metal layer can serve as a contact electrode for electrically connecting the device. The contact electrode may, for example, comprise a Schottky contact.

30 Advantageously, by forming the metal layer on the patterned dielectric layer, the field plate and the contact electrode are formed simultaneously, i.e. in the same

method step. Thus, ease of fabrication is achieved, potentially resulting in a more cost efficient manufacturing process.

In an exemplary embodiment the patterned metal layer and the patterned dielectric layer expose a third portion of the first main side of the wide-bandgap semiconductor layer in the active region, and a second recess is formed in the active region in the step of anisotropic etching together with the first recess using the patterned metal layer as the etching mask and filled with a filling material.

Simultaneous etching of the first recess and the second recess is enabled by using the field plate as the etching mask. Accordingly, more efficient fabrication of a power semiconductor device is enabled. Moreover, due to the simultaneous etching, the first recess and the second recess can be fabricated with the same depth.

In an exemplary embodiment, the patterned metal layer and the patterned dielectric layer expose a fourth portion of the first main side of the wide-bandgap semiconductor layer in the active region. The method further comprises a step of forming a contact electrode in direct contact with the fourth portion of the first main side of the wide-bandgap semiconductor layer before the anisotropic etching of the wide-bandgap semiconductor layer, and the contact electrode is used together with the patterned metal layer as the etching mask in the step of anisotropic etching of the wide-bandgap semiconductor layer.

By using the contact electrode together with the patterned metal layer as the etching mask for etching the wide-bandgap semiconductor layer, an additional processing step can be avoided, thus manufacturing of a power semiconductor device is facilitated. For example, the contact electrode prevents the etching of the wide-bandgap semiconductor layer in the active region during the etching of the first recess. Therefore the use of an additional etching mask shielding the wide-bandgap semiconductor layer in the active region can be avoided.

In an exemplary embodiment the step of forming the field plate comprises: forming the dielectric layer on the first main side of the wide-bandgap semiconductor layer; forming a first metal layer on the dielectric layer; and forming a second metal layer on the first metal layer, wherein the first and the second metal layer are formed of different metals; patterning the second metal layer, the first metal layer and the dielectric layer to expose at least the first portion of the first main side of the wide-

bandgap semiconductor layer in the termination region where the first recess is to be formed in the step of anisotropic etching, wherein, in the step of anisotropic etching, the first and the second metal layer are used at least as a part of an etching mask, and wherein the patterned first metal layer in the termination region forms at least part of the field plate in the power semiconductor device.

As the first metal layer and the second layer are formed of different metals, the first metal layer can serve as an etch stop for an etchant used for etching the second metal layer and thus prevent etching of the dielectric layer and wide-bandgap semiconductor layer underneath. An etching mask comprising both the first metal layer and the second metal layer enables forming a particularly well defined sidewall of the first recess in the wide-bandgap semiconductor layer. As a consequence the breakdown voltage of the power semiconductor may be further improved.

In an exemplary embodiment the step of patterning the second metal layer, the first metal layer and the dielectric layer further comprises: patterning the second metal layer to expose the first metal layer in areas of the first portion of the first main side of the wide-bandgap semiconductor layer in the termination region; forming trenches in the second metal layer in the active region to expose the first metal layer at the bottom of the trenches, refilling the trenches at least partially by a filling material, and patterning the first metal layer and the dielectric layer by anisotropic etching using the second metal layer and the filling material as an etching mask. In addition, the method comprises the following steps: removing the filling material after the step of patterning the first metal layer and the dielectric layer; thereafter removing a portion of the second metal layer in which the trenches are formed by isotropic etching of portions respectively separating neighbouring trenches; thereafter removing portions of the first metal layer and of the dielectric layer in the active region by anisotropic etching using the second metal layer as an etching mask to expose a fifth portion of the first main side of the wide-bandgap semiconductor layer in the active region; and forming a contact electrode contacting the fifth portion of the first main side of the wide-bandgap semiconductor layer.

This embodiment provides an alternative for fabricating the power semiconductor device according to the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Detailed embodiments of the invention will be explained below with reference to the accompanying figures, in which:

- 5 Fig. 1A illustrates an exemplary first embodiment of a power semiconductor device according to the invention;
- Fig. 1B illustrates dimensions used for describing embodiments according to the invention;
- 10 Fig. 1C illustrates an exemplary second embodiment of a power semiconductor device according to the invention in which the thickness of the dielectric layer increases in a lateral direction away from the active region;
- Fig. 1D illustrates an exemplary third embodiment of a power semiconductor device according to the invention in which trenches are formed in the active region;
- 15 Figs. 2A to 2I illustrate method steps in a first exemplary method for manufacturing the first embodiment of a power semiconductor device according to the invention shown in Fig. 1A.
- Figs. 3A to 3D illustrate method steps in a second exemplary method for manufacturing the second embodiment of a power semiconductor device according to the invention shown in Fig. 20 1B;
- Figs. 4A and 4B illustrate method steps in a third exemplary method for manufacturing the third embodiment of a power semiconductor device according to the invention shown in Fig. 1C; and
- 25 Figs. 5A to 5H illustrate method steps in a fourth exemplary method for manufacturing a fourth embodiment of a power semiconductor device according to the invention.

The reference signs used in the figures and their meanings are summarized in the list of reference signs. Generally, similar elements have the same reference signs
30 throughout the specification. In order to increase visibility, dimensions are not to

scale. However, this does not exclude that they consist of the same material or that severally components are integrally formed. The described embodiments are meant as examples and shall not limit the scope of the invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

5 Hereinafter exemplary embodiments of the semiconductor device according to the invention and manufacturing methods are described in detail. The power semiconductor device is, for example, a silicon carbide (SiC) Schottky diode.

First embodiment:

Referring to Figs. 1A and 1B, an exemplary embodiment according to the invention
10 comprises an n-type silicon carbide (SiC) layer 1, an n⁺-type SiC substrate 1', a dielectric layer 4, a field plate 5, a first recess 9, a backside electrode 10, a frontside electrode (contact electrode 8) and a passivation layer 11.

The SiC layer 1 (an example of the wide-bandgap semiconductor layer 1 in the claims) is formed on the SiC substrate 1', has exemplarily a relatively low doping
15 concentration of 10^{17} cm^{-3} or less and forms the drift layer in the final power semiconductor device. The SiC substrate 1' has, for example, a higher doping concentration of 10^{18} cm^{-3} or more and is formed on the backside electrode 10. Appropriate doping profiles of the SiC layer 1 and the SiC substrate 1' for use in a Schottky diode are well known in the prior art. The SiC layer 1 has a first main side
20 2 and a second main side 3. The first main side 2 and the second main side 3 extend in a lateral direction. The first main side 2 corresponds to a plane through the outermost part of the SiC layer 1 on a side opposite to the second main side 3. The SiC layer 1 comprises an active region AR and a termination region TR laterally surrounding the active region AR. The material of the SiC layer 1 and of the SiC
25 substrate 1' may be any polytype of SiC such as 4H-SiC, 6H-SiC or 3C-SiC, for example. A layer thickness d_{SiC} of the SiC layer 1 depends on the nominal blocking voltage of the power semiconductor device. The layer thickness d_{SiC} of the SiC layer 1 is defined as the largest distance between the first main side 2 and the second main side 3 in a direction perpendicular to the first main side 2 (see Fig. 1B). The
30 layer thickness d_{SiC} of the SiC layer 1 may be in the range from 5 μm to over 100 μm , and exemplary is in the range between 5 and 30 μm , more exemplarily between 5 μm and 20 μm .

The dielectric layer 4 is located between the first main side 2 of the SiC layer 1 and the field plate 5. The dielectric layer exposes a first portion 9 of the of the SiC layer 1 in the termination region TR. The dielectric layer 9 exposes a second portion of the SiC layer 1 in the active region AR. The dielectric layer 4 can comprise any
5 dielectric material as long as it can be formed on the SiC layer 1 (e.g. by depositing or growing) and patterned (e.g. by dry or wet etching or by lift-off or shadow mask). The dielectric layer 4 can be an oxide layer (e.g. a silicon oxide layer), or a nitride layer (e.g. a silicon nitride layer), or an oxynitride layer, for example. It can also comprise different dielectric materials in an alloy or in a stack of layers. The
10 thickness of the dielectric layer has an influence on the electric field relief that can be achieved by means of a field plate. The thinner the dielectric layer 4, the higher the breakdown voltage VBR which can be achieved. The dielectric layer thickness can, for example, be smaller as in prior art devices. For example, the thickness d_D of the dielectric layer 4 adjacent to the first recess is in a range between $0.02\text{ }\mu\text{m}$ and $1\text{ }\mu\text{m}$, exemplarily between $0.02\text{ }\mu\text{m}$ and $0.5\text{ }\mu\text{m}$ and more exemplarily between $0.02\text{ }\mu\text{m}$ and $0.3\text{ }\mu\text{m}$, wherein the thickness d_D of the dielectric layer 4 is defined as the distance between the intersection points of a line perpendicular to the first main side 2 with the upper surface and lower surface of the dielectric layer 4 (see Fig. 1B).

20 The field plate 5 is formed on the dielectric layer 4. The field plate 5 exposes the first portion of the SiC layer 1 in the termination region TR. The field plate 5 exposes a third portion of the SiC layer 1 in the active region AR. Exemplarily, the field plate 5 is formed out of metal but other materials are also appropriate as long as they are conducting and patternable. The field plate 5 may comprise, for example, one of
25 aluminium (Al), nickel (Ni), tungsten (W) or chrome (Cr). The field plate 5 may comprise an alloy or different metals in a stack of layers. For example, the thickness d_{FP} of the field plate 5, defined as the distance between the upper surface of the field plate 5 and the lower surface of the field plate (see Fig. 1B), is in a range between $1\text{ }\mu\text{m}$ and $500\text{ }\mu\text{m}$, exemplarily between $1\text{ }\mu\text{m}$ and $100\text{ }\mu\text{m}$ and more
30 exemplarily between $1\text{ }\mu\text{m}$ and $20\text{ }\mu\text{m}$. The lateral dimension w_{FP} of the field plate 5, defined as the distance from an edge of the field plate adjacent to the active region to an edge of the field plate adjacent to the first recess 9 (see Fig. 1B) is in the range of $1.5\text{ }\mu\text{m}$ and $1500\text{ }\mu\text{m}$.

The first recess 9 is formed in the termination region TR of the SiC layer 1. The first recess 9 is recessed from the first main side 2 of the SiC layer 1 and surrounds the active region AR. The recess is formed in the first portion of the SiC layer 1 exposed by the field plate 5. A sidewall 9e of the first recess 9 adjacent to the active region AR is laterally aligned with a circumferential edge 5e (outer edge) of the field plate 5 such that in an orthogonal projection onto a plane parallel to the first main side 2 an edge of the recess defined by the upper end of the sidewall is within less than 1 μm from the circumferential edge of the field plate 5, exemplarily less than 0.5 μm , exemplarily less than 0.2 μm . Thus, the sidewall 9e has a thickness (distance) between the first main side 2 and the upper surface of the field plate 5, which is the side of the field plate opposite to the SiC layer.

The first recess 9 in the termination region TR forms a mesa edge termination structure. For example, the depth d_R of the recess is at least 2 % of the layer thickness d_{SiC} of the SiC layer 1, exemplarily at least 30 %, more exemplarily at least 50 %. For example, the lateral dimension of the recess w_R is at least 10 % of the layer thickness of the SiC layer 1, exemplarily at least 50 %, more exemplarily at least 200 %.

For example, in an exemplary embodiment the SiC layer 1 has a thickness d_{SiC} of 15 μm ; the dielectric layer 4 has a thickness d_D in the range of 0.2 μm – 0.5 μm ; the field plate lateral dimension w_{FP} is in the range of 1.5 μm and 1500 μm and the depth d_R of the first recess 9 is between 150 nm and 30 μm . When the recess 9 is deeper than the thickness of the SiC layer 1 ($d_R > d_{\text{SiC}}$), then the recess 9 continues in the SiC substrate 1'.

The contact electrode 8 is formed in direct contact with a fourth portion of the first main side 2 of the silicon carbide layer 1 in the active region AR. Here, the contact portion 8' of the contact electrode 8 forms a Schottky contact with the SiC layer 1. Any metal appropriate for a Schottky contact can be used as a material. Titanium (Ti) or nickel (Ni) are known as materials appropriate for a Schottky contact to SiC and may be used in the contact portion 8', for example. The contact electrode 8 may further comprise an alloy or different metals in a stack of layers. For example, an additional electrode layer may be formed on the contact portion 8' of the contact electrode 8 to form an ohmic contact to the contact portion 8'. The contact electrode

8 may overlap with a portion of the field plate 5. The contact electrode 8 may be electrically connected to the field plate 5 and may be formed by the same material or a different one.

5 A passivation layer 11 may be formed on the whole front side of the semiconductor device. The passivation layer 11 may further comprise an opening 12 to expose the upper side of the contact electrode 8 for electrically contacting it from the outside.

Second embodiment:

10 A second embodiment according to the invention is described with reference to Fig. 1C. Due to the many similarities between the first embodiment and the second embodiment only differences of the first embodiment to the second embodiment are discussed. The remaining features are the same as in the first embodiment and for an explanation thereof it is referred to the first embodiment discussed above with reference to Figs. 1A to 1B. In contrast to the first embodiment, dielectric layer 4 is formed such that its thickness d_D increases with increasing lateral distance from 15 the active region AR. The thickness d_D may increase from a first value to a second value. The thickness may increase continuously from a first value to a second value. The angle between the straight line connecting the first value and the second value and a plane parallel to the first main side may be in the range between 0.1° and 90° , exemplarily between 1° and 10° , more exemplarily between 1° and 5° . The first 20 value may be 0 or a larger value, the second value is larger than the first value, for example larger than $0.05\ \mu\text{m}$, or larger than $0.1\ \mu\text{m}$ or larger than $0.5\ \mu\text{m}$. The smaller thickness d_D of the dielectric layer 4 in proximity to the active region AR increases the field plate's effect on the electrical charges in the silicon carbide layer 1, hence reducing the magnitude of the electrical field in the active region AR more 25 efficiently. The larger thickness d_D of the dielectric layer 4 below the circumferential edge 5e of the field plate 5 provides better protection against voltage breakdown due to dielectric failure.

Third embodiment:

30 A third embodiment according to the invention is described with reference to Fig. 1D. Due to the many similarities between the first embodiment and the third embodiment only differences of the first embodiment to the third embodiment are discussed. The remaining features are the same as in the first embodiment and for

an explanation thereof it is referred to the first embodiment discussed above with reference to Figs. 1A and 1B. The third embodiment differs from the first embodiment in that the active region AR of the SiC layer 1 also comprises at least one second recess 14 which has the same depth as the first recess 9 in the termination region TR. The at least one second recess 14 is filled with some filling material, for example insulating material such as a dielectric material or an oxide. This configuration may have a positive effect on leakage currents. The third embodiment may also have the dielectric layer 4 with increasing thickness as shown in the second embodiment.

10 Manufacturing method for the first embodiment:

In the following there is explained a method for manufacturing the power semiconductor device according to the first embodiment of the invention (Fig. 1A) with reference to Figs. 2A to 2I. Points discussed with respect to the first embodiment are valid for the following and complete the description.

15 In a first method step illustrated in Fig. 2A, there is provided the n-type silicon carbide (SiC) substrate 1' with the lower doped SiC layer 1 forming the drift region. For example, the SiC layer is formed by means of epitaxy. The SiC layer 1 has a first main side 2 and a second main side 3 extending in a lateral direction as shown in Fig. 2A. The SiC layer 1 comprises an active region AR and a termination region TR laterally surrounding the active region AR.

20 The dielectric layer 4 is formed in a next step on the first main side 2 of the SiC layer 1 as illustrated in Fig. 2B. The dielectric layer 4 covers the entire active region AR and the entire termination region TR. The dielectric layer 4 is in direct contact with the SiC layer 1.

25 Next, a metal layer 7 is formed on the dielectric layer 4 as illustrated in Fig. 2C. The metal layer 7 covers the entire active region AR and the entire termination region TR. The metal layer 7 is formed in direct contact with the dielectric layer 4. Preferentially, the metal used for forming the metal layer 7 is hardly etchable with an etchant used for SiC etching. In other words, the metal used for forming the metal layer 7 is preferentially such that it erodes less than SiC in an etching process described later. For example, the metal layer 7 may comprise one of the field plate

30

materials discussed with respect to the first embodiment and may have the same thickness.

In a next step, the metal layer 7 is patterned. For this, an etching mask 6 is formed on the metal layer 7 as shown in Fig. 2D. The etching mask 6 is formed such that it exposes at least a portion (an example of a first portion in the claims) of the metal layer 7 covering the termination region TR. The etching mask 6 may also expose a portion of the metal layer 7 covering the active region AR. The etching mask 6 may be a photoresist mask or similar.

A portion of the metal layer 7 exposed by the etching mask 6 is removed by anisotropic etching. In this way, the field plate 5 is formed. Herein, a portion of the metal layer 7 and a portion of the dielectric layer 4 is removed in the termination region TR, and a portion of the metal layer 7 and the dielectric layer 4 is removed in the active region AR. Due to the anisotropic etching, an edge of the field plate 5 (patterned metal layer 7) is aligned with an edge of the patterned dielectric layer 4. In particular, a circumferential edge 4e of the patterned dielectric layer 4 is laterally aligned with a circumferential edge 5e of the field plate 5 (patterned metal layer 7). The anisotropic etching may be performed by reactive ion etching (RIE) using a chlorine (Cl) based etching gas, for example. The etching mask 6 may be consumed during the etching process or removed afterwards. The resulting structure after the step of anisotropic etching is shown in Fig. 2E.

Next the contact electrode 8 is formed (e.g. by growing or depositing) in direct contact with a portion (an example of the fourth portion in the claims) of the first main side 2 of the silicon carbide layer 1 in the active region AR. Here, the contact portion 8' of the contact electrode 8 forms a Schottky contact with the SiC layer 1. An additional electrode layer (not shown) may be formed on the contact portion 8' to form an ohmic contact to the contact portion 8'.

Next the first recess 9 is formed in the SiC layer 1 in the termination region TR by anisotropic etching as illustrated in Fig. 2G. Therein, anisotropic etching is selective against the metal of the field plate 5 (patterned metal layer 7) and the metal of the contact electrode 8, in particular, the metal in the upper part of the contact electrode 8 (i.e. the part facing away from the first main surface 2). In other words, the field plate 5 and the contact electrode 8 (in particular the upper part of the contact

electrode 8) are used at least as a part of an etching mask preventing (slowing down) the etching of the material underneath it (i.e. downstream of the etching direction). Anisotropic etching may be performed by RIE using a fluorine (F) based etching gas, for example. The first recess 9 is formed in areas (an example of the first portion in the claims) which are exposed by the field plate 5 and the contact electrode 8. Accordingly, the first recess 9 is only formed in the recess region RR in the termination region TR. The first recess is not formed in the active region AR despite the opening in the field plate 5 because in the active region AR the contact electrode 8 covers the SiC layer 1. Therefore an additional fabrication step of providing an etching mask to prevent etching of the SiC layer in the active region AR can be avoided.

In the step of anisotropic etching of SiC, upper parts (i.e. the parts facing away from the first main surface 2) of the field plate 5 and the contact electrode 8 (both being part of the etching mask) may be partially removed (not shown), in case the etchant is not completely selective against them. However, due to the anisotropic character of the etching process, the lateral dimension of the etching mask (i.e. the field plate 5) is not changed during the etching process when forming the first recess 9, only the thickness of the contact electrode 8 and the field plate 5 is reduced. Thus, by anisotropic etching using the field plate 5 as part of the etching mask, a deep etch of the SiC layer 1 can be formed with high precision such that a sidewall 9e of the first recess 9 is aligned with an edge of the field plate 5. Exemplarily, the sidewall 9e of the first recess 9 adjacent to the active region is laterally aligned with the circumferential edge 5e of the field plate 5 such that in an orthogonal projection onto a plane parallel to the first main side 2 the edge of the first recess defined by the upper end of the sidewall 9e is within less than 1 μm , exemplarily less than 0.5 μm , exemplarily less than 0.2 μm from the circumferential edge 5e of the field plate 5. The first recess 9 in the termination region TR forms a mesa edge termination structure in the final power semiconductor device. The first recess 9 surrounds the active region AR and has for examples the dimensions as discussed with respect to the first embodiment.

In addition, the backside electrode layer 10 may be formed on the second main side 3. Moreover, a passivation layer 11 may be formed on the whole front side of the device to obtain a structure as shown in Fig. 2H. Finally, as illustrated in Fig. 2I

an opening 12 may be formed in the passivation layer 11 to expose the upper side of the contact electrode 8 for electrically contacting it from the outside.

In a modification of this method, the backside electrode 10 may be formed at an earlier step of the method or at a later step of the method. Accordingly, the patterning of the dielectric layer 4 may be performed at an earlier or later step of the method. For example, instead of patterning the dielectric layer 4 together with the metal layer 7 as shown in Fig. 2E, the dielectric layer 4 may be patterned in the step of the anisotropic etching of the SiC layer 1. Then, only the field plate 5 (patterned metal layer 7) is used as an etching mask and the contact electrode 8 is formed after the anisotropic etching of the SiC layer 1. The passivation layer 11 may be formed after the contact electrode 8 has been formed as shown in Fig 1H. However, the contact electrode 8 may also be formed after the formation of the passivation layer 11. Then, an opening 12 is formed in the passivation layer 11 to expose the SiC layer 1 in the active area AR for contacting the contact electrode 8.

Manufacturing method for the second embodiment:

Next, a method for manufacturing a power semiconductor device according to the second embodiment of the invention is explained with reference to Figs. 3A to 3D starting after the method step shown in Fig. 2B. Due to the many similarities between the method for manufacturing the first embodiment and the method for manufacturing the second embodiment, only differences of the methods discussed. The remaining features are the same as in the method for manufacturing the first embodiment and for an explanation thereof it is referred to the discussions above.

The manufacturing method for manufacturing the second embodiment differs from the one described above in that the dielectric layer 4 formed on the first main side 2 of the SiC layer 1 (see Fig. 2B) is patterned before the metal layer 7 is formed on the dielectric layer 4 (see Fig. 3A). This approach provides the advantage that the dielectric layer 4 can be formed in various configurations. For example, the dielectric layer 4 can be formed such that it has an opening exposing a portion (an example of the second portion in the claims) of the SiC layer in the active region AR and/or such that the thickness of the dielectric layer 4 increases with increasing lateral distance from the active region AR.

In the next step, a metal layer 7 is formed on the patterned dielectric layer 4 as illustrated in Fig. 3B. In the area where the patterned dielectric layer 4 exposes the first main side 2 of the SiC layer 1 in the active region (as an example of the second portion in the claims), the metal layer 7 contacts the SiC layer 1. Consequently, the metal layer 7 forms a contact electrode 8 in direct contact with a portion of the first main side 2 of the SiC layer 1 as described above with reference to Fig. 2F. In the termination region TR where the dielectric layer 4 is interposed between the metal layer 7 and the SiC layer 1, the metal layer 7 forms a field plate 5. As such, the field plate 5 and the metal contact 7 are integrally formed.

Next (see Fig. 3C), the field plate 5 is patterned to appropriate dimensions as described above with reference to Fig. 2D and to form the etching mask for the anisotropic etching of the SiC layer 1. In the example shown here, only the field plate 5 is patterned. However, alternatively, both the field plate 5 and a portion of the dielectric layer 4 may be patterned in this step as described above with reference to Fig. 2E. Thereafter, the areas (as an example of the first portion in the claims) exposed by the etching mask (i.e. field plate 5) are then etched by anisotropic etching as described above with reference to Fig. 2G to form the first recess 9 in the recess region RR in the termination region TR of the SiC layer 1 (see Fig. 3D). Here, the area (as an example of the first portion in the claims) of the SiC layer 1 exposed by the etching mask (field plate 5) is covered by a portion of the dielectric layer 4. Thus, both a portion of the dielectric layer 4 and a portion of the SiC layer 1 are removed in this etching step. However, in a modification of the method, the portion of the dielectric layer 4 covering the SiC layer 1 in the area exposed by the etching mask (i.e. field plate 5) may have already been removed earlier, such that the etching mask (i.e. field plate 5) directly exposes the area (an example of the first portion in the claims) of the SiC layer 1 where the first recess 9 is to be formed.

Finally, as for the first embodiment, a backside electrode 10 may be added as well as a passivation layer 11 (not shown in Figs. 3A - 3D).

Manufacturing method for the third embodiment:

A method for manufacturing the third embodiment according to the invention is described with reference to Figs. 4A and 4B starting after the method step shown in Fig. 3B. Therein, in the metal layer 7 patterning step described above with reference to Fig. 2E, the metal layer 7 is patterned such that it also exposes at least
5 a portion (an example of the third portion in the claims) of the SiC layer 1 in the active region AR (see Fig. 4A). The portion of the dielectric layer 4 exposed in the termination region TR by the metal layer 7 is removed in the same processing step. For example, the metal layer 7 may be patterned such that it comprises a plurality of ducts 13 exposing a plurality of areas of the SiC layer 1 in the activation region
10 AR. Each duct of the plurality of ducts 13 may have the same cross-section. The cross-sections of the plurality of ducts may however also vary. For example, the ducts 13 may have a circular cross-section or a polygonal cross-section. The diameters of the ducts 13 may, for example, vary between 0.5 μm and 2 μm . The ducts 13 may be regularly distributed. Alternatively the ducts 13 may be irregularly
15 distributed. As illustrated in Fig. 4B, by using the patterned metal layer 7 exposing at least a portion of the SiC layer 1 in the active region as an etching mask in the step of anisotropic etching the SiC layer 1, at least one second recess 14 is formed in the active region AR together with the first recess 9 in the termination region TR. When patterned metal layer 7 comprises a plurality of ducts 13, then a plurality of
20 trenches 14 are formed in the SiC layer 1 in the active region AR. Since the at least one second recess 14 in the active region AR and the first recess 9 in the termination region TR are formed simultaneously in the same etching step, they undergo the same etching duration. Thus, when the SiC layer 1 is directly exposed by the etching mask (field plate 5) or is covered by the same amount of material
25 (e.g. dielectric material), then the at least one second recess 14 in the active region AR and the first recess 9 in the termination region TR have the same depth and their sidewalls are parallel to each other. After this step, for example, the at least one second recess 14 is filled with some filling material (not shown), for example insulating material such as a dielectric material or an oxide. Further, the at least
30 one duct 13 in the metal layer 7 may be filled with a filling material (not shown). The filling material can be the same one as the one used for filling the at least one second recess 14, or a different one, for example the metal of the metal layer 7. Alternatively, a central part of the metal layer 7 coinciding with the active region AR

of the SiC layer may be removed, for example by etching, to expose the SiC layer 1 in the active region (not shown), and a contact electrode 8 may be formed as described with reference to Fig. 2F. Finally, a backside electrode 10 and/or a passivation layer 11 may added as described above with reference to Figs. 2H and 2G.

Alternative manufacturing method:

Another method to manufacture one of the embodiments according to the invention is described with reference to Figs. 5A – 5H. Due to the many similarities with the methods described above only differences are discussed. The remaining features are the same as explained before and for an explanation thereof it is referred to these.

As shown in Fig. 5A, a dielectric layer 4 is formed on the first main side of the silicon carbide layer 1 as described for the first method. Thereon a first metal layer 7 is formed, and a second metal layer 15 is formed on the first metal layer 7. The first 7 and the second 15 metal layer are formed of different metals such that the first metal layer 7 acts as an etch stop when etching the second metal layer 15. The first metal layer 7 and second metal layer 15 may exemplarily comprise one of the field plate materials mentioned above when describing the first embodiment. Preferentially, the first metal layer 7 is more etch resistive against an etchant used for etching the SiC layer 1 than the second metal. The first metal layer 7 may, for example, be thinner than the second metal layer 15. Next, as shown in Fig. 5B, the second metal layer 15 is patterned, for example according to the method described for manufacturing the first embodiment with reference to Fig. 2D, such that trenches 16 are formed in the second metal layer 15 in the active region AR to expose the first metal layer 7 at the bottom of the trenches and such that the first metal layer 7 is exposed in areas coinciding with the first portion of the SiC layer 1 in the termination region TR where the first recess 9 is to be formed. Thereafter, as shown in Fig. 5C, the trenches 16 in the second metal layer 15 are filled at least partially by a filling material 17. For example, the filling material 17 may be an oxide or a resist. Thereafter, as shown in Fig. 5D, the first metal layer 7 and the dielectric layer 4 are patterned by anisotropic etching using the second metal layer 15 and the filling material 17 as an etching mask to expose at least the portion of the first main

side 2 of the SiC layer 1 in the termination region TR where the first recess 9 (i.e. the mesa type termination) is to be formed. The sidewalls of the trenches (i.e. the portions of the second metal layer 15 separating neighbouring trenches 16) together with the filling material 17 filled inside the trenches 16 provide sufficient
5 etch resistivity to prevent etching of the first metal layer 7 and the dielectric layer 4 located underneath. Next, as shown in Fig. 5E, the first recess 9 is formed in the termination region of the SiC layer 1 by anisotropic etching using the first metal layer 7 and the second metal layer 15 at least as a part of the etching mask. During this etching process the filling material 16 in the trenches 17 may be consumed,
10 alternatively the filling material 16 may be removed before or after the step of the anisotropic etching of the SiC layer 1. Next, as shown in Fig. 5F, a portion of the second metal layer 15 in which the trenches 16 are formed is removed by isotropic etching of portions respectively separating neighbouring trenches, i.e. the sidewalls. The etchant used in this step is selective against the metal of the first
15 metal layer 7, i.e. the first metal layer 7 is not, or only hardly consumed in this etching step. Thereafter, as shown in Fig. 5G, portions of the first metal layer 7 and of the dielectric layer 4 are removed in the active region AR by anisotropic etching using the second metal layer 15 as an etching mask 17 to expose a portion of the first main side 2 of the silicon carbide layer 1 in the active region AR. In this step an
20 upper portion of the second metal layer 7 may be consumed. However, as explained with respect to the method for manufacturing the first embodiment, because of the anisotropic etching, this will only affect the thickness of the second metal layer 15 and not its lateral dimension. The second metal layer 15 may also be entirely consumed. The remaining portion of the first metal layer 7 and the
25 second metal layer 15 above the dielectric layer 4 form the field plate 5. Thereafter, as shown in Fig. 5H, a contact electrode 8 is formed (e.g. by growing or depositing) in direct contact with a portion (an example of the fourth portion in the claims) of the first main side of the silicon carbide layer 1 in the active region (AR) as explained with the method for manufacturing the first embodiment with reference to Fig. 2F.
30 Finally, a passivation layer 11 and a backside electrode 10 are added (not shown). Alternatively, the passivation layer 11 and/or backside electrode 10 may be formed at an earlier step, as explained before.

In a modification of this method, the step of anisotropic etching of the SiC layer 1 is performed after the step in which the trenches 16 are removed.

Modifications:

It will be apparent for persons skilled in the art that modifications of the above described embodiments are possible without departing from the idea of the invention as defined by the appended claims. In particular, that it is possible to combine features of the different embodiments.

In the above embodiments the manufactured power semiconductor device is a SiC Schottky diode. However, the power semiconductor device may be any other power semiconductor device that requires an edge termination, such as a JBS rectifier, JFET, or a pn diode, for example.

In the above described embodiments, the power semiconductor device comprises a silicon carbide (SiC) layer 1. The SiC layer 1 is an example of the wide-bandgap semiconductor layer 1 in the claims. Alternatively, the wide-bandgap semiconductor layer 1 can comprise other wide-bandgap semiconductor materials known in the art. For example, instead of being a SiC layer 1, the wide-bandgap semiconductor layer 1 may, for example, be a gallium nitride (GaN) layer or a gallium oxide (Ga₂O₃) layer. The wide-bandgap semiconductor layer 1 may also be, for example, a zinc oxide (ZnO) layer, a boron nitride layer (BN), an aluminium nitride layer (AlN), or a diamond (C) layer,

In the above described embodiments the SiC layer 1 is provided as a layer on a SiC substrate 1'. The SiC substrate 1' may however also be formed out of a different substrate material known in the art. For example, the SiC substrate 1' may be a gallium nitride (GaN) substrate or a gallium oxide (Ga₂O₃) substrate. Also, the wide-bandgap semiconductor layer 1 may be provided as a separate layer or wafer without the substrate 1'.

In the figures of all embodiments the angle formed by a sidewall of the recess 9, 14 and the first main side 2 is shown to be 90° but it may also be slightly smaller and also larger. Exemplarily, the angle formed by a sidewall of the recess 9, 14 and the first main side 2 may vary in a range between 60° and 120°, exemplarily between 70° and 110°, more exemplarily between 80° and 100°.

The above embodiments were explained with specific conductivity types. The conductivity types of the semiconductor layers in the above described embodiments might be switched, so that all layers which were described as p-type layers would be n-type layers and all layers which were described as n-type layers would be p-type layers.

It should be noted that the term “comprising” does not exclude other elements or steps and that the indefinite article “a” or “an” does not exclude the plural. Also elements described in association with different embodiments may be combined.

10	List of reference signs
	1 wide-bandgap semiconductor layer (e.g. SiC layer)
	1' substrate (e.g. SiC substrate)
	2 first main side
	3 second main side
15	4 dielectric layer
	4e circumferential edge of the dielectric layer
	5 field plate
	5e circumferential edge of the field plate
	6 etching mask
20	7 (first) metal layer
	7e circumferential edge of (first) metal layer
	8 contact electrode
	8' contact portion
	9 first recess (mesa-type termination structure)
25	9e sidewall of the first recess
	10 backside electrode
	11 passivation layer
	12 opening
	13 duct

	14	trench
	15	second metal layer
	15e	circumferential edge of second metal layer
	16	trench
5	17	filling material
	AR	active region
	RR	recess region
	TR	termination region
	d _R	depth of recess
10	d _{SiC}	layer thickness of the wide-bandgap semiconductor layer 1 (e.g. the SiC layer 1)
	d _D	layer thickness of the dielectric layer 4
	w _R	lateral dimension of the first recess 9
	w _{FP}	lateral dimension of the field plate
15		

Claims

1. A power semiconductor device comprising:
a wide-bandgap semiconductor layer (1), the wide-bandgap semiconductor layer (1) having a first main side (2) and a second main side (3) opposite to the first main side (2), wherein the first main side (2) and the second main side (3) extend in a lateral direction and wherein the wide-bandgap semiconductor layer (1) comprises an active region (AR) and a termination region (TR), the termination region (TR) laterally surrounding the active region (AR), wherein the wide-bandgap semiconductor layer (1) has a first recess (9), which is recessed from the first main side (2) in the termination region (TR), the first recess (9) surrounding the active region (AR);
a field plate (5) on the first main side (2) of the wide-bandgap semiconductor layer (1), the field plate (5) exposing a first portion of the wide-bandgap semiconductor layer (1) in the termination region (TR);
a sidewall (9e) of the first recess (9) adjacent to the active region (AR) is laterally aligned with a circumferential edge (5e) of the field plate (5) such that in an orthogonal projection onto a plane parallel to the first main side (2) an edge of the recess defined by the upper end of the sidewall is within less than 1 μm from the circumferential edge of the field plate (5), exemplarily less than 0.5 μm , exemplarily less than 0.2 μm ,
characterized in that
the wide-bandgap semiconductor layer (1) has a second recess (14) in the active region (AR) which is recessed from the first main side (2) of the wide-bandgap semiconductor layer (1),
a depth of the second recess (14) is the same as a depth of the first recess (9), and
the second recess (14) is filled with a filling material.

2. A power semiconductor device according to claim 1, further comprising a dielectric layer (4) interposed between the field plate (5) and the wide-bandgap semiconductor layer (1) to separate the field plate (5) from the wide-bandgap semiconductor layer (1).
- 5 3. A power semiconductor device according to claim 2, wherein a thickness of the dielectric layer (4) perpendicular to the lateral direction decreases with increasing lateral distance from the first recess (9).
- 10 4. A power semiconductor according to claim 2 or 3, wherein the dielectric layer (4) has a thickness adjacent to the first recess (9) which is in a range between 0.02 μm and 1 μm , or between 0.02 μm and 0.5 μm or between 0.02 μm and 0.3 μm .
- 15 5. A power semiconductor device according to any one of the claims 1 to 4, wherein the field plate (5) comprises at least one of aluminum, nickel, tungsten, and chromium.
- 20 6. A power semiconductor device according to any one of the claims 1 to 5, wherein a depth of the first recess (9) is at least 4 μm , or at least 6 μm .
- 25 7. A power semiconductor device according to any one of the claims 1 to 6, wherein the wide-bandgap semiconductor layer (1) comprises one of silicon carbide, gallium nitride and gallium oxide.
- 30 8. A method for manufacturing a power semiconductor device comprising the following steps:
providing a wide-bandgap semiconductor layer (1) having a first main side (2) and a second main side (3) opposite to the first main side (2), wherein the first and the second main side (3) extend in a lateral direction and wherein the wide-bandgap semiconductor layer (1) comprises an active region (AR) and a termination region (TR) laterally surrounding the active region (AR);

forming a field plate (5) on the first main side (2) of the wide-bandgap semiconductor layer (1), the field plate (5) exposing the first portion of the first main side (2) of the wide-bandgap semiconductor layer (1) in the termination region (TR); and

5 anisotropic etching of the wide-bandgap semiconductor layer (1) in areas where the field plate (5) exposes the first portion of the first main side (2) of the wide-bandgap semiconductor layer (1) in the termination region (TR) to form the first recess (9) in the wide-bandgap semiconductor layer (1) in the termination region (TR) wherein the first recess (9) surrounds the active region (AR) and the sidewall (9e) of the first recess (9) adjacent to the active region (AR) is laterally aligned with the circumferential edge (5e) of the field plate (5) such that in an orthogonal projection onto a plane parallel to the first main side (2) the edge of the recess defined by the upper end of the sidewall is within less than 1 μm from the circumferential edge of the field plate (5), or less than 0.5 μm , or less than 0.2 μm ,

15 characterized in that the step of forming the field plate (5) comprises:

forming a dielectric layer (4) on the first main side (2) of the wide-bandgap semiconductor layer (1);

forming a first metal layer (7) on the dielectric layer (4); and

20 patterning the first metal layer (7) and the dielectric layer (4) to expose at least the first portion of the first main side (2) of the wide-bandgap semiconductor layer (1) in the termination region (TR) where the first recess (9) is to be formed in the step of anisotropic etching,

wherein in the step of anisotropic etching the patterned first metal layer (7) is used at least as a part of an etching mask, and

25 wherein the patterned first metal layer (7) in the termination region (TR) forms the field plate (5) in the power semiconductor device.

9. The method according to claim 8, wherein the dielectric layer (4) is patterned before the step of forming the first metal layer (7) to form an opening in the dielectric layer (4) that exposes at least a second portion of the first main

side (2) of the wide-bandgap semiconductor layer (1) in the active region (AR).

10. The method according to claim 8 or 9, wherein
- 5 the patterned first metal layer (7) and the patterned dielectric layer (4) expose a third portion of the first main side (2) of the wide-bandgap semiconductor layer (1) in the active region (AR),
- a second recess (14) is formed in the active region (AR) in the step of anisotropic etching together with the first recess (9) using the patterned first
- 10 metal layer (7) as the etching mask, and
- the second recess (14) is filled with a filling material.
11. The method according to claim 8 or 9, wherein
- 15 the patterned first metal layer (7) and the patterned dielectric layer (4) expose a fourth portion of the first main side (2) of the wide-bandgap semiconductor layer (1) in the active region (AR),
- the method further comprises a step of forming a contact electrode (8) in direct contact with the fourth portion of the first main side (2) of the wide-bandgap semiconductor layer (1) before the anisotropic etching of the wide-
- 20 bandgap semiconductor layer (1), and
- the contact electrode (8) is used together with the patterned first metal layer (7) as the etching mask in the step of anisotropic etching of the wide-bandgap semiconductor layer (1).
- 25 12. The method according to claim 9, wherein the first metal layer (7) is formed to be in direct contact with the first main side (2) of the wide-bandgap semiconductor layer (1) through the opening in the dielectric layer (4).
13. The method according to claim 8, wherein the step of forming the field plate
- 30 (5) comprises:

forming a second metal layer (15) on the first metal layer (7), wherein the first and the second metal layer (7, 15) are formed of different metals;

patterning the second metal layer (15) to expose at least the first portion of the first main side (2) of the wide-bandgap semiconductor layer (1) in the termination region (TR) where the first recess (9) is to be formed in the step of anisotropic etching,

wherein, in the step of anisotropic etching, the second metal layer (7, 15) is used at least as a part of the etching mask.

- 10 14. The method according to claim 13, wherein the patterning of the second metal layer (15), the first metal layer (7) and the dielectric layer (4) comprises:

patterning the second metal layer (15) to expose the first metal layer (7) in areas of the first portion of the first main side (2) of the wide-bandgap semiconductor layer (1) in the termination region (TR);

forming trenches (16) in the second metal layer (15) in the active region (AR) to expose the first metal layer (7) at the bottom of the trenches (16),

refilling the trenches (16) at least partially by a filling material (17),

and

patterning the first metal layer (7) and the dielectric layer (4) by anisotropic etching using the second metal layer (15) and the filling material (17) as an etching mask

the method further comprising the following steps:

removing the filling material (17) after the step of patterning the first metal layer (7) and the dielectric layer (4);

thereafter removing a portion of the second metal layer (15) in which the trenches (16) are formed by isotropic etching of portions respectively separating neighbouring trenches;

5 thereafter removing portions of the first metal layer (7) and of the dielectric layer (4) in the active region (AR) by anisotropic etching using the second metal layer (15) as an etching mask to expose a fifth portion of the first main side (2) of the wide-bandgap semiconductor layer (1) in the active region (AR); and

forming a contact electrode (8) contacting the fifth portion of the first main side (2) of the wide-bandgap semiconductor layer (1).

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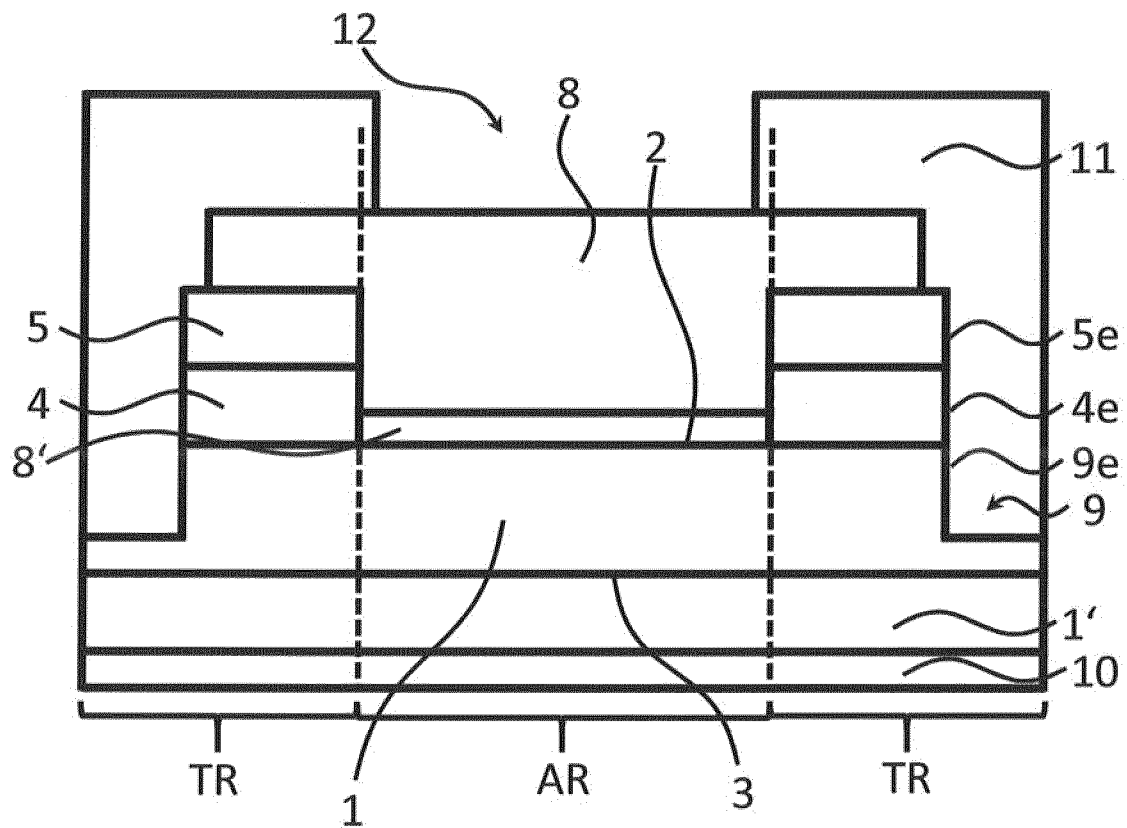


Fig. 1A

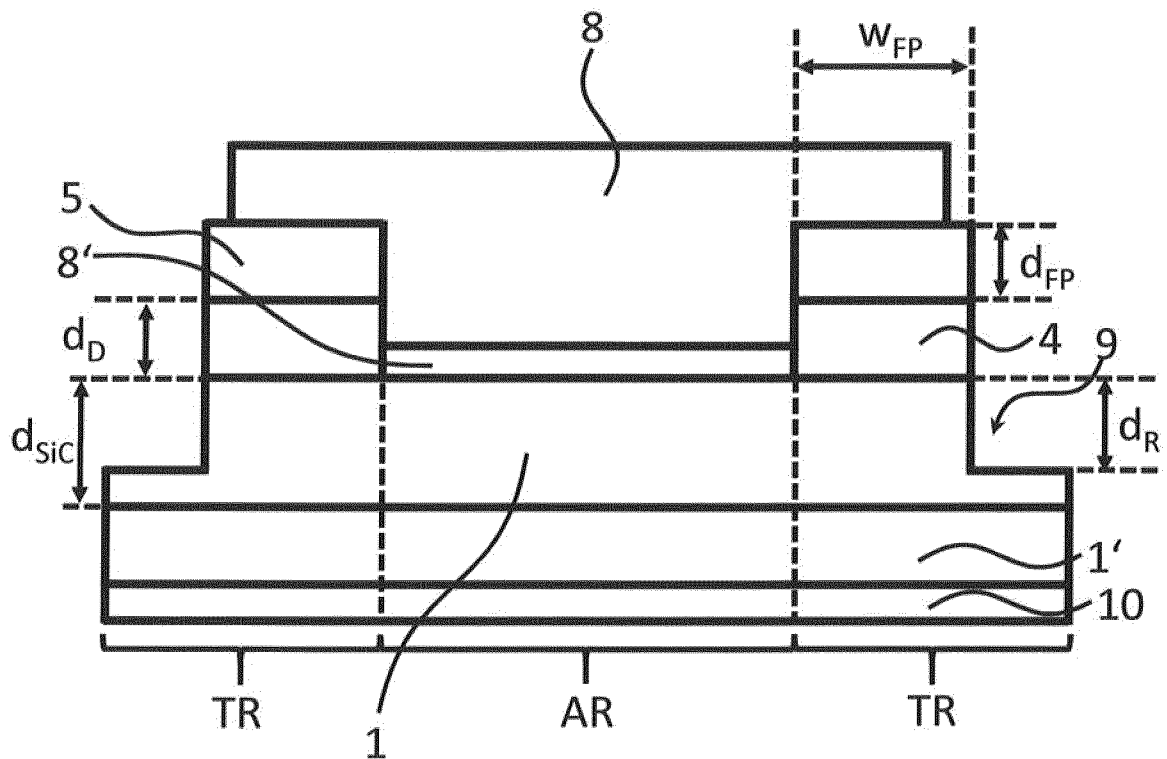


Fig. 1B

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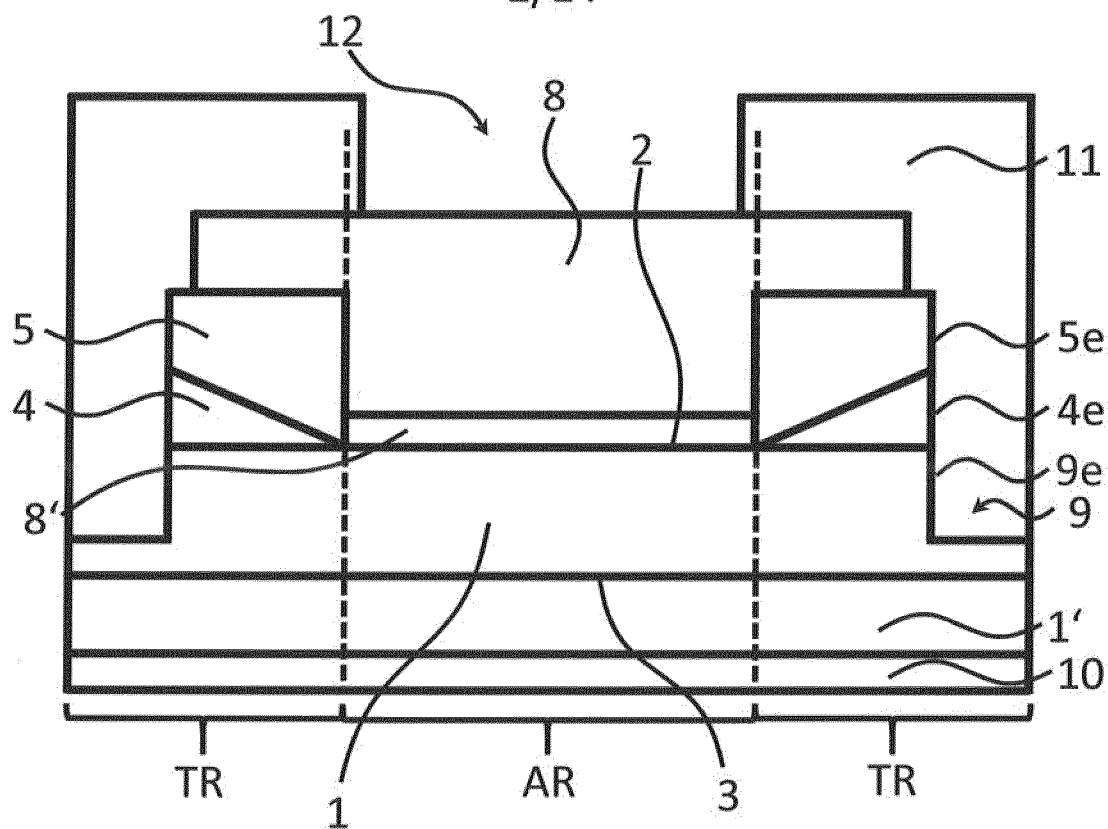


Fig. 1C

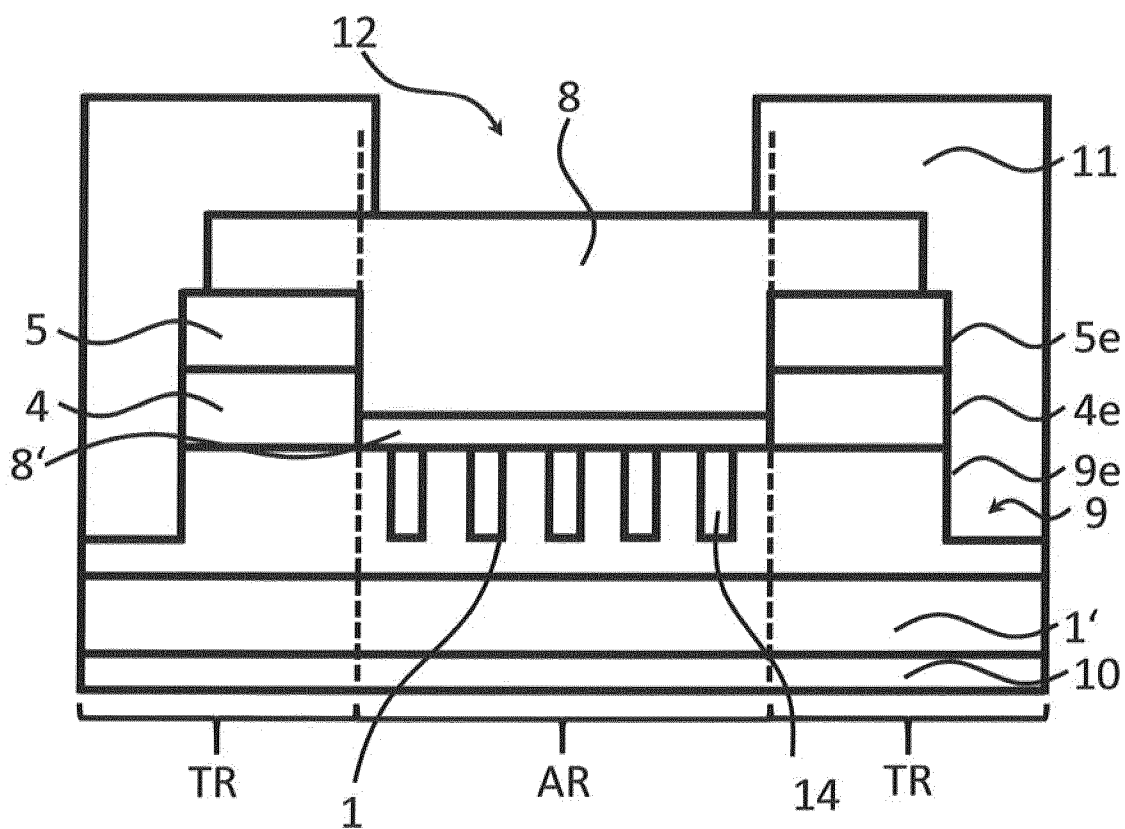


Fig. 1D

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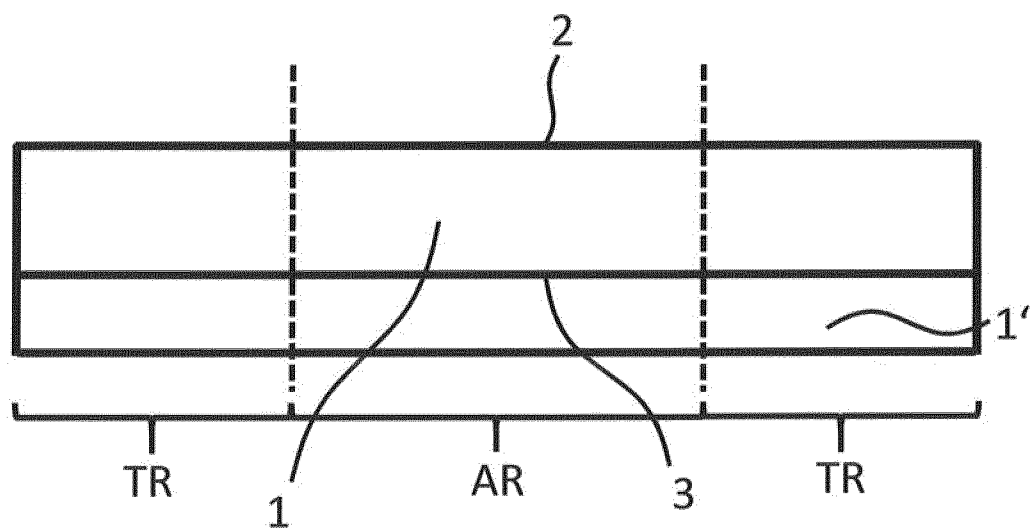


Fig. 2A

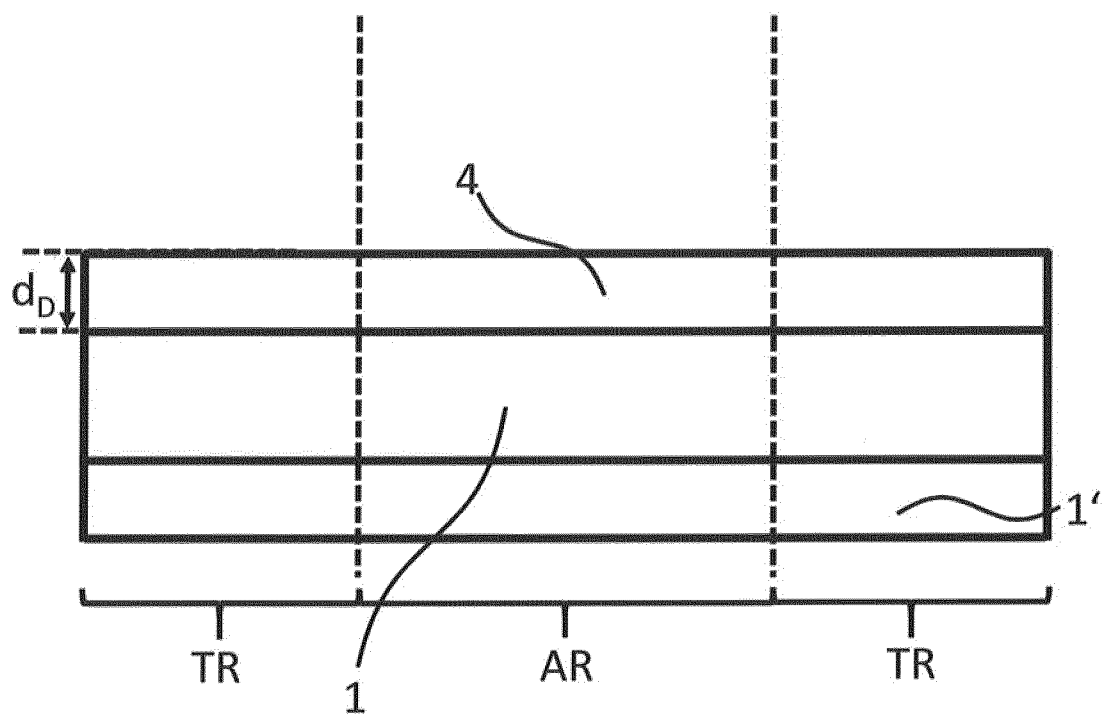


Fig. 2B

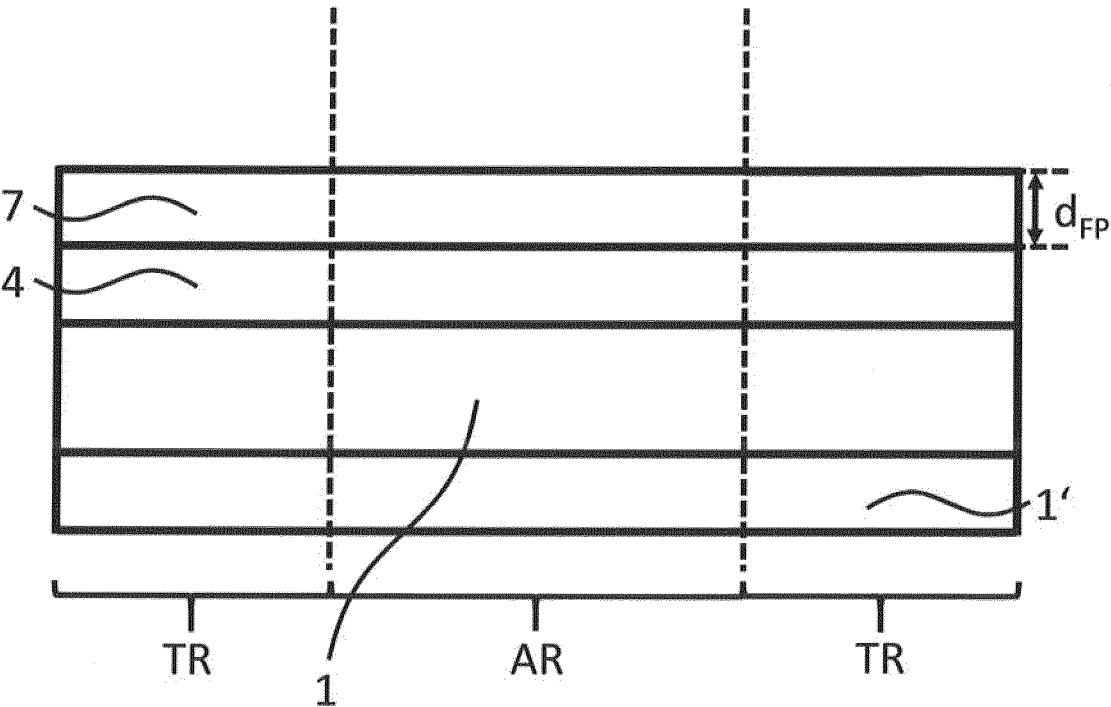


Fig. 2C

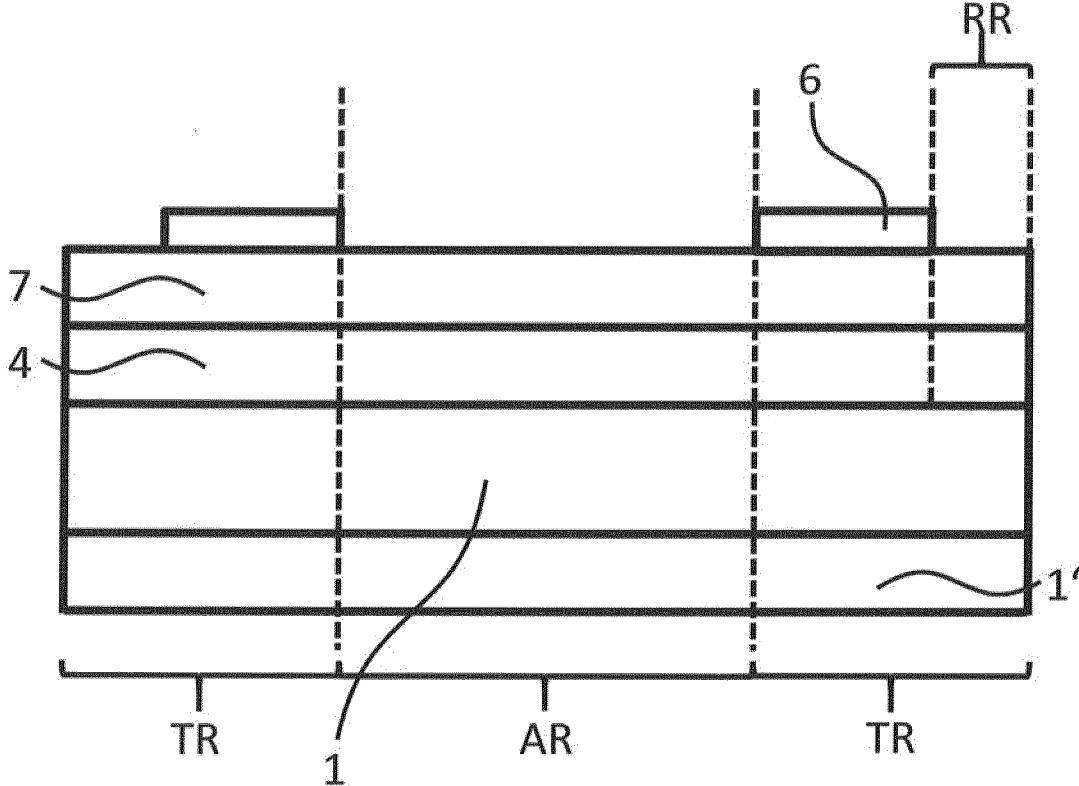


Fig. 2D

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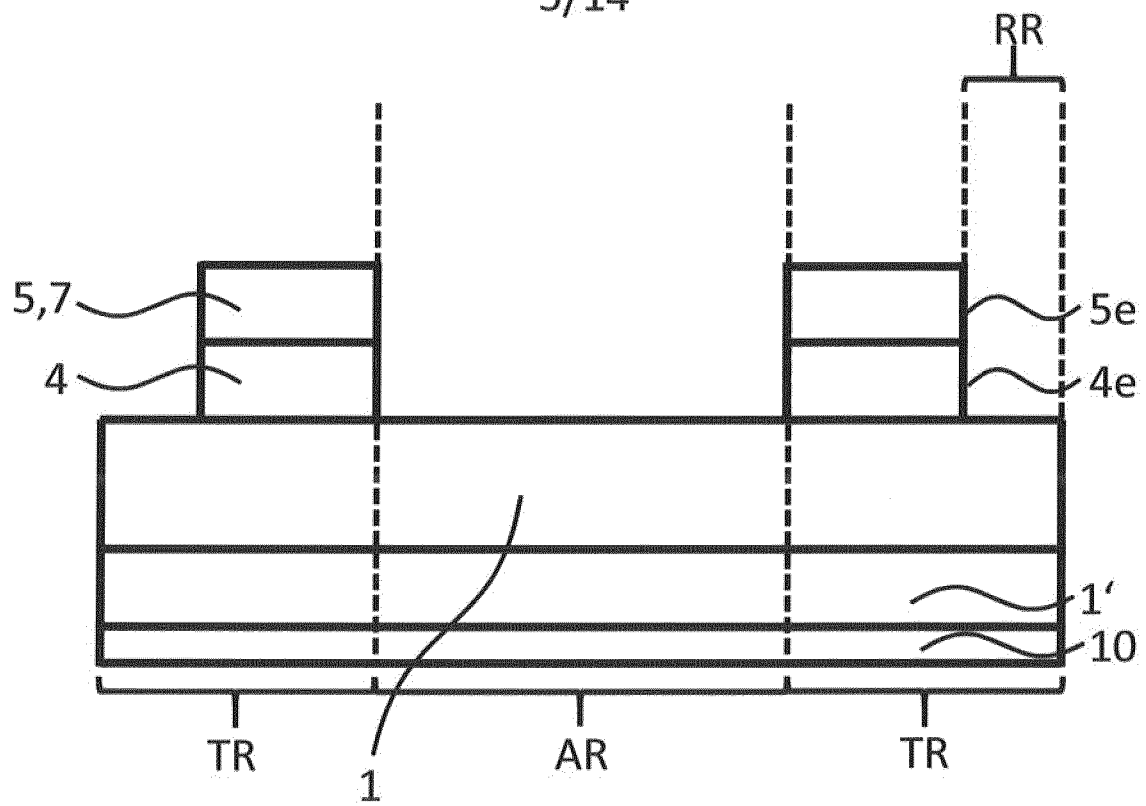


Fig. 2E

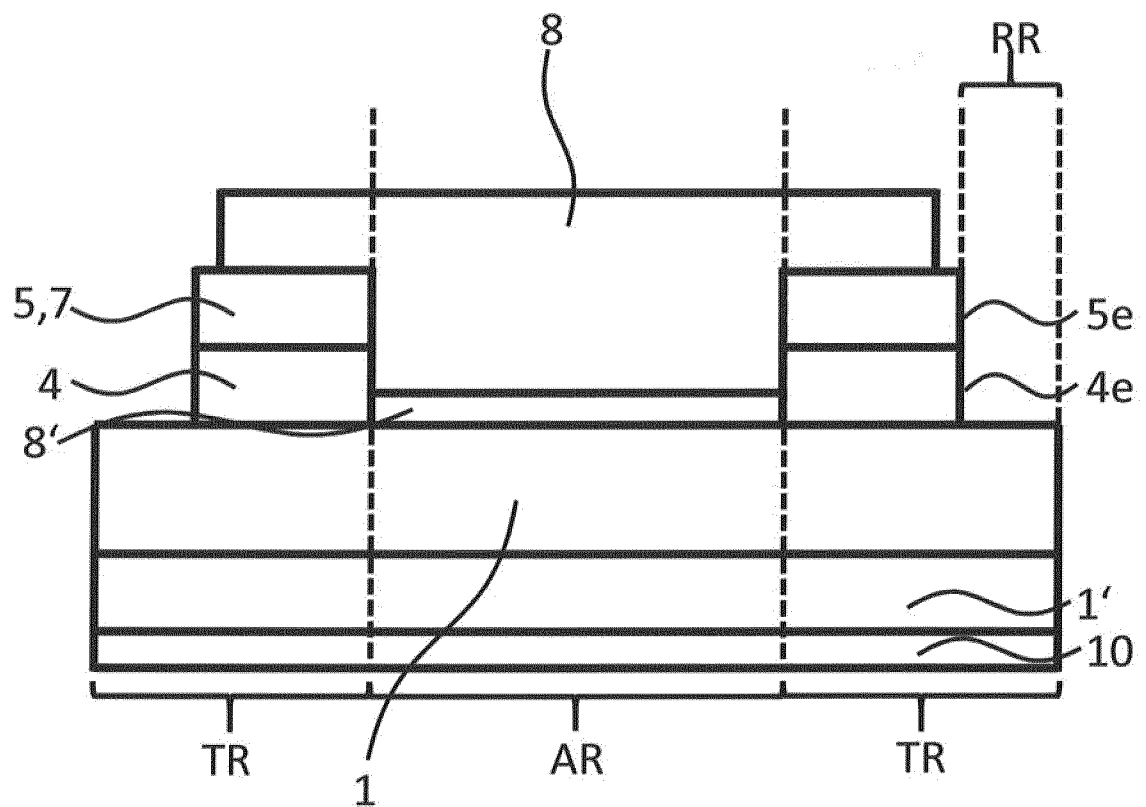


Fig. 2F

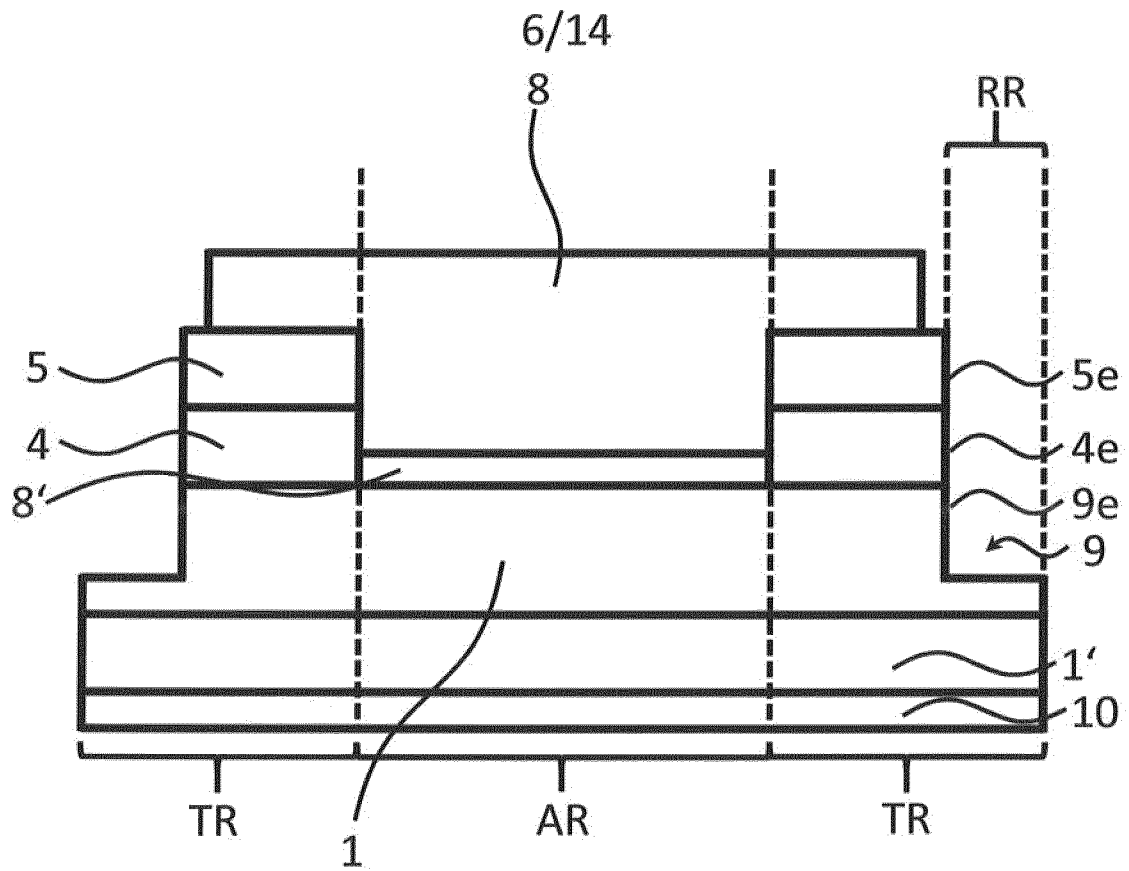


Fig. 2G

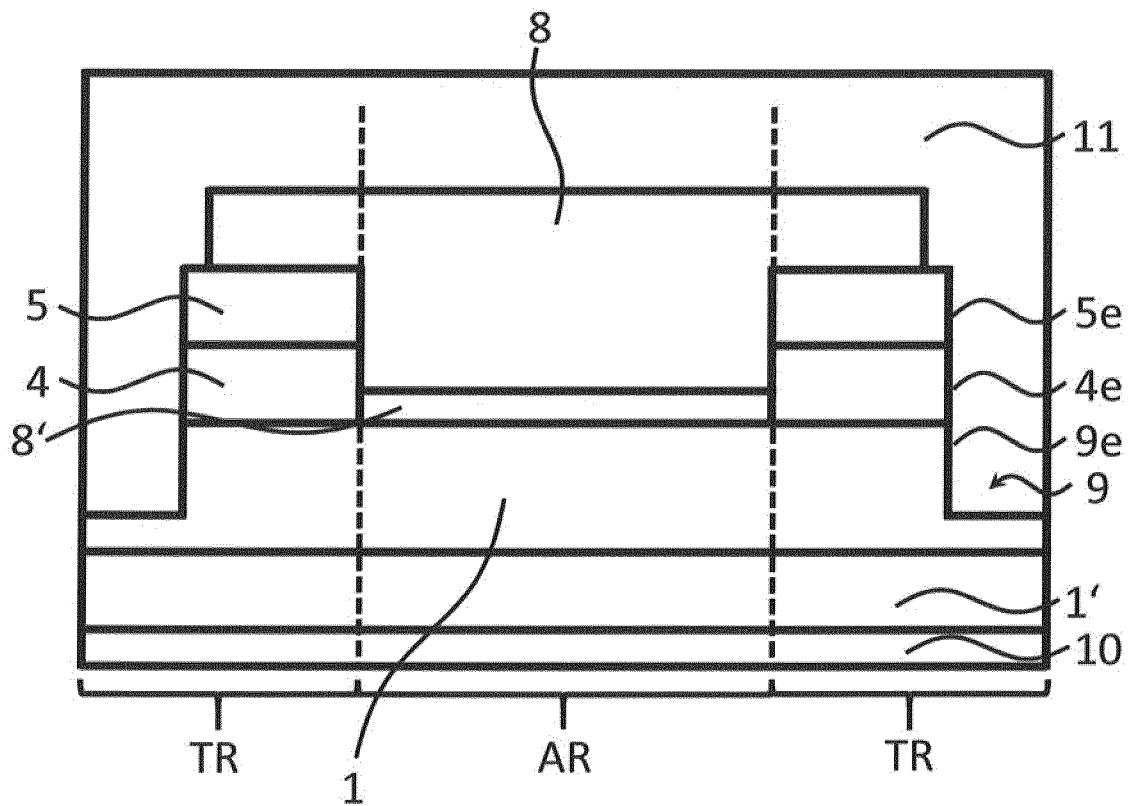


Fig. 2H

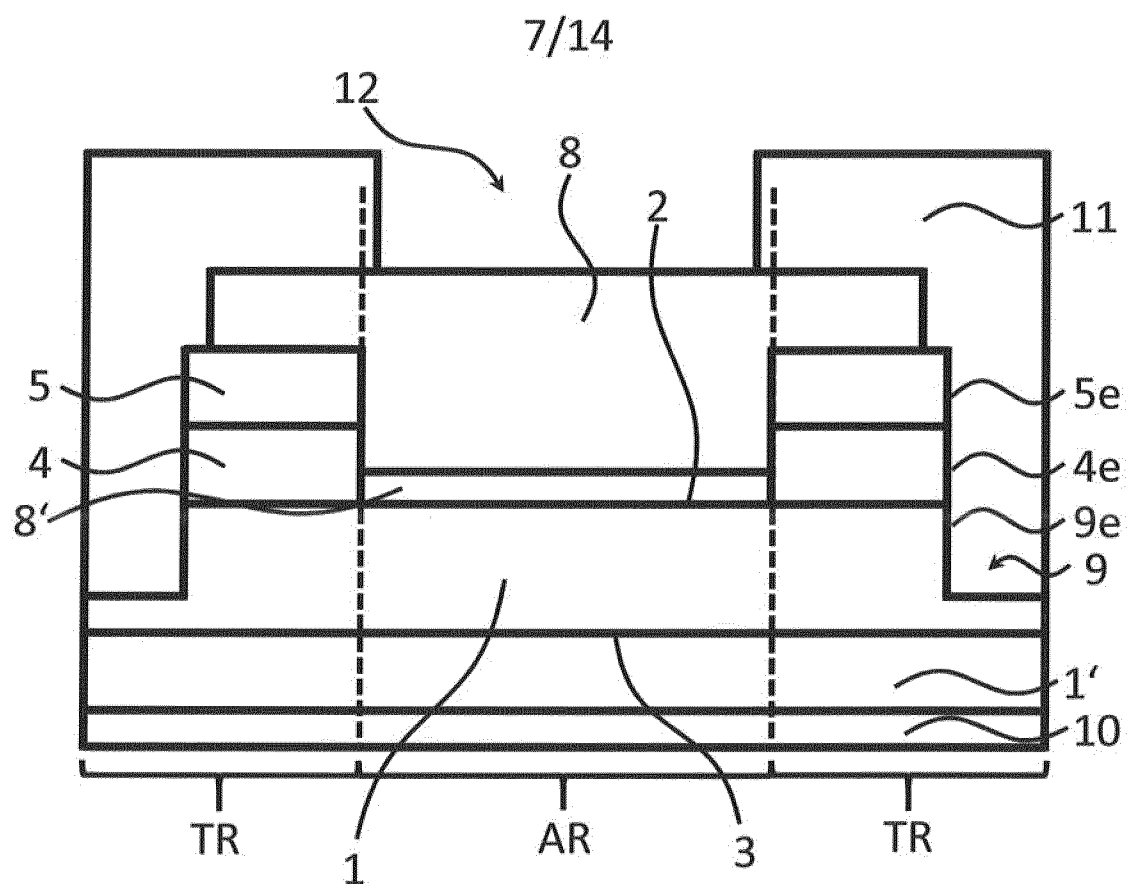


Fig. 21

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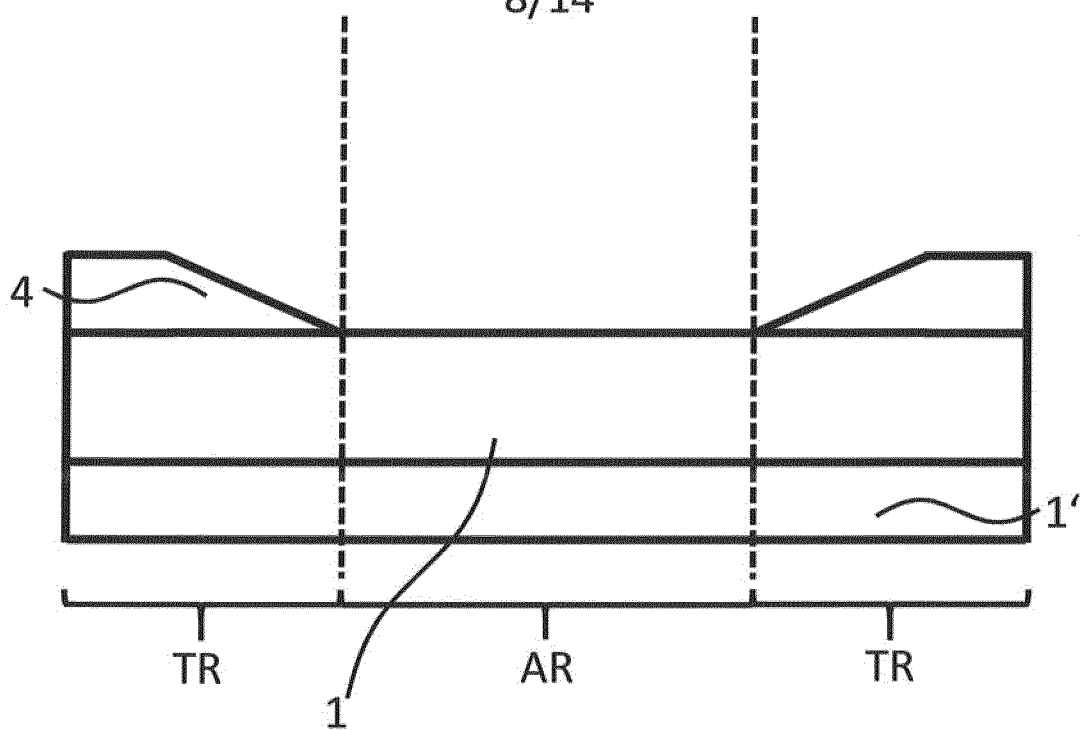


Fig. 3A

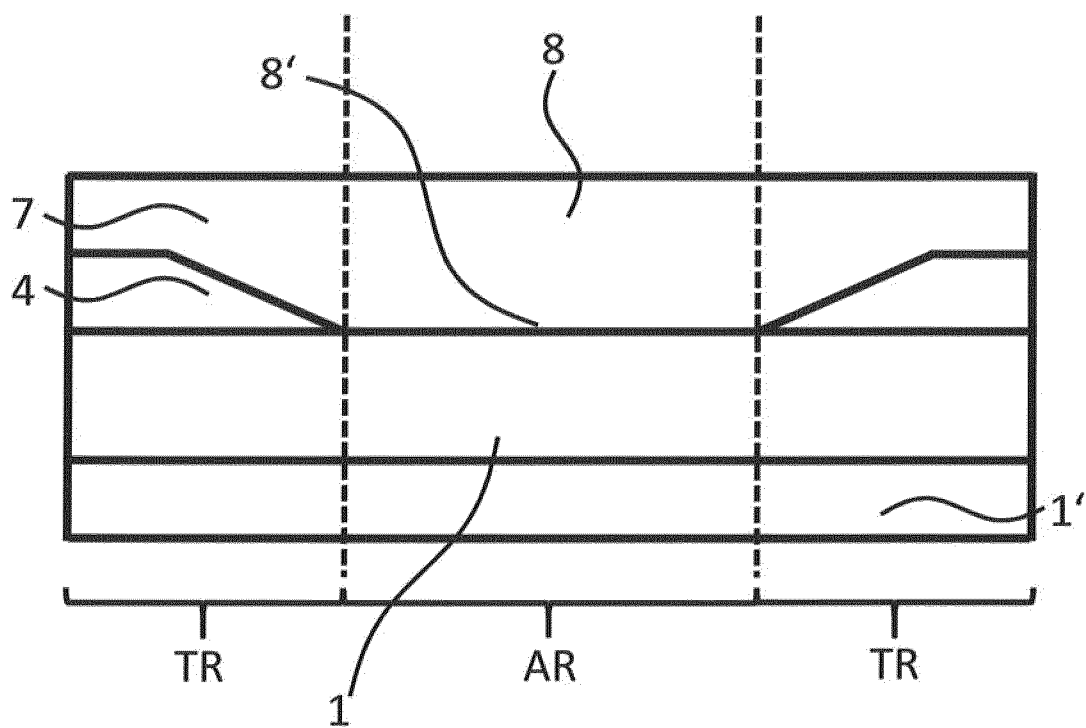


Fig. 3B

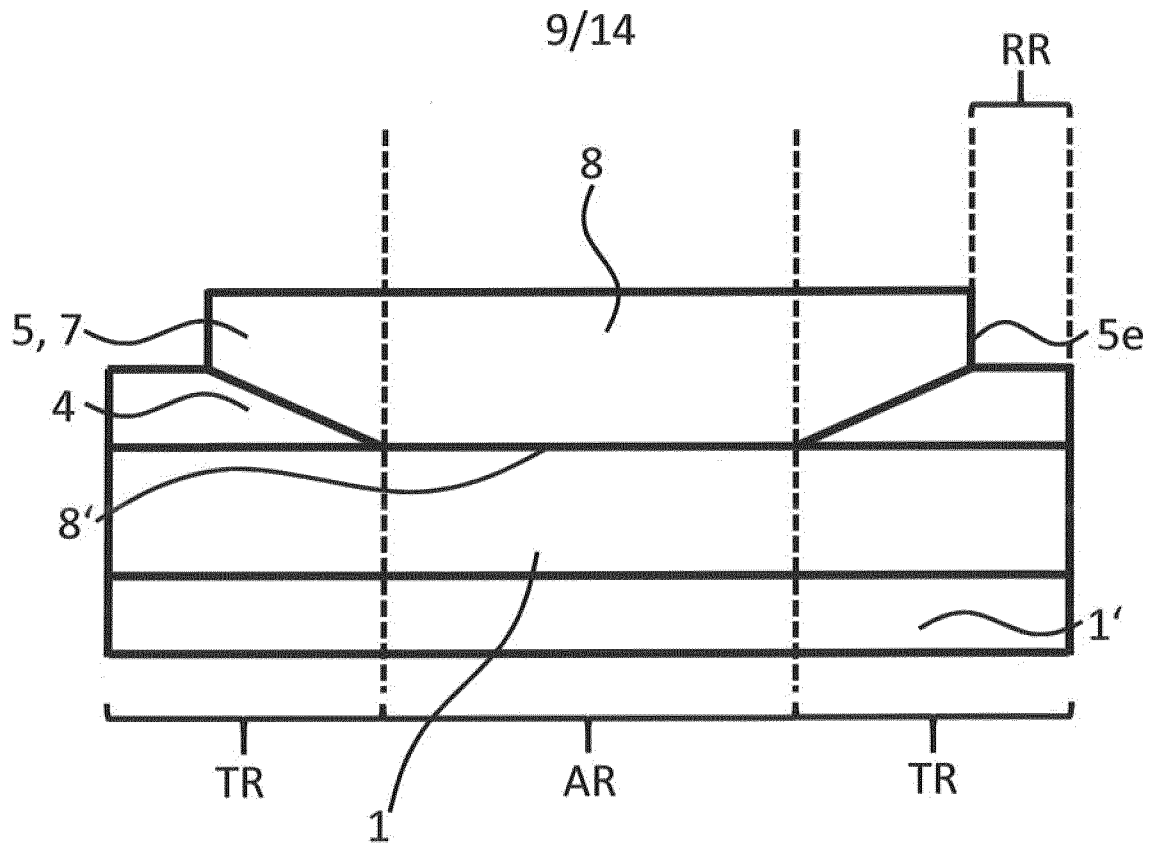


Fig. 3C

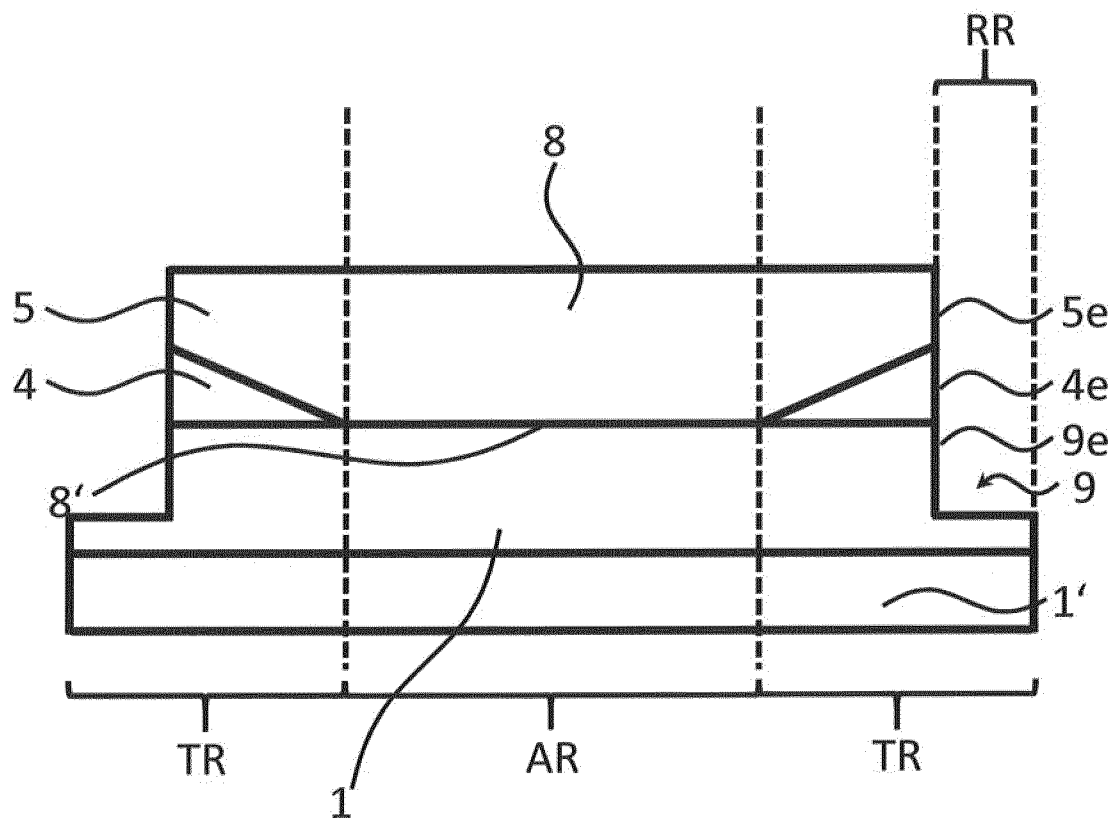
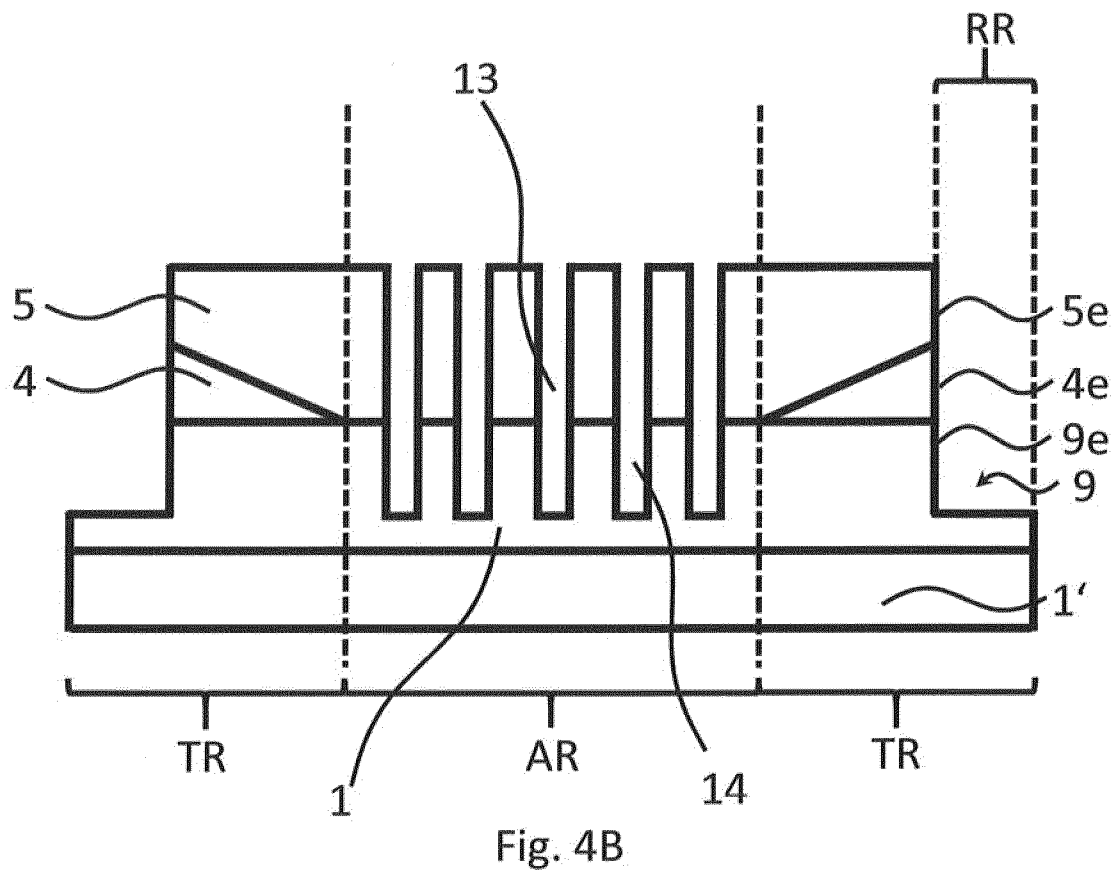
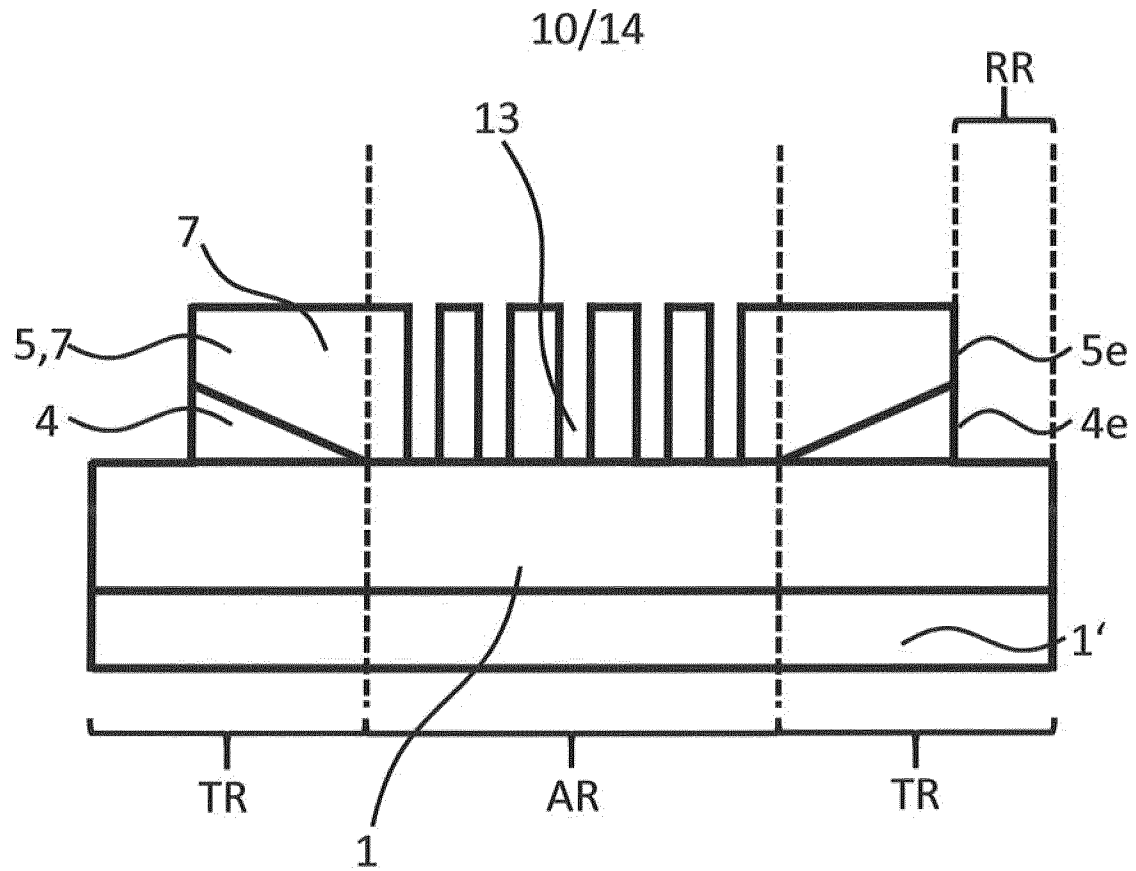


Fig. 3D



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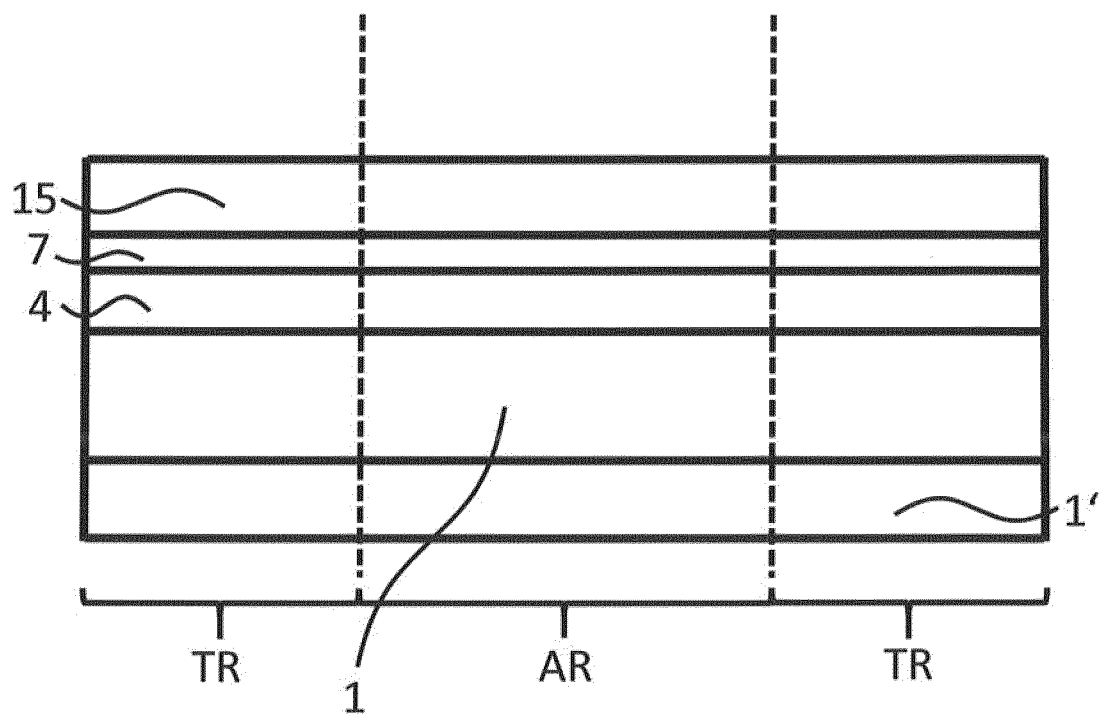


Fig. 5A

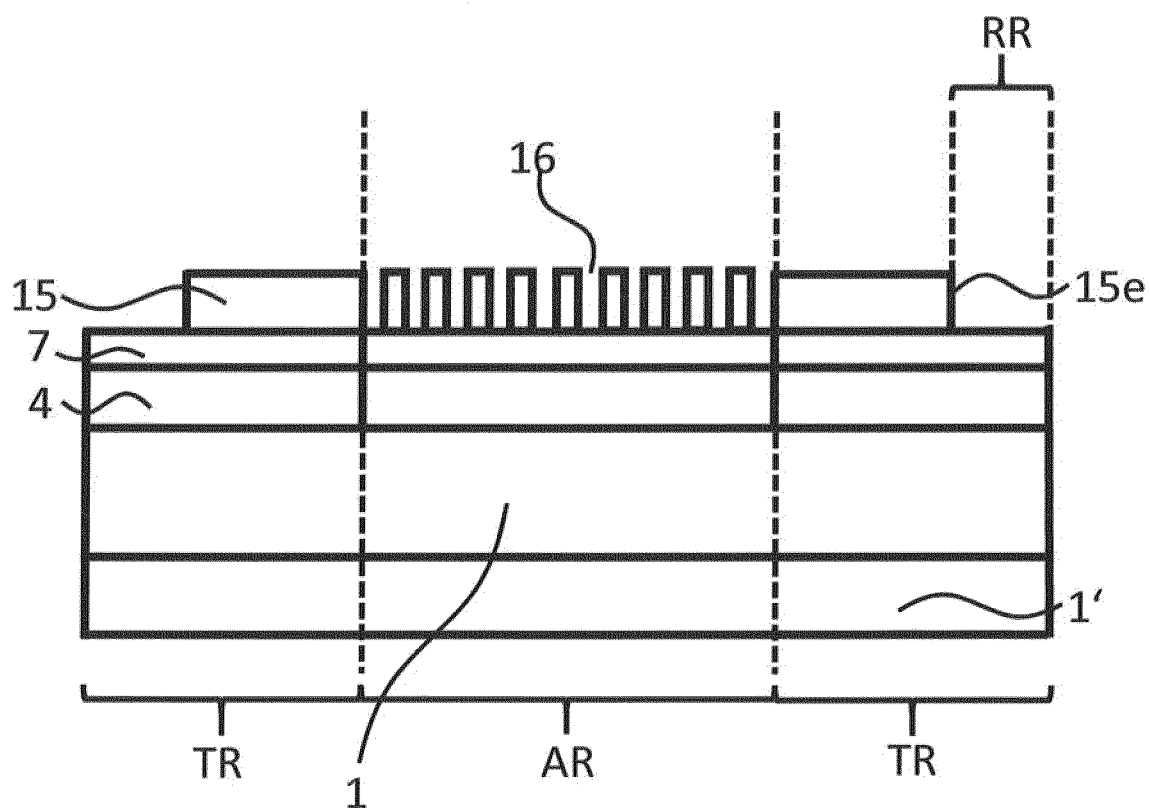
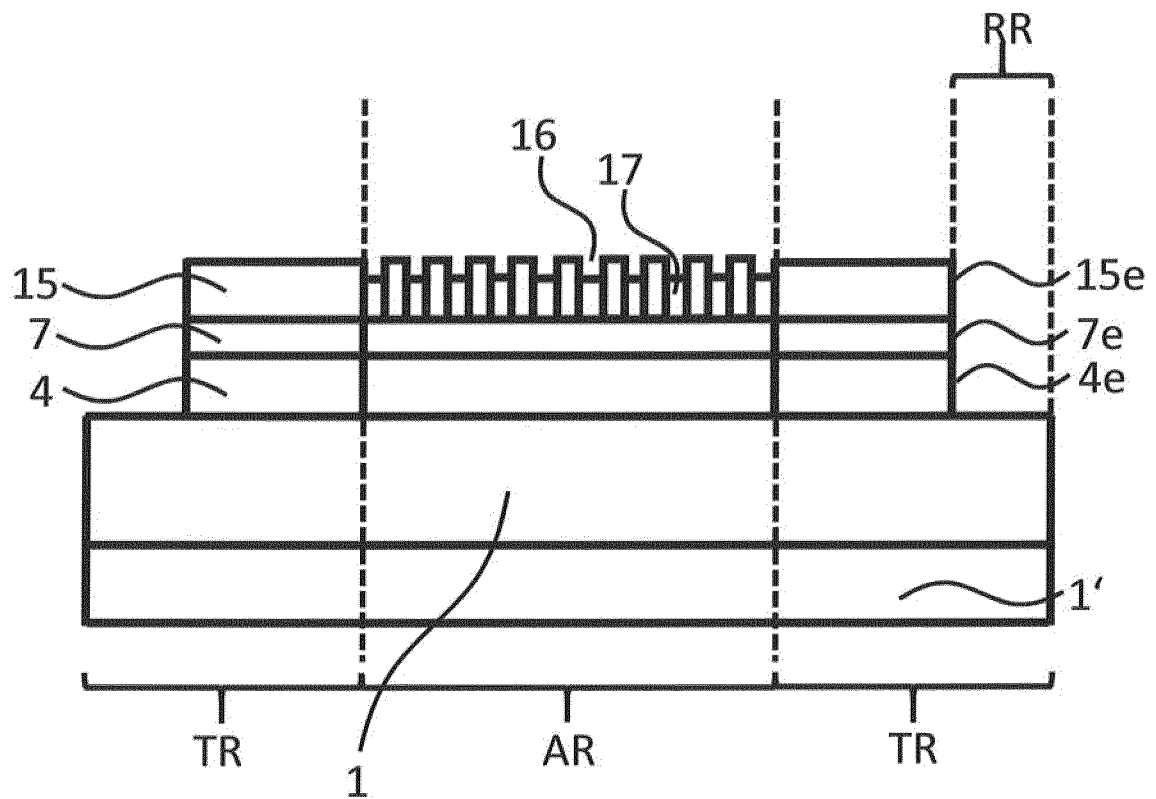
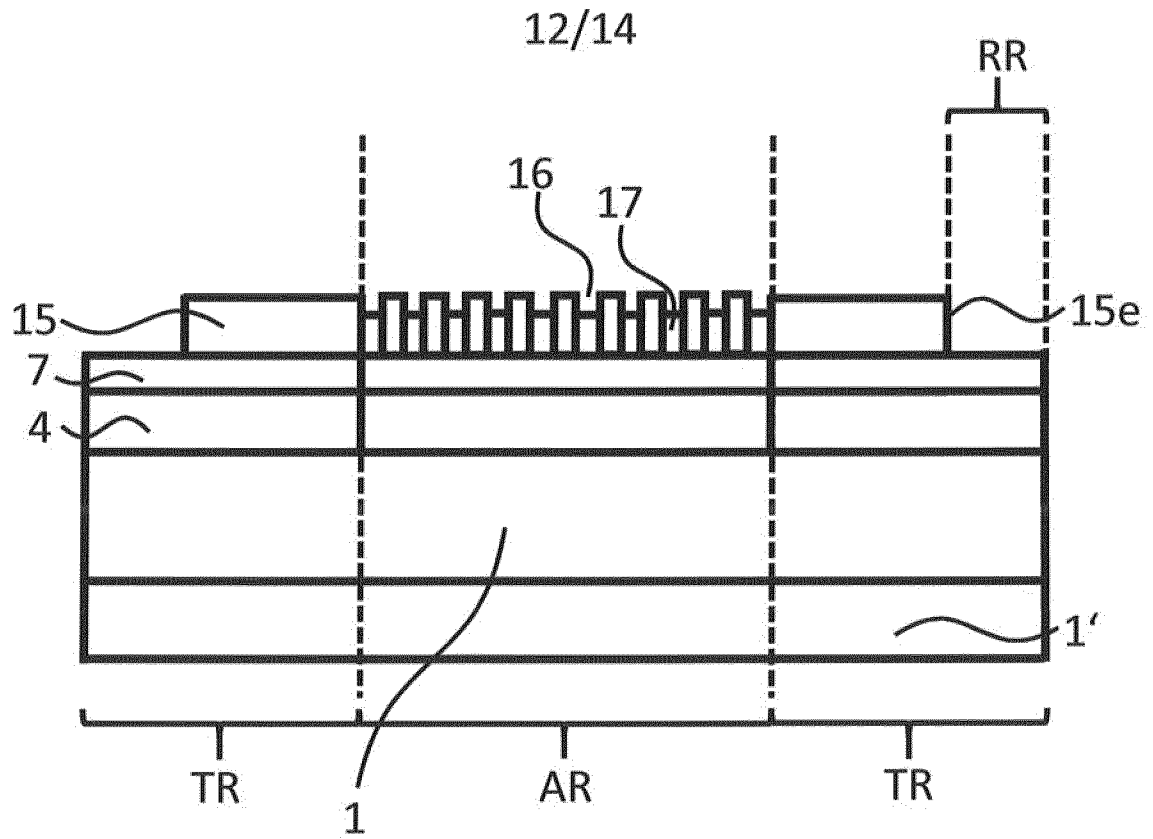


Fig. 5B



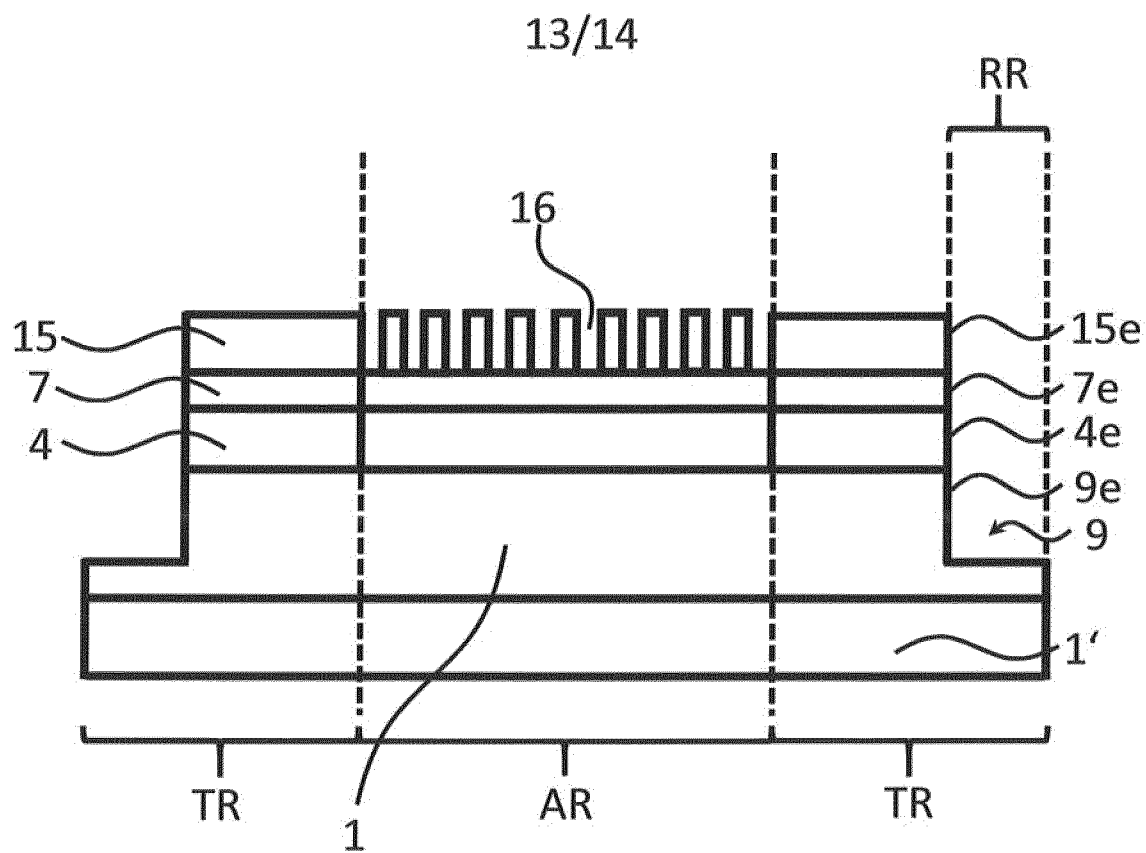


Fig. 5E

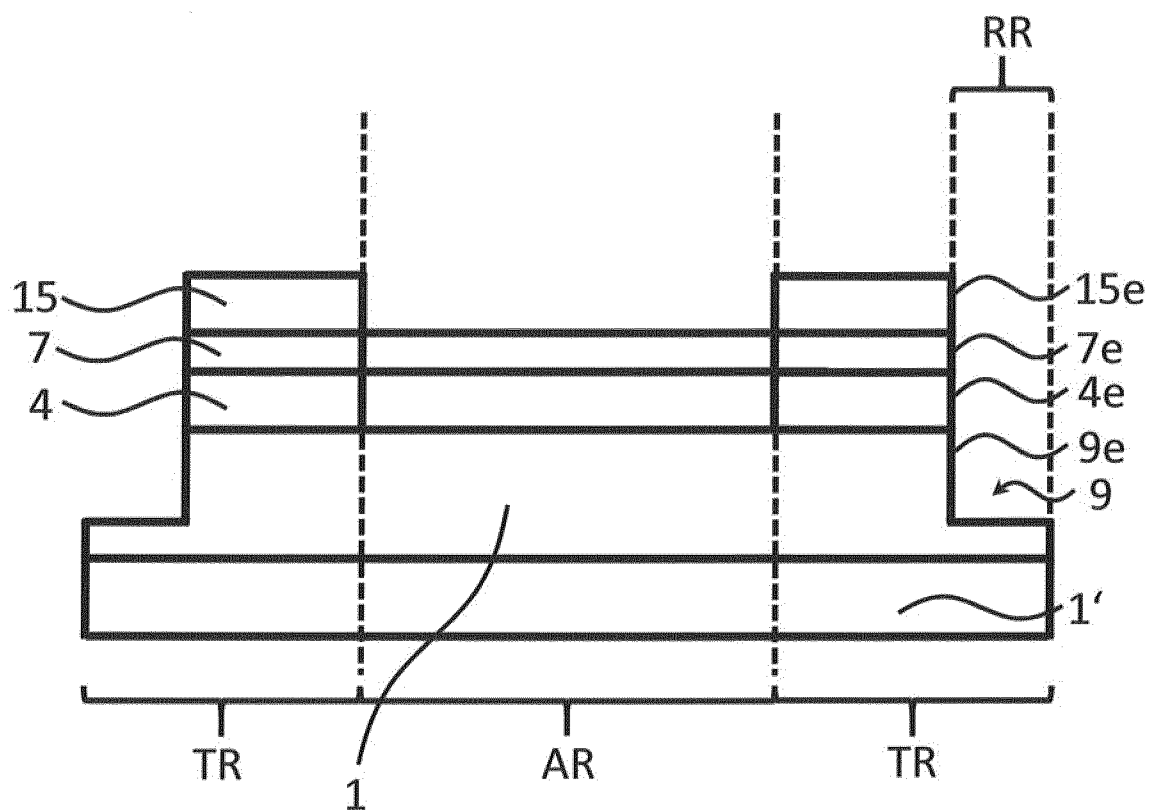


Fig. 5F

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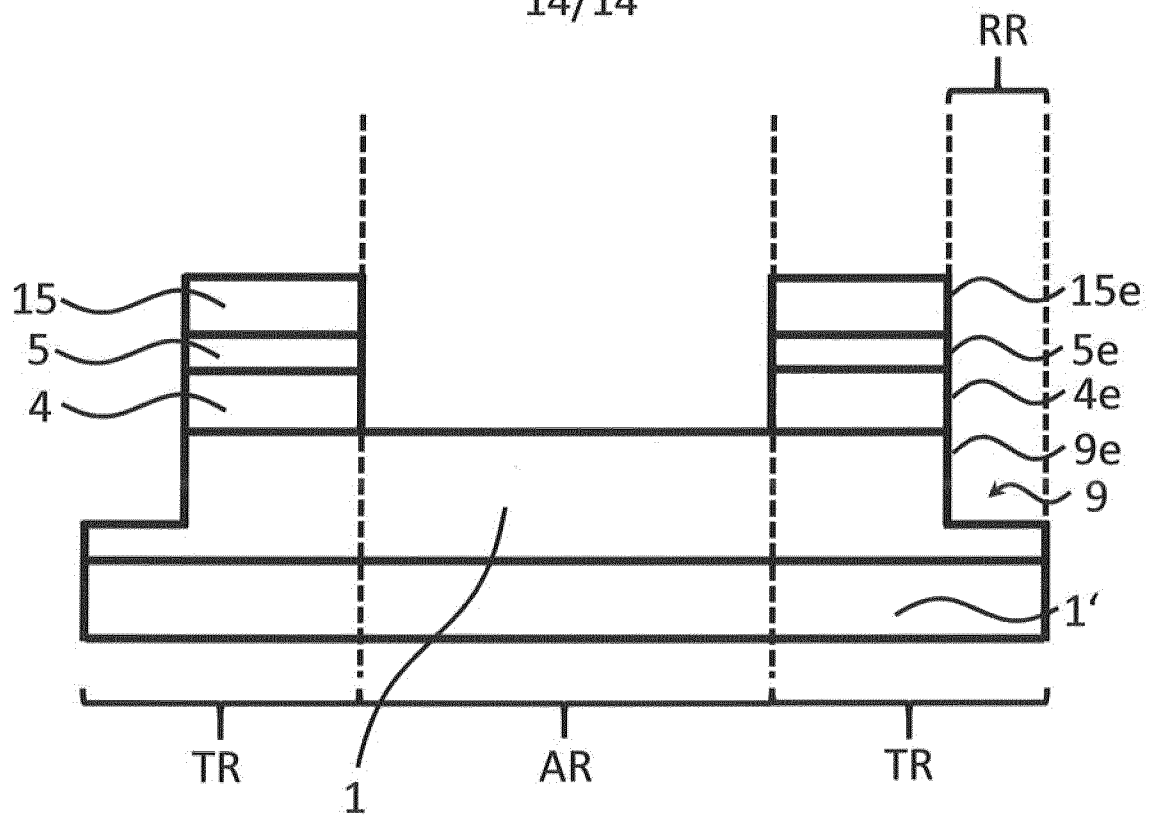


Fig. 5G

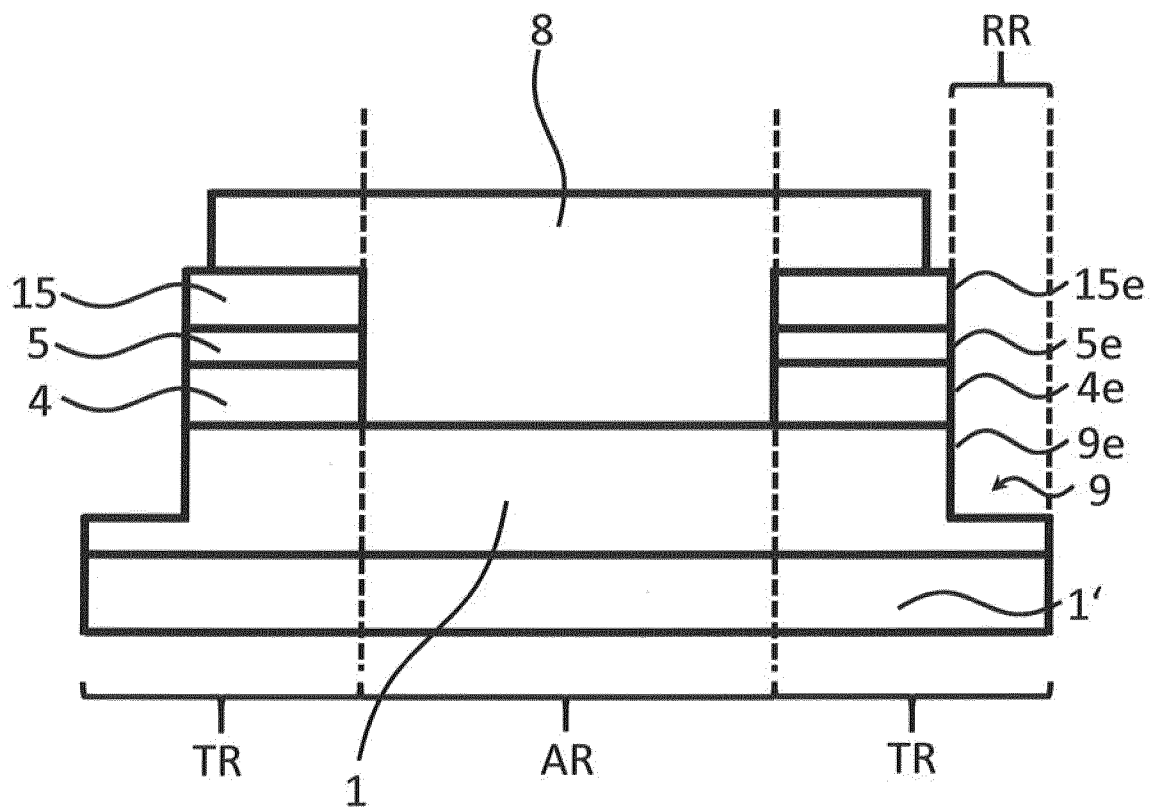


Fig. 5H

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/055376

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L29/872 H01L29/40 H01L21/329 H01L29/16 H01L29/06
ADD. H01L29/20 H01L29/861 H01L29/24

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/101369 A1 (ZHU TINGGANG [US]) 5 May 2011 (2011-05-05)	1,2,4-7
A	paragraph [0024]; figure 5 -----	8-14
X	EP 2 927 962 A1 (SUMITOMO ELECTRIC INDUSTRIES [JP]) 7 October 2015 (2015-10-07)	1-7
A	paragraphs [0025] - [0037]; figures 1,2 -----	8-14
A	US 2010/059761 A1 (HORII TAKU [JP] ET AL) 11 March 2010 (2010-03-11)	3
	paragraphs [0046], [0047]; figure 1 -----	
A	US 2005/258483 A1 (TEMPLIER FRANCOIS [FR] ET AL) 24 November 2005 (2005-11-24) Fig. 3 and related text -----	3
	-/--	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

25 April 2019

Date of mailing of the international search report

07/05/2019

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Fax: (+31-70) 340-3016

Authorized officer

Melodia, Andrea

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/055376

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 612 232 A (THERO CHRISTINE [US] ET AL) 18 March 1997 (1997-03-18) Fig. 2, 3 and related text -----	1-14
A	US 2007/108547 A1 (ZHU TING G [US] ET AL) 17 May 2007 (2007-05-17) paragraphs [0034] - [0038]; figures 2A-2E -----	1-14
A	US 7 078 780 B2 (CHIP INTEGRATION TECH CO LTD [TW]) 18 July 2006 (2006-07-18) Fig. 2A-2G and related text -----	1-14
A	JP 2016 181581 A (NIPPON INTER ELECTRONICS CORP) 13 October 2016 (2016-10-13) Fig. 1, 2 and related text -----	1-14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2019/055376

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2019/055376

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