(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 June 2004 (10.06.2004)

PCT

(10) International Publication Number
WO 2004/049445 A1

(51) International Patent Classification[7]: H01L 27/088, 27/092

(21) International Application Number:
PCT/US2003/032782

(22) International Filing Date: 14 October 2003 (14.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/301,617 22 November 2002 (22.11.2002) US

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(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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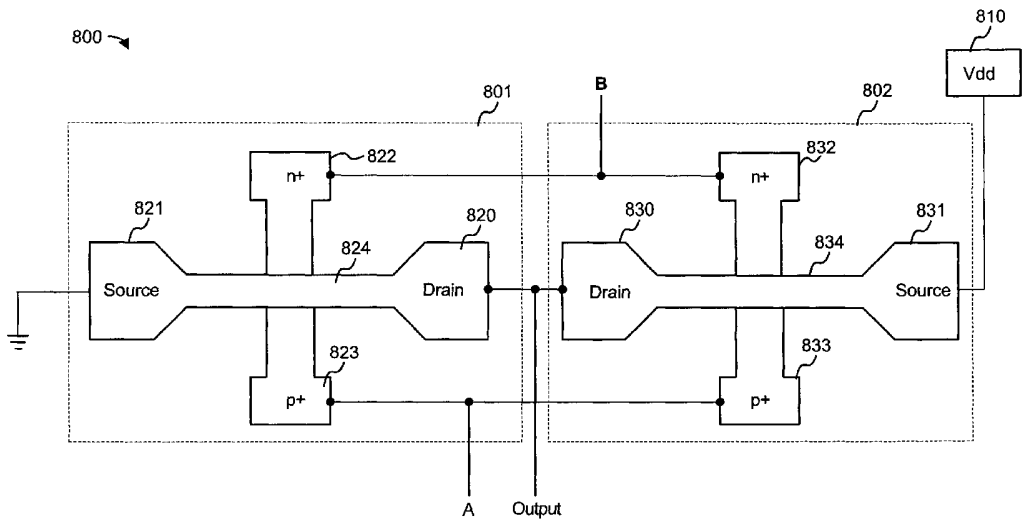
(54) Title: TWO TRANSISTOR NOR DEVICE



(57) Abstract: A NOR gate includes is constructed with two asymmetric FinFET type transistors (801, 802) instead of the conventional four-transistor NOR gate. The reduction in the number of transistors from four down to two allows for significant improvements in integrated semiconductor circuits.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

TWO TRANSISTOR NOR DEVICE

BACKGROUND OF THE INVENTION

A. Field of the Invention

The present invention relates generally to semiconductor manufacturing and semiconductor devices and, more particularly, to double gate metal-oxide semiconductor field-effect transistors (MOSFET).

B. Description of Related Art

Transistors, such as MOSFETs, are the core building block of the vast majority of semiconductor devices. Some semiconductor devices, such as high performance processors, can include millions of transistors. For these devices, decreasing transistor size, and thus increasing transistor density, has traditionally been a high priority in the semiconductor manufacturing area.

Conventional MOSFETs have difficulty scaling below 50nm fabrication processing. To develop sub-50nm MOSFETs, double-gate MOSFETs have been proposed. In several respects, the double-gate MOSFETs offer better characteristics than the conventional bulk silicon MOSFETs. These improvements arise because the double-gate MOSFET has a gate electrode on both sides of the channel, rather than only on one side as in conventional MOSFETs. When there are two gates, the electric field generated by the drain is better screened from the source end of the channel. Also, two gates can control roughly twice as much current as a single gate, resulting in a stronger switching signal.

Transistors on a semiconductor device are often connected into groups that implement higher level logical gates. One frequently used logical gate is the NOR gate. Conventionally, four transistors, such as four double-gate MOSFETs, are used to create a NOR gate.

It would be desirable to more efficiently implement a logical gate such as a NOR gate, as this would increase the overall efficiency of the semiconductor device.

SUMMARY OF THE INVENTION

Implementations consistent with the present invention include a NOR gate implemented with only two transistors.

One aspect of the invention is directed to an integrated semiconductor device. The device includes a number of asymmetric FinFETs, at least some of the FinFETs being arranged as pairs of FinFETs that define logic NOR gates.

A second aspect of the invention is directed to a logic NOR gate consisting of a first double-gate transistor and a second double-gate transistor. An output signal coupled to the first and second transistors reflects a logical NOR operation of two input signals coupled to the first and second transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

Fig. 1 is a schematic diagram that illustrates a top-level view of a FinFET consistent with principles of the invention;

Figs. 2-7 are schematic diagrams taken along the line A-A' in Fig. 1 that illustrate a method of forming an asymmetric FinFET;

Fig. 8 is a schematic diagram that illustrates a top view of a NOR gate constructed in a manner consistent with the present invention; and

Fig. 9 is a diagram illustrating deposition of polysilicon over two gate portions of a FinFET.

BEST MODE FOR CARRYING OUT THE INVENTION

The following detailed description of the invention refers to the accompanying drawings. The same reference numbers may be used in different drawings to identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and equivalents.

Two transistors are connected together to implement a NOR gate. Each one of the transistors may be an asymmetric FinFET having two separately addressable gates.

ASYMMETRIC FinFET

A FinFET, as the term is used herein, refers to a type of double-gate MOSFET in which a conducting channel is formed in a vertical Si "fin" controlled by a self-aligned double-gate. FinFETs are known in the art. Although conventional FinFETs are typically described as "double-gate" MOSFETs, the two gates are electrically connected and thus form a single logically addressable gate.

Fig. 1 is a top-level view of a FinFET 100 consistent with principles of the invention. FinFET 100 includes a source region 101, a drain region 102, and a channel region 103. The channel region 103 includes the transistor's fin, as described with respect to Fig. 2, below. Unlike conventional FinFETs, in which both sides of the gate are electrically connected together, FinFET 100 may additionally include two addressable gates, labeled as gates 104 and 105. The gates may further be asymmetrically doped. Gate 104 may, for example, be implanted with n-type dopants (e.g., As^+ or P^+) and gate 105 may be implanted with p-type dopants (e.g., B or BF_2), as described in more detail below.

Figs. 2-7 are cross-sectional views taken along the line A-A' in Fig. 1. Figs. 2-8 each illustrate steps in the manufacturing process of FinFET 100.

Referring to Fig. 2, FinFET 100 may be a silicon on insulator (SOI) device that includes a silicon substrate 210 and a buried oxide (BOX) layer 220 disposed on the silicon substrate. Substrate 210 and layer 230 may alternatively comprise germanium, metals, or combinations of such materials, such as silicon-germanium. Buried oxide layer 220 may be formed on silicon substrate 210 in a conventional manner. Buried oxide layer 220 may range, for example, from approximately 200 nm to 400 nm in thickness.

A silicon layer may be disposed on BOX layer 220 and etched to create the source, drain, and fin 225 (source and drain not shown in Fig. 2). Alternatively, source/drain regions 101 and 102 may be formed by depositing silicon and etching the silicon after the fin 225 is formed. In one implementation, fin 225 may range from, for example, approximately 5 nm to about 25 nm in width. Before etching fin 225, a Si_3N_4 layer 230 may be deposited via chemical vapor deposition (CVD) on fin 225. Layer 230 may alternatively be a SiO_2 layer. Layer 230 protects fin 225 during the fabrication process, and may be, for example, deposited to a thickness ranging from about 20-50 nm.

By oxidizing the silicon surface of fin 225, gate dielectric layers 235 may be grown on the side surface of fin 225. Gate dielectric layers 235 may be as thin as 0.8 nm to 2 nm in width.

Referring to Fig. 3, polysilicon spacers 240 may next be formed around fin 225 (and around gate dielectric layers 235 and layer 230) using conventional deposition and etching techniques.

Polysilicon spacers 240 may then be implanted with an n-type dopant using a tilted implant process (Fig. 4). The dopant may be, for example, As^+ or P^+, and may be implanted using a 3-6 keV (for P^+) or 12-15 keV (for As^+) ion beam at a tilt angle of between 15 and 45 degrees. Because of the presence of fin structure

225, including gate dielectric layers 235 and layer 230, the n-type dopant will be largely blocked from entering one side of polysilicon spacers 240 (e.g., as illustrated of the right side of Fig. 4).

Following the n-type dopant implantation, polysilicon spacers may be implanted with a p-type dopant using a tilted implant process. The ion beam of the implant process may be tilted at a complementary angle to that described with respect to Fig. 4. The dopant may be, for example, B or BF_2, and may be implanted using a 1-2 keV (for B) or 4-8 keV (for BF_2) ion beam at a tilt angle of between 15 and 45 degrees. Because of the presence of fin structure 225, including gate dielectric layers 235 and layer 230, the p-type dopant will be largely blocked from entering one side of polysilicon spacers 240 (e.g., as illustrated on the left side in Fig. 5). Accordingly, the two polysilicon spacers 240 will be asymmetrically doped with n-type and p-type dopants. One of ordinary skill in the art will appreciate that the order of the steps shown in Figs. 4 and 5 could be readily reversed.

Referring to Fig. 6, an undoped polysilicon layer 250 may then be deposited on FinFET 100. Polysilicon layer 250 will form the gates of FinFET 100. Layer 250 may be deposited via, for example, CVD to a depth of approximately 100 nm.

After depositing the polysilicon layer 250, FinFET 100 may be planarized such that layer 250 is substantially planar with the top surface of layer 230, as illustrated in Fig. 7A. This yields two electrically unconnected polysilicon layers, labeled as layers 251 and 252. FinFET 100 may then be annealed to create fully-silicided polysilicon layers 251 and 252, as illustrated in Fig. 7B. Layers 251 and 252 may be connected to gate pads 104 and 105 and may be independently controlled.

Other processes for creating asymmetric FinFETs, such as those illustrated in Fig. 7B may alternatively be employed. For example, the tilt implant process described with respect to Figs. 4 and 5 may be performed after polysilicon gate material is deposited and planarized. In each case, the resulting structure includes the two separately controllable gates, as illustrated in Fig. 7B.

NOR GATE

A NOR gate is a logic gate that is frequently used in integrated circuits. A NOR gate outputs a value based on two or more input signals. Conventionally, NOR gates are constructed using four transistors.

The logic for a two-input NOR gate is shown below in Table I.

Table I

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Consistent with an aspect of the invention, a NOR gate is constructed using two asymmetric FinFETs, such as FinFETs 100. Fig. 8 is a top view of NOR gate 800 constructed in a manner consistent with the present invention. NOR gate 800 may be located in an integrated semiconductor device.

NOR gate 800 includes two FinFETs, labeled as FinFETs 801 and 802. Each of FinFETs 801 and 802 are similar to FinFET 100. In particular, FinFET 801 includes a drain region 820, a source region 821, a first gate 822, a second gate 823, and a channel (fin) region 824. FinFET 802 similarly includes a drain region 830, a source region 831, a first gate 832, a second gate 833, and a channel region 834. First gates 822 and 832 may be doped with n-type impurities while second gates 823 and 833 may be doped with p-type impurities.

As shown in Fig. 8, gates 822 and 832 may be electrically connected; gates 823 and 833 may be electrically connected; and source 821 may be electrically connected to drain 830. Drain 820 may be connected to ground, and source 831 may be connected to a power supply 810.

In operation, the input signal lines to NOR gate 800 (labeled as inputs "A" and "B" in Fig. 8) are applied to the first and second pairs of electrically connected gates. Thus, input signal line A may connect to gates 823 and 833, while input signal line B may connect to gates 822 and 832. The output signal of NOR gate 800 is taken between source 821 and drain 830. The output value depends on inputs A and B according to the logic shown in Table I.

ADDITIONAL DISCLOSURE

In certain situations, it may be desirable to create integrated circuits that include both conventional FinFETs, which have a single connected double-gate, and the asymmetric FinFET described above, which has two separately addressable gates. In these situations, all of the FinFETs may be initially created as described

above in Figs. 2-7. An additional selective epitaxial growth step may then be applied to those of the FinFETs that are to be conventional FinFETs.

Fig. 9 illustrates deposition of polysilicon over the two gate portions of a FinFET 900. Polysilicon layer 901 may be selectively formed on those of the FinFETs in the integrated circuit that are designed to have a single connected gate structure. Polysilicon layer 901 may be, for example, formed to a depth of 100 nm by selective epitaxial growth.

In other situations, it may be desirable to form a Schottky type source/drain formation for the FinFET. This can be accomplished using a damascene approach in which the nitride layer over the fin is used as an etch-stop. Referring to Fig. 9, polysilicon layer 901 may be used as an etch stop to etch a trench over nitride layer 930. After removing the silicon, a trench is left over the source/drain area. Metal can then be deposited and polished using nitride layer 930 as a stop layer. The metal forms Schottky contacts with the silicon channel.

CONCLUSION

A NOR gate is described above that can be implemented with two FinFET type transistors instead of the conventional four transistors. Thus, the NOR gate described herein uses half the conventional number of transistors, thereby providing significant improvements in gate density and in overall functionality of the integrated silicon device.

In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the specific details set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention.

The dielectric and conductive layers used in manufacturing a semiconductor device in accordance with the present invention can be deposited by conventional deposition techniques. For example, metallization techniques, such as various types of chemical vapor deposition (CVD) processes, including low pressure chemical vapor deposition (LPCVD) and enhanced chemical vapor deposition (ECVD) can be employed.

The present invention is applicable in the manufacturing of semiconductor devices and particularly in semiconductor devices with design features of 100nm and below, resulting in increased transistor and circuit

speeds and improved reliability. The present invention is applicable to the formation of any of various types of semiconductor devices, and hence, details have not been set forth in order to avoid obscuring the thrust of the present invention. In practicing the present invention, conventional photolithographic and etching techniques are employed and, hence, the details of such techniques have not been set forth herein in detail.

Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.

WHAT IS CLAIMED IS:

1. A NOR gate comprising:

a first FinFET (801) including first and second independently controllable gate regions (822, 823), a source region (821), and a drain region (820);

a second FinFET (802) including first and second independently controllable gate regions (832, 833), a source region (831), and a drain region (830);

a first input line of the NOR gate connected to the first gate region (822) of the first FinFET (801) and the first gate region (832)of the second FinFET (802);

a second input line of the NOR gate connected to the second gate region (823) of the first FinFET (801) and the second gate region (833) of the second FinFET (802); and

an output line of the NOR gate connected to the source (820) of the first FinFET (801) and the drain (830) of the second FinFET (802).

2. The NOR gate of claim 1, wherein the first gate regions of the first and second FinFETs are doped with n-type impurities.

3. The NOR gate of claim 2, wherein the second gate regions of the first and second FinFETs are doped with p-type impurities.

4. The NOR gate of claim 1, wherein the first and second FinFETs are the only transistors included in the NOR gate.

5. An integrated semiconductor device including a plurality of FinFETs (801, 802), the device characterized in that:

at least some of the plurality of FinFETs being arranged as pairs of FinFETs that define logic NOR gates.

6. The integrated semiconductor device of claim 5, wherein the pairs of FinFETs include:

a first FinFET (801) including first and second independently controllable gate regions (822, 823), a source region (821), and a drain region (820); and

a second FinFET (802) including first and second independently controllable gate regions (832, 833), a source region (831), and a drain region (830);

a first input line connected to the first gate region (822) of the first FinFET (801) and the first gate region (832) of the second FinFET (802);

a second input line connected to the second gate region (823) of the first FinFET (801) and the second gate region (833) of the second FinFET (802); and

an output line connected to the source (821) of the first FinFET (801) and the drain (830) of the second FinFET (802).

7. A logic NOR circuit comprising:

a first double-gate transistor (801); and

a second double-gate transistor (802),

wherein an output signal coupled to the first and second transistors reflects a logical NOR operation of two input signals applied to the first and second transistors.

8. The logic NOR circuit of claim 7, wherein the first and second double-gate transistors are FinFETs.

9. The logic NOR circuit of claim 7, wherein the first and second double-gate transistors each include:

a first gate region (822 or 832);

a second gate region (823 or 833) configured to be controllable independently of the first gate region;

a source region (821 or 831); and

a drain region (820 or 830).

10. The logic NOR circuit of claim 9, wherein the first gate region is doped with n-type impurities.

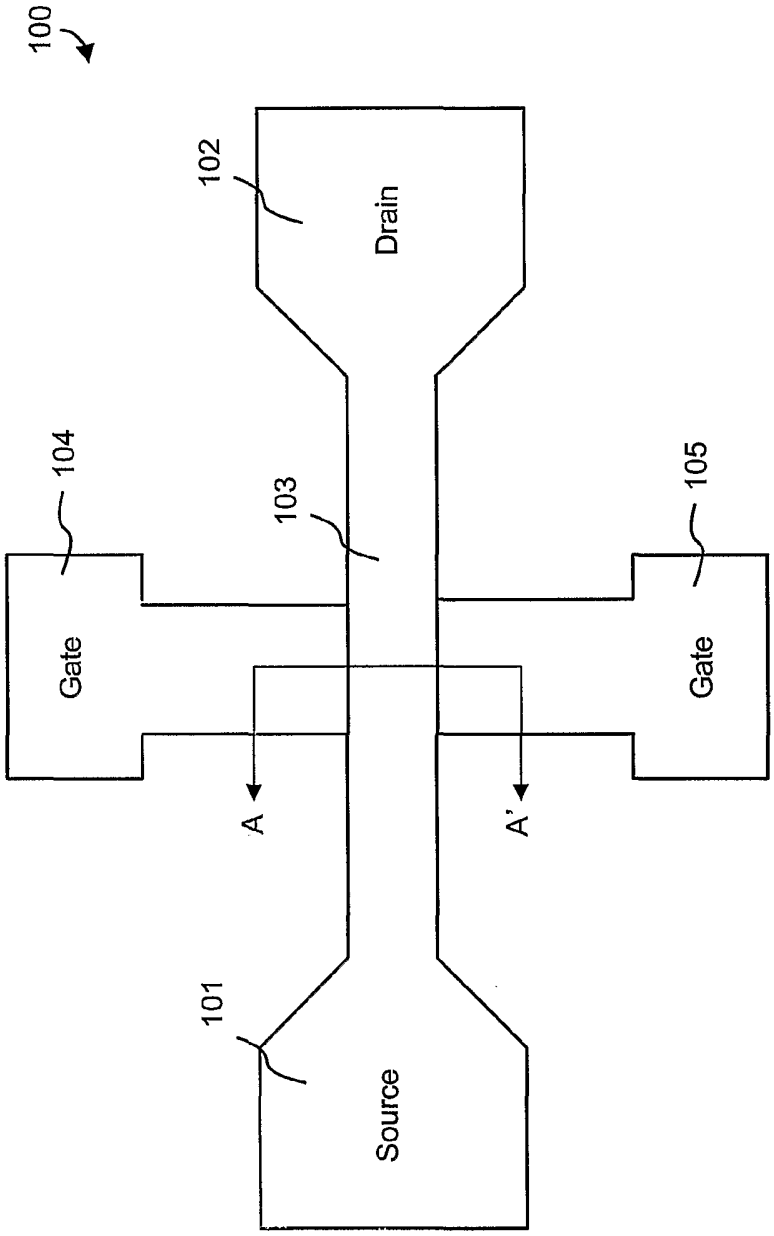


Fig. 1

Fig. 2

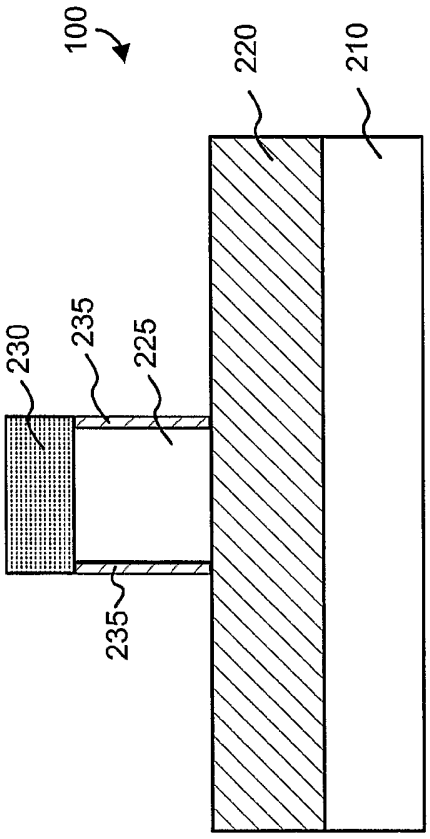


Fig. 3

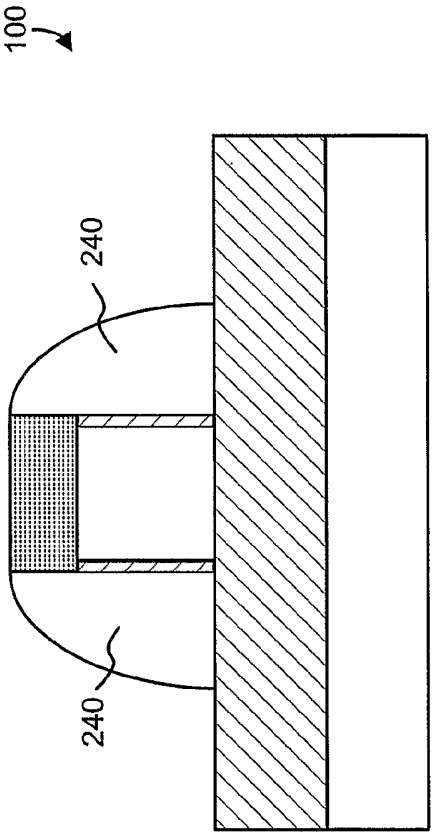


Fig. 4

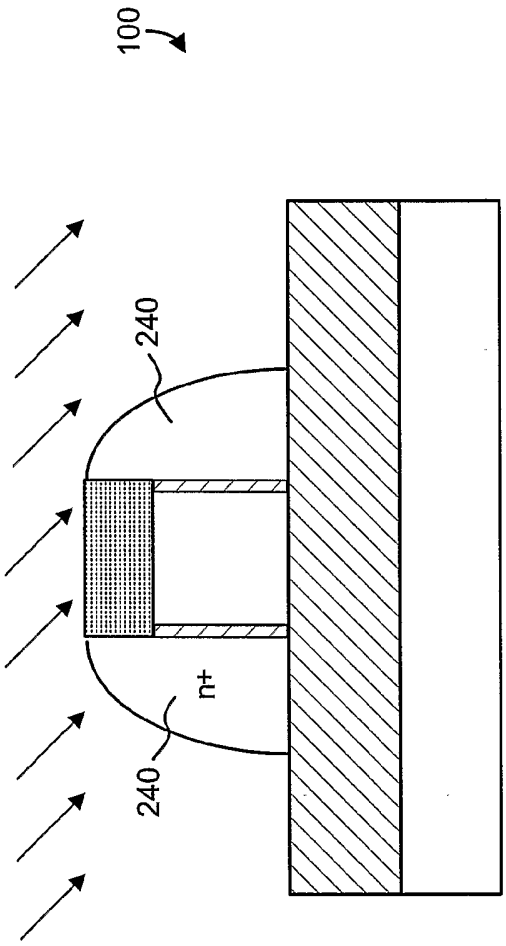


Fig. 5

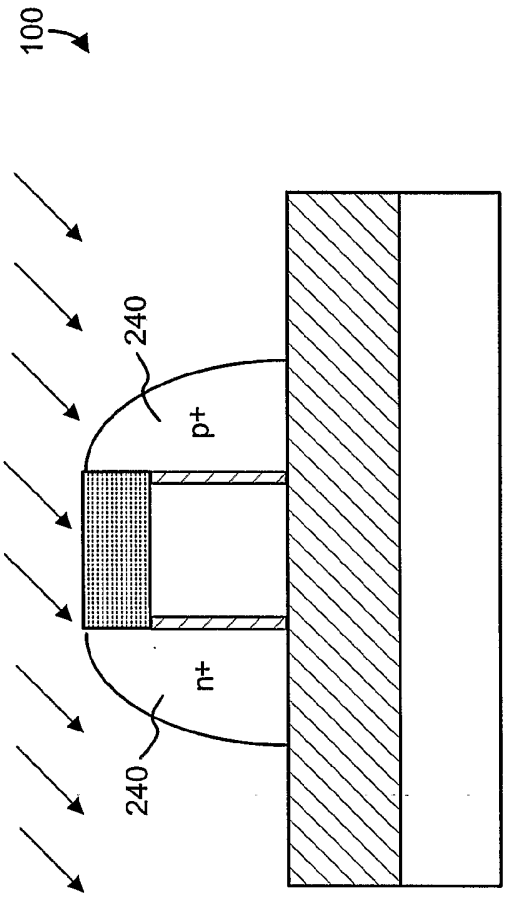


Fig. 6

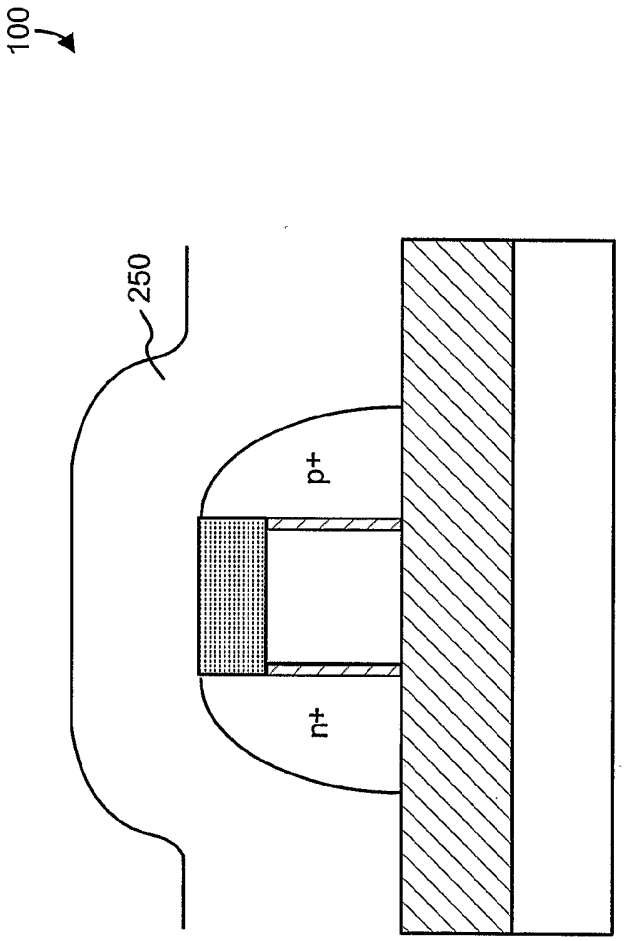


Fig. 7A

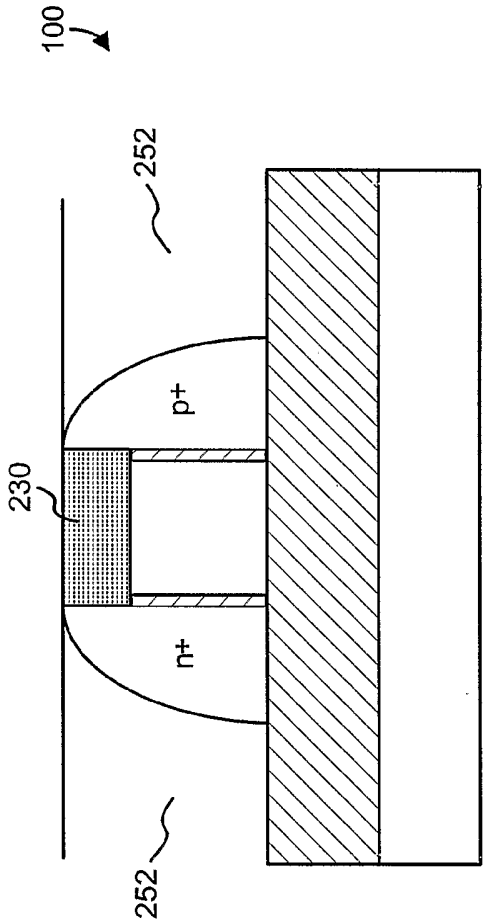
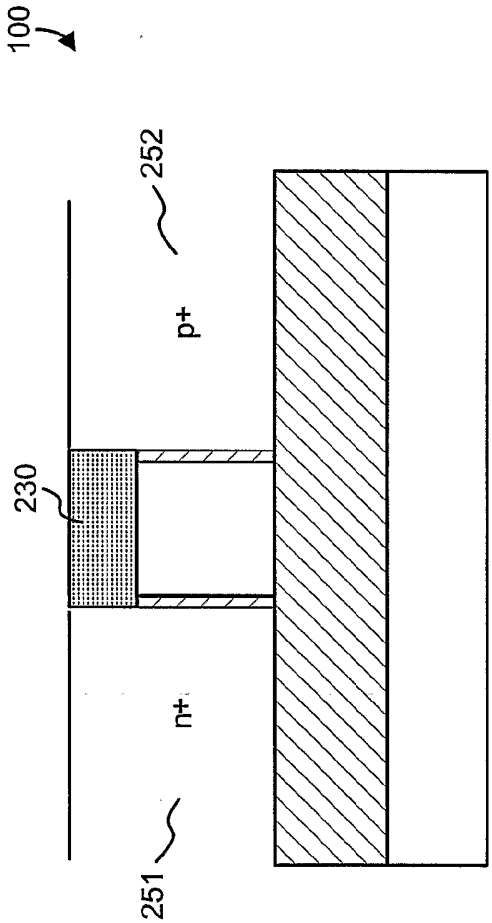


Fig. 7B



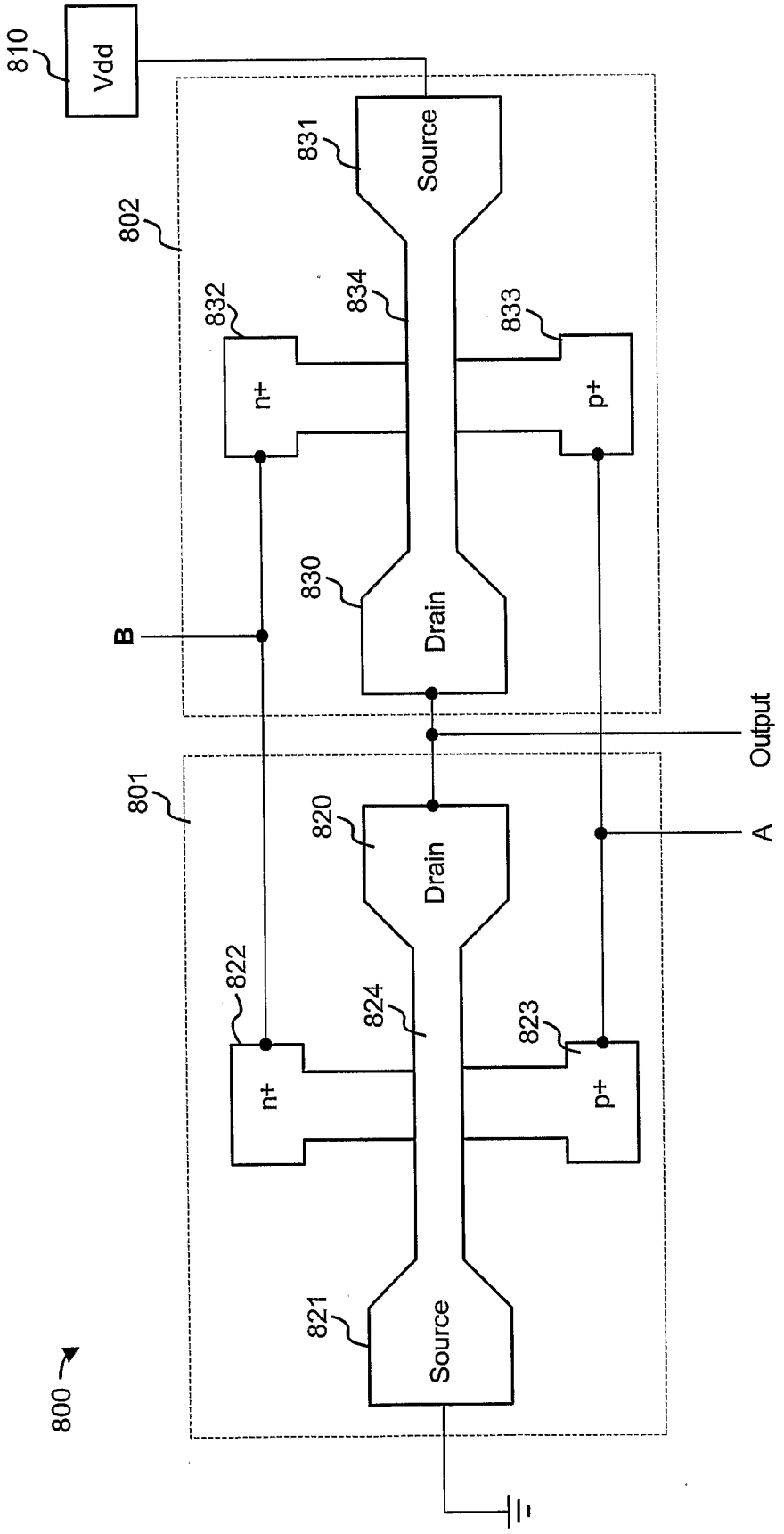
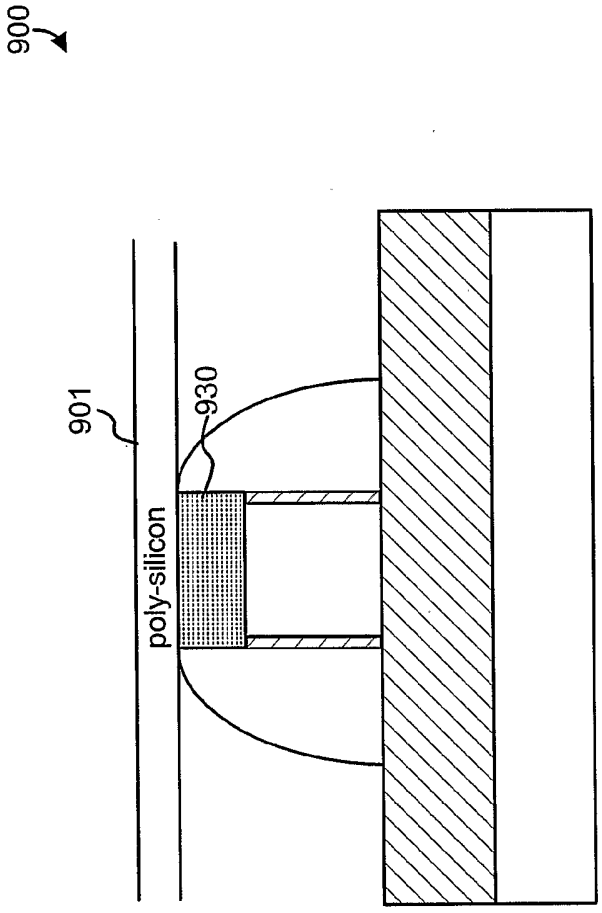

810
Vdd
831
Source
802
832
834
833
n+
p+
830
Drain
B
Output
801
820
Drain
A
822
824
823
n+
p+
821
Source
800

Fig. 8

Fig. 9



INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/32782

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/088 H01L27/092

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 684 (E-1650), 22 December 1994 (1994-12-22) -& JP 06 275826 A (FUJITSU LTD), 30 September 1994 (1994-09-30) abstract; figures 1,7 paragraphs '0007!,'0017!	1,4-9
Y		2,3,10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2004	05/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Wirner, C

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/32782

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	TETSU TANAKA ET AL: "ULTRAFAST OPERATION OF VTH-ADJUSTED P+-N+ DOUBLE-GATE SOI MOSFET'S" IEEE ELECTRON DEVICE LETTERS, IEEE INC. NEW YORK, US, vol. 15, no. 10, 1 October 1994 (1994-10-01), pages 386-388, XP000483212 ISSN: 0741-3106 abstract; figure 1 ---	2,3,10
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Information on patent family members

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