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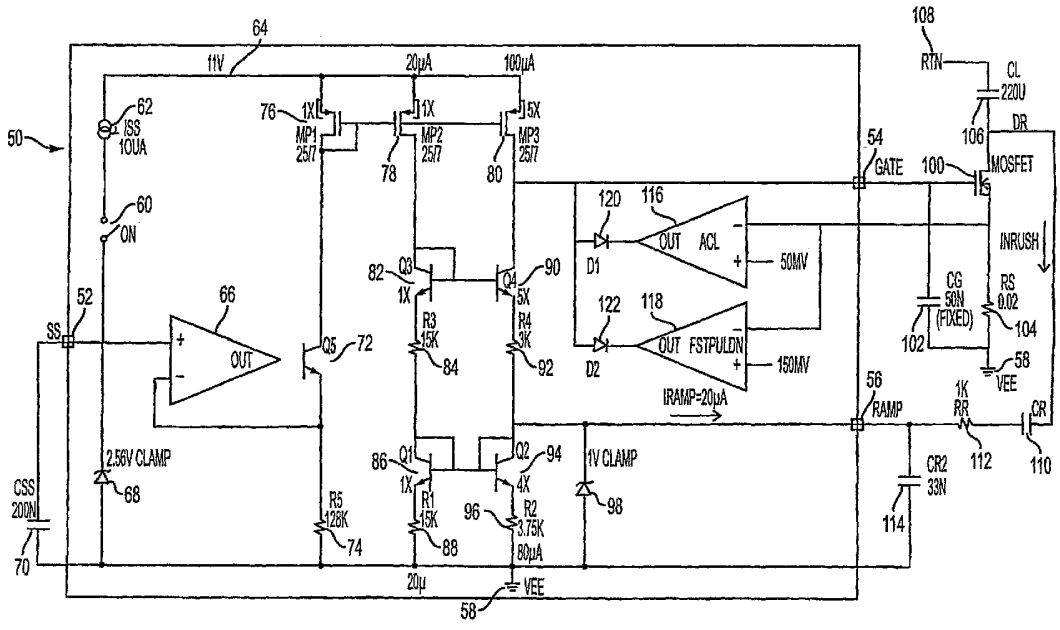
(54) **Title:** INRUSH CURRENT CONTROL SYSTEM WITH SOFT START CIRCUIT AND METHOD



(57) **Abstract:** A method of and system for controlling the inrush current generated in a MOSFET of an inrush current control system, wherein the MOSFET includes a source, gate and drain. The dV/dt at the drain of the MOSFET is controlled so as to set the inrush current level as a function of dV/dt, independent of current limit without requiring a separate capacitor connected between the gate and drain of the MOSFET so that the MOSFET can turn on and off more quickly.

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INRUSH CURRENT CONTROL SYSTEM WITH SOFT START CIRCUIT AND METHOD

Field of the Disclosure

[0002] The present disclosure generally relates to circuits for limiting inrush current, and more particularly to an inrush current control system with a soft start circuit, and methods of controlling the inrush current of a control system as a function of the ramp rate of a soft start voltage.

Background of the Disclosure

[0003] When circuit boards are inserted into live backplanes (typically at –48V), the input of a board's power module or switching power supply (or bypass capacitors if provided) can draw huge transient currents as they charge up. The transient currents can cause permanent damage to the board's components and glitches on the system power supply. By limiting inrush current caused by transient effects one protects the board from excessive current spikes. Three commercially available circuits for limiting inrush current are shown in Figs. 1-3.

[0004] In Fig. 1, the circuit shown is commercially available from the current assignee as the Hot Swap Controller LT4250, Hot Swap being a trademark of the present assignee. The controller includes an active current limit inverting amplifier ACL that is connected to external circuitry so as to limit the inrush currents to an adjustable value by controlling the gate voltage of an external N-channel pass transistor FET. The pass transistor FET is turned off if the input voltage is less than a programmable under voltage threshold or greater than an over voltage threshold. An adjustable current limit also protects the system against shorts. After a 500

microsecond timeout the current limit circuit activates an electronic circuit breaker. By placing an external capacitor C_R between the drain and the gate of the FET and using a current limited pull up in the ACL amplifier (represented by the I_{GATE} current source), the inrush current can be set by the ratio between the load capacitance C_L and C_R, which is independent of the circuit breaker threshold. By setting the inrush current well below the current limit of the circuit breaker threshold, the circuit breaker can be optimized to protect the FET. A small circuit breaker time t_{CB} reduces the power consumed by the FET upon a short-circuit event keeping it within its safe operating area. However, this technique typically requires a capacitor C_G between the gate and source of the FET that is much larger than C_R to avoid turning on the FET at insertion of a board equipped with the controller into a live backplane. Specifically, the capacitor C_G prevents the FET from momentarily turning on when the power pins first make contact with the live backplane. Without the capacitor C_G, capacitor C_R would pull the gate of the FET up to a voltage roughly equal to V_{EE} times C_R/C_{GS}(the gate-source capacitance of the FET) before the circuit can power up and actively pull the gate of the FET low. By placing the capacitor C_G in parallel with the gate capacitance of FET, the problem is solved. This large C_G makes the turn-off of the FET difficult in a hard short event and increases the SOA requirement. The approach also complicates the selection of the compensation network used to stabilize the active current limit.

[0005] In a second controller shown in Fig. 2, commercially available from the present assignee as the LTC4252, output current is controlled by three stages of current limiting: a timed circuit breaker, active current limiting and a fast feed forward path that limits peak current under worst-case catastrophic fault conditions. Active current limit is used during the generation of inrush current in order to eliminate C_R and reduce the value of C_G (components used in the Fig. 1 controller). One drawback of this approach is the long circuit-breaker time t_{CB} required to accommodate the current limit servo time to avoid timeout during startup and input step. When a short occurs, the FET experiences the full current limit through the long t_{CB}, which results in a large SOA requirement and makes the selection of the FET difficult in a high power application. Reducing the current limit as a function of V_{OUT} (cuurent limit foldback) reduces the SOA requirement during startup and the input step. It also performs satisfactorily during a hard short.

However, in a soft short event, the FET may still experience the full scale current limit for t_{CB}, which in turn can result in a large stress on the FET.

[0006] A third circuit shown in Fig. 3, commercially available from Supertex of Sunnyvale California as the HV301/311, also controls the output current with an active current limiting circuit. During the initial power application, the gate of the external pass device (NMOSFET) is clamped low to suppress contact bounce. Thereafter, under voltage/over voltage (UV/OV) supervisors and power-on-reset work together to suppress gate turn-on of the NMOSFET until mechanical bounce has ended. An active current limit control circuit is then activated during power-up to limit the inrush current. The capacitor C_2, connected between the RAMP pin and the drain of the NMOSFET, allows the inrush current to be lower than the current limit. However, the current limit circuit is still active and there is no way to distinguish between normal inrush current and a current overload. Similar to the LTC4252, a long circuit-breaker time t_{CB} (100ms typical) is required to avoid circuit-breaker timeout during startup. Thus, when an output short occurs, the NMOSFET will conduct at the current limit level for the whole t_{CB}, severely stressing the NMOSFET.

[0007] Fig. 4 illustrates a circuit, which is described in greater detail in U.S. Patent No. 5952817, assigned to the present assignee. This circuit is a switching regulator that slows down both the voltage and current slew rates. However, the purpose of slowing down both the voltage and current slew rates is to reduce the high frequency noise introduced to the power supply and ground. A Miller capacitor C_V, 20, and the adjustable current I_{VSLEW} set the voltage slew rate, dV/dt, at node 22. Amplifiers 24, 26 and 28 act to control the slew rate of the transistor Q1 current.

Summary of the Disclosure

[0008] In accordance with one aspect of the current disclosure, the method of a system for and method of controlling the inrush current generated in a MOSFET of an inrush current control is disclosed. The method and system control the dV/dt at the drain of the MOSFET so as to set the inrush current level as a function of dV/dt, independent of current limit without requiring a separate capacitor connected between the gate and drain of the MOSFET.

[0009] In accordance with another aspect of the present disclosure a system for and method of controlling the turn on output current of an inrush current control system is disclosed. The system and method are designed to control the dV/dt at the drain of a FET so as to set the inrush current through the FET as a function of dV/dt ; and control the dI/dt of the turn on output current as a function of the ramp rate of a soft start voltage produced at an input of the control system when the control system is turned on.

[00010] In accordance with one disclosed embodiment a ramp voltage is generated at the drain of the MOSFET when the voltage on the gate of the MOSFET is sufficient for the MOSFET to turn on.

[00011] In accordance with one disclosed embodiment the inrush current control system includes a component coupled to the drain of the MOSFET, such that a ramp voltage is generated at the drain of the MOSFET and the inrush current is limited. The component can include a capacitive or/and a resistive element coupled to the drain of the MOSFET.

[00012] In accordance with one disclosed embodiment wherein the current is limited through the MOSFET during an over current condition, and/or during an output short event.

[00013] In accordance with one disclosed embodiment the rate of rise of the inrush current, dI/dt is also controlled.

[00014] In accordance with one disclosed embodiment over current protection is provided without affecting the inrush current.

[00015] In accordance with one disclosed embodiment the inrush current control system includes a current input, and a ramp pin output, the ramp pin output being coupled to the drain of the MOSFET, and the voltage at the ramp pin is held during power up or power step conditions.

[00016] In accordance with another aspect of the present disclosure a system for and method of controlling the turn on output current of an inrush current control system is disclosed. The system and method are designed to control the dV/dt at the drain of a FET so as to set the inrush current level through the FET as a function of dV/dt ; and control the dI/dt of the inrush current as a function of the ramp rate of a soft start voltage produced at an input of the control system when the control system is turned on.

[00017] In accordance with one disclosed embodiment the soft start voltage is clamped to a predetermined value.

[00018] In accordance with one disclosed embodiment the soft start voltage limit is established by a clamping circuit.

[00019] In accordance with one disclosed embodiment the inrush current control system includes a capacitor coupled to the drain, and a ramp current is generated through the capacitor to the drain of the FET as a function of the soft start voltage. In accordance with one disclosed embodiment, the capacitor is configured so that the FET can turn off independently of the value of the capacitor.

Brief Description of the Drawings

[00020] Reference is made to the attached drawings, wherein elements having the same reference character designations represent like elements throughout, and wherein:

[00021] Fig. 1 is a partial schematic and partial block diagram of a first prior art inrush current control system;

[00022] Fig. 2 is a partial schematic and partial block diagram of a second prior art inrush current control system;

[00023] Fig. 3 is a partial schematic and partial block diagram of a third prior art inrush current control system;

[00024] Fig. 4 is a partial schematic and partial block diagram of a switching regulator that slows down both the voltage and current slew rates to avoid excessive current overloads;

[00025] Fig. 5 is a partial schematic and partial block diagram of an embodiment of a inrush current control system designed in accordance with at least one aspect of the invention;

[00026] Fig. 6 is a timing diagram illustrating the inrush control behavior of the control system shown in Fig. 5.

Detailed Description of the Drawings

[00027] A preferred embodiment of the inrush current control system is shown in Fig. 5. The system preferably is in the form of an integrated circuit 50 having a soft start terminal pin (SS) 52 an output terminal pin (GATE) 54, an output terminal pin (RAMP) 56, and a system ground terminal (V_{EE}) 58. The system includes a switch 60, which closes when the device is connected to a power supply (not shown). One contact of the switch is connected to a current source I_{SS} 62, which in turn is connected to a positive voltage rail 64. The other contact of the switch 60 is connected to the non-inverting input of an amplifier 66. The non-inverting input of the amplifier 66 is also connected to the cathode of the clamping circuit 68, illustrated as a Zener diode, and the soft start junction (SS) 52. The anode of diode 68 is connected to system ground (V_{EE}) 58. Junction (SS) 52 is also connected to one plate of the external soft start capacitor (C_{SS}) 70. The other plate of the capacitor (C_{SS}) 70 is also connected to system ground (V_{EE}) 58.

[00028] The output of the amplifier 66 is connected to the base of the bipolar transistor (Q_5) 72. The emitter of transistor (Q_5) 72 is connected to the inverting input of the amplifier 66, and to the resistor (R_5) 74. The latter in turn is connected to system ground (V_{EE}) 58. The collector of the transistor (Q_5) 72 is connected to the drain of MOSFET (MP_1) 76, which forms a part of a current mirror, the latter preferably including MOSFETs (MP_1) 76, (MP_2) 78 and (MP_3) 80. Each of the MOSFETs (MP_1) 76, (MP_2) 78 and (MP_3) 80 has its source connected to the voltage rail 64, and its gates connected together. The gate of the MOSFET (MP_1) 76 is connected to its drain and the collector of the transistor (Q_5) 72. The MOSFET (MP_2) 76 has its drain connected to the collector and base of the bipolar transistor (Q_3) 82, which in turn has its emitter connected

through the resistor (R_3) 84 to the collector and base of the bipolar transistor (Q_1) 86. The emitter of transistor (Q_1) 86 is connected through resistor (R_1) 88 to system ground (V_{EE}) 58.

[00029] The drain of the MOSFET (MP_3) 80 is connected to the (GATE) terminal 54 and to the collector of bipolar transistor (Q_4) 90. The latter has its collector tied to the base and collector of the transistor (Q_3) 82. The emitter of transistor (Q_4) 90 is connected through resistor (R_4) 92 to the (RAMP) terminal 56, and to the collector and base of the bipolar transistor (Q_2) 94. The emitter of transistor (Q_2) is connected to through the resistor (R_2) 96 to system ground (V_{EE}) 58. The (RAMP) terminal 56 is also connected to the cathode of the clamping circuit 98, which is illustrated as a Zener diode having its anode connected to system ground (V_{EE}) 58. The clamping circuit 98 holds the (RAMP) terminal close to the regulated 1V level during input voltage step.

[00030] The (GATE) terminal 54 is connected to the gate of the MOSFET 100 of an external circuit (external to the integrated circuit) and through capacitor (C_G) 102 to system ground (V_{EE}) 58 . The source of MOSFET 100 is connected through resistor (R_S) 104 to system ground (V_{EE}) 58. The drain of the MOSFET 100 is connected through capacitor (C_L) 106 to a voltage source (RTN) 108, and to one plate of capacitor (C_R) 110. The other plate of the capacitor (C_R) 110 is connected through resistor (RR) 112 to the (RAMP) terminal 56. The (RAMP) terminal 56 is also connected through capacitor (CR_2) 114 to system ground (V_{EE}) 58.

[00031] In addition to the foregoing the preferred inrush current control system includes two over-current protection components besides the inrush control circuits, both preferably provided as a part of the integrated circuit 50. The two over-current protection components preferably includes an active current limit (ACL) amplifier 116 having its inverting input connected to sense voltage from the source of the MOSFET 100, its output connected to the cathode of diode 120 (which in turn has its anode connected to the gate terminal 54) and its non-inverting input connected to a 50mV source so that the amplifier serves as a circuit breaker comparator with an input threshold of 50mV. The other over-current protection component preferably includes a fast pull down (FSTPULDN) comparator 118 having its inverting input also connected to receive the sensed voltage from the source of the MOSFET 100, its output connected to the cathode of

diode 122 (which in turn has its anode connected to the gate terminal 54) and its non-inverting input connected to an input threshold of 150mV.

[00032] In operation, FET 100 turn-on starts when the system is connected to a power supply and the switch (S) 62 is closed (at time t_0 as shown in Fig. 6). As the I_{SS} current flows though the switch 62, it will start charging external soft-start capacitor C_{SS} with a pull-up current from the I_{SS} source. Current flow to the capacitor C_{SS} will create a voltage drop across C_{SS}. This will also produce an output signal of the amplifier 66 at the emitter of transistor (Q_5) 72. This will result in pull-up current flowing through the transistor (Q_5) 72 and the resistor (R_5) 74. The voltage thereby generated across the resistor (R_5) 74 is the same voltage appearing across the capacitor (C_{SS}) 70. The current flowing from MOSFET (MP_1) 76 is mirrored so as that a current flows from the MOSFETs (MP_2) 78 and (MP_3) 80. The current flowing the resistors (R_1) – (R_4) 82, 86, 90 and 96, generate 300mV of emitter degeneration through transistors (Q_1)-(Q_4) 82, 86, 90 and 94 so as to help the circuit withstand residual noise at the (RAMP) terminal 54.

[00033] The voltage applied across the capacitor (C_{SS}) 70 will thus generate a GATE current (I_{GATE}) at the terminal 54 for GATE pull-up. When the GATE voltage at (GATE) terminal 54 reaches the threshold voltage of the MOSFET 100 (at t_1 in Fig 6), the I_{INRUSH} current will start flowing through the MOSFET 100, which is set by a RAMP current (I_{RAMP}) that starts to flow through C_R. The RAMP current rises until it reaches a constant when the voltage across capacitor (C_{SS}) 70 reaches its clamped value (at t_2 in Fig 6). In one example the component values are set so that the V_{SS} across capacitor C_{SS} is clamped to 2.56V (the bias voltage of the clamping circuit), corresponding to a constant I_{GATE} of 11μA and a constant I_{RAMP} of 20 μA as illustrated in Fig. 6. The RAMP pin voltage at the RAMP terminal 56 is regulated at 1V, and the ramp rate at the DRAIN terminal 54 sets the current I_{INRUSH} of the FET 100 through the resistor 104 as follows:

(1) $$I_{INRUSH} = I_{RAMP} \cdot C_L/C_R$$

[00034] The capacitor CR_2 and the resistor RR are used to filter the noise at the RAMP terminal 56 and each are optional.

[00035] When the DRAIN is ramped down to V_{EE}, I_{RAMP} drops to 0 (at t_3 in Fig 6) and I_{GATE} pulls the GATE up to the supply of the ramp control circuit (at t_4 in Fig 6).

[00036] Fig. 6 illustrates the operation of the system and shows that the ramp rate of the voltage across capacitor C_{SS} 70 determines the dI/dt of I_{INRUSH}. Specifically,

(2) $dV_{SS}/dt = I_{SS}/C_{SS}$;

(3) $dV_{SS}/dt \cdot 1/R_5 = dI_{RAMP}/dt = I_{SS}/(C_{SS} \cdot R_5)$;

and

(4) $dI_{INRUSH}/dt = (dI_{RAMP}/dt) \cdot (C_L/C_R) = (I_{SS} \cdot C_L)/(C_{SS} \cdot R_5 \cdot C_R)$

[00037] The exemplary embodiment thus sets the I_{INRUSH} current by a capacitor C_R between the DRAIN and a dedicated RAMP terminal that is regulated separately from the GATE of the FET 100. The advantages of this approach include (1) it does not require a large C_G that relates to C_R so the turn-off of the FET 100 can be fast even for large load applications; and (2) it incorporates a soft start technique that controls the dI/dt of the I_{INRUSH} current. Other advantages will be will be evident to those skilled in the art.

[00038] Used in conjunction with the over-current protection components (ACL amplifier 116 and FSTPULDN comparator 118) as shown in Fig. 5, the inrush current control technique presented in this disclosure provides a general method that reduces the SOA requirement of the MOSFET. In an over-current condition, when the voltage drop across R_S 104 exceeds 50mV, the ACL amplifier 116 is activated and a short circuit breaker timer (520μs typical) is started. The ACL amplifier 116 servos the GATE of the MOSFET 100 to maintain a constant output current of $50mV/R_S$. When the circuit breaker timer expires, the MOSFET 100 is turned off. In a low-impedance output short event, when the voltage drop across R_S exceeds 150mV, the FSTPULDN comparator 118 immediately pulls down the gate of MOSFET 100. Once the voltage drop across R_S 104 falls below 150mV, but is still above 50mV, the ACL amplifier 116 servos the GATE of MOSFET 100 until the circuit breaker timer expires. Because the inrush control is independent of the current limit or circuit breaker functions, the circuit breaker timer

can be very short so as to substantially reduce the stress on the FET 100 in an over-current condition such as an output short.

[00039] It should be noted that the capacitor (C_R) of the Fig. 1 embodiment of the prior art has been moved in the embodiment shown in Fig. 5 so as to be connected between the drain of the FET (capacitor 110 (C_R)) and the (RAMP) terminal 56. This reduces and may eliminate the need for a discrete component in the form of a capacitor between the gate of the MOSFET 100 and V_{EE} (it should be noted that some parasitic capacitance will still be present at the gate, but elimination of the discrete component greatly improves the performance of the circuit). For example, a typical capacitance value of the capacitor C_G for the Fig. 1 controller is 470 nanofarads. Where a capacitor C_G is used in the Fig. 5 embodiment, it can have a typical value of 50 nanofarads, thus allowing for a significant reduction in capacitance value of almost 10:1. The capacitance 102 (C_G) is vital to the Fig. 1 controller during live insertion for all of the FETs. However, by moving the capacitor C_R, the value of capacitor 102 (C_G) can be greatly reduced, and in some cases, depending on the threshold level of the MOSFET used, can even be eliminated. The resistor 112 is optional depending upon system requirements. The result is that the MOSFET 100 can turn on and off much faster. In addition, the large value of C_G in the Fig. 1 controller complicates loop compensation. However, with the arrangement described in connection with Fig. 5, the capacitor 110 (C_R)can be replaced by a resistive element. Thus, benefits of the Fig. 5 embodiment include (a) significantly reducing the value of or eliminating the need for capacitor C_G by rerouting capacitor C_R so that it is connected between the RAMP terminal and the DRAIN of the FET 100, (b) allowing the MOSFET 100 to respond much faster since the ACL 66 does not need to drive a large capacitor C_G, and (c) simplifying and making more stable the compensation loop of the circuit.

[00040] Further, the component(s) connected between the RAMP terminal 56 and the DRAIN of the MOSFET 100 (shown as a capacitor C_R 110 and resistor 112, although in some instances only one of those components are necessary) are used to generate a ramp signal (current) from the DRAIN of the MOSFET 100 (or output voltage) so as to limit the inrush current flowing through the MOSFET 100.

[00041] Thus, the method of and system for controlling the dI/dt of an inrush output current of a inrush current control system provided in accordance with the present disclosure have been described. The exemplary embodiment described in this specification have been presented by way of illustration rather than limitation, and various modifications, combinations and substitutions may be effected by those skilled in the art without departure either in spirit or scope from this disclosure in its broader aspects and as set forth in the appended claims.

[00042] The system and method of the present disclosure as disclosed herein, and all elements thereof, are contained within the scope of at least one of the following claims. No elements of the presently disclosed system and method are meant to be disclaimed, nor are they intended to necessarily restrict the interpretation of the claims.

What is claimed is:

1. A method of controlling the inrush current generated in a MOSFET of an inrush current control system, wherein the MOSFET includes a source, gate and drain, the method comprising:

controlling the dV/dt at the drain of the MOSFET so as to set the inrush current level as a function of dV/dt, independent of current limit without requiring a separate capacitor connected between the gate and drain of the MOSFET.

2. A method according to claim 1, wherein the inrush current control system includes a current input, a gate pin output and a ramp pin output, the ramp pin output being coupled to the drain of the MOSFET, and the gate pin output being coupled to the gate of the MOSFET,

wherein the method further comprises:

forcing current out of the ramp pin when the MOSFET is turned on.

3. A method according to claim 1, wherein the inrush current control system includes a component coupled to the drain of the MOSFET, and

the step of controlling the dV/dt at the drain of the MOSFET includes:

generating a ramp current through the component so as to generate a ramp voltage at the drain of the MOSFET and limit the inrush current.

4. A method according to claim 3, wherein the step of generating a ramp current includes generating a ramp current through a capacitive element coupled to the drain of the MOSFET.

5. A method according to claim 3, wherein the step of generating a ramp current includes generating a ramp current through a resistive element coupled to the drain of the MOSFET.

6. A method according to claim 1, the method further comprising:
limiting the current through the MOSFET during an over current condition.

7. A method according to claim 1, the method further comprising:
limiting the current through the MOSFET during an output short event.

8. A method according to claim 1, wherein the step of controlling the dV/dt at the drain, also includes controlling the rate of rise of the inrush current, dI/dt.

9. A method according to claim 1, wherein the inrush current control system includes a current input, and a ramp pin output, the ramp pin output being coupled to the drain of the MOSFET,
the method further comprising:
holding the voltage at the ramp pin during power up or power step conditions.

10. A method of controlling the turn on output current of an inrush current control system, comprising:

controlling the dV/dt at the drain of a FET so as to set the inrush current level of the FET as a function of dV/dt ; and controlling the dI/dt of the turn on output current as a function of the ramp rate of a soft start voltage produced at an input of the control system when the control system is turned on.

11. A method according to claim 10, further including

clamping the soft start voltage to a predetermined value.

12. A method according to claim 11, wherein

clamping the soft start voltage to a limit includes establishing the limit by a clamping circuit.

13. A method according to claim 10, wherein the inrush current control system includes a capacitor connected in between a soft short input pin and a voltage level source V_{EE},

wherein the method further includes

generating a ramping current to turn on the FET as a function of the voltage at the soft short input pin.

14. A method according to claim 10, wherein the inrush current control system includes a capacitor coupled to the drain,

wherein the method further includes

generating the inrush output current through the FET,

wherein the capacitor is configured so that the FET can turn off independently of the value of the capacitor.

15. A circuit configuration for controlling the inrush current generated in a MOSFET of an inrush current control system, wherein the MOSFET includes a source, gate and drain, the circuit configuration comprising:

a control circuit configured and arranged so that the dV/dt at the drain of the MOSFET sets the inrush current level as a function of dV/dt, independent of current limit without requiring a separate capacitor connected between the gate and drain of the MOSFET.

16. A circuit configuration according to claim 15, wherein the control circuit includes a current input, a gate pin and a ramp pin output, wherein the ramp pin is coupled to the drain of the MOSFET, and wherein a ramp voltage is generated at the drain of the MOSFET when the voltage on the gate of the MOSFET is sufficient for the MOSFET to turn on..

17. A circuit configuration according to claim 15, wherein the inrush current control system includes a component coupled between the ramp pin and the drain of the MOSFET, and

the control circuit generates a ramp current through the component so as to generate a ramp voltage at the drain of the MOSFET and limit the inrush current.

18. A circuit configuration according to claim 17, wherein the component is a capacitive element coupled to the drain of the MOSFET.

19. A circuit configuration according to claim 17, wherein the component is a resistive element coupled to the drain of the MOSFET.

20. A circuit configuration according to claim 15, further comprising:

a current limiter coupled to the MOSFET and configured so as to limit the current through the MOSFET during an over current condition.

21. A circuit configuration according to claim 15, further comprising:

a current limiter coupled to the MOSFET and configured so as to limit the current through the MOSFET during an output short event.

22. A circuit configuration according to claim 15, wherein the control circuit configured and arranged so that the dV/dt at the drain of the MOSFET sets the inrush current level as a function of dV/dt is further configured and arranged so as to control the rate of rise of the inrush current, dI/dt.

23. A circuit configuration according to claim 22, further including an over current protection subcomponent configured and arranged so as to provide over current protection with respect to the inrush current.

24. A circuit configuration according to claim 15, further including a current input, and a ramp pin output, the ramp pin output being coupled to the drain of the MOSFET such that the voltage at the ramp pin is held at a relatively constant value during power up or power step conditions.

25. A circuit configured and arranged so as to control the turn on output current of an inrush current control system, comprising:

a control circuit configured and arranged so as to control the dV/dt at the drain of a FET so as to set the inrush current level through the FET as a function of dV/dt ; and control the dI/dt of the turn on output current as a function of the ramp rate of a soft start voltage produced at an input of the control circuit when the control system is turned on.

26. A circuit according to claim 25, further including

a voltage clamp configured and arranged so as to clamp the soft start voltage to a predetermined value.

27. A circuit according to claim 25, further including a soft start pin and a capacitor coupled between the soft start pin and a voltage source V_{EE}, the circuit being configured and arranged so that a ramp current is generated through the capacitor as a function of the voltage at the soft start pin.

28. A method according to claim 25, wherein the inrush current control system includes a capacitor coupled to the drain, and the inrush control system is configured and arranged so that the FET can turn off independently of the value of the capacitor.

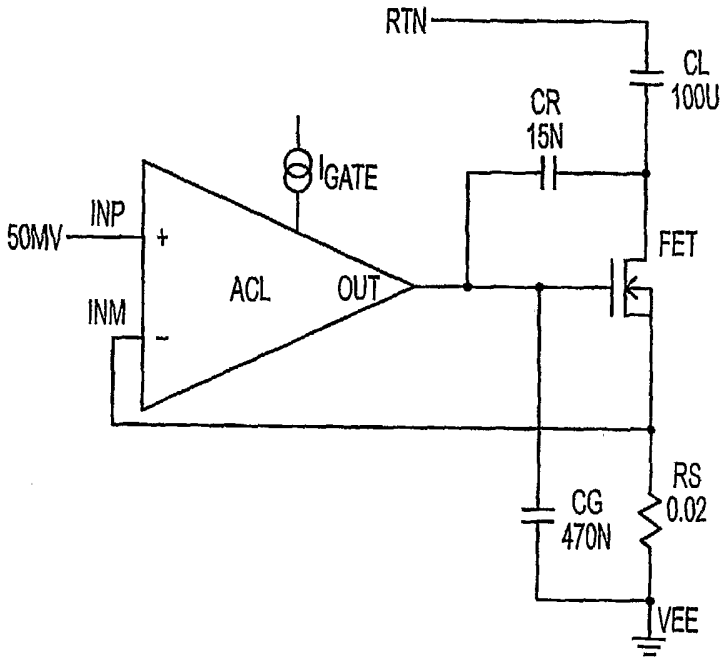


FIG. 1
PRIOR ART

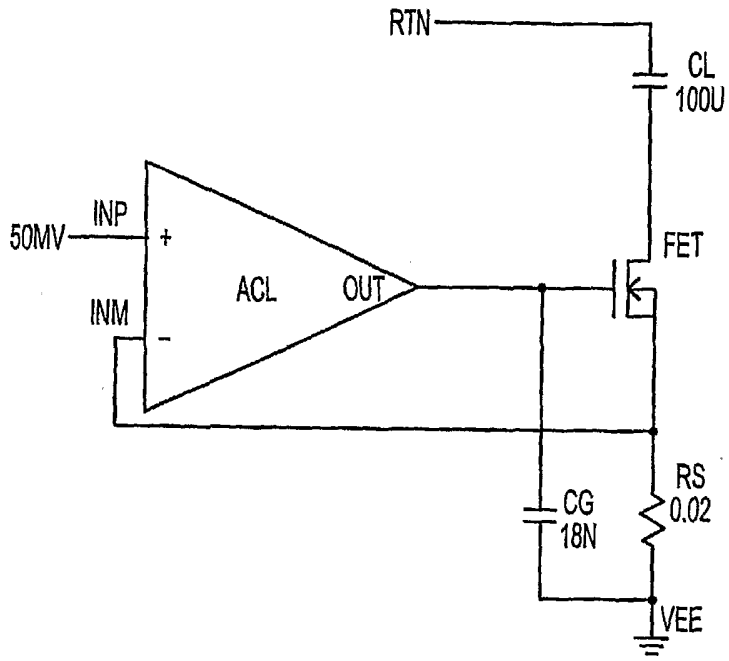


FIG. 2
PRIOR ART

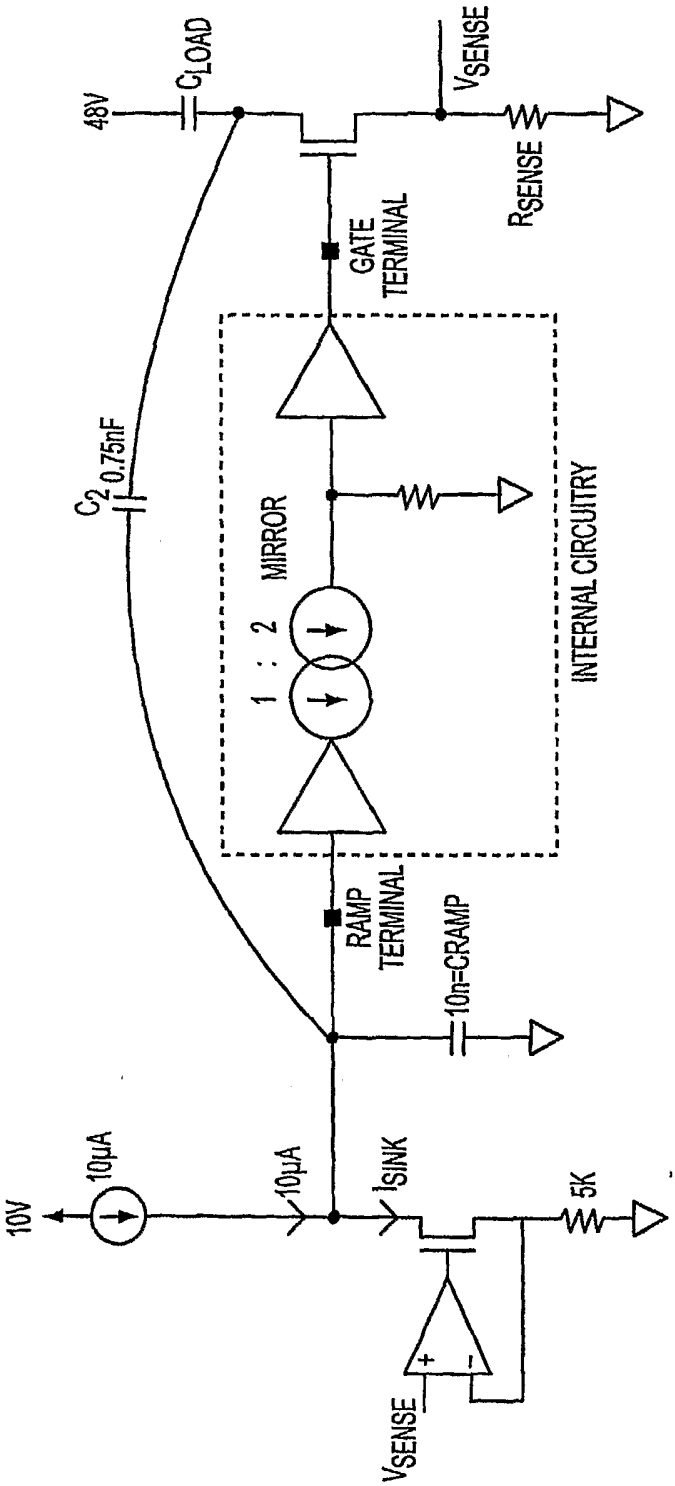


FIG. 3
PRIOR ART

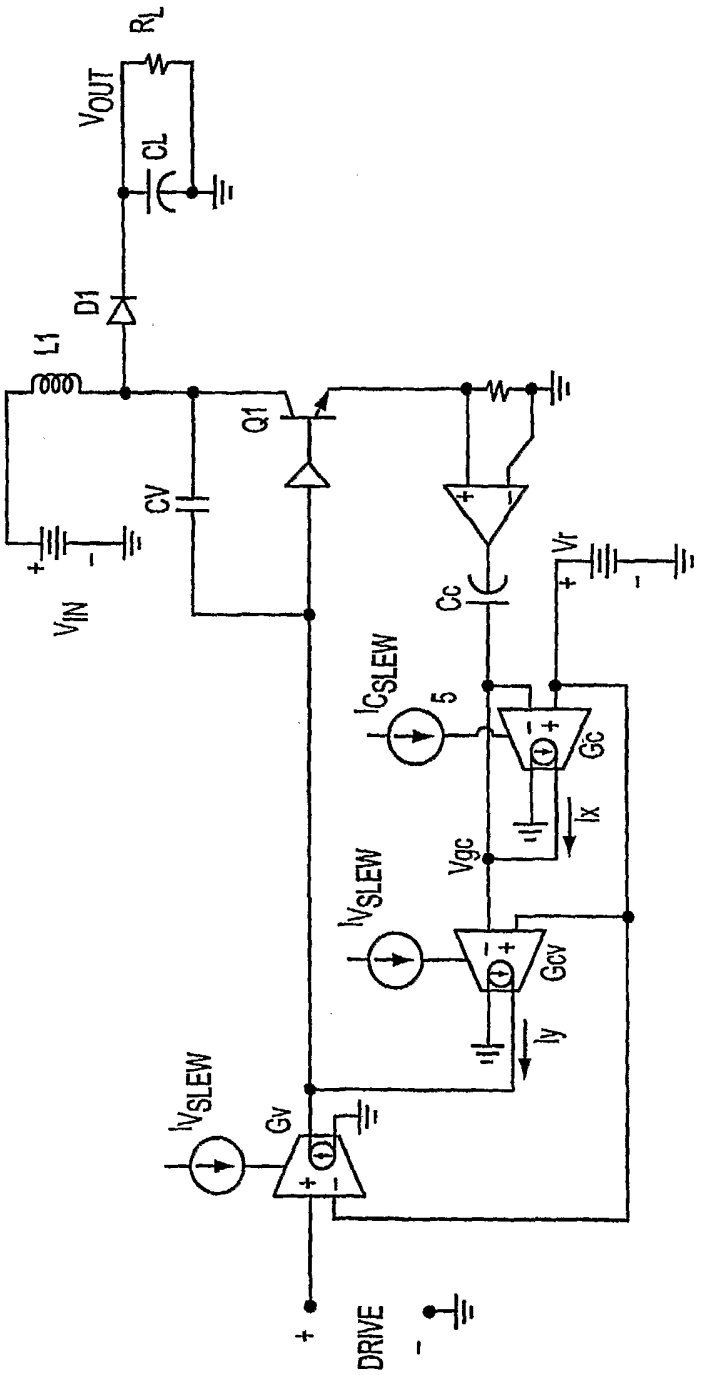
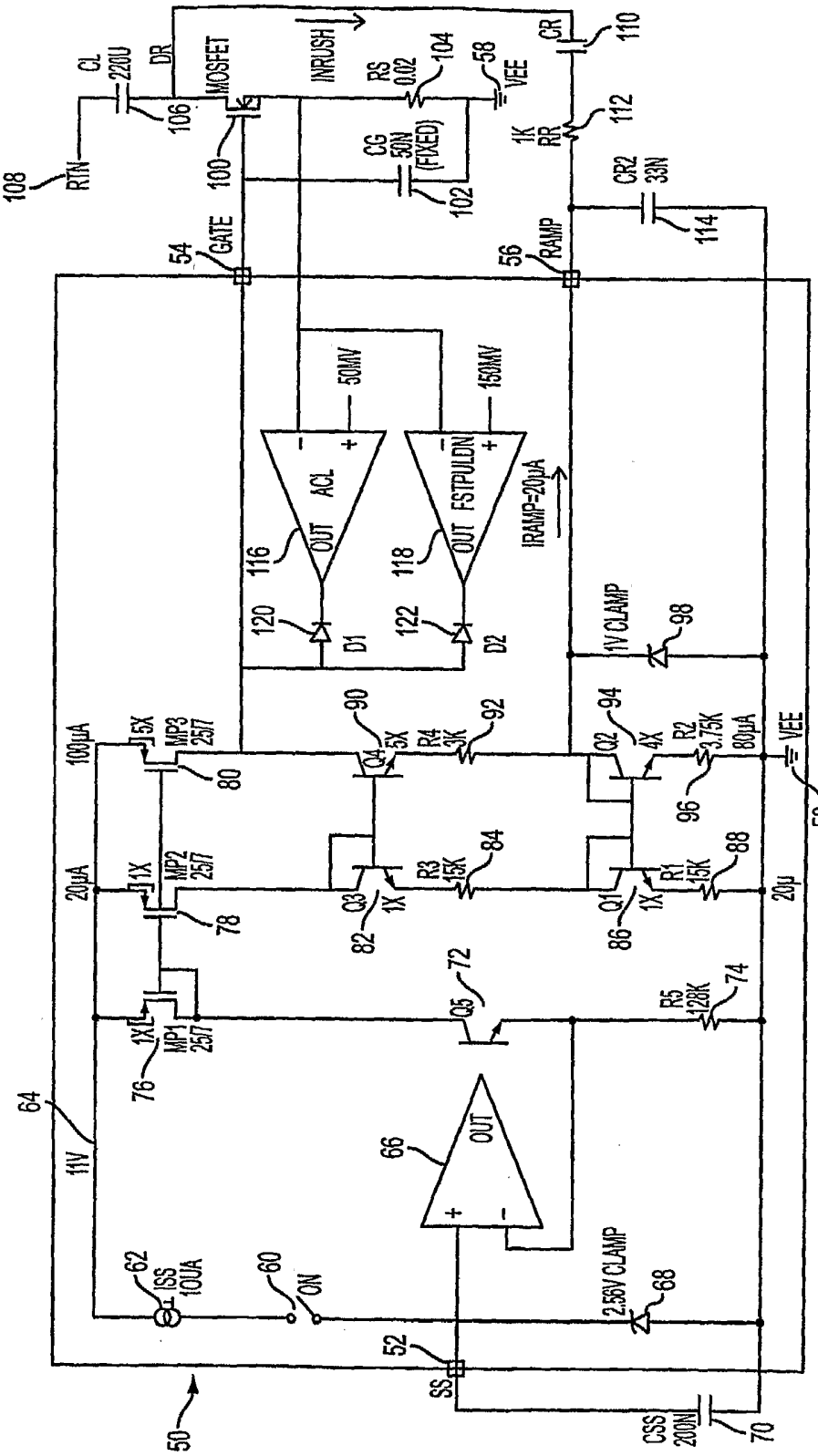


FIG. 4
PRIOR ART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DR
MOSFET
INRUSH
RS
0.02
104
58
VEE
CR
110
106
1K
RR
112
108
RTN
100
CG
50N
(FIXED)
102
CR2
33N
114
54
GATE
56
RAMP
50MV
150MV
ACL
FSTPULDN
OUT
IRAMP=20µA
116
118
120
122
D1
D2
1V CLAMP
98
100µA
5X
MP3
25/7
80
90
Q4
5X
R4
3K
92
Q2
94
4X
R2
3.75K
80µA
VEE
96
58
20µA
1X
MP2
25/7
78
R3
15K
84
Q3
1X
82
Q1
1X
R1
15K
88
86
20µ
72
Q5
R5
128K
74
1XL
MP1
25/7
76
64
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ON
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68
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SS
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200N
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FIG. 5

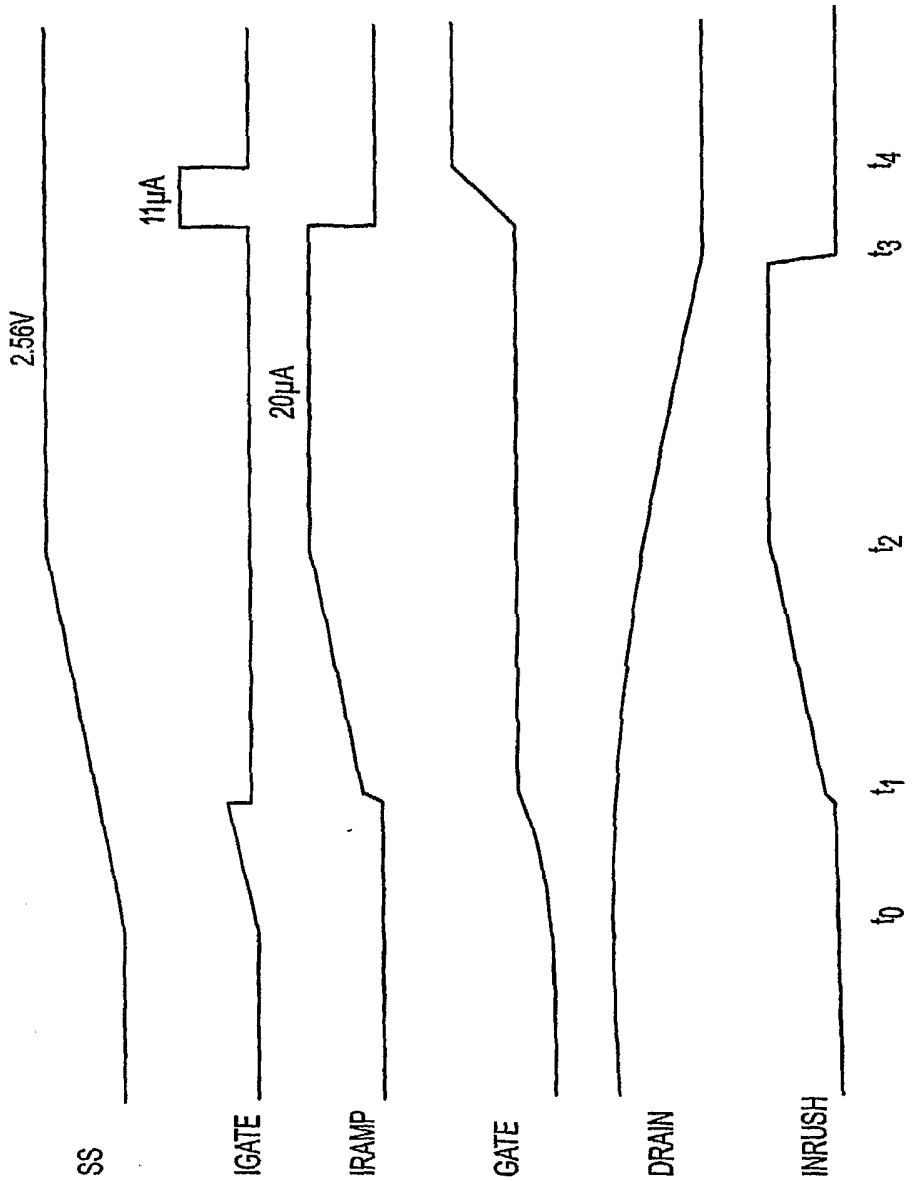

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/021272

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/082

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 540 893 A (BLOOMER ET AL) 10 September 1985 (1985-09-10) column 11, line 26 - column 12, line 68; figures 1b,1d	1-5, 8-19,22, 24-28
Y		6,7,20, 21,23
Y	EP 0 674 389 A (STMICROELECTRONICS S.R.L) 27 September 1995 (1995-09-27) column 4, line 29 - column 6, line 14; figure 3	6,7,20, 21,23
X	US 6 583 974 B1 (JUNTUNEN ASKO ET AL) 24 June 2003 (2003-06-24) column 2, lines 21-50; figure 2	1-3,5,8, 10, 15-17, 19,22,25

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 September 2006	22/09/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Moll, Peter

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/021272

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	US 5 194 760 A (BRAUN ET AL) 16 March 1993 (1993-03-16) column 3, lines 6-44; figure 3	1-4,8, 10, 14-18, 22,25,28
X	US 5 390 070 A (NIEDERMEIER ET AL) 14 February 1995 (1995-02-14) column 3, line 31 - column 4, line 36; figures 1,3	1,8,10, 15,22,25

INTERNATIONAL SEARCH REPORT

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International application No
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