BARRIER MATERIAL AND PROCESS FOR CU INTERCONNECT

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ABSTRACT

A semiconductor diffusion barrier layer and its method of manufacture is described. The barrier layer includes at least one layer of TaN, TiN, WN, TbN, VN, ZrN, CrN, WC, WN, WCN, NbN, AlN, and combinations thereof. The barrier layer may further include a metal-rich surface. Embodiments preferably include a glue layer about 10 to 500 Angstroms thick, the glue layer consisting of Ru, Ta, Ti, W, Co, Ni, Al, Nb, AlCu, and a metal-rich nitride, and combinations thereof. The ratio of the glue layer thickness to the barrier layer thickness is preferably about 1 to 50. Other alternative preferred embodiments further include a conductor annealing step. The various layers may be deposited using PVD, CVD, PECVD, PEALD and/or ALD methods including nitridation and silicidation methods.
FIG. 3

FIG. 4
FIG. 5
602 Provide substrate having a low-k dielectric layer with an opening.

604 Seal pores of the low-k dielectric layer.

605 Apply metal nitride barrier layer in opening.

608 Apply metal-rich nitride glue layer in opening.

610 Apply conductor seed layer in opening.

612 Fill opening with conductor.

614 CMP planarize

616 Anneal conductor

618 Apply cap layer

FIG. 6
BARRIER MATERIAL AND PROCESS FOR CU INTERCONNECT

TECHNICAL FIELD

[0001] This invention relates generally to semiconductor device fabrication and more particularly to a structure and method for improved resistance to electromigration problems with conductive lines and vias, such as copper, between interconnected layers.

BACKGROUND

[0002] In modern integrated circuits, minimum feature sizes, such as the channel length of field effect transistors, have reached the deep sub-micron range; thereby steadily increasing performance of these circuits in terms of speed and power consumption. As the size of the individual circuit elements is reduced, so is the available real estate for conductive interconnects in integrated circuits. Consequently, these interconnects have to be reduced to compensate for a reduced amount of available real estate and for an increased number of circuit elements provided per chip.

[0003] In integrated circuits having minimum dimensions of approximately 0.35 μm and less, a limiting factor of device performance is the signal propagation delay caused by the switching speed of the transistor elements. As the channel length of these transistor elements has now reached 0.18 μm and less, however, capacitance between neighboring conductive structures is increasingly problematic. Parasitic RC time constants therefore require the introduction of a new materials and methods for forming metallization layers.

[0004] Traditionally, metallization layers are formed by a dielectric layer stack including, for example, silicon dioxide and/or silicon nitride with aluminum as the typical metal. Since aluminum exhibits significant electromigration at higher current densities, copper is replacing aluminum. Copper has significantly lower electrical resistance and reduced electromigration problems.

[0005] The introduction of copper, however, entails a plurality of issues to be dealt with. For example, copper may not be deposited in higher amounts in an efficient manner by well-established deposition methods, such as chemical and physical vapor deposition. Moreover, copper may not be efficiently patterned by well-established anisotropic etch processes and therefore the so-called damascene technique is employed in forming metallization layers including copper lines. Typically, in the damascene technique, the dielectric layer is deposited and then patterned with trenches and vias that are subsequently filled with copper by plating methods, such as electroplating or electroless plating.

[0006] A further issue is the ability of copper to readily diffuse in silicon dioxide. Therefore, copper diffusion may negatively affect device performance, or may even lead to a complete failure of the device. It is therefore necessary to provide a diffusion barrier layer between the copper surfaces and the neighboring materials to substantially prevent copper from migrating to sensitive device regions. Silicon nitride is known as an effective copper diffusion barrier, and is thus frequently used as a dielectric barrier material separating a copper surface from an interlayer dielectric, such as silicon dioxide.

[0007] Although copper exhibits superior characteristics with respect to resistance to electromigration compared to aluminum, the ongoing shrinkage of feature sizes, however, leads to increased current densities, thereby causing a non-acceptable degree of electromigration. Electromigration is a diffusion phenomenon occurring under the influence of an electric field, which leads to copper diffusion in the direction of the moving charge carriers. This can produce voids in the copper lines that may cause device failure. It has been confirmed that these voids typically originate at the copper-silicon nitride interface and represent one of the most dominant diffusion paths in copper metallization structures. It is therefore of great importance to produce high quality interfaces between the copper and the diffusion barrier layer to reduce the electromigration to an acceptable degree.

[0008] As previously noted, the device performance of extremely scaled integrated circuits is substantially limited by the parasitic capacitances of adjacent interconnect lines, which may be reduced by decreasing the resistivity thereof and by decreasing the capacitive coupling in that the overall dielectric constant of the dielectric layer is maintained as low as possible. Since silicon nitride has a relatively high dielectric constant k of approximately 7 compared to silicon dioxide (k≈4) or other silicon dioxide based low-k dielectric layers (k<4), it is generally preferable to form the silicon nitride layer with a minimum thickness. It turns out, however, that the barrier characteristics of the silicon nitride layer depend on the thickness thereof so that thinning the silicon nitride layer, as would be desirable for a reduced overall dielectric constant, may not be practical to an extent as required for further scaling semiconductor devices including copper metallization layers without compromising device performance.

[0009] In light of the above-specified problems, a need exists for diffusion barrier layers exhibiting an improvement with respect to diffusion barrier efficiency, resistance to electromigration, lower parasitic capacitance, and other problems.

SUMMARY OF THE INVENTION

[0010] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention, in which improved structures and methods relating to copper diffusion barriers yield devices having enhanced electromigration performance.

[0011] In a preferred embodiment, a semiconductor device comprises a substrate and a dielectric layer on the substrate. The dielectric layer has at least one opening. The dielectric layer, if porous, may optionally undergo a pore-sealing process thereby improving its dielectric characteristics. A diffusion barrier layer is deposited on the dielectric layer. A conductor, preferably copper, is deposited over the barrier. An optional glue layer is deposited between the barrier layer and the conductor.

[0012] In an alternative preferred embodiment, the thickness ratio of the glue layer to the barrier layer is about 1 to 50. Another alternative embodiment comprises treating the barrier with an electron beam or an RTP process to improve properties such as adhesion and conductivity.

[0013] In other preferred embodiments, the barrier layer comprises a layer about 10 to 30 Angstroms thick. The
barrier layer includes at least one layer of TaN, TiN, WN, 
TbN, VN, ZrN, CrN, WC, WN, WCN, NbN, AlN, and 
combinations thereof. The barrier layer may be applied 
using physical vapor deposition (PVD), chemical vapor 
deposition (CVD), plasma enhanced chemical vapor depo-
sition (PECVD), or plasma enhanced atomic layer depo-
sition (PEALD).

[0014] In other preferred embodiments, the glue layer 
comprises a metal-rich nitride about 10 to 500 Angstroms 
and/or an oxide. It is applied using PVD, CVD, PECVD, PEALD, or 
preferably ALD. Alternative preferred embodiments may 
include a glue layer comprising at least one layer of Ru, Ta, 
Ti, W, Co, Ni, Al, Nb, AlCu, and combinations thereof.

[0015] Still other preferred embodiments may further 
include a cap layer deposited at least upon the conductor. 
It may be deposited by ALD, PVD, PECVD, PEALD, and/or 
CVD methods, including nitridation and silicidation meth-
ods. The cap layer preferably includes at least one layer of 
Co, W, Al, Ta, Ti, Ni, or Ru, and combinations thereof.

[0016] Other alternative preferred embodiments further 
include a conductor annealing step. Preferably, the annealing 
step is performed at about 150 to 450° C., for about 0.5 to 
5 minutes, in N2/H2 forming gas.

[0017] Additional features and advantages of embodi-
ments of the invention will be described hereinafter, which 
form the subject of the claims of the invention. It should 
be appreciated by those skilled in the art that the specific 
embodiments disclosed might be readily utilized as a basis 
for modifying or designing other structures or processes for 
carrying out the purposes of the present invention. It should 
also be realized by those skilled in the art that such equiva-
alent constructions and variations on the example embodi-
ments described do not depart from the spirit and scope of 
the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] For a more complete understanding of the present 
invention, and the advantages thereof, reference is now 
made to the following descriptions taken in conjunction with 
the accompanying drawings, in which:

[0019] FIG. 1 is a cross sectional view of a semiconductor 
device at an intermediate step in an exemplary damascene 
process further illustrating a barrier layer according to 
preferred embodiments;

[0020] FIG. 2 is a cross-sectional view showing a pre-
ferred embodiment that includes barrier, glue, and seed 
layers;

[0021] FIG. 3 is a cross-sectional view showing a con-
ductor deposited on the glue layer according to preferred 
embodiments;

[0022] FIG. 4 is a cross-sectional view showing CMP 
planarization according to preferred embodiments;

[0023] FIG. 5 cross-sectional view showing a cap layer 
according to preferred embodiments; and

[0024] FIG. 6 is a process flow diagram according to 
several embodiments of the present invention.

[0025] Corresponding numerals and symbols in the dif-
ferent figures generally refer to corresponding parts unless 
otherwise indicated. The figures are drawn to clearly illus-
trate the relevant aspects of the preferred embodiments and 
are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE 
EMBODIMENTS

[0026] The operation and fabrication of the presently 
preferred embodiments are discussed in detail below. How-
ever, the embodiments and examples described herein are 
not the only applications or uses contemplated for the 
invention. The specific embodiments discussed are merely 
illustrative of specific ways to make and use the invention, 
and do not limit the scope of the invention or the appended 
claims.

[0027] This invention relates generally to semiconductor 
device fabrication and more particularly to a structure and 
method for improved resistance to electromigration prob-
lems with conductive lines and vias, such as copper, between 
interconnected layers. The present invention will now be 
described with respect to preferred embodiments in a spe-
cific context, namely the creation of copper conductive lines 
and vias in the damascene process. It is believed that 
embodiments of the invention are particularly advantageous 
when used in this process. It is further believed that embodi-
ments of this invention are advantageous when used in other 
semiconductor fabrication applications wherein diffusion 
barriers and electromigration, for example, are a concern. It 
is further believed that embodiments described herein will 
benefit other integrated circuit interconnection applications 
on specifically mentioned. Therefore, the specific embodi-
ments discussed are merely illustrative of specific ways to 
make and use the invention, and do not limit the scope of 
the invention.

[0028] Referring now to FIG. 1, there is shown a cross 
section of the representative intermediate damascene struc-
ture 100 created in the surface of a semiconductor substrate 
102 that is to be treated in accordance with an exemplary 
damascene process and embodiments of the invention. The 
substrate 102 may comprise, for example, functional and 
logical devices, or it may comprise other interconnected 
layers. The details of the damascene process are described 
by Bao et al. in U.S. Pat. No. 6,248,665 and in U.S. patent 
publication 2004/0121583, both of which are hereby incor-
pored by reference.

[0029] Referring to FIG. 1, in an exemplary application 
of the present invention, there is shown a cross sectional, side 
view representation of a portion of a semiconductor device 
having a semiconductor wafer with an anisotropically etched, 
intermediate, dual damascene structure 100. Within 
the intermediate damascene structure 100 is a recessed feature 
85 having a via portion 104 and an overlying trench 
line portion 106. While there are several ways to form a dual 
damascene structure, one approach involves at least two 
photolithographic patterning and anisotropic etching steps to 
first form via openings 104 followed by a similar process to 
form overlying trench line openings 106 encompassing one 
or more via openings 104.

[0030] Still referring to FIG. 1, a first etch stop layer 103, 
formed of, for example silicon nitride (Si3N4), is provided 
over a conductive region 108, for example a copper damas-
cene structure formed in an underlying dielectric insulating 
layer 110. In accordance with the conventional damascene
process, the word copper is known to include suitable copper alloys. Overlying the first etch stop layer 103 is another insulating dielectric layer 112, also referred to as an intermetal dielectric (IMD) layer.

[0031] For example, the IMD layer 112 is a low-k (i.e., k less than about 4) dielectric, for example a carbon doped silicon dioxide, also referred to as organo silicate glass (OSG) and C-oxide. In alternative embodiments, low-k materials may include borophosphosilicate glass (BPSG), borosilicate glass (BSG), phosphosilicate glass (PSG), deposited over the surface of the semiconductor structures to a thickness of between about 5000 to 9000 Angstroms and preferably planarized. Exemplary organic low-k materials include polyarylene ether, hydrogen silesquioxane (HSQ), methyl silesquioxane (MSQ), polysilsequioxane, polyimide, benzocyclobutene, and amorphous Teflon. Other types of low-k materials suitably used with the method of the present invention include fluorinated silicate glass (FSG) and porous oxides. In preferred embodiments, the dielectric layer is preferably a low-k material containing C, O, Si, and F, such as fluorine-doped —(O—Si(CH3)2—O)—.

[0032] Open pores in low-k materials, e.g. IMD layer 112, are known to degrade performance. Therefore embodiments include a pore-sealing method comprising porous pore sealing using Ar and NH3, e-beam pore sealing, metal organic pore sealing, or preferably vapor pore sealing. In preferred embodiments, a low-k surface is subjected to treatment with 4MS (tetramethyldisilane) at a temperature of about 400°C. The 4MS used in the treatment of the present invention can be replaced by trimethylsilane, dimethylsilane or methylsilane. The vapor can be composed of organic or metal-organic molecules, preferably having a size larger than 10 Å. The temperature ranges from about 350-450°C for about 5-30 seconds.

[0033] The e-beam pore sealing employs an electron beam with a typical condition of 2000-5000 keV, 1-6 mA, and 75-100 μC/cm2. Plasma pore sealing uses an Ar plasma to bombard the low-k surface to block the pores of the sidewalls of the dual damascene opening. The barrier layer is preferably about 10 to 30 Angstroms thick, and it forms a barrier for Cu diffusion. The barrier layer 116 may include a metal nitride such as TaN, TiN, WN, TiN, VN, ZrN, CrN, WC, WN, WCN, NbN, TiN, and combinations thereof. In alternative embodiments the barrier layer 116 is metal rich, either throughout the bulk or only on the surface. In metal-rich, barrier layers, the ratio of nitrogen to metal is preferably less than about one (atomic ratio).

[0037] In alternative preferred embodiments, the barrier layer includes a first barrier layer on the surface of the low-k dielectric layer and a second barrier layer on the first barrier layer. The first barrier layer includes an atomic layer deposited (ALD) material selected from the group consisting essentially of Ta, W, and combinations thereof. The second barrier layer is selected from the group consisting essentially of Ni, Co, Al, AlCu alloy, W, Ti, Ta, Ru, and combinations thereof. An optional Cu seed layer may be deposited on the second barrier layer.

[0038] The barrier layer 116 may be applied using physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or plasma enhanced atomic layer deposition (PEALD). In preferred embodiments, the barrier layer 116 comprises TaN, and it is deposited using atomic layer deposition (ALD).

[0039] An ALD deposited, TaN barrier layer 116 is particularly advantageous in forming a damascene structure with reduced capacitance and reduced electromigration effects. As semiconductor dimensions continue to shrink, capacitance between conductive structures is increasingly problematic. Applicants have found that ALD barrier 116 deposition is more preferred than, for example, PVD. In the preferred embodiment comprising a TaN barrier 116, for example, applicants found that ALD significantly reduces the parasitic capacitance between neighboring conductive structures by as much as 11.5%, as compared to PVD. An ALD deposited barrier, therefore, enables thinner metal lines because the metal line with ALD barrier has a lower effective resistivity.

[0040] In still other embodiments, the barrier layer 116 includes a Ta/TaN bi-layer structure. Ta/TaN bilayer embodiments include PEALD TaN and ALD Ta, ALD TaN and PEALD Ta, or PEALD TaN and PEALD Ta.

[0041] As shown in FIG. 2, preferred embodiments contain a glue layer 118 between the barrier layer 116 and an overlying conductor (described below, see FIG. 3, 120). Glue layer 118 enhances adhesion between and adjacent layers. The glue layer 118 preferably contains materials that bond with copper and/or the underlying barrier layer. It may be about 10 to 500 Angstroms thick, preferably less than about 150 Å. It is also preferably metal-rich.

[0042] In alternative embodiments, the glue layer 118 preferably comprises two layers (not specifically shown). The first layer is preferably a metal-rich thin layer from about 130 to 170 Angstroms, preferably about 150 Angstroms. The second layer is stoichiometric metal nitride layer about 500 to 600 Angstroms, preferably about 550 Angstroms. The glue layer 118 may be applied using PVD, CVD, PEALD, PEALD, and, preferably, ALD at a deposition rate less than about 1Å/sec at about 100-300°C.
Alternative embodiments include a glue layer 118 consisting of Ru, Ta, Ti, W, Co, Ni, Al, Nb, AlCu alloy, and combinations thereof. In preferred embodiments, the ratio of the glue layer 118 thickness to the barrier layer 116 thickness is about 1 to 50.

Prior to deposition of a conductor, a seed layer 119 is optionally deposited over the glue layer 118 by, for example, PVD and/or CVD. Seed layer 119, preferably copper, is PVD deposited to form a continuous layer about 400 to 700 Å thick over the wafer process surface, thereby providing a continuously conductive surface for forming the bulk of the copper during the ECD process.

Still referring to FIG. 2, the embodiment summarized therein is preferably annealed at about 300 °C for about 1 minute. Annealing advantageously lowers the effective resistivity of the barrier/glue/seed stack. Typically glue layers include Ta and Co exhibit the most improvement.

In other embodiments of the present invention, there is an alternative method to improve adhesion between the barrier layer and adjacent layers. The deposition of the barrier layer, as described above, may further include a thermal treatment such as electron beam annealing or rapid thermal processing, RTP. Preferred treatments advantageously enhance wetability and/or adhesion between the barrier layer and the copper layer.

The thermal adhesion process is preferably performed at an intermediate stage during the ALD deposition of the barrier. Typically, barrier formation such as ALD TaN includes multiple steps. First, a Ta precursor is used to form a saturated surface layer. Next, the saturated surface layer is reduced and nitrided using NH3 to form a Ta3N5 monolayer. The thermal adhesion treatment occurs between these two steps. In the case of a WCN barrier, which is a three-step deposition process, the thermal adhesion is performed prior to the reduction step. The RTP may be incorporated into the ALD chamber. A typical RTP temperature is about 200 to 400 °C.

Referring to FIG. 3, following deposition of glue layer 118, a conductor 120, preferably copper, is electroplated according to a conventional electro-chemical deposition (ECD) process to fill the dual damascene trench 106 and via 104 including an overlying portion above the trench level. In alternative embodiments, a seed layer (not shown) is between glue layer 118 and conductor 120. Although other copper filling methods, such as PVD and CVD, may be used, electroplating (electrodeposition) is preferred because of its superior gap-filling and step coverage. Alternative embodiments may include the conductor 120 comprising at least one of Cu, Al, Au, or Ag, and combinations thereof, or alloyed compositions thereof.

A chemical mechanical polishing (CMP) may be used to polish the conductor fill to the level of the feature. In another alternative, electropolishing or overburden reduction may be used in place of CMP or serially with CMP. In the alternative, a simultaneous CMP and plating process may be performed. As shown in FIG. 4, the CMP process forms a recessed area 121 due to preferential removal of the softer conductor 120.

Referring still to FIG. 4, in another embodiment, an upper portion 122 of the recessed conductor is removed. The depth of the recessed area 121 is increased by first oxidizing the upper portion 122 of the exposed conductor, e.g., copper, followed by another CMP step or wet etching step to remove the oxidized upper portion 122 of the copper feature.

Following CMP planarization, alternative preferred embodiments include a seed layer (not shown) and conductor 120 anneal. Preferably, the annealing step is performed at about 150 to 450 °C, for about 0.5 to 5 minutes, in N2/H2 forming gas. The anneal causes metals in the seed layer to migrate or diffuse throughout the copper fill layer 120, thereby forming a copper-metal fill layer 120. Preferably, the Cu seed layer includes titanium. Annealing advantageously causes the Ti to distribute approximately uniformly within conductor layer 120 and form a uniform copper-titanium fill layer 120. The anneal also causes granularity of the surface of the conductor layer 120 and results in improved adhesion between the conductor layer 120 and a cap layer (as shown in FIG. 5) that is deposited over this surface.

Referring to FIG. 5, in an embodiment of the present invention, following the CMP, a cap layer 124 is deposited over the damascene structure. The cap layer 124 is preferably deposited to a thickness of about 50 Angstroms to about 500 Angstroms. The cap layer 124 is preferably sufficiently thick to avoid copper diffusion. It is deposited by conventional ALD, PVD, PECVD, PEALD, and/or CVD methods, including nitridation and silicidation methods known in the art. The cap layer 124 preferably includes at least one layer of W, Al, Ta, Ti, Ni, Ru, or nitrides thereof. Preferred embodiments include a Co or nitride-Co cap layer deposited by CVD or ALD.

Still other embodiments may include a cap layer comprising at least one layer of a carbon-containing dielectric (such as SiC, SiOC, SiCN), a nitrogen-containing dielectric, a nitrogen-containing conductive layer, or a silicon-containing layer.

Returning to FIG. 5, following the CMP and capping processes, an etch stop layer 126 of silicon nitride may be deposited over the process wafer surface including over the barrier capping layer overlying the copper feature.

Referring now to FIG. 6, there is shown a process flow diagram including several of the preferred embodiments of the present invention. In process 602, a substrate is provided, and within the substrate a feature opening is formed in a low-k dielectric insulating layer (ILD). In process 604, the pores of the low-k dielectric are sealed. In process 605, the feature opening is lined with a metal nitride barrier layer. In process 606, the barrier layer is treated to enhance adhesion. In process 608, a metal-rich nitride glue layer is applied. In process 610, a Cu seed layer is applied. In process 612, the feature opening is filled with a conductor. In process 614, the structure is CMP planarized. In process 616, the conductor is annealed. In process 618, a cap layer is applied.

The embodiments of the invention described above are exemplary and not limiting, and variations that are apparent to those skilled in the art that include the features of the invention are within the scope of the invention and the appended claims. Although embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions
and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A semiconductor device having enhanced electromigration performance, the device comprising:
   a low-k dielectric layer, the low-k dielectric layer having a surface with a recessed feature;
   a diffusion barrier layer on the surface of the low-k dielectric layer;
   a glue layer on the diffusion barrier layer; and
   a conductor on the glue layer, the conductor filling the recessed feature.

2. The semiconductor device of claim 1, further including a cap layer on the conductor, wherein the cap layer is selected from the group consisting essentially of Co, W, Al, Ta, Ti, Ni, Ru, and combinations thereof.

3. The semiconductor device of claim 1, wherein the diffusion barrier layer includes a first barrier layer on the surface of the low-k dielectric layer and a second barrier layer on the first barrier layer.

4. The semiconductor device of claim 3, wherein the first barrier layer is selected from the group consisting essentially of Ta, W, and combinations thereof.

5. The semiconductor device of claim 3, wherein the second barrier layer is selected from the group consisting essentially of Ni, Co, Al, AIrCu alloy, W, Ti, Ta, Ra, Ru, and combinations thereof.

6. The semiconductor device of claim 3, wherein the second barrier layer is selected from the group consisting essentially of TaN, TiN, WN, TbN, VN, ZrN, CrN, WC, WN, WCN, NbN, AlN, and combinations thereof.

7. The semiconductor device of claim 1, wherein the diffusion barrier layer is selected from the group consisting essentially of TaN, TiN, WN, TbN, VN, ZrN, CrN, WC, WN, WCN, NbN, AlN, and combinations thereof.

8. The semiconductor device of claim 7, wherein the diffusion barrier layer is metal rich.

9. The semiconductor device of claim 7, wherein the diffusion barrier layer further includes a metal rich surface.

10. The semiconductor device of claim 7, wherein the diffusion barrier layer further includes a thermal treatment to enhance adhesion.

11. The semiconductor device of claim 1, wherein the diffusion barrier layer is about 10 to 30 Angstroms.

12. The semiconductor device of claim 1, wherein the low-k dielectric layer comprises C, O, Si, and F.

13. The semiconductor device of claim 2, wherein the cap layer is selected from the group consisting essentially of a carbon-containing dielectric, a nitrogen-containing dielectric, a nitrogen-containing conductor, a silicon-containing conductive layer, and silicon, and combinations thereof.

14. The semiconductor device of claim 1, wherein the glue layer is selected from the group consisting essentially of a metal-rich nitride, Ru, Ta, Ti, W, Co, Ni, Al, Nb, AlrCu, and combinations thereof.

15. The semiconductor device of claim 14, wherein a thickness ratio of the glue layer to the diffusion barrier layer is about 1 to 50.

16. The semiconductor device of claim 14, wherein a thickness of the glue layer is about 10 to 500 Angstroms.

17. The semiconductor device of claim 14, wherein the metal-rich nitride comprises TaN and wherein an atomic ratio of nitrogen to tantalum is less than about 1.

18. The semiconductor device of claim 1 wherein the conductor is selected from the group consisting essentially of Cu, Al, Au, and Ag, and combinations thereof.

19. A method of reducing electromigration effects in a copper damascene device, the method comprising:
   forming a low-k dielectric layer, the low-k dielectric layer having a surface with a recessed feature;
   forming a diffusion barrier layer over the surface of the low-k dielectric layer;
   forming a glue layer upon the diffusion barrier layer;
   filling the recessed feature with a conductor;
   annealing the conductor; and
   forming a cap layer upon the conductor.

20. The method of claim 19, wherein the conductor is selected from the group consisting essentially of Cu, Al, Ta, Ti, Ni, Ru, and combinations thereof.

21. The method of claim 19, wherein the diffusion barrier layer is selected from the group consisting essentially of TaN, TiN, WN, TbN, VN, ZrN, CrN, WC, WN, WCN, NbN, AlN, and combinations thereof.

22. The method of claim 19, wherein the diffusion barrier layer is about 10 to 30 Angstroms.

23. The method of claim 19, wherein the cap layer is selected from the group consisting essentially of a carbon-containing dielectric, a nitrogen-containing dielectric, a nitrogen-containing conductor, a silicon-containing conductive layer, and silicon, and combinations thereof.

24. The method of claim 19, further including thermally treating the diffusion barrier layer.

25. The method of claim 19, wherein the glue layer is deposited using physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or plasma enhanced atomic layer deposition (PEALD).

26. The method of claim 25, wherein the glue layer is deposited using physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or plasma enhanced atomic layer deposition (PEALD).

27. The method of claim 25, wherein a thickness ratio of the glue layer to the diffusion barrier layer is about 1 to 50.
28. The method of claim 25, wherein a thickness of the glue layer is about 10 to 500 Angstroms.

29. The method claim 25, wherein the metal-rich nitride comprises TaN and wherein an atomic ratio of nitrogen to tantalum is less than about 1.

30. The method of claim 19, wherein the conductor annealing step comprises annealing at about 150 to 450°C for about 0.5 to 5 minutes in forming gas.

31. The method of claim 19, wherein the diffusion barrier layer is deposited using physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or plasma enhanced atomic layer deposition (PEALD).

32. The method of claim 19, wherein the cap layer is deposited using physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or plasma enhanced atomic layer deposition (PEALD).

33. A method for forming a semiconductor device, comprising:

- providing a substrate, the substrate including a low-k dielectric layer with an opening;
- performing a pore sealing process;
- forming a barrier layer within the opening;
- forming a glue layer on the barrier layer;
- forming a seed layer on the glue layer;
- forming a conductor on the seed layer;
- and forming a cap layer on the conductor.

34. The method of claim 33, wherein the cap layer is selected from the group consisting essentially of Co, W, Al, Ta, Ti, Ni, Ru, and combinations thereof.

35. The method of claim 33, wherein the barrier layer is selected from the group consisting essentially of TaN, TiN, WN, TiN, VN, ZrN, CrN, WC, WN, WCN, NbN, AlN, and combinations thereof.

36. The method of claim 33, wherein the barrier layer is about 10 to 30 Angstroms.

37. The method of claim 33, wherein the cap layer is selected from the group consisting essentially of a carbon-containing dielectric, a nitrogen-containing dielectric, a nitrogen-containing conductor, a silicon-containing conductive layer, and silicon, and combinations thereof.

38. The method of claim 33, wherein the glue layer is selected from the group consisting essentially of a metal-rich nitride, Ru, Ta, Ti, W, Co, Ni, Al, Nb, AlCu, and combinations thereof.

39. The method of claim 33, wherein a thickness ratio of the glue layer to the barrier layer is about 1 to 50.

40. The method of claim 33, wherein a thickness of the glue layer is about 10 to 500 Angstroms.

41. The method claim 38, wherein the metal-rich nitride comprises TaN and wherein an atomic ratio of nitrogen to tantalum is less than about 1.

42. The method of claim 33, further comprising annealing the conductor at about 150 to 450°C for about 0.5 to 5 minutes in forming gas.

43. The method of claim 33, wherein the pore sealing process comprises vapor pore sealing.