

Nov. 18, 1958

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2,861,260

READING SATURABLE CORES

Filed Feb. 7, 1957

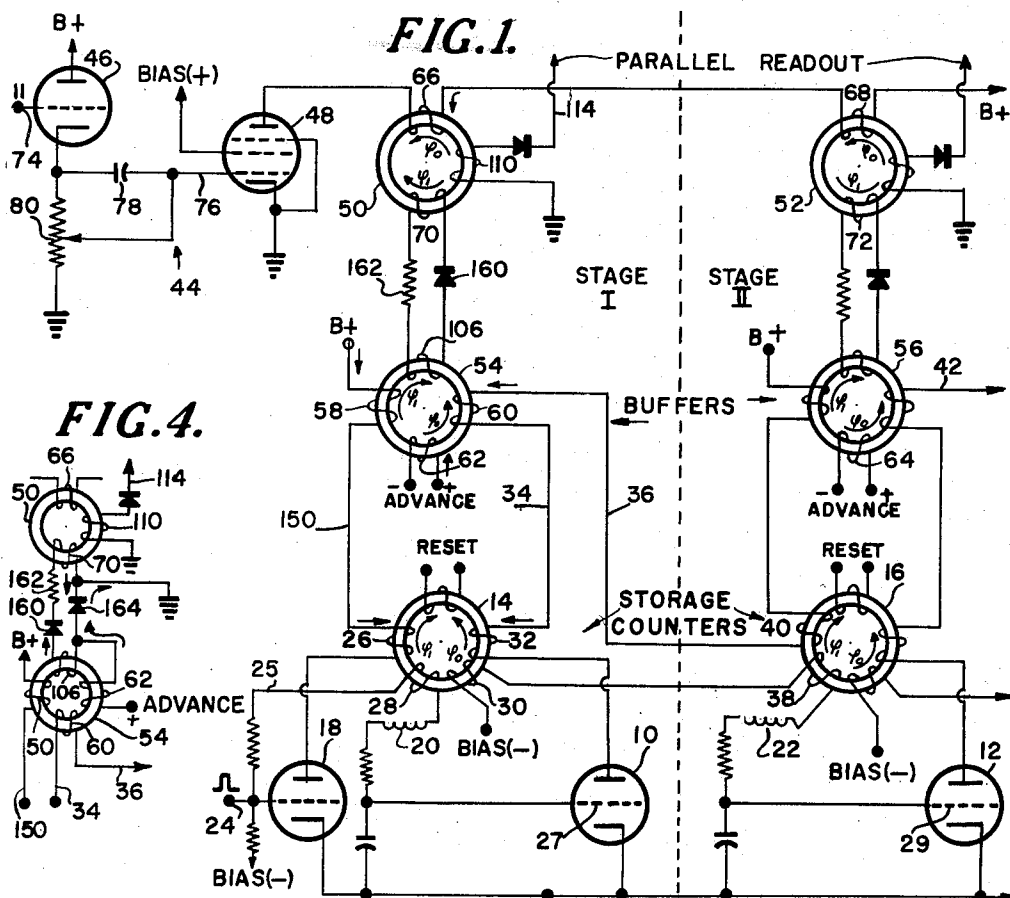


FIG. 4.

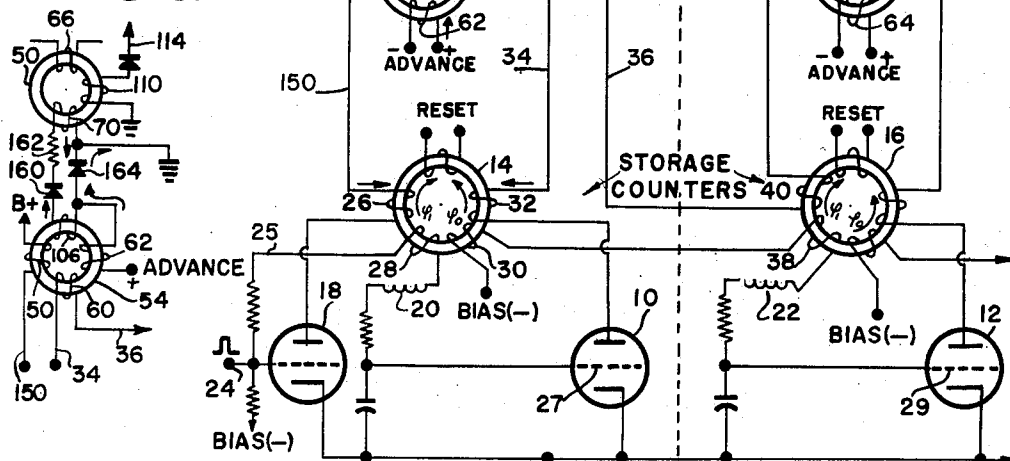


FIG. 2.

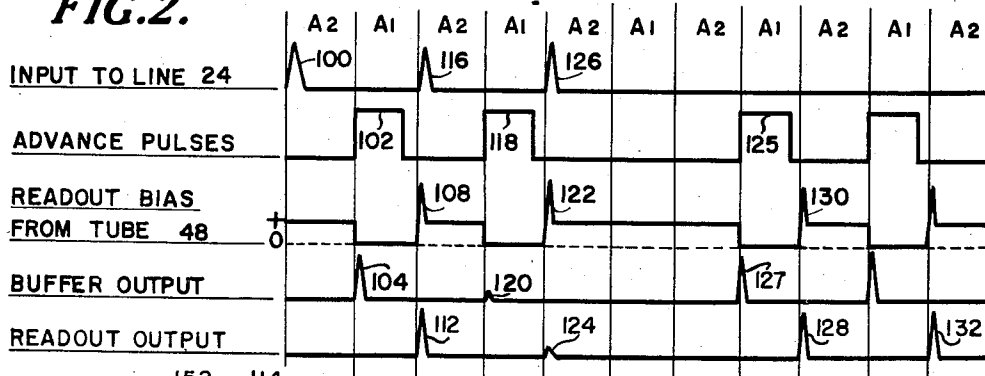
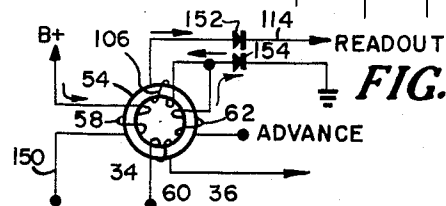


FIG. 3.

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READING SATURABLE CORES

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Application February 7, 1957, Serial No. 638,770

28 Claims. (Cl. 340—174)

This invention relates to magnetic devices which utilize the hysteresis characteristic of magnetic materials as a means for gating digital information.

The value of saturable reactors comprised of suitably wound small cores of ferromagnetic material for use as storage and logical elements in electronic data handling systems is being increasingly recognized, particularly because of their miniature size, low power requirements, dependability, and their ability to retain stored information for long periods of time in spite of power failure. The cores of such reactor elements are able to store binary information in the form of residual magnetization after the cores are magnetized to saturation in either of two directions. The saturation can be achieved by passing a current through a winding on the core. When the magnetomotive force thus created is opposite in polarity to the direction of the pre-existing residual magnetic induction, the direction of the static residual magnetization of the core is reversed. The resultant change in flux produces a sizable voltage pulse across every winding on the core, which pulse may be utilized in a variety of ways such as to drive a second saturable reactor element to saturation in a predetermined polarity. On the other hand, the application of a magnetomotive force which merely drives a reactor element further into saturation in the same direction as that of the residual flux produces a change in flux which is small compared to that created in a reversal of flux polarity so that a correspondingly small voltage pulse is induced in each winding on the core.

In order to achieve a large ratio between voltage pulses induced in switching the polarity of a saturable reactor element as compared to that obtained in driving it further into saturation in the direction of its pre-existing residual magnetization, the core material is preferably one having at least a quasi-rectangular hysteresis characteristic so that the residual flux density is a relatively large percentage of the flux density present during the application of a saturating magnetomotive force. A number of suitable magnetic materials are available such as Deltamax, 4-79 Permalloy, and certain ferromagnetic ferrites. In order to improve high frequency response by reducing eddy current losses, metallic ferro-alloys are preferably used in thin strips which may be wrapped around ceramic spools while ferrite cores may be molded and windings placed directly thereon, inasmuch as ferrites are relatively free from eddy current effects.

While saturable reactor elements can be used extensively as storage and switching elements in electronic data handling systems, they cannot by themselves entirely eliminate vacuum tubes or transistors and the like, because saturable reactor elements are current driven devices and so must be associated with suitable current generating means. Accordingly, a great many logical circuits employing reactor elements and vacuum tubes or transistors in close interrelation are being utilized with the reactor elements serving to store information

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and the vacuum tubes or transistors used to switch the information.

In circuits employing closely related saturable reactor elements and vacuum tubes or transistors, a major problem has been to read out the information stored in the reactor elements without causing one or more tubes or transistors to generate an unwanted current. This problem exists both where it is desired to read out the stored information while retaining it in the saturable reactor storage elements, so-called "non-destructive readout," and where the readout operation may leave one or more of the storage elements with a different stored digit, so-called "destructive readout." Unwanted currents generated in the associated vacuum tubes or transistors in the readout operation invariably prevent non-destructive readout and may produce errors, even in destructive readout.

It is accordingly an object of this invention to provide a novel system for reading out information from saturable reactor elements.

It is a further object of this invention to provide means for reading out digital information non-destructively from circuits composed of interrelated saturable reactor elements and current-generating devices. It is another object of this invention to provide novel means for destructively reading out digital information from saturable reactor elements which are closely associated with current-generating devices.

It is a more specific object of this invention to provide means for reading out information either destructively or non-destructively from a binary-coded counter composed of interrelated saturable reactor elements and vacuum tubes.

These and other objects of the invention as well as the invention itself will be best understood from the following description and claims when taken in connection with the drawings in which:

Figure 1 is a fractional circuit diagram of a conventional, vacuum tube, magnetic counter which is modified according to the principles of this invention to obtain non-destructive readout.

Figure 2 is a timing diagram illustrating the readout from one stage of the counter of Figure 1.

Figure 3 is a fragmentary diagram showing the manner in which the circuit of Figure 1 may be modified for purposes of economy if destructive readout is permissible.

Figure 4 shows another modification of Figure 1 whereby the saturable reactor buffer elements are switched only under no-load conditions and the feature of non-destructive readout is retained.

The cores of the saturable reactor elements are shown in the drawings to be toroidal in shape. However, the shape of the cores is not critical so long as adequate coupling is achieved between the core and its windings. Toroidal cores are especially satisfactory in this respect and incidentally produce a minimum external field.

Reference is now made to Figure 1 which shows the first two stages of a multi-stage binary-coded counter which is provided with means for gating out information stored thereby in parallel, non-destructively. The counter per se is shown and described on pages 42 and 43 of an article by Bernard M. Gordon and Renato N. Nicola entitled "Special-Purpose Digital Data-Processing Computers" appearing in May 2, 1952, "Proceedings of the ACM." No indication is given in the article as to gating out information from the counter in parallel. Each stage of the counter as shown in the article contains one transistor, or as herein described, one vacuum tube 10, 12, etc., respectively, and one saturable reactor storage or counting element 14, 16, etc., respectively, and each of the reactor cores is provided with five wind-

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ings. An additional transistor or triode 18 is utilized at the input of the first stage to initiate the counting action. It should be noted, however, that the counter has been modified by the inclusion in each stage of an inductive impedance such as choke 20, 22, etc., respectively, having a value in the order of one millihenry. The choke is not essential but has been found to improve the reliability of the counter, especially at the very high frequencies made possible by the availability of improved ferromagnetic materials.

Although vacuum tubes have been used in illustration with the counter herein, it will be understood, as in keeping with the above cited article, that transistors may be used in their stead.

Briefly, the operation of the magnetic counter apart from its readout modification is as follows. Assuming that storage elements 14, 16 are initially in the state of residual magnetization which was arbitrarily designated as the "0" or counter-clockwise flux state, a positive voltage pulse indicative of a binary "1" on input lead 24 is fed over a first unidirectional path to input circuit means including triode 18 which causes triode 18 to conduct current through winding 26 on storage element 14. The resultant magnetomotive force switches element 14 to the "1" or clockwise flux state, inducing a sizable voltage pulse across every winding thereon. The voltage induced across winding 28 counteracts the input pulse on leads 24 and 25 via the second input circuit means and unidirectional path to prevent the raising of grid 27 and thereby prevent the triggering of triode 10, while the voltage induced across winding 30 merely drives the grid 29 of triode 12 more negative.

A second positive input pulse on line 24 again causes triode 18 to conduct, but storage element 14 is already in the "1" state so that the back E. M. F. induced across winding 28 is insufficient to prevent the input pulse on line 25 from passing through winding 28 and choke 20 to raise grid 27 to trigger tube 10 to conduction. The output of tube 10 is applied to winding 32 and because of the transformer coupling between windings 32 and 28, the grid of tube 18 takes a negative swing in the manner of a blocking oscillator. This allows the plate current from tube 10 to increase, since the plate current from tube 18 decreases with a negative swing towards cutoff and produces a positive swing on the grid of tube 10 by transformer action between windings 26 and 28. Therefore, storage element 14 is driven to the "0" stage. The blocking-oscillator action is modified by the choke 20 to assure the saturation of element 14 in the "0" state, and by virtue of the plate current in lines 34, 36, the saturation of storage element 16 is assured of being in a state arbitrarily designated the "1" or clockwise flux state. The switching of element 16 to "1" creates a back E. M. F. across winding 38 which blocks the voltage pulse generated across winding 30 from raising grid 29 and thereby from triggering tube 12.

A third positive pulse on input lead 24 again causes plate current to flow through winding 26 to switch element 14 to the "1" state while transformer coupling between windings 26 and 28 prevents succeeding stages from being affected. A fourth pulse, as did the second pulse, switches element 14 to the "0" state and causes plate current from triode 10 to flow through winding 40, but since element 16 is already in the "1" state, the voltage induced across winding 30 by the output of tube 10 through winding 32 raises grid 29 to trigger triode 12. Element 16 is accordingly returned to the "0" state by the output of tube 12, and a "carry" pulse on line 42 switches the state of the storage element of the third stage (not shown) to an arbitrarily designated "1" state, etc.

Parallel non-destructive readout from the binary counter may be achieved by adding two saturable reactor elements to each stage of the counter and by supplying a single readout control circuit 44 comprised of a cathode

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follower 46 and a gate tube 48. One saturable reactor element 50, 52, etc., respectively, in each stage may be conveniently referred to as the readout element and the other additional elements 54, 56, etc., respectively, serve as buffers between the storage and readout elements. It will be appreciated that buffer elements 54, 56 will assume the same polarity as storage element 14, 16 at all times in the absence of magnetomotive forces not yet considered. For instance, when plate current through winding 26 switches storage element 14 to the "1" state, the plate current also flows through winding 58 to switch buffer element 54 to a "1" or clockwise flux state. Then when blocking oscillator action increases the plate current from tube 10 while cutting off the plate current from tube 18, the predominant current through winding 60 will switch buffer element 54 to the "0" or counter-clockwise flux state.

In order to effect parallel readout, a two-phase, interlaced sequence of current pulses are utilized, their alternate periods of time in the sequence being conveniently designated as A_1 and A_2 periods. The A_2 periods are reserved for the input and output of information while A_1 periods are used to shift the information from the buffer elements 54, 56 to the readout elements 50, 52. An advance pulse may then be passed through windings 62, 64 only during an A_1 period. The advance pulse may conveniently, but does not necessarily, have a relatively square waveform of duration slightly shorter than one A_1 period, and when applied to buffer elements 54, 56, always drives those elements to the "0" or counter-clockwise flux state.

Readout control is effected from circuit 44; the gate tube 48 thereof is normally biased to conduction so that a constant current flows through windings 66, 68, and like windings in other stages (not shown) to produce a magnetomotive force in elements 50, 52, etc., which sets these elements in the arbitrarily designated "0" or counter-clockwise flux polarity. The amplitude of this current can be readily adjusted so that the magnetomotive force is large enough to prevent any pulses in windings 70, 72 from switching elements 50, 52, respectively, to the "1" or clockwise flux state. The biasing current can be removed by applying a negative voltage on line 74 to cut off the normally conducting cathode follower tube 46 so that the potential of lead 76 going to the control grid of pentode 48 takes a negative swing, cutting off pentode 48. By removing the negative voltage on lead 74, cathode follower tube 46 again becomes conducting, thereby causing the potential of line 76 to go positive, and current again flows through windings 66, 68. However, A. C. coupling by condenser 78 between cathode follower 46 and the control grid of tube 48 gives a sharp increase to the plate current pulse of tube 48 when it is brought to conduction. This surge of current may be several times the amplitude of the steady biasing current, and thus it can apply sufficient magnetomotive force to saturable reactor elements 50, 52 to return them to the "0" state if they were switched to the "1" state during removal of the biasing current. This current surge quickly falls off to the lower steady value which is preferably just sufficient to retain readout elements 50, 52 at "0" to hold power losses to a minimum. It will be appreciated by those skilled in the art that the amplitude and duration of the current surge on reapplication of the biasing current is dependent upon the RC time constant of capacitor 78 and potentiometer 80 and so can be varied by adjusting either or the latter as shown. It has been found that a steady biasing current in the order of 30 milliamperes and a current surge on its reapplication of 75 milliamperes are satisfactory.

The method of reading out information from the magnetic counter in parallel, non-destructively, may best be understood with reference to the timing diagram of Figure 2 considered in connection with the first stage of

Figure 1. For exemplary purposes, an input of three successive pulses representing binary "1's" followed by a continuous stream of "0's" or the absence of pulses is applied to the first stage of the counter which was initially cleared. The first "1" pulse 100 is applied during an A_2 time period to set storage element 14 and buffer element 54 to the "1" state. This "1" may be read out in parallel by applying during the next A_1 period an advance pulse 102 to winding 62 of buffer element 54 while simultaneously reducing or removing the bias current from winding 66 of readout element 50. The advance current drives buffer element 54 to the "0" or counter-clockwise flux state and induces a pulse 104 across winding 106 to switch readout element 50 to its "1" or clockwise flux state. The current surge 108 through winding 66 on re-application of the bias current resets element 50 to "0," inducing a voltage pulse across windings 70 and 110. The pulse 112 across winding 110 as read out on line 114 may be used for a variety of purposes including the switching of a saturable reactor element in another counter or register. The readout pulse across winding 70, in turn, effectively maintains correspondence between the states of the buffer core 54 and the storage element 14 in the absence of other inputs on line 24, and in this particular instance the readout pulse tends to return the buffer core 54 to the "1" state, but the second "1" pulse 116 appears simultaneously on lead 24. This pulse 116 resets storage element 14 to "0" as was explained above in connection with the counter action and a relatively large current pulse flows through winding 60 on buffer element 54. The current through winding 60 and the current flowing through winding 106 produce opposing magnetomotive forces with the result that buffer element 54 remains in the "0" state and so again corresponds to the residual state of storage element 14. The application of an advance pulse 118 at the next A_1 period merely drives buffer element 54 further into the "0" state and so induces an insignificant pulse 120 across winding 106 so that readout element 50 remains at "0" even though the bias current was removed, and re-application of the bias at 122 neither affects buffer element 54 nor generates a readout pulse on line 114 other than the relatively small blip 124 produced in driving element 50 further into saturation in the "0" direction. The next input pulse 126 finds both storage and buffer elements 14, 54 at "0" and so switches them to "1."

The contents of the magnetic counter are retained indefinitely until the next input pulse arrives on line 24 regardless of whether readout is initiated by removing the bias current and simultaneously applying an advance pulse or regardless of how many times the stored information is read out. In the example illustrated by Figure 2, no readout is further called for after blip 124 until the second succeeding A_1 period, at which time the "1" stored in buffer element 54 is transferred by applying advance pulse 125 to cause pulse 127 to be presented to readout element 50 for readout at the beginning of the next A_2 period on line 114 as pulse 128. The current surge 130 also returns buffer element 54 to the "1" state so that a readout operation during the succeeding cycle produces another "1" pulse 132 on line 114.

While the discussion of readout from the counter of Figure 1 has been confined to its first stage, it will be appreciated that a practical application may call for simultaneous readout from the entire counter. Accordingly, a single advance pulse may be applied to all buffer elements and the biasing current will flow through a winding on each readout element. Of course, each stage or groups of stages could be individually controlled without difficulty in the event that such control were desirable.

It should also be noted that the application of an advance current to a buffer element and the resetting of the buffer element from the readout elements in no way affect the storage or saturable core counting elements 14,

16 because each line 34, 150, for example, coupling a winding on a buffer element to a winding on a storage element is in a unidirectional path including a unidirectional current conducting device such as a vacuum tube or transistor and is therefore open-circuited as by vacuum tubes 10 and 12. For this reason, no voltages are induced which would drive a tube to conduction except as a result of the counting action. By the same token the application of a reset pulse to the storage elements does not affect the buffer elements so that an advance pulse must also be supplied thereto without removing the bias current in order to clear the circuit of Figure 1 completely. It should be noted that except when clearing the counter, advance pulses are applied to the buffer elements only when the bias from tube 48 is simultaneously reduced or removed from the readout elements, so that the information stored in the buffer elements is not destroyed.

Reference is now made to Figure 3 to illustrate the manner in which the circuit of Figure 1 could be modified if destructive readout from a binary-coded magnetic counter is permissible. However, as modified by Figure 3, the readout is destructive only in the sense that a subsequent readout from any stage could not be effected until the information stored in that stage had been altered by the receipt of new information. Since this embodiment of the invention does not affect the magnetic counter, only a fragmentary view of the first stage is shown in Figure 3 beginning with leads 34 and 150 from windings on storage element 14 of Figure 1 and extending to lead 36 to a succeeding storage element, for example, element 16 of stage 2. If magnetic element 54 is in the "1" state, a positive current applied to advance winding 62 drives element 54 to the "0" state to induce a sizable voltage pulse across winding 106. To this pulse, rectifier 152 presents a low forward impedance while rectifier 154 would normally present a high forward impedance. However, the advance current flows from winding 62 through rectifier 154 to ground to bias it to conduction so that rectifier 154 also presents a low impedance and allows a reverse current flow in the form of the induced pulse, and a signal representing the "1" appears on line 114. No current is induced in windings 58 and 60 since their input lines 150 and 34, respectively, are open-circuited by vacuum tubes such as tubes 18 and 10 of Figure 1. Unidirectional device 154 may be forwardly biased in any other manner, but is preferably biased by the advance pulses as shown. When readout is called for while magnetic element 54 stores a "0," the advance pulse merely drives element 54 further into the "0" direction so that virtually no pulse is generated across winding 106. It should be noted that rectifiers 152, 154 as well as other rectifiers included in the circuits used to illustrate this invention are preferably semi-conducting diodes.

While the reading out of a "1" from magnetic element 54 of Figure 3 leaves that element in the "0" state in the absence of provision for feedback of the "1" from the device to which line 114 transmits that "1," the counting or storage element connected to lines 150 and 34 (e. g., element 14 of Figure 1) is not affected so that the "1" information is not lost. However, no means is provided for placing the "1" still stored by element 14 back into buffer element 54; therefore, a subsequent, accurate, parallel readout cannot be obtained without inserting enough new information to put every stage of the counter through at least one change in state. Accordingly, readout using the modification of Figure 3 is considered to be destructive, though not wholly so.

The readout device of Figure 3, however, offers certain advantages over that of Figure 1. It offers economy in circuit components in requiring one less saturable reactor element per stage and in eliminating the readout control circuit 44 of Figure 1. It offers economy in power in eliminating the biasing current flowing from pentode 48 and the current flowing through the normally conducting cathode follower 46. Another consideration is the no-

load switching of buffer element 54 in the modification of Figure 3 since rectifiers 152, 154 block any current caused by the voltage which may be generated across output winding 106 while driving buffer element 54 with pulses on either of lines 34 or 150. On the other hand, when the buffer element 54 of Figure 1 is driven by a current on line 34 to the "0" state, the voltage pulse across winding 106 of Figure 1 generates a current which passes through the rectifier 160 in its direction of low impedance and so is limited only by resistor 162. This additional loading requires a substantial increase in the power output of tube 10. If the additional power required is too large for a particular application, a second rectifier 164 may be included in series opposition with rectifier 160 in the leads between winding 106 on the buffer element and winding 70 on the readout element as indicated in Figure 4 which is a fragmentary modification of the circuit of Figure 1. Rectifier 164 is then enabled for reverse current flow by advance current pulses flowing through winding 62 in a manner similar to rectifier 154 of Figure 3. However, since there is no advance pulse flowing in winding 106 at the time core 50 is read out, diode 164 appears to be "disabled"; thus the readout from core 54 is destructive. In certain applications where a reduction in the loading of the storage (or buffer) core is important, this alternative form of circuit (Fig. 4) may be useful.

It will be appreciated that numerous modifications could be made in the circuits used to illustrate this invention and various other embodiments thereof could be designed by one skilled in the art without departing from the scope of the invention. Therefore, it is intended that the matter contained in the foregoing description and illustrated by the appurtenant drawings be considered as illustrative and not limitative, the scope of the invention being defined by the appended claims.

We claim:

1. Apparatus for reading without destroying the state of a bistable saturable core element operable alternately between two states in response to succeeding input signals comprising bistable saturable core buffer means coupled with said core element in such a manner that said input signals cause correspondence in the states of the buffer means and said core element, said buffer means having input means for receiving advance signals which when applied allow an output from the buffer means which is indicative of the state thereof, and readout means including output winding means associated with said buffer means for reading the output from the buffer means, said output being ineffective to change the state of said saturable core element.

2. Apparatus as in claim 1 wherein said readout means includes two opposing unidirectional current conducting devices, one of said devices being biased for reverse current flow to pass said output during the time when an advance signal is applied.

3. Apparatus as in claim 2 wherein said one unidirectional device is connected with the advance signal input means for biasing of said one device by an advance signal.

4. Apparatus as in claim 1 wherein said readout means includes bistable readout saturable core means and coupling means including unidirectional means for coupling said output winding means to the readout core means, the arrangement being such that said output from the buffer means permits a readout from the readout core means, said readout being indicative of the state of said core element and operating in effect at least on said buffer means to maintain correspondence of states between said core element and the buffer means.

5. Apparatus as in claim 4 wherein said readout saturable core means includes a saturable magnetic core having a biasing winding for receiving controllable bias which upon increase after a reduction thereof during the application of an advance signal provides said readout.

6. Apparatus as in claim 4 wherein said unidirectional

means includes a single unidirectional current conducting device.

7. Apparatus as in claim 4 wherein said unidirectional means includes two opposing unidirectional current conducting devices, one of which is biased for reverse current flow to pass said output from the buffer means during the time when an advance signal is applied.

8. Apparatus as in claim 7 wherein said one unidirectional device is connected to the advance signal input means for biasing of said one device by an advance signal.

9. Apparatus for reading without destroying the state of a bistable saturable core element having two input circuit means each including a unidirectional current path, comprising bistable saturable core buffer means coupled with said core element in said unidirectional paths so that succeeding input signals delivered to said two input circuit means cause correspondence in the states of the buffer means and said core element, said buffer means having input means for receiving advance signals which when applied allow an output from the buffer means, said output being indicative of the state of the buffer means, and readout means including output winding means associated with said buffer means for reading the output of the buffer means while said unidirectional paths prevent said reading from changing the state of the saturable core element.

10. A bistable saturable core binary counting element comprising said bistable saturable core having at least first, second, third, and fourth windings, two circuit paths each including a unidirectional current conducting device and said first and fourth windings, respectively, an inductive impedance coupling said second winding with the unidirectional device associated with said fourth winding, the first and second windings being further coupled to receive input signals one of which operates via said first and second windings to shift said counting element to a first state and a successive one of which operates via said second and fourth windings to shift the counting element to a second state, the arrangement being such that said third and fourth windings provide outputs for every second input signal.

11. Apparatus for reading in parallel without destroying the contents of a counter, said counter including a plurality of bistable saturable core elements connected in cascade by associated circuitry so that each element provides an output signal for every second input signal applied at its input, each of said core elements comprising a stage of the counter, the output signal of any one stage being the input signal of the succeeding stage, each stage further including bistable saturable core buffer means coupled with its associated core element in such a manner that the input signals thereto cause correspondence in the stable states of the respective buffer means and core elements, each of said buffer means having input means for receiving advance signals which when applied allow outputs from the buffer means indicative respectively of the stable state thereof, and readout means for each stage including output winding means associated with each buffer means for reading simultaneously the respective outputs from the buffer means, said outputs being ineffective to change the states of the core elements.

12. Apparatus for reading without destroying the state of a bistable saturable core counting element in a stage of a multi-stage saturable core signal counter, comprising said saturable core counting element with first and second input means, each of which includes unidirectional circuit means, said counting element being operable between first and second flux states in response to successive countable signals effectively received alternately by said first and second input means respectively, said second input means partially forming also output means for providing an output signal to be counted by a succeeding stage when a countable signal passes through said second input means and shifts the counting element to its sec-

ond state, and bistable saturable core buffer means having read-out means associated therewith, said buffer means being shiftable between first and second states and having first, second and third inputs and an output, the first and second inputs being coupled respectively into the unidirectional circuits of said first and second input means of the counting element so that said successive countable signals shift the buffer means between two states in correspondence with the state of the counting element, said third input being adapted to receive advance signals which when applied are interleaved in time with the countable signals, the arrangements being such that to provide readout, an advance signal is applied to produce an output from the buffer means through said readout means for reading the indication of the state of the buffer means and of the counting element, the readout being ineffective to change the state of the counting element because of said unidirectional circuit means.

13. Apparatus as in claim 12 wherein said readout means includes two unidirectional current conducting devices connected in series opposition with the output of said buffer means, one of said devices being biased for reverse current flow to pass the buffer means output during the time when an advance signal is applied.

14. Apparatus as in claim 13 wherein said one unidirectional device is connected with the third input of the buffer means for biasing of said one device by an advance signal.

15. Apparatus as in claim 12 wherein said readout means includes a bistable readout saturable core having an output, a first input for receiving controllable bias, a second input and unidirectional means coupling the output of said buffer means to the second input of the readout means, the arrangement being such that an application of an advance signal permits a readout from the output of said readout means during an increase of the bias at said first input following a reduction thereof during an advance signal application, said readout then allowing the state of the buffer means to correspond to the state of said counting element.

16. Apparatus as in claim 15 wherein said unidirectional means includes two opposing unidirectional current conducting devices, one of which is biased for reverse current flow to pass the buffer means output during the time when an advance signal is applied.

17. Apparatus as in claim 16 wherein said one unidirectional device is connected with the third input of the buffer means for biasing of said one device by said advance signals.

18. Apparatus for reading without destroying the state of a bistable saturable core counting element in a stage of a multi-stage saturable core signal counter, comprising said saturable core counting element having at least first, second, third, and fourth windings, two circuit paths each including a unidirectional current conducting device and said first and fourth windings respectively, the second winding being coupled to the fourth winding by its associated unidirectional device, first and second windings being further coupled to receive input signals, one of which operates via said first and second windings to shift said counting element to a first state and a successive one of which operates via said second and fourth windings to shift the counting element to a second state for supplying input signals from said fourth winding to a homologue of said first winding in a succeeding stage, said third winding operating by transformer action with the fourth winding to supply like input signals for a homologue of said second winding in said succeeding stage, and a bistable saturable core buffer element having first and fourth windings connected in said circuit paths respectively with the first and fourth windings of said counting element so that the state of the buffer element shifts with the state of the counting element and corresponds thereto, and readout means including an output winding on said buffer element for reading the state

of said counting element, said buffer element further including an advance winding for receiving advance pulses which when applied provide a binary output for said readout means while said unidirectional devices prevent an applied advance pulse from inducing a change of state in said counting element.

19. Apparatus as in claim 18 further including an inductive impedance in circuit between said second winding of the counting element and its associated unidirectional device.

20. Apparatus as in claim 18 wherein said readout means includes two opposing unidirectional current conducting devices connected in series with said output winding, one of said devices being biased for reverse current flow to pass said buffer element output during the time when an advance signal is applied.

21. Apparatus as in claim 20, wherein said one unidirectional device is connected with said advance winding for biasing of said one device by an advance pulse.

22. Apparatus as in claim 18, wherein said readout means includes a bistable readout saturable core element having an output winding and a unidirectional element in circuit therewith, a first input winding, coupling means including unidirectional means for coupling the first input winding to said output winding of the buffer element, and a second input winding for receiving controlled bias, the arrangement being such that said output from the buffer element permits a readout from the readout output winding, said readout being indicative of the state of the counting element and operating in effect at least on said buffer element to maintain correspondence of states between said counting element and the buffer element following the application of an advance pulse.

23. Apparatus as in claim 22 wherein said unidirectional means includes a single unidirectional current conducting device.

24. Apparatus as in claim 22, wherein said unidirectional means includes two opposing unidirectional current conducting devices connected in series with said output winding on the buffer element, one of said devices being biased for reverse current flow to pass said buffer element output during the time when an advance signal is applied.

25. Apparatus as in claim 24, wherein said one unidirectional device is connected with said advance winding for biasing of said one device by an advance pulse.

26. In apparatus for reading without destroying the binary contents of at least one stage of a multi-stage signal counter having a bistable saturable core counting element in each stage, bistable saturable core buffer means having first and second input means unidirectionally associated respectively with first and second input means of said saturable counting element, the first and second input means of the counting element being adapted to receive alternately, in effect, the signals to be counted, the counting element and the saturable buffer means being shiftable between first and second states in response to signals at the first and second input means of the counting element, respectively, said buffer means having further a third input means for receiving advance signals which cause said buffer means to be in its second state and output means for providing an output signal from the buffer means upon receipt of an advance signal if the core means was then in said first state, bistable readout saturable core means having an output and two inputs, one of which is coupled to the output means of the buffer means, the other readout input being controllably biased by a normal biasing signal large enough to counteract said output signal from the buffer means, the arrangement being such that to provide readout, the normal biasing signal is reduced while an advance signal is applied to provide an output signal if the buffer means changes its state thereby, following which the resumption of at least said normal biasing signal at the readout

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means causes a readout output indicative of the state of the buffer means, said buffer means being then returned, if necessary, to correspond in state to the state of the counting element by an input from the readout means to said output means of the buffer means.

27. Apparatus as in claim 26, wherein said one input of the readout core means is coupled to the output means of the buffer means by two opposing unidirectional current conducting devices, one of said devices being biased

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for reverse current flow to pass said buffer output signal during the time when an advance signal is applied.

28. Apparatus as in claim 27, wherein said one unidirectional device is connected with the third input means of the buffer means for biasing of said one device by an advance signal.

No references cited.