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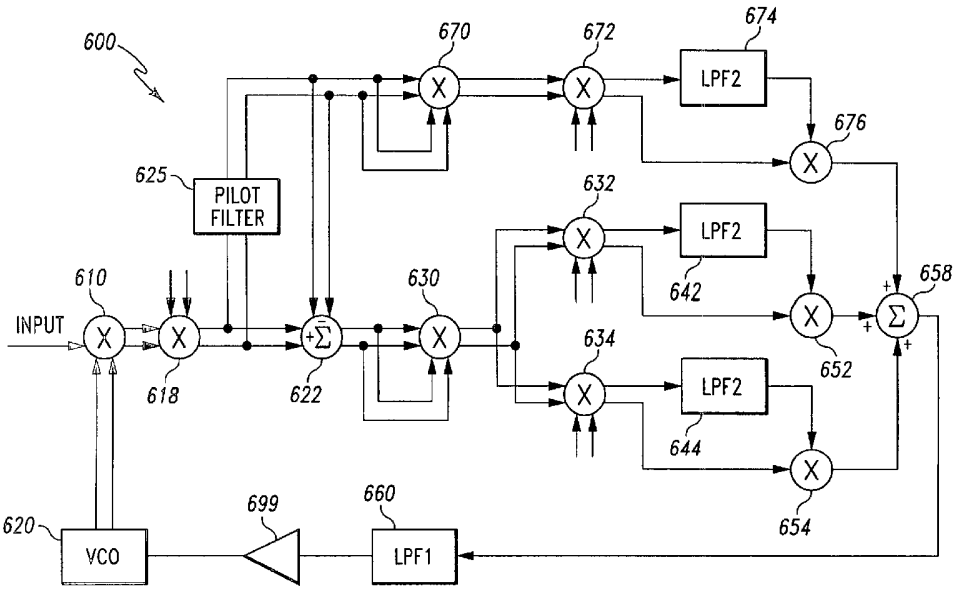
(54) Title: DATA-DIRECTED FREQUENCY-AND-PHASE LOCK LOOP FOR DECODING AN OFFSET-QAM MODULATED SIGNAL HAVING A PILOT



(57) Abstract: A data-and-pilot directed frequency-and-phase lock loop for an offset-QAM modulated signal having a pilot signal comprises a pilot acquisition loop and a pair of data-directed acquisition loops. The pilot is extracted from the main signal by a pilot filter, then used both by the pilot acquisition loop and to remove the pilot from the signal to the data-directed acquisition loops. The outputs of the pilot and the two data-directed acquisition loops are summed and returned to the VCO to complete the feedback loop.

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DATA-DIRECTED FREQUENCY-AND-PHASE LOCK LOOP FOR DECODING AN OFFSET-QAM MODULATED SIGNAL HAVING A PILOT

CLAIM OF PRIORITY

This utility patent application claims priority to U.S. Provisional Patent Applications Nos. 60/370,295, 60/370,283, and 60/370,296, the entire specifications of which are hereby incorporated herein.

BACKGROUND

In order to provide the widest possible coverage for a digital transmission, such as for cell phones or a digital television broadcast, it's desirable to use multiple transmitters that are separated from each other spatially. This permits a wider area to be covered, uses less total broadcast power, and can help to fill in dark areas where the transmission from one transmitter may be blocked. Thus, using multiple transmitters can provide wider and more complete coverage for virtually any digital transmission.

However, using multiple transmitters creates a serious problem when the receiver is at a "seam" between two transmitters, because the additional signal can appear as a "ghost" that can be as large as the "main" signal. Furthermore, destructive interference creates a series of perfect or near perfect nulls.

Existing receiver technology handles ghosts by filtering them out in order to interpret the "main" signal. But in a multi-transmitter environment this strategy is unworkable. It makes little sense to design a system to filter out a ghost that can be an arbitrarily large fraction of the "main" signal's size. Furthermore, near the margins the best this subtractive strategy can ever provide is a signal strength equal to the stronger transmitter's signal—the energy from the secondary signal is wasted.

Even when the ghosts are smaller than 100% of the "main" signal, there is an equal probability of pre- and post- ghosts. In the most common situation, the strongest signal is the one following the most direct path. Ghosts are most often produced by "multipathing," that is, by portions of the signal following paths of

different lengths from the transmitter to the receiver. Thus, ghosts are typically produced by one or more strong reflections. The first signal to arrive is typically the most direct, and therefore the strongest, and so in the usual situation the ghost is a post-ghost. In a multi-transmitter environment, though, while the receiver is near a seam the stronger signal can easily arrive after the ghost. With signals arriving from two directions, it is possible that the more direct path may be the longer one. Consequently, pre-ghosts are about as likely as post-ghosts, and may be arbitrarily strong. Furthermore, if the transmitters are out of sync with each other by even a small amount, where the one lagging happens to be the closer one the receiver will likely see pre-ghosts.

Existing technology relies on the assumption that post-ghosts predominate (i.e., existing systems are not generally designed to deal with Raleigh fading). Thus, existing receivers generally will be either inefficient or incapable of dealing with a multi-transmitter environment, even if the ghosts are sufficiently small compared to the "main" signal.

In short, in a multi-transmitter environment, the "main" signal becomes a meaningless concept at the seams of the transmission. In order to operate efficiently in a multi-transmitter environment, a digital receiver must operate with a different paradigm. What is needed is a digital receiver that employs an additive strategy—that is, one in which the energy from one or more relatively large ghosts can be captured and used to aid in the synchronization process, rather than filtered out and discarded. Such a receiver could both function with ghosts 100% of the size of the "main" signal, and provides substantially superior performance whenever ghosts exceed about 70% of the size of the "main" signal. Since this condition can often occur even in a single-transmitter environment having a large number of reflective surfaces and masking objects, such a receiver would also provide greatly improved reception in, for example, urban environments.

In the typical transmitter-receiver system, from the receiver's perspective most of the signal is useless for synchronization, because it is indistinguishable from white noise. The more information that is packed into a signal, the more closely it will resemble white noise, so this is both a desirable and inevitable feature of the signal. Nevertheless, some bandwidth must be "wasted" in order to

provide the receiver a means to orient itself. Typically, one of two strategies is employed. In some systems, a pilot signal is included. This is a sharp peak of energy in a very narrow frequency band, which is very easy for the receiver to pick out.

A phase-lock loop, such as the one shown in Figure 1, indicated generally at 100, is a typical way to synch up a receiver using a pilot. A multiplier 110 multiplies the signal and the output of a voltage controlled oscillator 120 ("VCO") to produce a beat note (a sine wave with a frequency equal to the difference between the frequency of the pilot signal and the VCO's output). The beat note passes through a low-pass filter 130. The output of the filter 130 is amplified at 199and input to the VCO 120 to complete the feedback loop. Those skilled in the art will appreciate that the low-pass filter 130 has competing design parameters. The more narrow the band pass of the filter 130 the smaller the response, so the slower the loop 100 is to lock up. However, a wide pass filter passes more noise and makes it harder for the loop 100 to capture at all.

It will be appreciated that the response of the loop 100 is driven by the frequency difference output of the first multiplier 110. The direction of error can only be determined by observing the slope of the time rate-of-change of the output. The second filter 130 distorts the sine wave, increasing the amplitude on the closer side, and decreasing it on the further side. Convergence is driven by this asymmetry of the distorted beat note.

However, because the amplitude of the beat note drops with increasing frequency difference, that distortion output drops as well, so the response of the phase-lock loop 100 decreases as the frequency of the VCO 120 diverges from the signal frequency. Thus, unless the signal happens to be close to the initial VCO 120 frequency, it will converge slowly, or not at all. A typical phase lock loop can capture when the initial VCO 120 frequency is within a factor of about 3-10 times the bandwidth of the loop.

Another, more robust, strategy for synching is to provide a signal in which information in the data is redundant in the frequency domain. The receiver can look for a correlation in the data created by this repetition to synch up. The receiver could use this same technique to find correlations in the data from signals

from multiple transmitters. In mathematical terms, the correlation between the repeated signal portion can be identified by fully complex convolution. Convolution inherently corrects for the asymmetry produced by the slope of the Nyquist band, so that the peak value occurs when the limits of integration exactly correspond to the beginning and the end of the repeated data segment (and it's negative time image).

A typical existing means for performing such a convolution is the Costas Loop, shown in Figure 2. The Costas Loop operates on a complex signal, such as a QAM signal. As with the phase-lock loop, a first multiplier 210 multiplies the signal with the output of a VCO 220, though, as shown in Figure 2, this is a complex multiplication, which produces both an I' (in phase) and a Q' (quadrature) output. As with the phase-lock loop, the output of the first multiplier is passed through a low-pass filter 230 where the unwanted (frequency sum) portion of multiplied signal is removed. The in-phase and quadrature portions are then multiplied by a second multiplier 240 to produce a beat note (assuming the sideband isn't balanced—otherwise it's merely a DC voltage.) The beat note is passed through a second low-pass filter 250, then amplified at 299 and returned to the VCO 220 to complete the feedback loop. Thus, the portion of the Costas loop following the second multiplier 240, which drives the convergence of the loop, is basically a phase-lock loop. Consequently, like the phase-lock loop, the Costas loop has the disadvantage of slow convergence.

A frequency-and-phase-lock loop ("FPLL") (shown in Figure 3, and described in U.S. Patent No. 4,072,909 to Citta, which is hereby incorporated by reference in its entirety) provides faster convergence. The FPLL has a first low-pass filter 330 and a second low-pass filter 350 which perform the function of the second low-pass filter 250 in the Costas loop, which separate the averaging and noise-elimination functions. Thus, the first low-pass filter 330 can have a relatively wide band pass, so that the FPLL can acquire even when the signal and initial VCO frequencies are off by as much as a factor of 1000. The second low-pass filter 350 can have a relatively narrow band-pass, in order to give good averaging during lock-up. The output of the second multiplier 340 is a rectified sine wave with a DC offset. The DC offset provides the direction information,

rather than an integration of a distorted sine wave, which provides a much stronger response when the frequency difference is relatively large. The output of the second filter 350 is amplified at 399 and returned to the VCO 320 to complete the feedback loop.

Because of the way the FPLL uses the complex information to provide both magnitude and direction information, it locks up faster, and phase noise that is less than 90 degrees out of phase doesn't disrupt the lock. However, the FPLL does not perform a convolution of the data, and is therefore dependent upon a pilot to operate. It is therefore not suitable for use with, for example, a double sideband suppressed signal.

A data-directed frequency acquisition loop ("DDFL"), as disclosed in the concurrently-filed application, entitled Data-Directed Frequency Acquisition Loop, which is hereby incorporated in its entirety, and shown in Figure 4, provides a data-synch loop which combines the desired features of the Costas Loop—synching by finding a correlation in repeated data through convolution—with the desired faster convergence of a frequency-and-phase-lock loop. The DDFL is indicated generally at 400. A first multiplier 410 multiplies the input signal by the output of a VCO 420. The output of the first multiplier 410 is filtered by a first low-pass filter 415, and the filtered output is squared by a second multiplier 430. The in-phase component is filtered by a second low-pass filter 440, then multiplied by the quadrature component by a third multiplier 450. The output of the third multiplier 450 is filtered by a third low-pass filter 460, amplified at 499, and returned to the VCO 420 to complete the feedback loop.

A data-directed frequency-and-phase lock loop ("DDFPLL"), as disclosed in the concurrently-filed application, entitled Data-Directed Frequency-and-Phase Lock Loop, which is hereby incorporated in its entirety, and is shown in Figure 5 and indicated generally at 500, provides a data-synch loop that is even more robust than the DDFL.

As previously discussed, ghosting can create a series of perfect or near perfect nulls in the signal, especially in urban environments, which contain numerous reflective surfaces. Although the DDFL and DDFPLL provide robust mechanisms for synching a receiver, it is possible for a ghosts to destroy the

portions of the signal containing the repeated data in the Nyquist slope. It will be appreciated that a pilot signal is an odd function, while redundant information in a Nyquist band is an even function. Therefore, it is impossible for any single ghost to annihilate both a pilot signal and the redundancy in the data. Therefore, with a system which can synch by either a pilot signal or redundancy in the data, the minimum arrangement of ghosts necessary to defeat lock-up requires an additional ghost.

Thus, what is needed is a system and method for synching a digital receiver by locking onto either a pilot signal or redundancy in the Nyquist slopes, in response to channel distortion that prevents acquisition by the other. The present invention is directed towards this need, among others.

SUMMARY OF THE INVENTION

A first embodiment data-and-pilot directed frequency-and-phase lock loop according to the present invention comprises: a signal input; a VCO; a first through tenth multipliers, a narrow band-pass filter; a first through forth low-pass filters; and a first and second summers. The VCO has an in-phase and quadrature output. The first multiplier has as input the signal input and the in-phase and quadrature outputs of the VCO. The first multiplier further has a first output. The second multiplier has as input the first output, the second multiplier further having a second output. The narrow band-pass filter has as input the second output. The narrow band-pass filter further has a third output. The third multiplier has as input the third output. The third multiplier further has a fourth output that is a convolution of the third output. The fourth multiplier has as input the fourth output. The fourth multiplier further has a fifth output. The first low-pass filter has as input an in-phase component of the fifth output. The first low-pass filter further has a first filtered output. The fifth multiplier has as input the first filtered output and a quadrature component of the fifth output. The fifth multiplier further has a sixth output. The first summer has as input the second output and the third output. The first summer further has a seventh output that is a difference between the second output and the third output. The sixth multiplier has as input the seventh output, the sixth multiplier further has an eighth output that is a convolution of the seventh output. The seventh and eighth multipliers have as input the eighth output. The seventh and eighth multipliers further have a ninth and tenth output, respectively. The second and third low pass filters have as input in-phase portions of the ninth and tenth outputs, respectively. The second and third low pass filters have a second and third filtered output, respectively. The ninth and tenth multiplier have as inputs the second and third filtered outputs, respectively, and quadrature portions of the ninth and tenth outputs, respectively. The ninth and tenth multipliers further have an eleventh and twelfth outputs, respectively. The second summer has as input the sixth, eleventh, and twelfth outputs. The second summer further has a thirteenth output. The fourth low-pass filter has as input the

thirteenth output. The fourth low-pass filter further has a fourteenth output. The fourteenth output is returned to the VCO to complete a feedback loop.

A second embodiment data-and-pilot directed frequency-and-phase lock loop according to the present invention comprises a signal input, a VCO, a first through fifth multipliers; a narrow band-pass filter; a first through third low-pass filters; and a first and second summers. The VCO has an in-phase and quadrature output. The first multiplier has as input the signal input and the in-phase and quadrature outputs of the VCO. The first multiplier further has a first output. The narrow band-pass filter has as input the first output. The narrow band-pass filter further has a second output. The second multiplier has as input the second output. The second multiplier further has a third output that is a convolution of the second output. The first low-pass filter has as input an in-phase component of the third output. The first low-pass filter further has a first filtered output. The third multiplier has as input the first filtered output and a quadrature component of the third output. The third multiplier further has a fourth output. The first summer has as input the first output and the second output. The first summer further has a fifth output that is a difference between the first output and the second output. The fourth multiplier has as input the fifth output. The fourth multiplier further has an sixth output that is a convolution of the fifth output. The second low pass filter has as input in-phase portion of the fifth output. The second low pass filter has a second filtered output. The fifth multiplier has as inputs the second filtered output and a quadrature portion of the fifth output. The fifth multiplier further has an sixth output. The second summer has as input the fourth and sixth outputs. The second summer further has a seventh output. The third low-pass filter has as input the seventh output. The third low-pass filter further has an eighth output. The eighth output is returned to the VCO to complete a feedback loop.

A third embodiment data-and-pilot directed frequency-and-phase lock loop according to the present invention comprises a pilot directed acquisition loop and a data-directed phase-lock loop. The pilot-directed acquisition loop has a pilot input and a pilot output. The data-directed phase-lock loop has a data input and a data output. The pilot output and the data output are used to produce a feedback signal that is a non-linear combination of the pilot input and the data input.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a prior art phase lock loop.

Figure 2 is a prior art Costas loop.

Figure 3 is a prior art frequency-and-phase-lock loop.

Figure 4 is data-directed frequency-acquisition loop.

Figure 5 is a data-directed frequency-and-phase lock loop.

Figure 6 is a data-and-pilot directed frequency-and-phase lock loop according to the present invention.

Figure 7 is a graph showing the magnitude of the individual correlation signals of the pilot detector and the data detector in a data-and-pilot directed frequency-and-phase lock loop according to the present invention.

Figure 8 is a graph of the in-phase and quadrature components of the correlation in a pilot detector and in a data detector, respectively, of a data-and-pilot directed frequency-and-phase lock loop according to the present invention.

Figure 9 shows an alternative embodiment data-and-pilot directed frequency-and-phase lock loop according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

For the purposes of promoting an understanding of the principles of the invention, reference will now be made to the embodiment illustrated in the drawings and specific language will be used to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended, and alterations and modifications in the illustrated device, and further applications of the principles of the invention as illustrated therein, are herein contemplated as would normally occur to one skilled in the art to which the invention relates.

A data-and-pilot directed frequency-and-phase lock loop ("DPDFPLL") according to the present invention provides extremely robust acquisition, even in the face of the worst receiving environments, including urban environments with multiple ghosts and perfect nulls. Furthermore, the DPDFPLL provides a robust, continuous control signal, even when confronted with a perfect null, regardless of its phase. The DPDFPLL operates by simultaneously using a pilot signal and signal redundancy in both Nyquist slopes in an offset-QAM signal. As with the DDFL and DDFPLL, during lock-up the DPDFPLL combines desirable features of a Costas loop and a frequency-and-phase-lock loop; the DDFPLL synchs using redundancy of the data in the frequency domain, such as in a double sideband suppressed signal, but has an output that converges like the FPLL, and that is not disrupted by noise that displaces the signal phase by 90 degrees or less. Additionally, the DPDFPLL comprises a loop that synchs using a pilot signal. Together, these loops produce a circuit that provides uniquely robust frequency acquisition and phase-lock.

A preferred embodiment DPDFPLL according to the present invention is shown in Figure 6, and indicated generally at 600. The input signal and the output of a VCO 620 are multiplied by a first multiplier 610. The output of the first multiplier 610 is multiplied with a fixed frequency by a second multiplier 618. In the preferred embodiment this frequency is ¼ of the symbol rate, since this requires multiplication only by 1 and –1, and because it provides the maximum

separation of the correlations of the two Nyquist slopes, but it will be appreciated that any frequency can theoretically be used.

The output of the second multiplier 618 is sent both to a first summer 622, and to a pilot filter 625. The pilot filter 625 is a narrow band-pass filter centered about the frequency where the pilot signal is expected. The output of the pilot filter 625 is then used both in a pilot acquisition loop, as described further hereinbelow, and also to remove the pilot from the signal used in two data-directed acquisition loops, as described further hereinbelow.

The output of the pilot filter 625 is used in a pilot acquisition loops as follows: The pilot signal is convolved by a third multiplier 670. The output of the third multiplier 670 is shifted by a fourth frequency-shift multiplier 672. The fourth frequency-shift multiplier 672 reverses the effect of the second frequency-shift multiplier 618. As will be apparent to those skilled in the art, in the preferred embodiment the fourth frequency-shift multiplier multiplies by ¾ of the symbol rate, in order to reverse the multiplication by ¼ of the symbol rate performed by the first multiplier 610. It will be appreciated that the function of the second frequency-shift multiplier 618 is to permit the pair of data-directed acquisition loops to simultaneously find the correlations in the data in the two Nyquist slopes by offsetting their respective power spectra so they are not centered at the same origin. Thus, the second and fourth frequency-shift multipliers 618 and 672 are not needed for the operation of the pilot acquisition loop by itself, but to permit it to function in conjunction with the two data-directed acquisition loops.

The in-phase output of the fourth multiplier 672 is then filtered by a low-pass filter and then multiplied with the quadrature output by a fifth multiplier 676, as in a typical frequency-and-phase lock loop. The output of the fifth multiplier 676 is then sent to a second summer 658, where it is summed with the outputs of the pair of data-directed acquisition loops, as described hereinbelow.

The output of the pilot filter 625 is used in a pair of data-directed acquisition loops as follows: The output of the pilot filter 625 subtracted from the output of the second multiplier 618 by the first summer 622. The resulting signal is convolved by a sixth multiplier 630. The output of the sixth multiplier 630 is used to synch up through a pair of frequency acquisition loops. The signal is sent

to a seventh frequency-shift multiplier 632 and an eighth frequency-shift multiplier 634. In the preferred embodiment the frequency-shifts generated by these multipliers are ¼ and ¾ of the symbol rate, but it will be appreciated that this is a function of the frequency shift imposed by the second multiplier 618. (The difference between the seventh and eighth frequency-shift multipliers' 632 and 634 will always be ½ a cycle.) The in-phase portions of the outputs of the frequency-shift multipliers 632 and 634 are filtered by low pass filters 642 and 644, and then multiplied by the corresponding quadrature portion of the outputs of the phase-shift multipliers 632 and 634 by a ninth multiplier 652 and a tenth multiplier 654, respectively. The outputs of the ninth and tenth multipliers 652 and 654 are summed by the second summer 658.

The output of the second summer 658 is filtered by a third low-pass filter 660, amplified at 699, and returned to the VCO 620 to complete the feedback loop.

It will be appreciated that the data-and-pilot frequency-and-phase lock loop 600 comprises a DDFPL, similar to the one shown in Figure 5, combined with a pilot-directed frequency acquisition loop. The pilot-directed frequency acquisition loop comprises the complex multiplier 670, frequency-shift multiplier 672, low-pass filter 674, and multiplier 676. The frequency-shift multiplier 672 is added to a typical prior art pilot-directed acquisition loop in order effectively to combine it with the data-directed loop, as described hereinabove.

Figures 7 and 8 illustrate an important advantage of combining a data-directed phase-lock loop with a pilot-directed acquisition loop. Figure 7 is a graph showing the magnitude of the individual correlation signals of the pilot detector and the data detector in the circuit 600 as a function of the phase of a perfect null ghost as it travels through a complete cycle (i.e., the magnitude of the signals being input to the adder 658 from the pilot-directed loop and the from the data-directed loop, respectively). The curve 710 is the magnitude of the correlation signal of the data detector, and the curve 720 is the magnitude of the pilot detector. When the perfect null is perfectly aligned with the pilot, the pilot is annihilated, and the pilot detector provides no feedback signal. Likewise, when the perfect null is properly aligned, the data detector is zeroed. The remarkable robustness of the data-and-pilot directed frequency-and-phase lock loop derives in part from the fact that these

zeros do not line up—whenever the pilot detector is zeroed, the data detector has a good response, and vise versa. Consequently, it is absolutely impossible for any single ghost to completely zero both the pilot detection and the data detection.

Figure 8 illustrates the principle that permits the pilot-directed loop and the data-directed loop effectively to be combined. Figure 8 is a graph of the in-phase and quadrature components of the correlation in the pilot detector 810 and in the data detector 820, respectively (i.e. the inputs to the multiplier 676 and to the multipliers 652 and 654, respectively). Through the first quarter of a cycle (points A through E) the outputs of the pilot detector and data detector could simply be summed. That is, the in-phase and quadrature components of the outputs of the correlators 670 and 630 could be added, and then multiplied by a single multiplier. But the data detector passes through a null at point E, and thereafter reverses sign. Between point E and point G the sum would still drive convergence, but more weakly than the pilot detector alone would. At point G the pilot detector and data detector would be exactly canceling each other, producing a null. Past point G the sum would actually be driving away from a lock.

However, by combining the pilot detector and the data detector non-linearly a phase-lock signal can be produced that has no nulls. This is possible because, as shown in Figure 8, the phase relationship between the pilot detector's signal and the data detector's signal are always either the same, or exactly 180° out from each other. Thus, if the data detector's signal is inverted during the portions of a cycle in which they are 180° out, the result is a smooth signal with no nulls. This is exactly what a DDFPL does, as discussed in the concurrently filed application entitled Data-Directed Frequency-and-Phase Lock Loop. Thus, the output of a DDFPL can be combined directly with the output of a pilot-directed phase-lock loop, as is done in the preferred embodiment of by the adder 658.

It will be appreciated that other non-linear ways to combine the output of a pilot detector and a data detector may also be used. For example, a multiplier could be used to directly invert the in-phase portion of the data detector's signal during the appropriate half-phase. This configuration would actually require slightly less hardware than the preferred embodiment (one less multiplier), but this embodiment converges less efficiently.

It will be appreciated that, though the pilot signal is typically located in the lower Nyquist band in an offset-QAM signal, it could also be positioned in the upper Nyquist band. In this case the frequency shift multiplier should be reversed, so that the first multiplier 610 multiplies by ¾ of the symbol rate, and the fourth multiplier 618 multiplies by ¼ of the symbol rate.

It will likewise be appreciated that the circuit 600 can be adapted for use with a QAM signal, in which the pilot is centered. In this case, there is no need for any of the frequency-shift multipliers (including the seventh frequency-shift multiplier 632, discussed further hereinbelow), nor for the low-pass filter 642 and ninth multiplier 652, since the pilot and the data would already be separated.

Those skilled in the art will also appreciate that other pilot-based phase-lock loops and data-directed phase-lock loops can be combined to produce a data-and-pilot directed frequency-and-phase lock loop according to the present invention. For example, Figure 9 shows an alternative embodiment DPDFPLL circuit 900 according to the present invention with somewhat simpler hardware than the preferred embodiment circuit 600, in which corresponding elements have been numbered correspondingly (so the VCO 620 in the circuit 600 is numbered 920 in the circuit 900). The circuit 900 comprises a DDFL similar to the one shown in Figure 4 (comprising the complex multiplier 930, low pass filter 942, and multiplier 952), combined with a pilot acquisition loop (comprising the complex multiplier 970, low-pass filter 974, and multiplier 976). The DDFL has the same characteristic as does the DDFPL in the preferred embodiment, of inverting the output (relative to, for example, a Costas loop) during half of a cycle, so that it functions in a circuit according to the present invention analogously to the DDFPL used in the preferred embodiment. It will be appreciated that the DDFL and the pilot acquisition loop in the circuit 900 have identical hardware configurations; the difference in their inputs is the only thing that distinguishes them.

Other alternative embodiments can likewise be formed by the non-linear combination of the correlation of a pilot signal and of a double-sideband suppressed data signal, as will be apparent to those skilled in the art.

Certain other alternative embodiments can be formed by the substitution, permutation, or both, of the elements of any of these embodiments. For example,

elements of the circuit 600 shown in Figure 6 can be substituted, permutated, or both, to produce a number of equivalent alternative embodiment circuits. In this example, it will be appreciated that the amplifier 699 may actually be incorporated into the filter 660. Those skilled in the art will recognize that filters typically include amplification to offset reductions in signal strength caused by the filtering. It will be appreciated that the amplification could equivalently be performed by a separate amplifier, either prior to or after filtration.

Furthermore, it will be appreciated that many of the multipliers can actually be substantially simpler hardware components. For example, the VCO can simply produce a signal of oscillating 1s and –1s. In this case, the potential multiplication required by the multipliers comprising the first complex multiplier 610 is limited to a change of signs. Similarly, the two of the real multipliers comprising the second multiplier 630 multiply the same input by itself. Thus, the range of possible outputs contains only half the possibilities of the domain of inputs. Consequently, this function can more easily be performed by a lookup table that provides the square of the input than by an actual multiplier, which requires many more gates. Other simplifications of the hardware are possible, and will be apparent to persons of ordinary skill in the art.

While the invention has been illustrated and described in detail in the drawings and foregoing description, the same is to be considered as illustrative and not restrictive in character, it being understood that only the preferred embodiment, and certain other embodiments deemed helpful in further explaining how to make or use the preferred embodiment, have been shown. All changes and modifications that come within the spirit of the invention are desired to be protected.

We Claim:

1. A data-and-pilot directed frequency-and-phase lock loop having a symbol rate, and comprising:

a signal input;

a VCO having an in-phase and a quadrature output;

a first multiplier having as input the signal input and the in-phase and quadrature outputs of the VCO, the first multiplier further having a first output;

a second multiplier having as input the first output, the second multiplier further having a second output;

a narrow band-pass filter having as input the second output, the narrow band-pass filter further having a third output;

a third multiplier having as input the third output, the third multiplier further having a fourth output that is a convolution of the third output;

a fourth multiplier having as input the fourth output, the fourth multiplier further having a fifth output;

a first low-pass filter having as input an in-phase component of the fifth output, the first low-pass filter further having a first filtered output;

a fifth multiplier having as input the first filtered output and a quadrature component of the fifth output, the fifth multiplier further having a sixth output;

a first summer having as input the second output and the third output, the first summer further having a seventh output that is a difference between the second output and the third output;

a sixth multiplier having as input the seventh output, the sixth multiplier further having an eighth output that is a convolution of the seventh output;

a seventh and eighth multipliers having as input the eighth output, the seventh and eighth multipliers further having a ninth and tenth output, respectively;

a second and third low pass filters having as input in-phase portions of the ninth and tenth outputs, respectively, the second and third low pass filters having a second and third filtered output, respectively;

a ninth and tenth multiplier having as inputs the second and third filtered outputs, respectively, and quadrature portions of the ninth and tenth outputs,

respectively, the ninth and tenth multipliers further having an eleventh and twelfth outputs, respectively;

a second summer having as input the sixth, eleventh, and twelfth outputs, the second summer further having a thirteenth output; and

a fourth low-pass filter having as input the thirteenth output, the fourth low-pass filter further having a fourteenth output;

wherein the fourteenth output is returned to the VCO to complete a feedback loop.

2. The data-and-pilot directed frequency-and-phase lock loop of Claim 1, wherein:

the second multiplier multiplies by ¼ the symbol rate;

the fourth multiplier multiplies by ¾ the symbol rate; and

the seventh and eighth multipliers multiply by ¼ and ¾ the symbol rate, respectively.

3. The data-and-pilot directed frequency-and-phase lock loop of Claim 1, wherein the seventh and eighth multipliers multiply by fixed frequencies having a difference of ½ the symbol rate.

4. The data-and-pilot directed frequency-and-phase lock loop of Claim 1, wherein the second and fourth multipliers multiply by fixed frequencies that add up to the symbol rate.

5. The data-and-pilot directed frequency-and-phase lock loop of Claim 1, wherein the second multiplier multiplies only by 1 and –1.

6. The data-and-pilot directed frequency-and-phase lock loop of Claim 1, wherein the narrow band-pass filter is centered about an expected pilot frequency.

7. A data-and-pilot directed frequency-and-phase lock loop, comprising:

a signal input;

a VCO having an in-phase and quadrature output;

a first multiplier having as input the signal input and the in-phase and quadrature outputs of the VCO, the first multiplier further having a first output;

a narrow band-pass filter having as input the first output, the narrow band-pass filter further having a second output;

a second multiplier having as input the second output, the second multiplier further having a third output that is a convolution of the second output;

a first low-pass filter having as input an in-phase component of the third output, the first low-pass filter further having a first filtered output;

a third multiplier having as input the first filtered output and a quadrature component of the third output, the third multiplier further having a fourth output;

a first summer having as input the first output and the second output, the first summer further having a fifth output that is a difference between the first output and the second output;

a fourth multiplier having as input the fifth output, the fourth multiplier further having an sixth output that is a convolution of the fifth output;

a second low pass filter having as input in-phase portion of the fifth output, the second low pass filter having a second filtered output;

a fifth multiplier having as inputs the second filtered output and a quadrature portion of the fifth output, the fifth multiplier further having an sixth output;

a second summer having as input the fourth and sixth outputs, the second summer further having a seventh output; and

a third low-pass filter having as input the seventh output, the third low-pass filter further having an eighth output;

wherein the eighth output is returned to the VCO to complete a feedback loop.

8 The data-and-pilot directed frequency-and-phase lock loop of Claim 7, wherein:

the second multiplier multiplies by ¼ the symbol rate;

the fourth multiplier multiplies by ¾ the symbol rate; and

the seventh and eighth multipliers multiply by ¼ and ¾ the symbol rate, respectively.

9 The data-and-pilot directed frequency-and-phase lock loop of Claim 7, wherein the seventh and eighth multipliers multiply by fixed frequencies having a difference of ½ the symbol rate.

10. The data-and-pilot directed frequency-and-phase lock loop of Claim 7, wherein the second and fourth multipliers multiply by fixed frequencies that add up to the symbol rate.

11. The data-and-pilot directed frequency-and-phase lock loop of Claim 7, wherein the second multiplier multiplies only by 1 and –1.

12. The data-and-pilot directed frequency-and-phase lock loop of Claim 7, wherein the narrow band-pass filter is centered about an expected pilot frequency.

13. A data-directed frequency-and-phase lock loop adapted to decode an offset-QAM modulated signal having a pilot.

14. A data-and-pilot directed frequency-and-phase lock loop, comprising:
a pilot-directed acquisition loop having a pilot input and a pilot output;
a data-directed phase-lock loop having a data input and a data output;
wherein the pilot output and the data output are used to produce a feedback signal that is a non-linear combination of the pilot input and the data input.

15. The data-and-pilot directed frequency-and-phase lock loop of Claim 14, wherein the data-directed phase-lock loop is a DDFL.

16. The data-and-pilot directed frequency-and-phase lock loop of Claim 14, wherein the data-directed phase-lock loop is a DDFPL.

17. The data-and-pilot directed frequency-and-phase lock loop of Claim 14, wherein the non-linear combination is performed by adding the pilot input and data input directly during a first half of each phase, and by inverting the in-phase portion of one of the pilot input and the data input and adding the result to the other of the pilot input and the data input during a second half of each phase.

18. The data-and-pilot directed frequency-and-phase lock loop of Claim 14, wherein the non-linear combination is performed by:

correlating the pilot input to produce a pilot correlation;

correlating the data input to produce a data correlation;

combining the pilot correlation and the data correlation.

19. The data-and-pilot directed frequency-and-phase lock loop of Claim 14, further comprising a plurality of frequency shift multipliers.

20. The data-and-pilot directed frequency-and-phase lock loop of Claim 19, wherein the plurality of frequency shift multipliers comprise a first multiplier and a second multiplier that multiply by fixed frequencies having a difference of ½ the symbol rate.

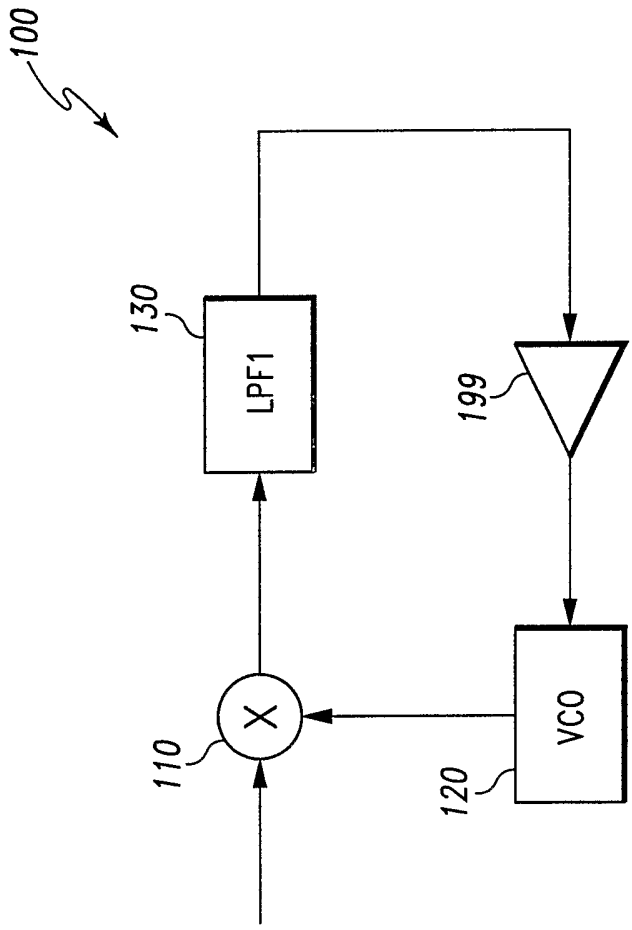

Fig. 1

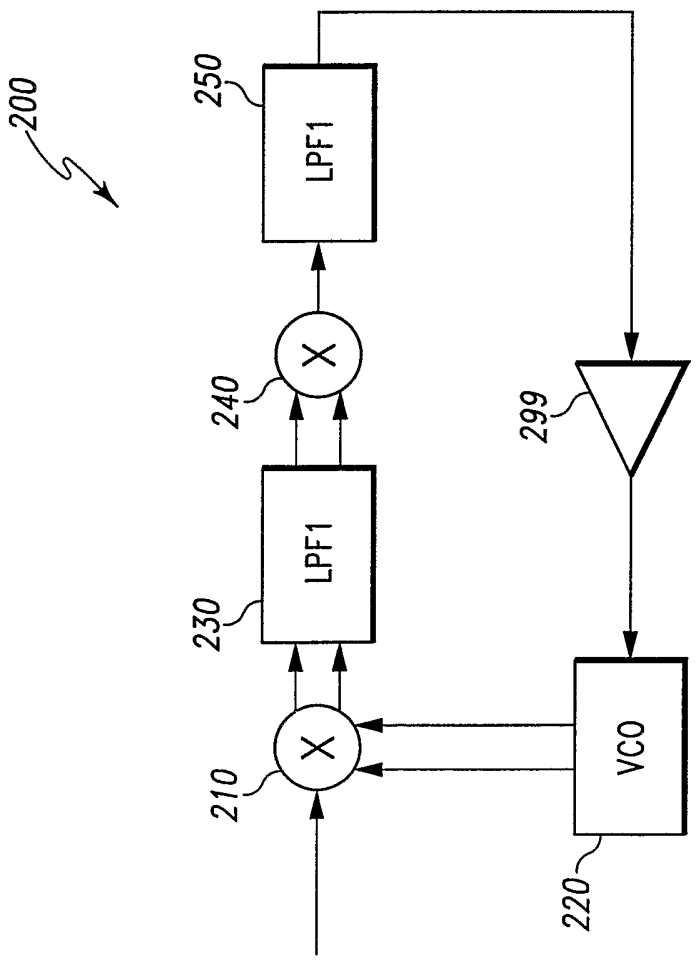

Fig. 2

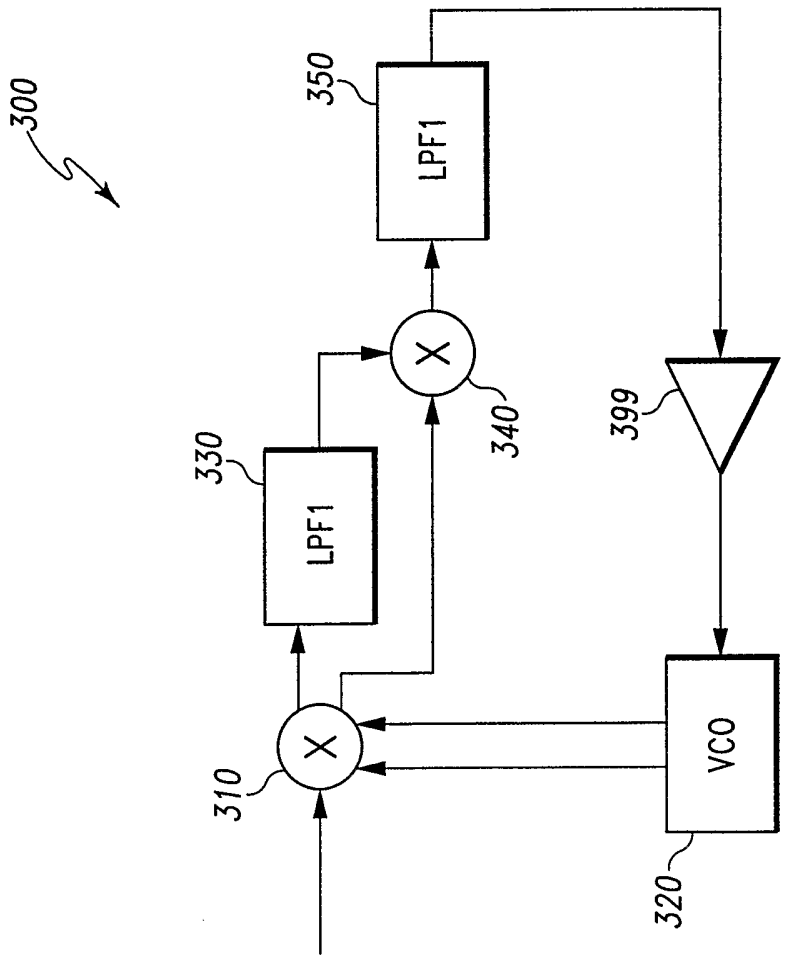

Fig. 3

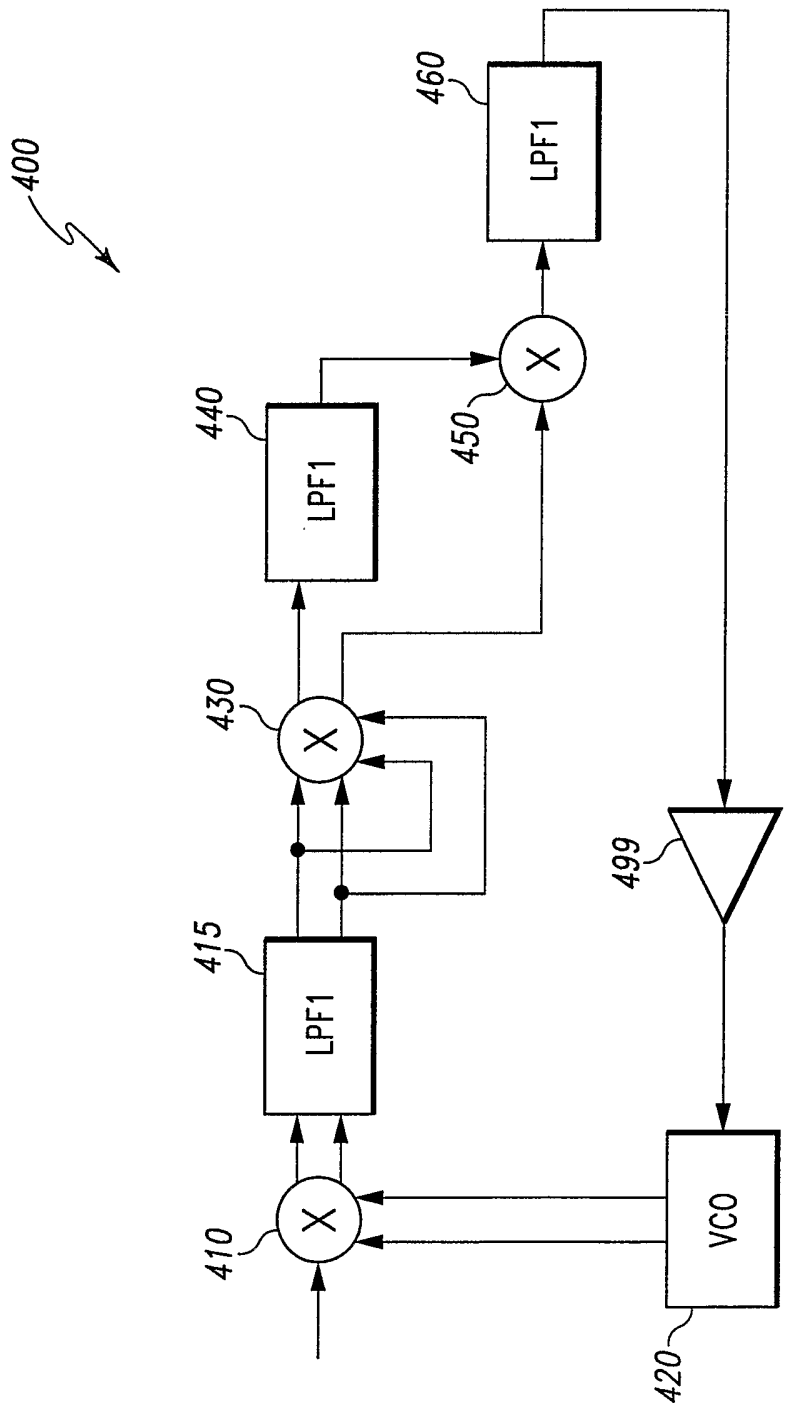

Fig. 4

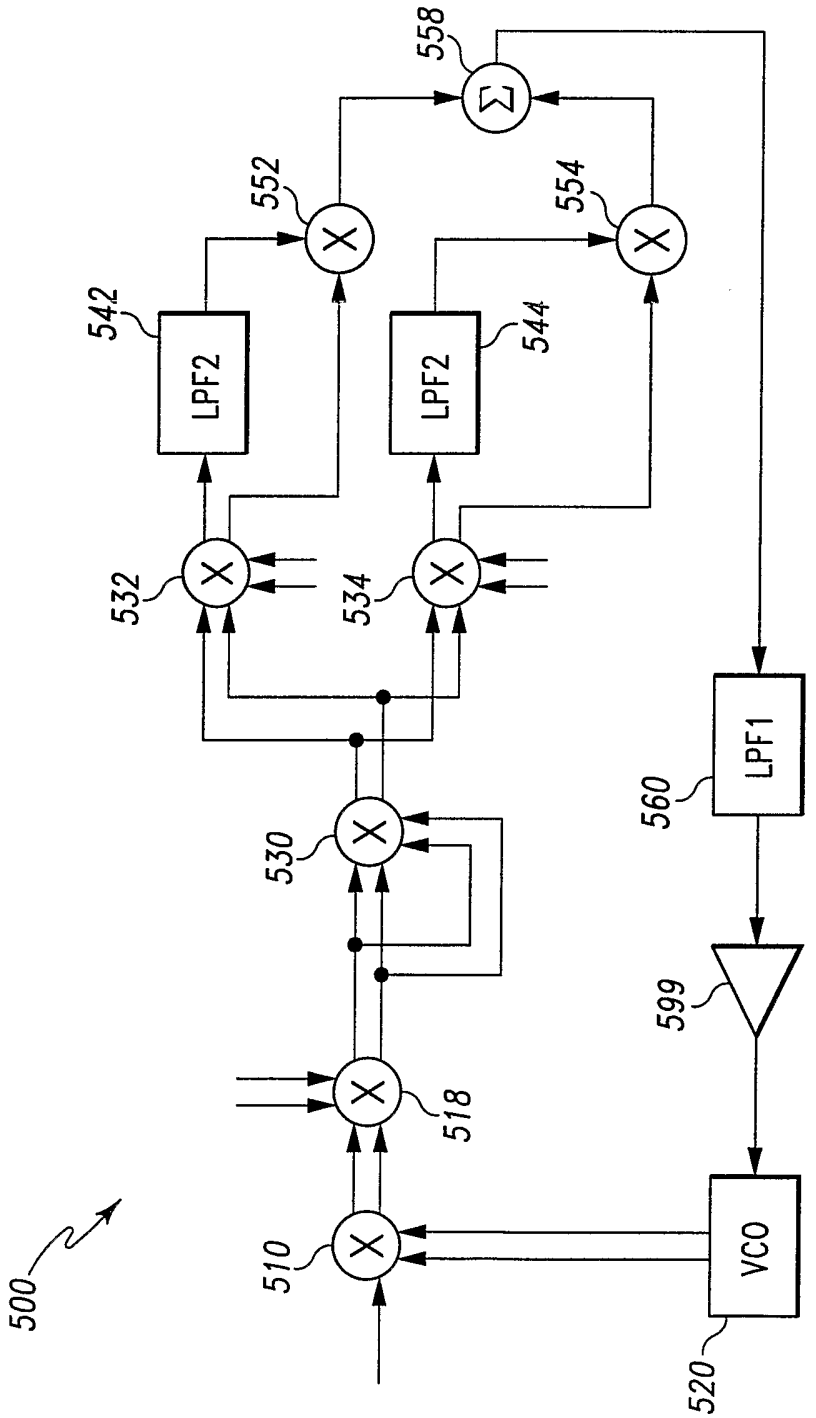
500
510
518
520
530
532
534
542
544
552
554
558
560
599
LPF2
LPF2
LPF1
VCO
Σ

Fig. 5

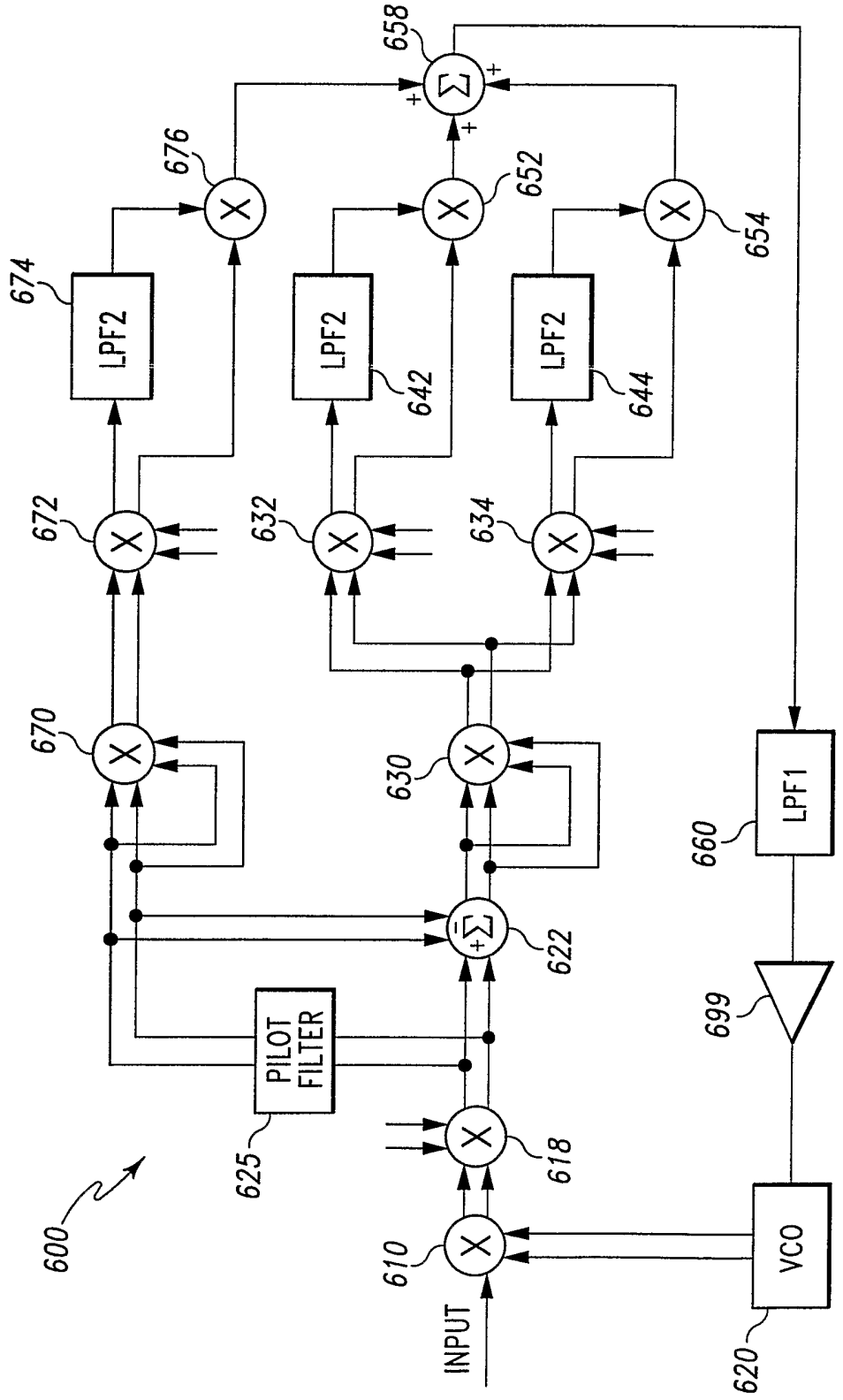
600
610
618
625
INPUT
620
VCO
699
660
LPF1
622
630
670
672
632
634
642
644
674
LPF2
676
652
654
658
PILOT FILTER

Fig. 6

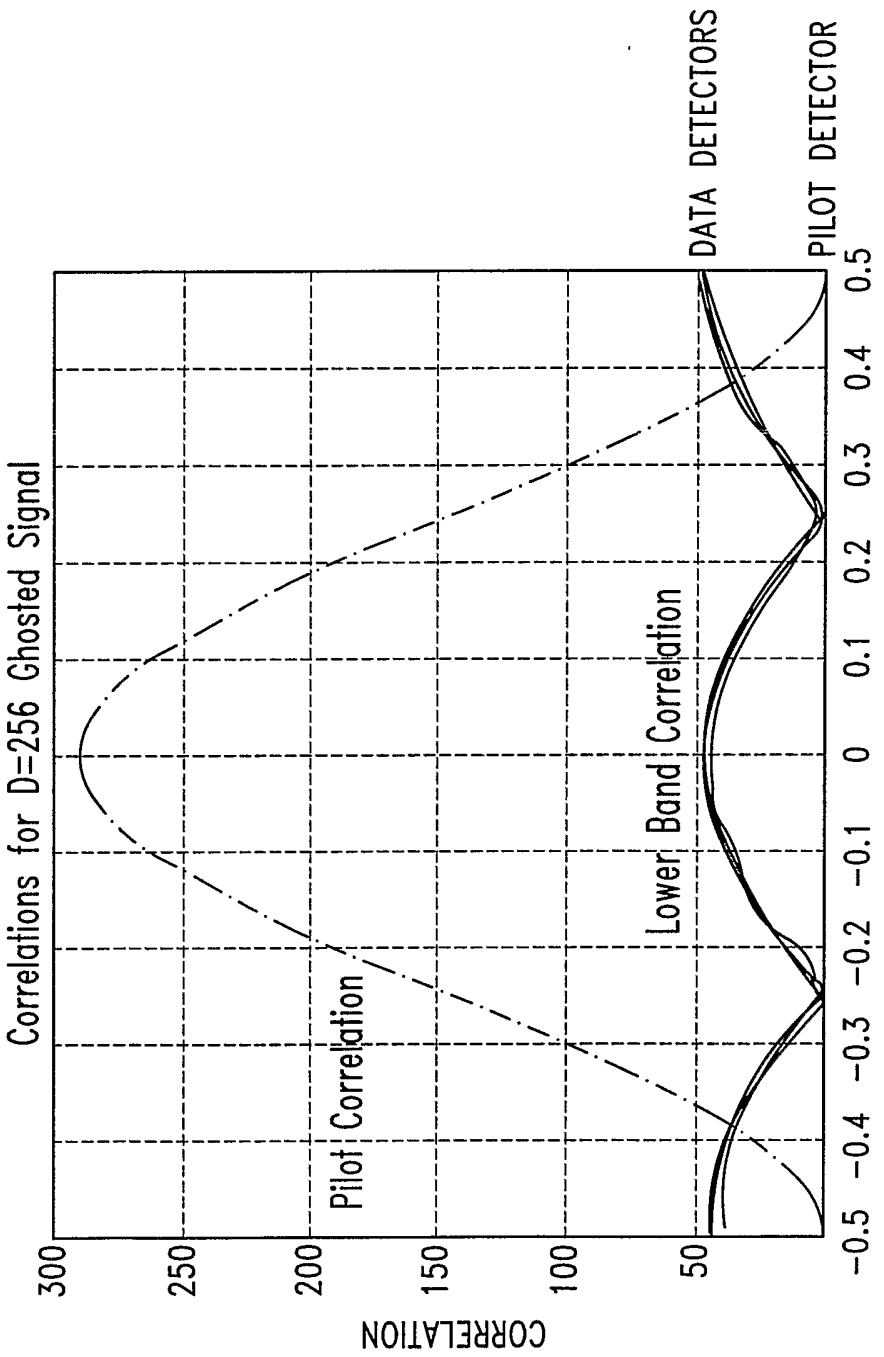
Correlations for D=256 Ghosted Signal
CORRELATION
300
250
200
150
100
50
Pilot Correlation
Lower Band Correlation
DATA DETECTORS
PILOT DETECTOR
-0.5 -0.4 -0.3 -0.2 -0.1 0 0.1 0.2 0.3 0.4 0.5
Normalized Phase
Phase of the Ghost
(Moving Null Across Band)

Fig. 7

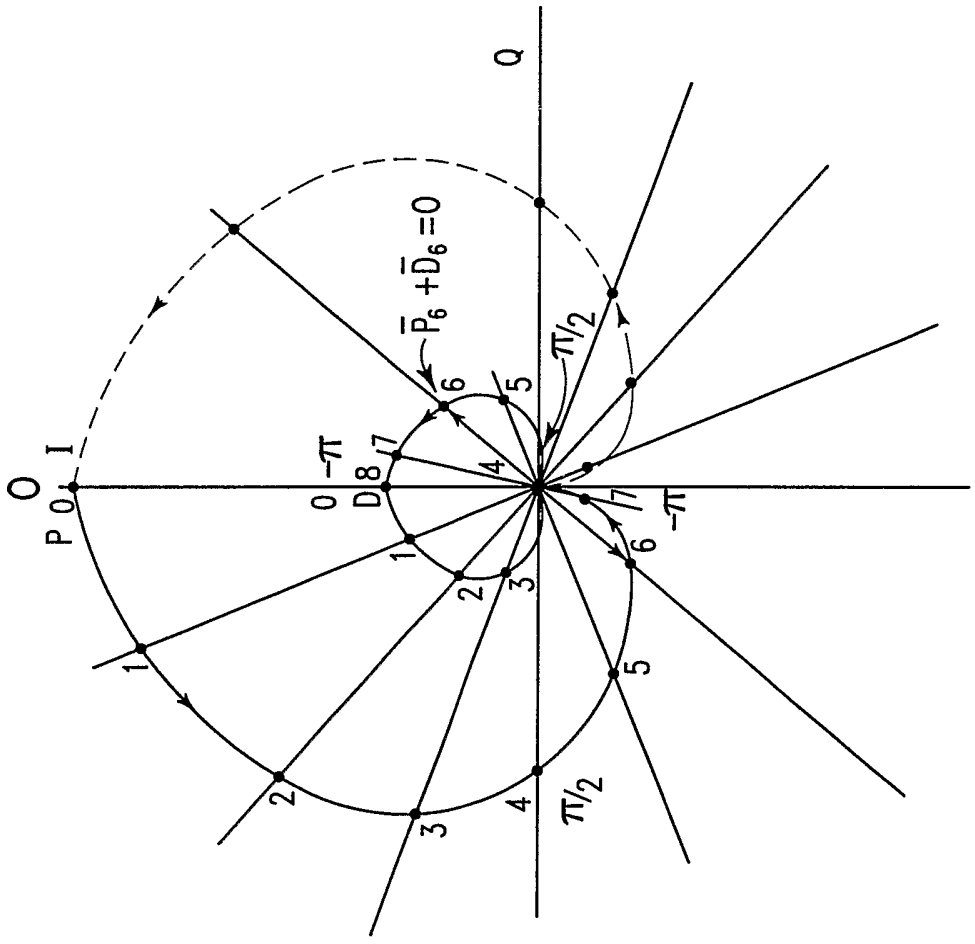

Fig. 8

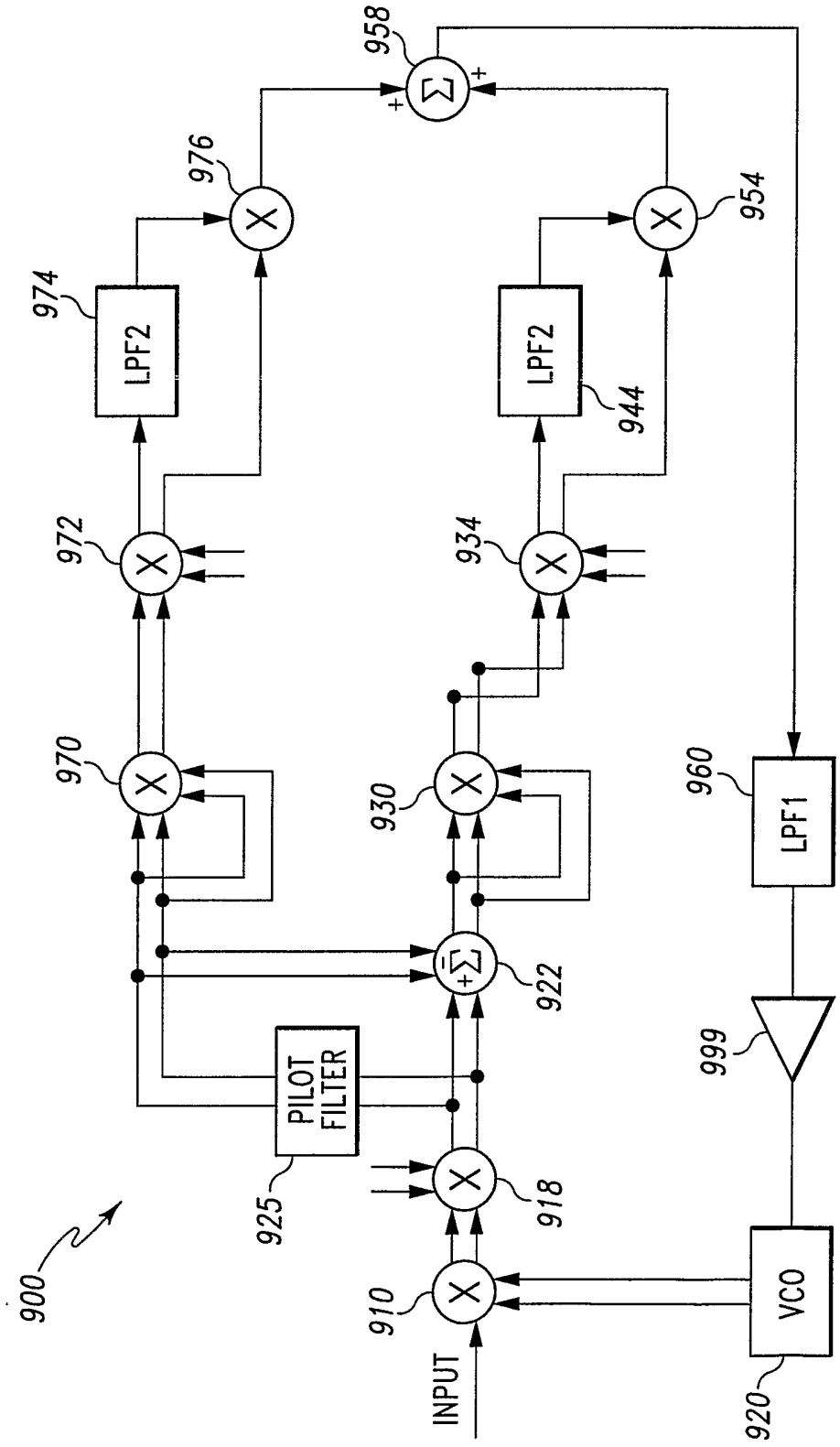
900
910
INPUT
920
VCO
925
PILOT FILTER
918
922
930
934
944
954
958
960
LPF1
970
972
974
LPF2
976
LPF2
999

Fig. 9