United States Patent [19]

Mesnil et al.

[11] **3,923,139**

[45] **Dec. 2, 1975**

[54] **DEVICE FOR ACQUISITION, STORAGE AND ECHELON OF CHARACTERS IN A PRINTER OF THE SERIES TYPE**

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[21] Appl. No.: **497,150**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 363,737, May 24, 1973, abandoned.

[30] **Foreign Application Priority Data**

May 25, 1972 France 72.18601

[52] **U.S. Cl.** **197/19**

[51] **Int. Cl.²** **B41J 5/00**

[58] **Field of Search** ..... 197/1 R, 16, 18, 19, 20, 197/48, 49, 55, 82, 176, 187

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Primary Examiner—Wm. H. Grieb

Attorney, Agent, or Firm—Waters, Schwartz & Nissen

[57] **ABSTRACT**

A control unit for controlling the print logic of a series printer, of the type wherein a printing head is continuously linearly driven by a constant speed motor and is automatically returned to a rest position when a line has been completely printed, and wherein the text to be printed is supplied under the form of digital coded signals to the print logic.

The logic control means comprise a buffer unit for sequentially receiving the coded characters and sequentially transmit the same to the print logic, and logic circuit controlling the addressing in the buffer, the input and the output of data in and out of the buffer unit, and the coupling of the head to the motor.

This control unit enables the pseudo-incremental operation of a conventional series prints with input data rate starting from a nil value.

4 Claims, 16 Drawing Figures

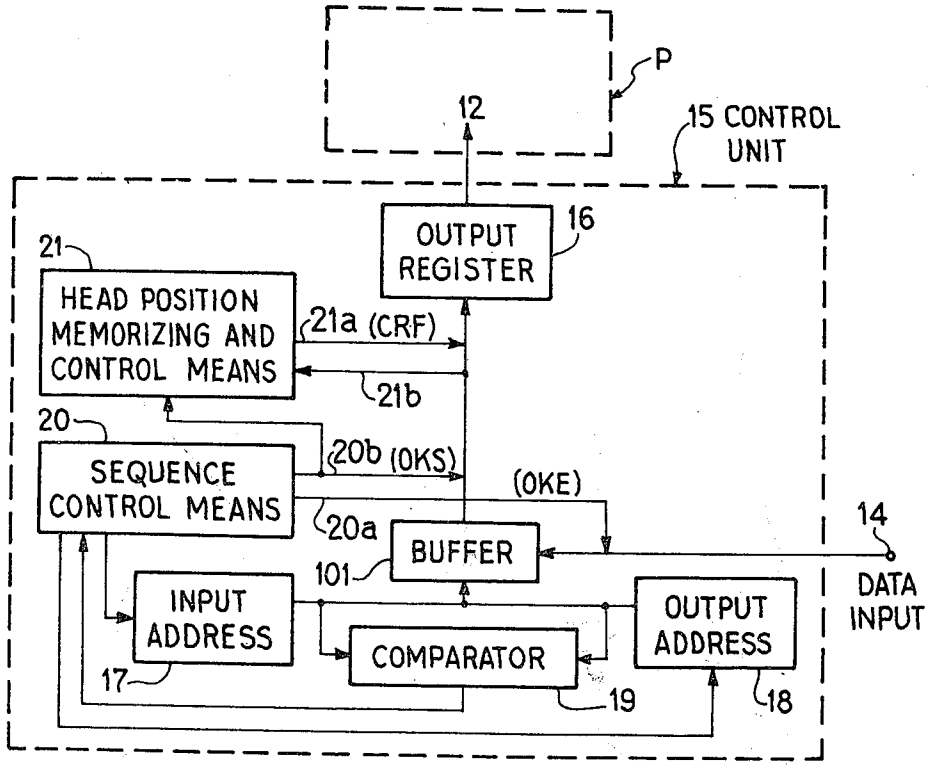


FIG.1 PRIOR ART

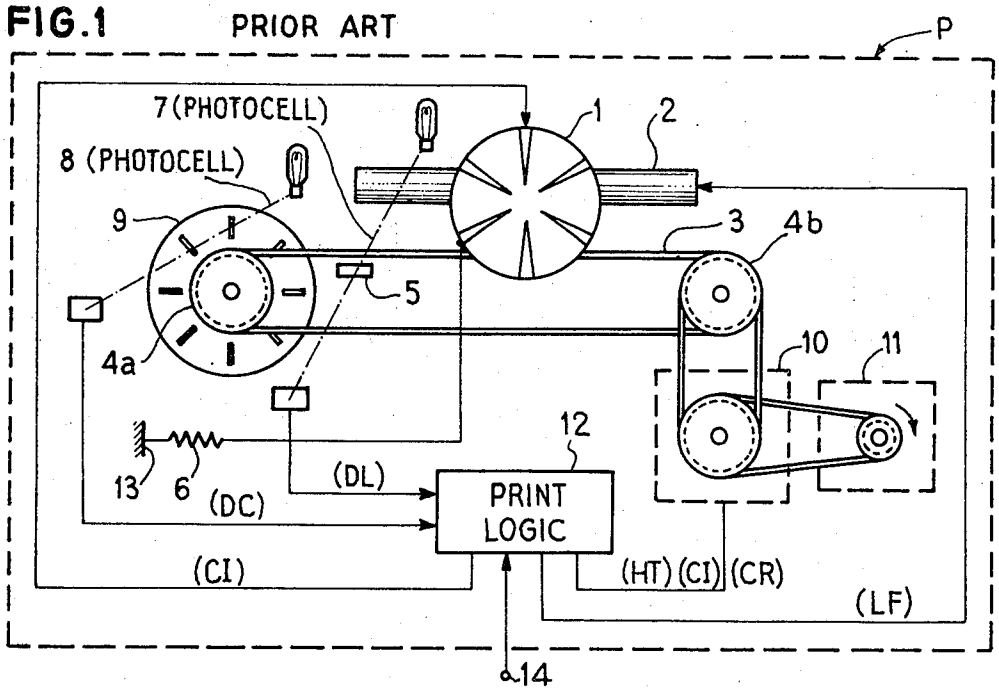


FIG.2

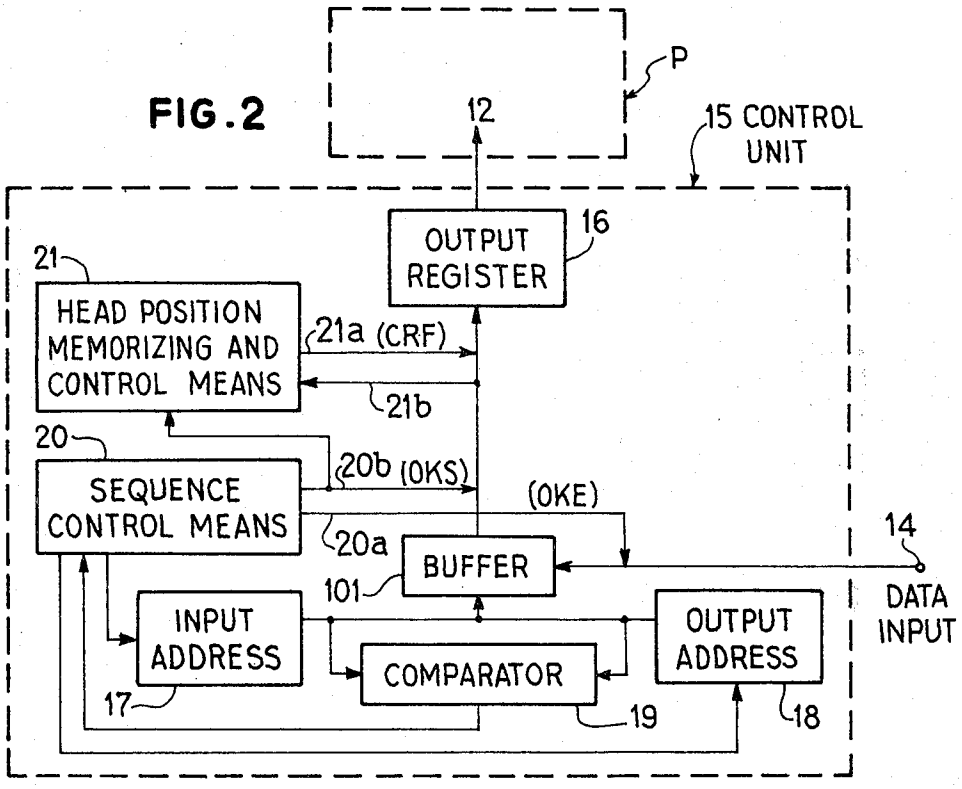


FIG. 3

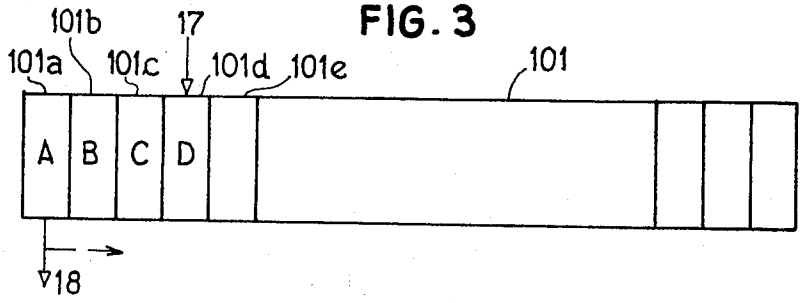


FIG. 4

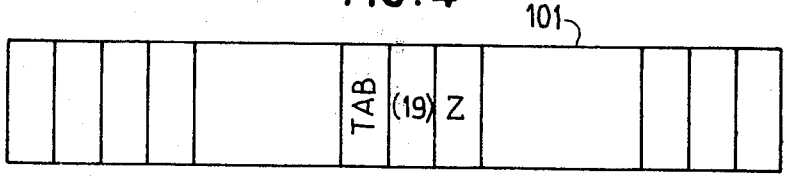


FIG. 5

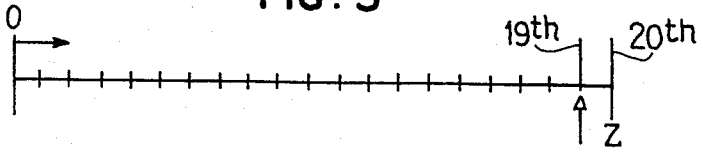
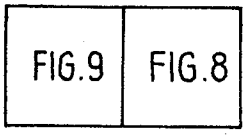


FIG. 7



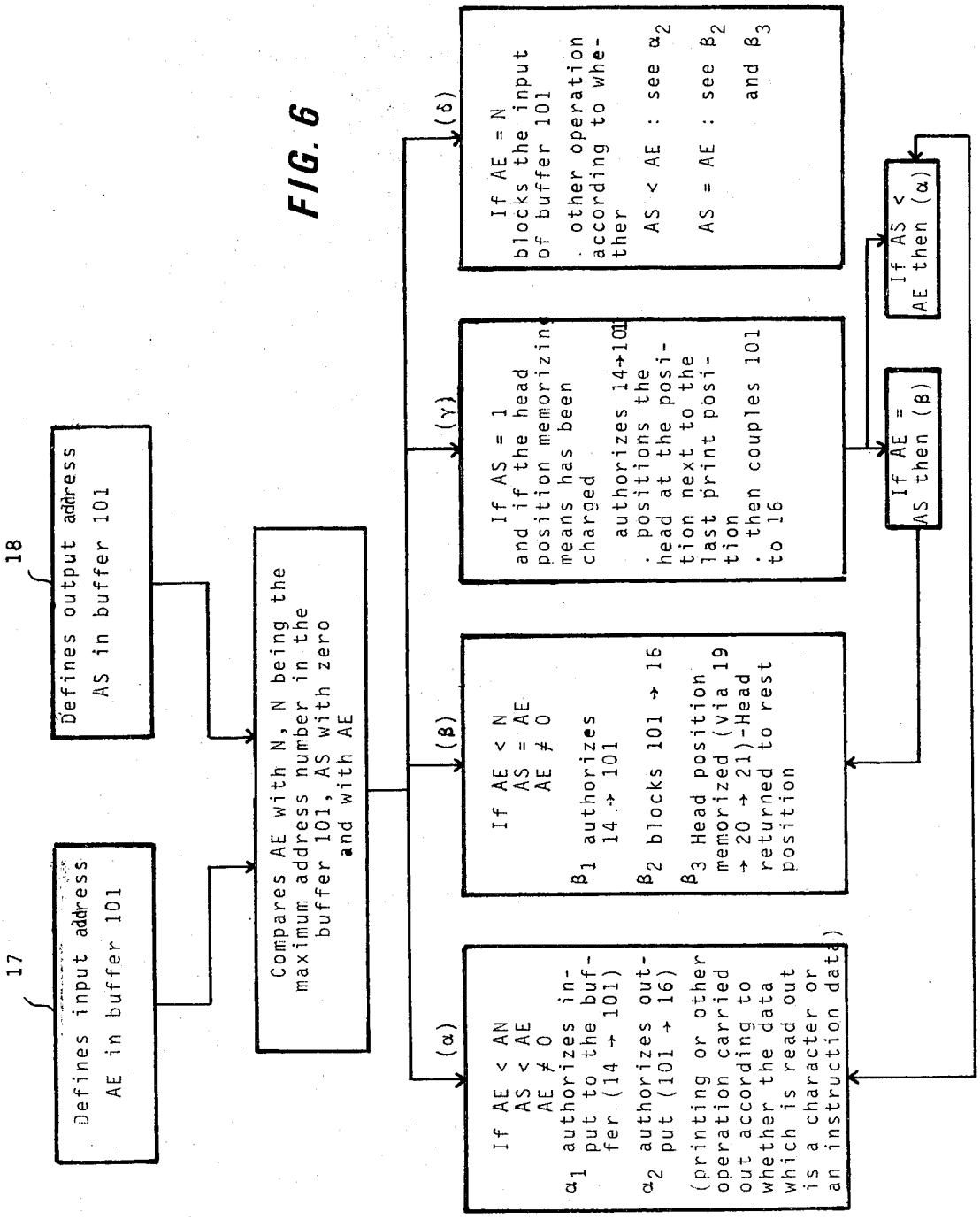

17
Defines input address
AE in buffer 101
18
Defines output address
AS in buffer 101
Compares AE with N, N being the maximum address number in the buffer 101, AS with zero and with AE
(α)
If AE < AN
AS < AE
AE ≠ 0
α1 authorizes input to the buffer (14 → 101)
α2 authorizes output (101 → 16)
(printing or other operation carried out according to whether the data which is read out is a character or an instruction data)
(β)
If AE < N
AS = AE
AE ≠ 0
β1 authorizes 14 → 101
β2 blocks 101 → 16
β3 Head position memorized (via 19 → 20 → 21)-Head returned to rest position
(γ)
If AS = 1
and if the head position memorizing means has been charged
authorizes 14→101
. positions the head at the position next to the last print position
. then couples 101 to 16
(δ)
If AE = N
blocks the input of buffer 101
. other operation according to whether
AS < AE : see α2
AS = AE : see β2 and β3
If AE = AS then (β)
If AS < AE then (α)

FIG. 6

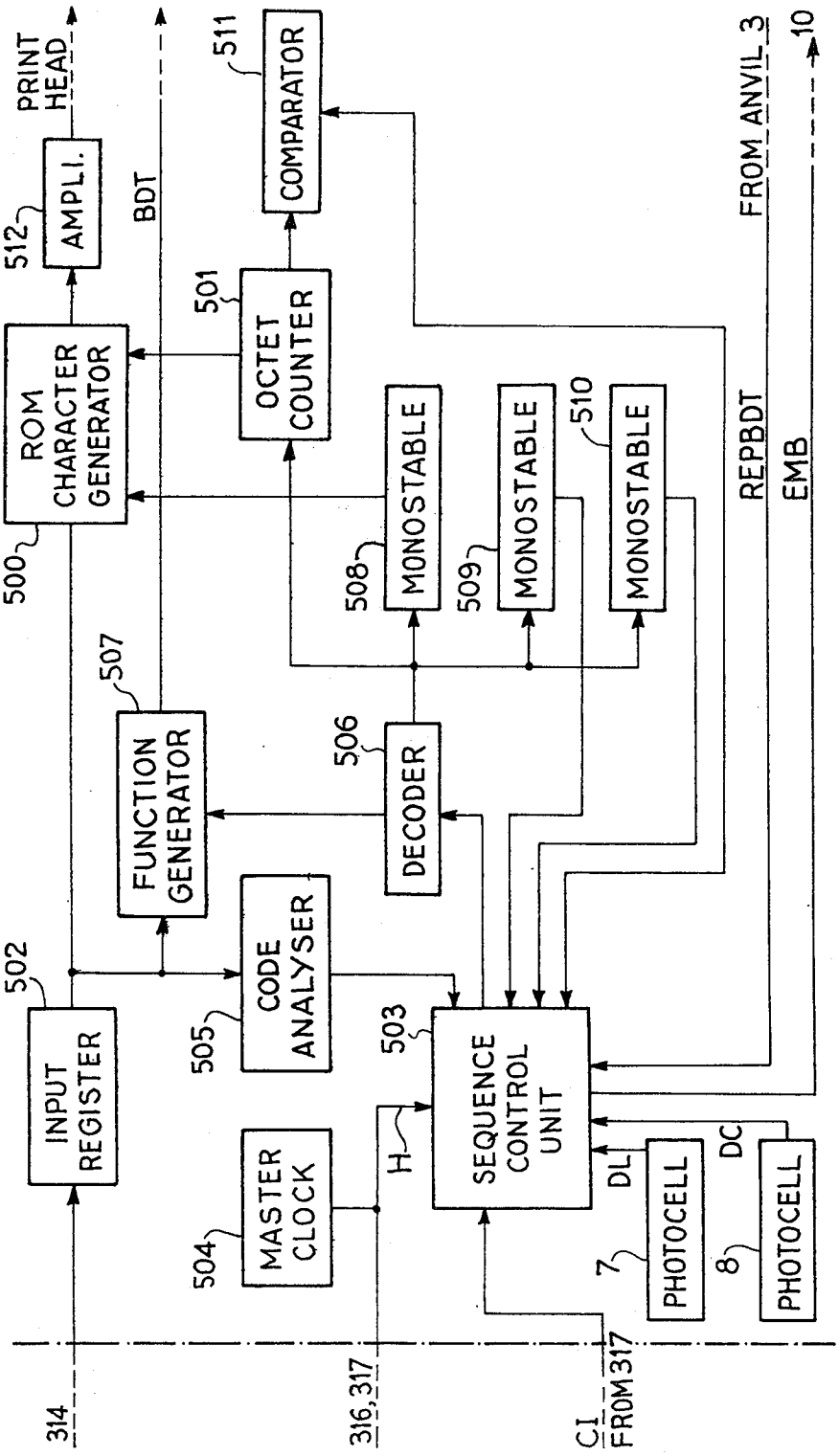


FIG. 8 PRINT LOGIC

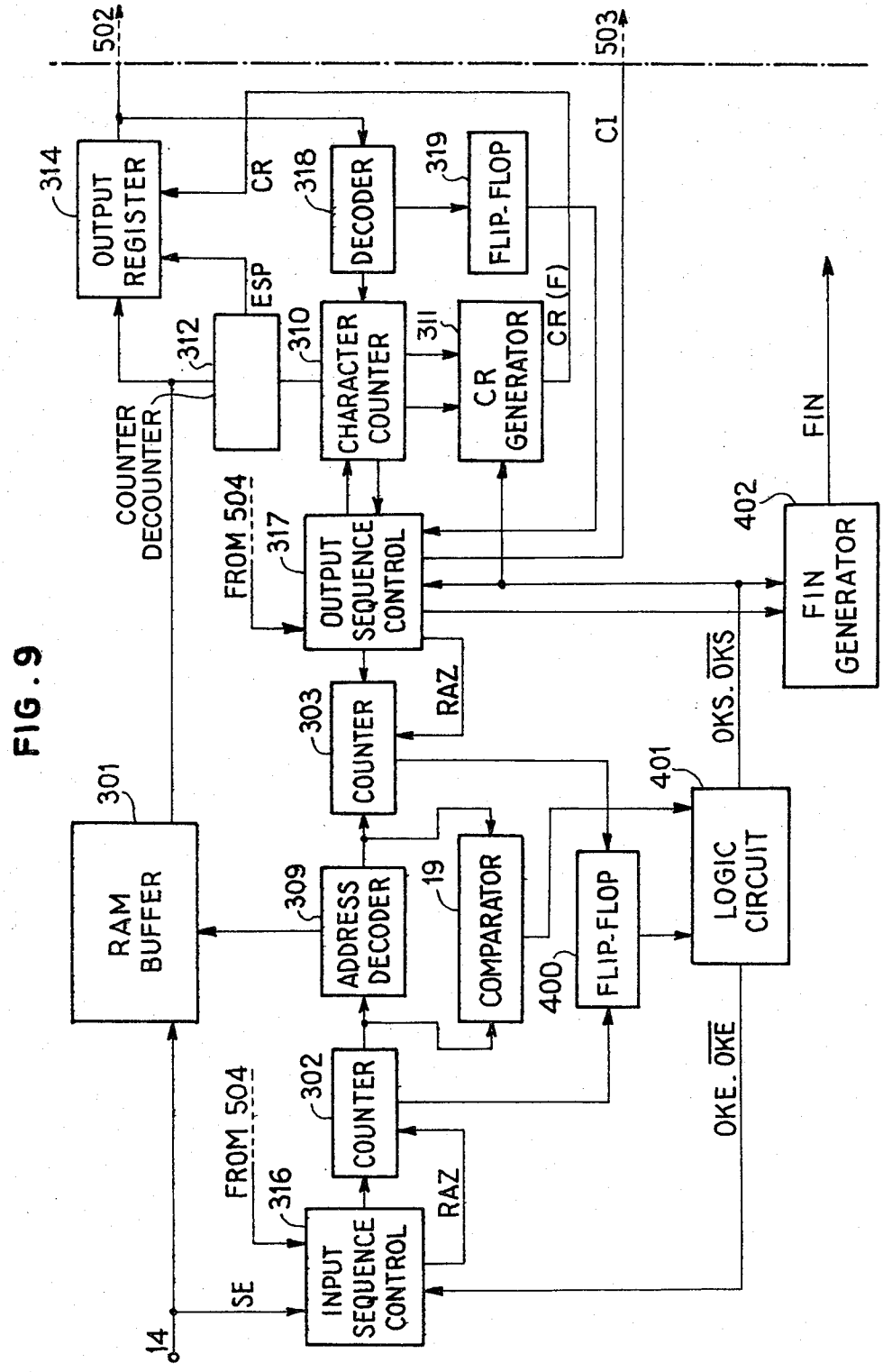

502
503
314
OUTPUT REGISTER
CR
318
DECODER
319
FLIP-FLOP
C1
ESP
312
310
CHARACTER COUNTER
311
CR GENERATOR
CR (F)
COUNTER DECOUNTER
FROM 504
317
OUTPUT SEQUENCE CONTROL
402
FIN
FIN GENERATOR
303
COUNTER
RAZ
OKS. $\overline{OKS}$
401
301
RAM BUFFER
309
ADDRESS DECODER
19
COMPARATOR
400
FLIP-FLOP
LOGIC CIRCUIT
OKE. $\overline{OKE}$
302
COUNTER
FROM 504
316
RAZ
INPUT SEQUENCE CONTROL
SE
14

FIG. 9

FIG. 10 PRINT LOGIC SEQUENCE CONTROL

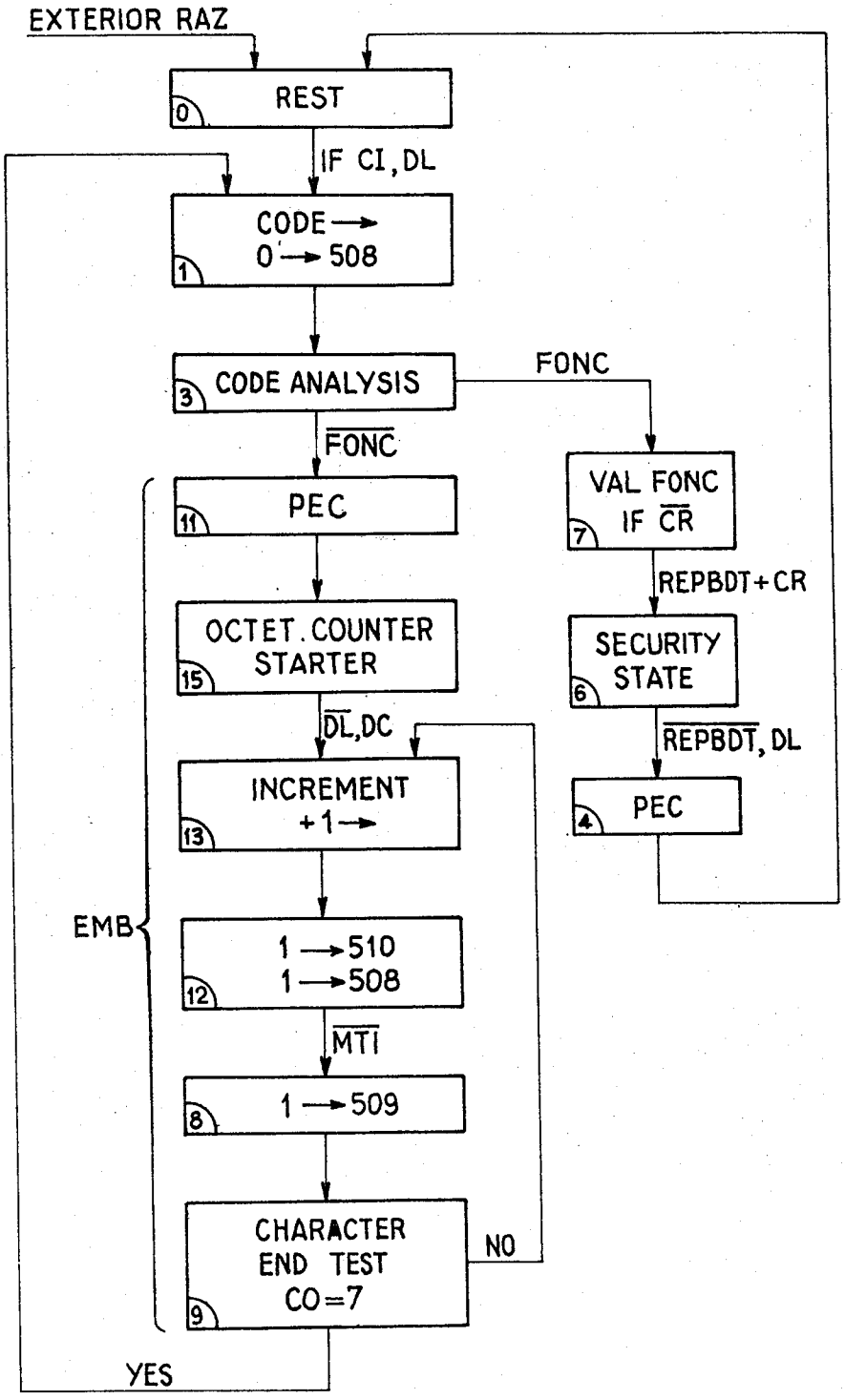


FIG. 11

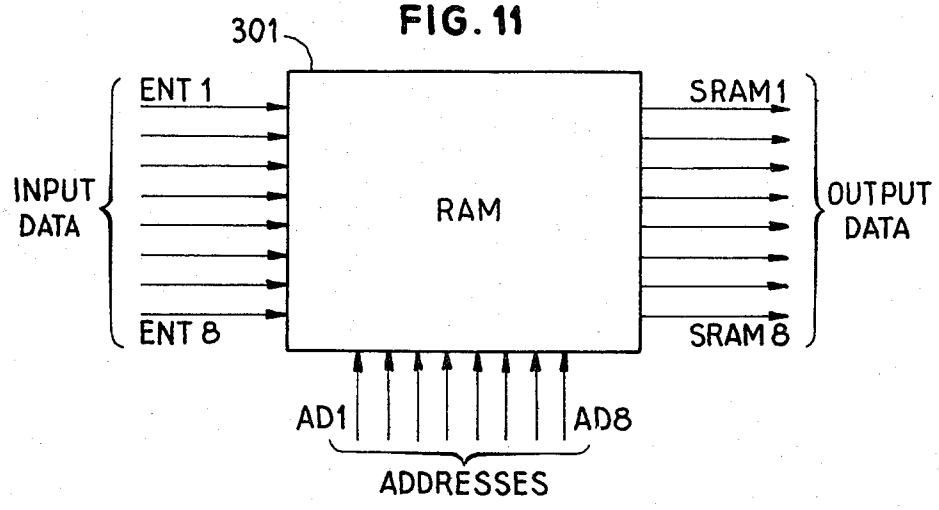


FIG. 12

INPUT SEQUENCE CONTROL

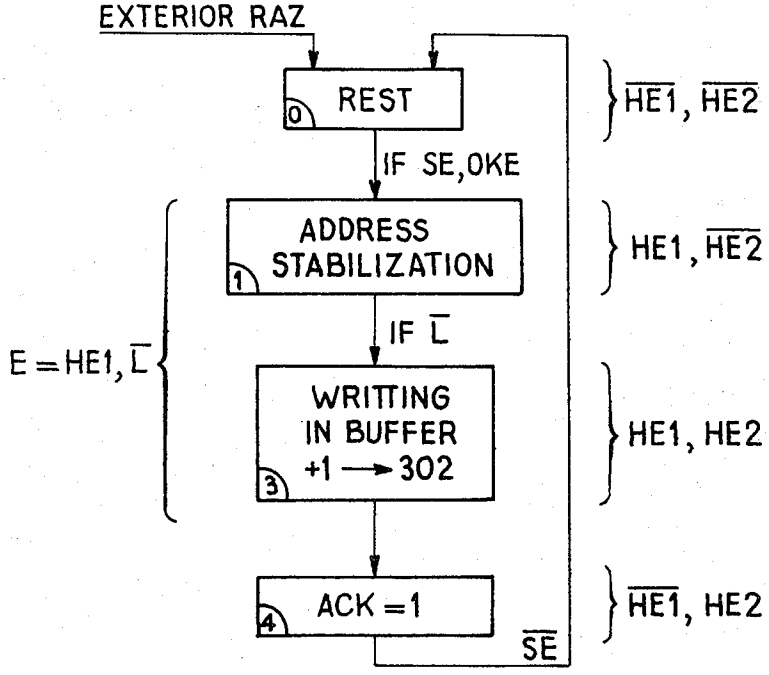


FIG. 13

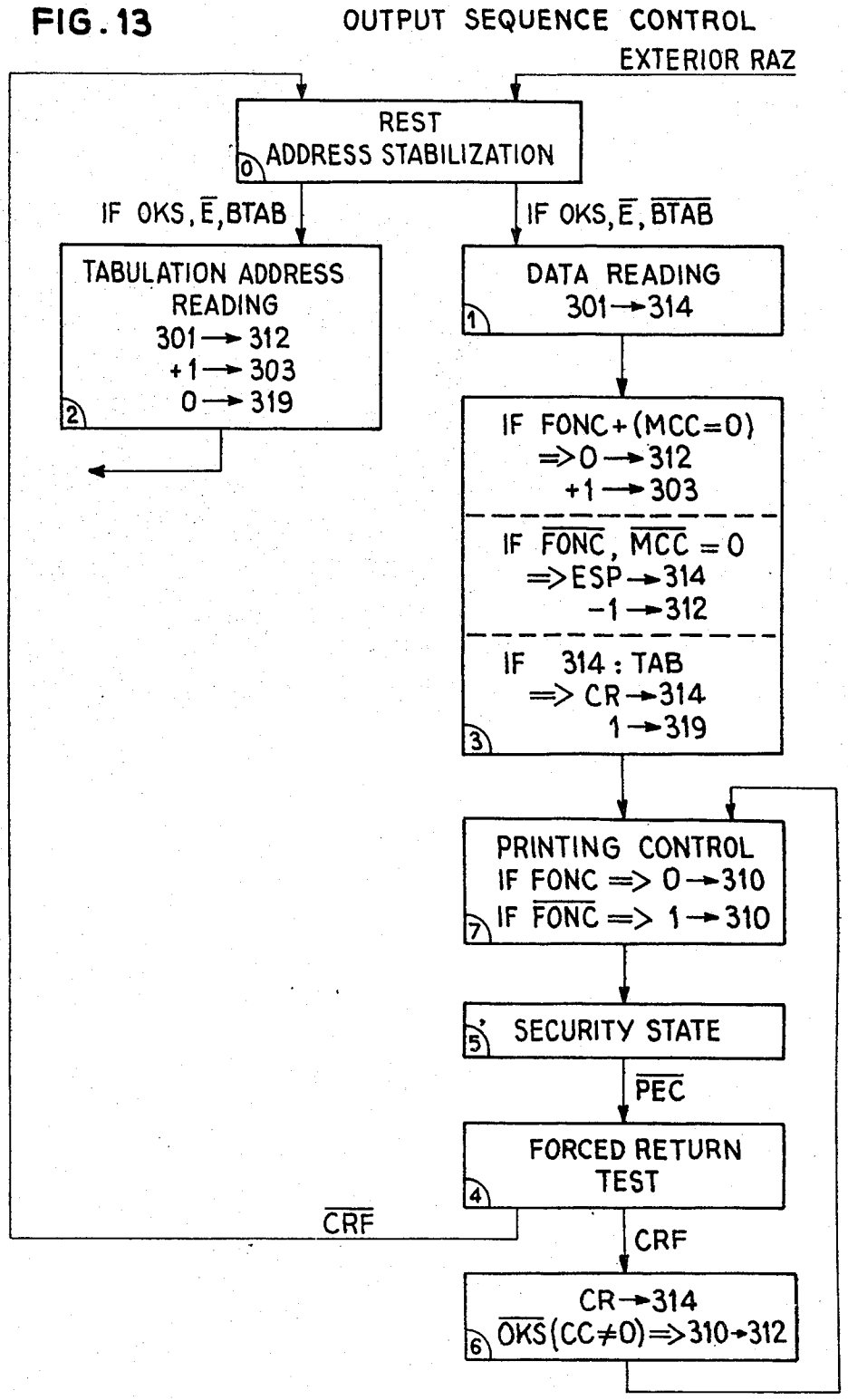

OUTPUT SEQUENCE CONTROL
EXTERIOR RAZ
REST
ADDRESS STABILIZATION
0
IF OKS, $\overline{E}$, BTAB
IF OKS, $\overline{E}$, $\overline{BTAB}$
TABULATION ADDRESS READING
301 → 312
+1 → 303
0 → 319
2
DATA READING
301 → 314
1
IF FONC + (MCC=0)
⇒ 0 → 312
+1 → 303
IF $\overline{FONC}$, $\overline{MCC}$ = 0
⇒ ESP → 314
−1 → 312
IF 314 : TAB
⇒ CR → 314
1 → 319
3
PRINTING CONTROL
IF FONC ⇒ 0 → 310
IF $\overline{FONC}$ ⇒ 1 → 310
7
SECURITY STATE
5
$\overline{PEC}$
FORCED RETURN TEST
4
$\overline{CRF}$
CRF
CR → 314
$\overline{OKS}$ (CC≠0) ⇒ 310 → 312
6

FIG. 14

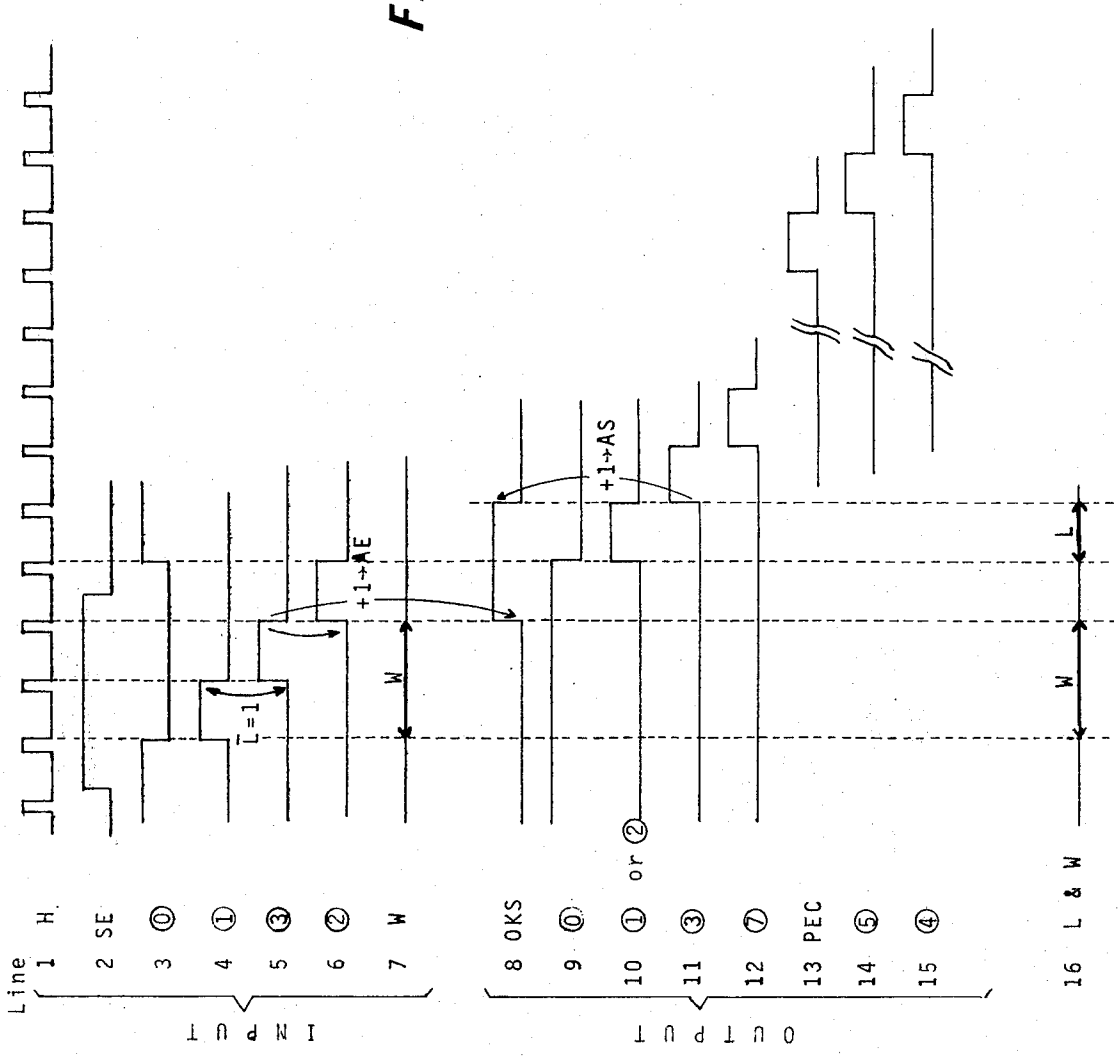

Line
1 H
2 SE
3 ⓪
4 ①
5 ③
6 ②
7 W
8 OKS
9 ⓪
10 ① or ②
11 ③
12 ⑦
13 PEC
14 ⑤
15 ④
16 L & W
INPUT
OUTPUT
L=1
+1→AE
+1→AS
W
L
W

FIG. 15

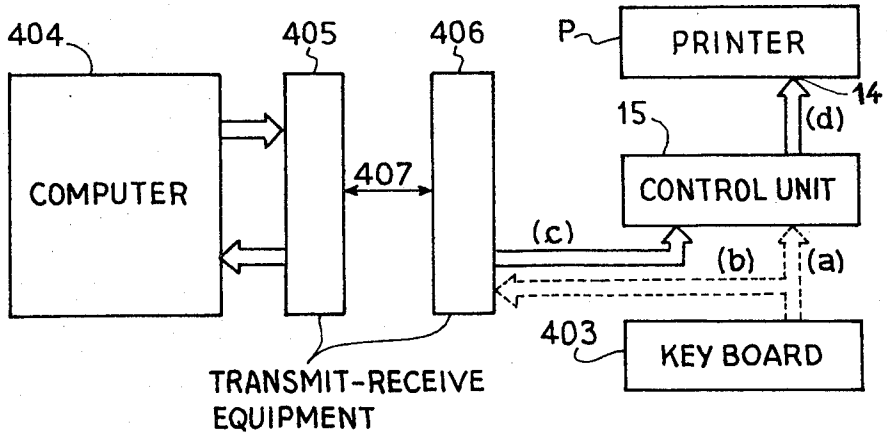
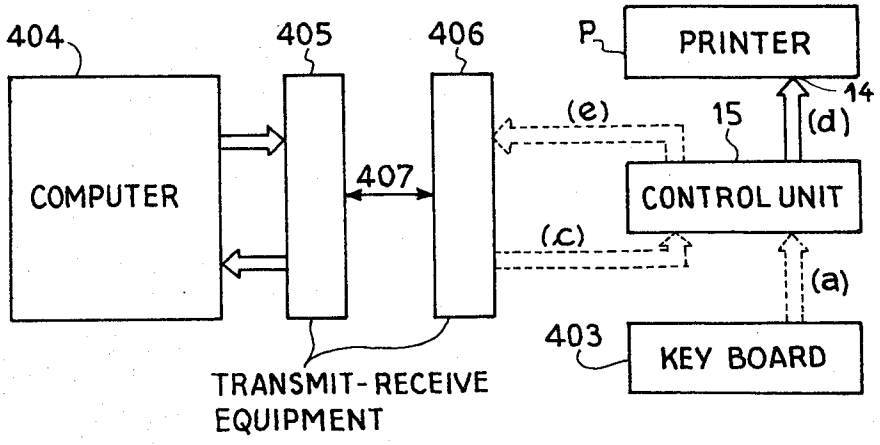

404
405
406
P
PRINTER
14
15
(d)
407
COMPUTER
CONTROL UNIT
(c)
(b)
(a)
403
KEY BOARD
TRANSMIT-RECEIVE
EQUIPMENT

FIG. 16


404
405
406
P
PRINTER
14
(e)
15
(d)
407
COMPUTER
CONTROL UNIT
(c)
(a)
403
KEY BOARD
TRANSMIT-RECEIVE
EQUIPMENT

DEVICE FOR ACQUISITION, STORAGE AND ECHELON OF CHARACTERS IN A PRINTER OF THE SERIES TYPE

This is a continuation-in-part of U.S. Ser. No. 363,737 filed May 24, 1973, now abandoned.

The present invention relates to automatic series printers of the type wherein a printing head is continuously linearly driven by a constant speed motor in front of a stationary anvil or platen and is spring-biased so as to automatically return to a rest position at the level of the next print line, ahead of the beginning of the latter when the coupling of the head to its drive mechanism is put off and wherein coded print data are serially fed to the printer.

Printers of this type are particularly interesting because of the simplicity of their drive mechanism and their high speed.

They are generally associated with a print logic including an input storage unit and decoding circuits.

This type of printer allows only for synchroneous operation, i.e. for simultaneous data supply at the input of the printer and data printing. When, which is generally the case, they are fitted with an input storage unit, they may be also momentarily operated with an input data supply occurring at a rate greater than the printing rate, as long as the storage unit has not been filled up. However, they cannot be operated with, for instance, a type-writer data feed, the rate of the latter, of the order of a few characters/second, being smaller than the print rate, of the order of 180 characters/sec.

Therefore, heretonow, when input data flow rate are smaller than the print flow rate are, only incremental printers, i.e. printers driven by a step-by-step motor have been utilized, which printers are particularly onerous, due to the complexity of the necessary control circuits of the motor, and to the motor itself.

Accordingly, it is the object of this invention to achieve the asynchroneous edition of alphanumerical characters independently of the rhythm of acquisition of the said characters — which may range between a nil value and a maximum value determined by the characteristics of the printer — using an automatic series type printer of the first referred type or "continuous type".

When the rhythm of acquisition is equal or greater than the print rate or nominal rate of the printer, the latter operates in continuous mode. When this rhythm is lower than the nominal rate, the printer then operates in an incremental mode. Therefore, in the following, the printer according to the invention will be designed as a "pseudo-incremental" printer.

This, and other objects of the invention are achieved by the insertion of a buffer type control unit, in the control circuits of a continuous series printer.

In accordance with a specific feature of the invention, the printing head ceases its advance when there is no longer any new character to print, and, after the memorization of the last position reached, is brought back automatically at the beginning of the line without this backward return being accompanied by a jump of the paper thus permitting a good visibility of all the printed characters of the line.

In accordance with a further feature of the invention, the printing head resumes its advance immediately after when one or several new characters have to be printed, sweeping at the maximum speed the portion of the line already printed and subsequently positioning the new characters.

In accordance with yet a further feature of the invention, the repetition of a sequence of characters "SPACE" does no longer necessitate the successive acquisition, an equal number of times, of the said character, but only the knowledge of the number of spaces to achieve, this resulting notably in an increase of speed.

These and other features of the invention will be more clearly understood from the following description.

In the accompanying drawing:

FIG. **1** is a diagrammatic sketch showing a prior art printer apparatus for use in the present invention;

FIG. **2** is a block diagram of a printer according to the invention;

FIGS. **3, 4** and **5** are diagrams illustrating the operation of a particular circuit according to the invention;

FIG. **6** is the flow diagram of the control unit according to the invention;

FIG. **7** shows the arrangement of FIGS. **8** and **9**;

FIG. **8** shows a particular print logic of a printer for use with the invention;

FIG. **9** shows a preferred embodiment of the control unit according to the invention;

FIG. **10** is a flow diagram of the sequence control devices shown in FIG. **8**;

FIG. **11** shows a detail of FIG. **9**;

FIGS. **12** and **13** are flow diagrams respectively of the input and of the output sequence control devices of FIG. **9**;

FIG. **14** is an explanatory time chart; and,

FIGS. **15** and **16** illustrate two different utilization possibilities of the control unit according to the invention.

In the following, the symbols used for the logic circuits are as indicated below.

i. x indicates a signal x is true, which means that the corresponding logic level is operative; for brevity, the term "present" is used in the following; $\bar{x}$ indicates that the signal x is false which means that the corresponding logic level is inoperative; for brevity, the term "absent" is used in the following; alternatively the notation $x = 1$ and $x = 0$ may be used for indicating respectively that x is present and x is absent;

ii. $x = yz$ indicates that x appears only if y and z are operative or present;

iii. $x = y + z$ indicates that x appears if at least one among signals y and z is present;

iv. $x = y \neq z$ indicates that x appears only if y and z are not equal, or are not simultaneously present, according to whether y and z are numbers or logic signals.

Also, for a bistable device z, the same reference indicates the true output of the device ("1" state) and reference $\bar{z}$ indicates the false output of the device ("0" state).

Due to the complexity of the circuits and the tremendous numbers of letters, letter groups, and numeral references which it is necessary to use for a clear description of the invention, alphabetical and numerical listings are supplied preliminary to the detailed description of the invention, for the reader's convenience.

ACK	Acknowledgment signal from the exterior control device, not shown but coupled to 14;
AE	BUFFER INPUT ADDRESS
AS	BUFFER OUTPUT ADDRESS
AD	TABULATION ADDRESS

-continued

BTAB	BISTABLE DEVICE for memorizing code HT — set to state 1 by code HT, at the output of RP — reset to O when output sequence control unit in state 2;
CC	Content of character counter 310;
CI	PRINT CONTROL SIGNAL — must be fed together with the character code; initiates the sequence of the sequence control unit of the PRINT LOGIC sequences when CI terminates, the head is automatically returned to its rest position, CI controlling the clutch coupling the printing head to the motor;
CO	Content of OCTET COUNTER 501 scanning the 7 octets of the ROM controlling the headwires;
CRF	Function code elaborated by the control unit forcing the head to return to its rest position (de-energizes the head clutch by sending a CR code (8 bits) to the sequence control unit of the print logic;
CR	Function code (8 bits) directly fed as an input data controlling the return of the head to the rest position; (nota: signals CR and CRF act similarly, but do not have the same origin: signal CR is an input data, signal CRF is elaborated by the logic system of the control unit);
DC	Signal synchronizing the beginning of a character printing generated by the photo-cell arrangement 8, it initiates an electronic timing for the control of the wires of the head, according to the 7 columns of each character, as soon as signal DL authorizes the printing;
DL	Signal synchronizing the line beginning — generated by the photo-cell arrangement when the head actuates the shutter; it authorizes the printing of a line;
E	Logic signal which appears when input sequence control unit in state 1 (HE 1) or 3 (HE 3) and output sequence control neither in state 1 nor in state 2, $E = HE\ 1.L$;
FONC	Function code;
FIN	Signal indicating that the buffer is empty and the head at the rest position and that a next print operation, if any, will start at the beginning of a line;
H	Clock signals from master clock 504;
H_1, H_2, H_3, H_4	the four bistable devices building up the sequence control unit of the Print Logic. Driven by the master clock, this sequence control unit may have $2^4 = 16$ different states;
HT	Tabulation code;
HE_1, HE_2	The two bistable devices building up the four states input sequence control unit of the buffer;
HL_1, HL_2, HL_3	the three bistable devices building up the eight states output sequence control unit of the buffer;
$I_1 - I_8$	The eight bits of the character code;
L	Signal indicating that the output sequence control unit is either in state 1 or in state 2; $L = \overline{HL_3}\ (\overline{HL_2}.HL_1 + \overline{HL_1}.HL_2)$
MCC	Content of counter 312;
MT_1, MT_2	Monostable devices timing the printing. The duration of the pulse generated by MT_1, when it is triggered, may be adjusted in order to format the length of a character;
MT_3	Monostable enabling the reading of the ROM — also controllable, it controls the duration of the pulses applied to the electro-magnets of the head;
OKE	Signal authorizing entering of data into the buffer;
OKS	Signal authorizing the output of data from the buffer;
PEC	Acknowledgment signal indicating that a data instruction has been duly executed;
PROM	Programmable ROM;
R	CARRY from a counter;
RAM	Random access memory (buffer memory 101);
ROM	Read-only memory (character generator 500);
RAE	R from the buffer input address counter;
RAS	R from the buffer output address counter;
REP BDT	Response from the paper control device;
RC	Storage register at the input of the Print Logic;
RP	Eight bit register coupled at the output of the buffer;
SE	Strobe signal; must be present together with any input data (character or function data). Controls that the logic voltage levels are stabilized before any operation of the circuitry; is supplied by the exterior data source (not shown, coupled to 14);
VALFONC	Enabling signal from the input data to the paper control device;
VALSOR	Enabling signal for the output of the characters from the buffer to the printing machine (through the Print Logic);
ZAS	Re-set to zero of the buffer output address counter only;
ZAEAS	Re-set to zero of both the buffer input and output address counters.
1	Printing head
2	Anvil
3	Head carrying belt
4a, 4b	Head driving pulleys
5	Shutter, actuated by the head, cooperating with assembly 7 (light source and transducer)
6	Spring, urging the head to the rest position (left most position) when the clutch is de-energized
7	Photo-electric assembly (light source and transducer) supplying signal DL when shutter 5 is actuated by head 1
8	Photo-electric assembly cooperating with regularly slotted disc 9 for supplying signal DC
9	Slotted disc carried by pulley 4a
10	Electrically clutchable pulley, coupling motor 11 to drive pulley 4b
11	Continuous speed drive motor
12	Print Logic
13	Frame of the apparatus
14	Data input
15	CONTROL UNIT
16	OUTPUT REGISTER (Control Unit)
17	BUFFER/INPUT ADDRESS CONTROL
18	BUFFER/OUTPUT ADDRESS CONTROL
19	COMPARATOR
20	SEQUENCE CONTROL MEANS
21	Head position memorizing and control means
101	BUFFER (RAM)
101a–101e	Addresses in 101
301	BUFFER (cf. 101)
302, 303	COUNTERS
309	ADDRESS DECODER
310	CHARACTER COUNTER (→ CC)
311	Carriage return (CR) signal generator
312	Parallel-load counter decounter memorizing the count of 310 when the latter is reset to zero, while not full
316	Input sequence control unit
317	Output sequence control unit
318	Decoder
319	Flip-flop supplying tabulation signal
400	Flip-flop driven by the carrier of counter 302 and 303
401	Logic circuit elaborating OKE and OKS signals
402	"FIN" signal generator
403	Keyboard
404	Computer
405, 406	TRANSM.-RECEIV. EQUIPMENT
500	(ROM) character generator — (Print Logic) control the actuation of the wires of the printing head
501	Octet counter (→ CO)
502	Input register
503	Sequence control unit
504	Master clock
505	Code analyzer
506	Decoder
507	Paper function generator
508	MONOSTABLE — enables the reading of 500
509	" } built up a writing clock
510	" }
511	COMPARATOR (compare CO to seven)
512	AMPLI. CIRCUITS

In FIG. 1 the references between parentheses indicate the nature of the signals which are fed through the connecting lines placed below the parentheses; these signals are defined in the listing and will be explicited in the following.

Referring to FIG. 1 in more detail, there is shown an example of a printer apparatus for use in the present invention.

The printer uses a print head 1, which is movably supported on a pair of locating ways (not shown), parallel to an anvil or platen 2 which does not move axially. The head is uniformly moved from the left side towards the right side by means of a drive belt 3 guided in a narrow loop configuration by two pulleys 4*a* and 4*b*, pulley 4*a* being driven by a constant speed motor, e.g. a synchronous single-phase motor drive means 11, continuously rotating at a constant rate in the direction of the arrow, through an electromagnetically clutch-

able belt and pulley coupling **10.** For the sake of clarity, the electrical supply means of the motor and clutch means and control means of the latter which are entirely conventional are not shown.

When the electromagnetic clutch **10** is de-energized, the print head is automatically returned to its rest position, at the leftmost extremity, by a spring **6** generally associated with a dashpot not shown, an extremity of which is attached to the head one, the other extremity being fixed to the frame of the appartaus, symbolically shown at **13.** Of course, spring **6** may be replaced by any other biasing system (electromagnetic e.g.).

The energizing of the clutch **10** starts the displacement of the head from the rest position towards the right. In order that printing operation be effected only when the head is uniformly moved, the beginning on the printed line is shifted from the rest position. To this end, a photocoupling assembly shown schematically at **7,** comprising a light source and a transducer detects the passage of the head, the latter actuates a shutter **5** which normally masks the light source. Upon the actuation of the shutter a line beginning signal DL is generated.

A regularly slotted disc **9** associated with photocoupling device **8** (light source and a transducer) generates a signal DC synchronizing the beginning of the printing of a character. Signals DL and DC are applied to a conventional print logic **12** which receives at input terminal **14** from an exterior control device not shown coded data input and controls the operation of the head, which is for example of the wire or needle type described in U.S. Pat. No. 3,854,564 patented Dec. 17, 1974 for "Printing heads for printing machines", which patent is a continuation of Ser. No. 169,759 filed Aug. 6, 1971, now abandoned.

To this end, under the control of the data supplied to input **14** and of signals DL and DC, the print logic **12** controls:

the paper jump by means of a line feed signal LF applied to the platen **2**

the printing operation by means of a signal CI which is applied to the head, for controlling the print elements of the same (actuation of selected electro-magnets in the case of a head of the above referred type) and to clutch **10** for energization thereof

the continuous displacement of the head, no printing operation being then carried out, by means of a signal HT (tabulation signal) for inserting a "space" or "blank" either at the beginning of the line or in the course of a line.

An example of a print logic elaborating such signals may be found in U.S. Pat. No. 3,400,798, the principle of the logic circuit described therein being appliable as well to series data feed as to parallel feed, and as well to selector magnets in a movable printing head as to stationary magnets.

When data recorded in code form are applied to the input I, they are decoded in the print logic and, if they are character signals, they are applied to the head control inputs in synchronism with the signal DC, while at the same time the logic controls the energization of the clutch (signal CI). For a correct operation, the character data must be supplied to input **14** at the printing rate; they can also be supplied at a greater rate if the logic comprises a storage unit.

When the head reaches the rightmost printing position, a known detector, not shown, (a photocell arrangement or any other device determining that the line is ended) controls the de-energizing of the clutch **10.**

This kind of printer cannot allow for a data input rate lower than the print head. Indeed, either the clutch is not de-energized when no data are present for printing and irregular blanks would appear between characters, function of the travel of the head between successive data acquisition, or the clutch is de-energized (which is the most general case) and the head returned at its rest position: in this latter case, the successive data will be either printed one on each other or at the beginning of successive lines if the de-energizing of the clutch controls the paper jump.

FIG. **2** shows a pseudo-incremental printer system according to the invention.

It comprises essentially the same basic printer and print logic as that shown in FIG. **1.** In addition, a control unit **15** for the print logic is inserted between the data input **14** and the print logic **12.**

The principle of the invention, which allows the incremental operation of a synchroneous type printer is the following: when, at a given instant, there are no more characters to be printed, the position of the printing head when the last character was printed is recorded, while the head is returned towards its rest or leftmost position, the return of the head being not accompanied by a paper jump.

When new characters arrive, the printing operation starts again, on the same line as that where it occurred before the head was returned to its rest position, and begins at the position next to the last printed character.

To this end, control unit **15** comprises essentially a buffer unit **101** of the RAM type, the output of which is coupled, through an output register **16** to the print logic **12,** means, **17** and **18,** for respectively defining the input address AE and the output address AS in the buffer, comparator means **19** comparing said addresses to each other and to the maximum capacity of the buffer, and sequence control means for respectively authorizing the input of data into the buffer or the output of data from the same, according to the results of said comparison in comparator **19** and means, **21,** for memorizing the position of the printing head when printing is interrupted, for forcing then the head to the rest position and returning the head to the position next to the last print position upon feeding to input **14** a character data.

FIG. **2** is a general block diagram merely showing the logic functions of the various basic parts of control unit **15.** Authorization signals from sequence control means **20** to buffer **101** are fed through lines **20***a* and **20***b*.

Signal OKE on line **20***a* authorizes the connection of input **14** to buffer **101** and therefore the transfer of an input data to the latter at address AE, while signal OKS on line **20***b* authorizes the transfer of the data in the buffer at the address AS to the output register **16.**

Upon supply of signal $\overline{OKS}$ (i.e. NO signal OKS) sequence control means **21,** memorizes the head position and supplies to output register (which, at this time, is not fed by buffer **101**), via line **21***a* an instruction data for forcing the head to return to the rest position (signal CRF which is similar to signal $\overline{EMB}$ i.e. de-energizing of the clutch **10** in the particular case of printer concerned here). When sequence control means **21** supplies again an OKS signal, the coupling of the buffer **101** to the register **16** then triggers, via line **21***b* means **21** which now controls the returning of the head to the position next to the last print position.

FIGS. 3, 4 and 5, illustrate the process of acquisition of data and printing of characters.

Buffer **101** comprises for example 256 memory units, each of which may receive a group of 8 bits constituting an octet and located by the corresponding address *a*, *b*, *c*, *d*, *e* . . . (sub-units **101***a* – **101***e*, FIG. 1). In this case output register **16**, which receives a single data, is an 8 bit register.

It has been supposed, in the figure, that each of these memory positions had received respectively, in the order of their acquisition, the characters A, B, C and D, it being understood that any interval of time may separate the acquisition of two consecutive characters.

Addressing devices **17** and **18** define respectively the address of the last entered character and the address of the first character to be edited, that is — in the particular case of FIG. 3 — the addresses *d* and *a* of characters D and A. It therefore follows that, each time a new character is introduced in the register **101**, the input address is shifted one step towards the right and that, each time a new character is edited, the output address, in its turn, and independently of the first address, shifted one step towards the right. If, as has been supposed by way of an example in FIG. 3, there has been successively introduced in the register **101** the characters A B C and D which constitute the word ABCD, the input addresses are successively the addresses *a*, *b*, *c* and *d*.

Assuming that the printing head has been correctly positioned, the output addressing device **18** will initially designate the position **101***a* in buffer **101**, and authorize the edition of character A; then it proceeds to advance in its turn character by character, as a function of the travelling speed of the printing head, to designate the positions **101***b*, **101***c* and **101***d* of the buffer **101**, authorizing at each time the edition of characters B, C and D. When it will designate the position **101***d* already defined by the input address control means **17**, the edited word will be the word ABCD. At this moment, the head control means **21** according to the invention will control the return of the printing head at the rest position, under control of spring **6**. No paper jump (or line feed) being initiated, this position is ahead the beginning of the line which was just being printed and which will be referred to in the following as the "printing line", a short distance being provided between the rest position and the beginning printing line for regulation of the space between characters, due to the inertia of the head, as already explained with reference to FIG. **1**.

The address of the last character edited D is then memorized in an auxiliary memory in means **21** in order to permit the printing head to resume its advance, immediately on the arrival of a new character up to the position where this latter should have been edited, by the generation of a number of spaces equal to the contents of the auxiliary memory.

FIGS. 4 and 5 illustrate another possibility of the device according to the invention; it relates to the particular case of the edition of a word or of a character which has to be preceded by a sequence of spaces. As an illustration, it is supposed that the character to edit Z should be preceded by a number $n = 19$ of spaces, starting from the beginning of the line. In this case, one introduces in the consecutive positions of the buffer **101**, first of all the code "TABULATION", as indicated in FIG. **4** then the number of spaces to generate defined by the position of the character to be edited (here, the 20th) diminished by 1 unit (which corresponds to 19 consecutive spaces), the number obtained being converted in the binary code and finally the code of the character to edit (Z in the example considered). The successive analysis of the contents of consecutive positions of the buffer **101** by the output addressing device **18** results, as shown in FIG. **5**, in a displacement of the printing head from the beginning of the printing line up to the physical position where has to be edited the character Z, that is the 20th in the example considered.

This feature of the device provides the advantage of saving the number of positions of memory necessary for the successive generation of several codes "TABULATION", at the same time that it authorizes an increase of acquisition speeds for the following characters.

Theoretically:

Signal OKS appears as long as there is at least one data remaining in buffer **101**.

Signal OKE appears as long as the buffer is not filled up, i.e. as long as AE<256 in the present example.

In fact, for practical reason, input to and output from the buffer are not absolutely simultaneous and means are provided for synchronizing input and output operations as will be seen further down with reference to a specific example shown in FIGS. 7–12, a master clock supplying enabling signals.

The various blocks of control unit **15** are determined by their functions, which are synoptically summarized in the flow diagram of FIG. **6**.

A preferred example of carrying out the control unit according to the invention will now be described in detail with reference to FIGS. **7**, **8**, **9**, **10**, **11**, **12** and **13**, FIG. **7** showing the arrangement of FIGS. **8** and **9**, and FIGS. **10**, **11**, **12** and **13** showing details of the circuits shown in FIGS. **8** and **9**.

For a better understanding, a printer P for use in this invention will be described in detail, although it is evident that the invention may be used with different printers. It is assumed that the printer P has the following features.

Each character is built up by a mosaic of dots, each of which is obtained by the mechanical action of the extremity of an elongated element, wire or needle, which strikes the paper through an ink ribbon.

The head comprises seven wires in a vertical plane, respectively actuated by seven electromagnets. The energization of one or more of the electromagnets gives rise to the printing of one or more dots along seven horizontal lines, the head being uniformly moved parallel to the print anvil, from the left towards the right. Such heads are well known in the art and will not be further described nor shown. Advantageously, the head may be of the type of the above mentioned copending application.

The graphisms of the character are stored in ROM (read-only memories). For instance, two ROM are incorporated in the printer of 256 octets each. Since each character occupies eight octets, 64 characters may be generated by character generator **500**, built up by said two ROM. The code used is 8 bits code ASCII, the 3 bits of higher weight being used for selecting the ROM concerned while the 5 bits of lower weight is used for selecting the character in this ROM.

A counter **501** whose content CO varies from 0 to 7, controls the scanning of the seven successive addresses at which the octets are stored. The triggering of this counter will be explained further down.

The information (direct data information from an exterior control device: typewriter, output of a computer . . . ; if conventional printer or indirect data information supplied through control unit **15** according to the invention) are supplied to input register **502** which comprises eight octets.

The data supplied to register **502** are either function code data or character code data. Examples of function code data are:

CR: head return to rest position without paper jump;
LF: head return with line feed.

Code analyzer **505** determines whether it is a function code or a character code. Code analyzer **505** output signal is applied to one of the control input of a sequence control unit **503,** driven by a master clock **504** which generates sync. signals H, having a repetition period ranging preferably between 2 to 5μs. Signals H are applied to sequence unit **503** so that change of states of the latter if any occurs only at predetermined times. Signals H are also applied to the sequence control means **20** of control unit **15.**

Sequence control unit **503,** which drives all the logic operations of the print logic, is built up of four bistable devices H_1, H_2, H_3, H_4 not shown, which allow for 16 different output states according to the following table.

H_4	H_3	H_2	H_1	State reference
0	0	0	0	00
0	0	0	1	01
0	0	1	0	02
0	0	1	1	03
0	1	0	0	04
0	1	0	1	05
0	1	1	0	06
0	1	1	1	07
1	0	0	0	08
1	0	0	1	09
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Sequence control unit has further input for signals DC and DL from the photo-cells arrangement **7** and **8,** and for other signals which will be explicited hereinafter.

When no signals, but the clock signals H, are applied to unit **503** the latter is in state 00, signal H being applied here only as enabling signal, and not as triggering signals.

When unit **503** receives both a print control signal CI from the control unit **20,** which is generated in a manner which will be further described, and the signal DL, it is triggered to state 01, during which the data code are fed to register **502.** Then, if signal CI lasts, it is triggered when the next pulse H appears, to state 03; in the contrary, it returns to state 00.

If the data code is recognized in analyzer **505** as being a function code, it triggers unit **503** to state 07. The code is then decoded in decoder **506** which supplies either the corresponding enabling signal VALFONC, if it is a function code, to function generator **507** which is coupled at the output of register **502** or a triggering signal to octet counter **501** and to three monostable circuits **508, 509, 510** the function of which will be further explained.

If the instruction is a line feed with head return, for instance, the paper movement control device, not shown here, and symbolically represented in FIG. **1** by the arrow towards anvil **2,** generates an acknowledgement signal REPBDT which triggers unit **513** to state 06. When this signal is over ($\overline{\text{REPBDT}}$) and the head is at the rest position, unit **503** is triggered to state 04 where the acknowledgement signal PEC is sent to the control unit **15,** resetting the latter to state 00.

If it is a character code, unit **503** is triggered by analyzer **505** to state 11 and then signal PEC is sent to control unit **15.** The clutch **10** (FIG. **1**) is then energized (signal EMB). Octet counter **501** is reset to zero. Upon supply of signals DL and DC, unit **503** is cyclically triggered, seven times, to states 13, 12, 08, 09 by means of monostable devices **509, 510** which act as a writing clock, device **509** being controllable, thereby allowing for the adjustment of the width of a printed character. Controllable monostable device **508,** coupled to character generator **500** monitors the duration of the pulses applied through amplifier circuit **512** to the head electromagnets. Each time unit **503** is triggered to state 13, counter CO is incremented. At state 09, it is checked in comparator **511** if its contents CO $\neq$ 7, unit **503** is triggered to state 13 and the character printing is continued; if CO = 7, unit **503** is reset to state 01 for reading of the reset character code, whereby counter **501** is also reset to zero.

If a data accompanied by a signal CI does not appear before a time gap of 5,5 ms has elapsed after the last signal PEC of the printing of a character, the next clock signal returns automatically unit **503** to the state 00, where the clutch **10** is deenergized, and, therefore, the head **1** returned to the leftmost rest position.

FIG. **10** shows the flow diagram of sequence control unit **503.** The 16 states (00 to 15) are not all used; however, four bistable are used, since three bistables allow only for eight states, which would not fit since 12 states are necessary (states 00, 01, 03, 04, 06, 07, 08, 09, 11, 12, 13, 15).

According to the invention the data from the exterior control device are not directly applied to register **502** but to control unit **15.** FIG. **9** shows a preferred embodiment of unit **15,** particularly well fitted for use with the print logic of FIG. **8.**

The buffer **101** of FIG. **2** is here built up by a RAM **301** having a capacity of 256 octets, shown in more details FIG. **11.** While, for compactness, the input and output lines of device **301** are shown as single lines, they are in fact built up by eight parallel lines ENT1 – ENT8 for the input and SRAM1 – SRAM8 for the output. Also, they are eight address lines whether for the input or the output of data.

Each time data is present at general input **14,** a counter **302** is incremented; this counter indicates the address where this data must be recorded in the buffer. Similarly, a counter **303** is incremented each time data is taken out of buffer **301,** and indicates the address this data is to be found.

Thus the operative address AD is selectively indicated by counter **302** or **303** each of which has eight bits and can therefore address the 256 memory positions of the buffer. The content of these counters is decoded in decoder **309.** The assembly **302–309** on the one hand, **303–309** on the other hand, corresponds respectively to devices **17** and **18** of FIG. **2.**

The conditions for input a signal into buffer **301** are: buffer not full; and output address AS ≠ input address AE; a signal OKE is then generated.

The conditions for output a signal are: buffer not empty; output address AS ≠ input address AE (in fact AS<AE since AS>AE is impossible);
a signal OKS is then generated.

To these ends, a bistable or flip-flop **400** is set to the "1" state by the carry of counter **302** (state R) and reset to zero (state R) by the carry of counter **303.** Logic circuits **401** having two inputs respectively coupled to the outputs of comparator **19** and of flip-flop **400** elaborate signals:

$OKE = R\ (AE \neq AS)$
$OKS = R.(AE \neq AS)$

The sequence control unit **20** of FIG. **2** is built up by two devices
device **316:** input sequence control unit;
device **317:** output sequence control unit.

Signal OKE is applied to device **316** while signal OKS is applied to device **317.** These two devices are also driven by the master clock **504** of FIG. **8** as is sequence control unit **503,** so that the output signals do not appear simultaneously.

Each 7 bits data to be entered into the buffer, must be accompanied by a strobe signal SE, applied to input sequence control unit **201.** As long as signal SE is present, the voltages must be absolutely stable. While the data signal is built up by eight logic levels applied in parallel on eight feed lines, signal SE is applied on a separate line, to unit **316.** However, for compactness all the exterior control signals are shown as applied on a unique terminal **14.**

Input unit **316** is built up by two bistable devices HE_1, HE_2. It may be triggered to four different states according to the following table.

HE_2	HE_1	State reference
0	0	0
0	1	1
1	0	2
1	1	3

State 0 is a non-operating or "rest" state, the buffer waiting for data to be entered.

If signal OKE is present, the strobe signal SE initiates the following cycle of unit **201:**
state 1: the address indicated by counter **302** stabilizes;
then state 3: the input data is written in the buffer, if, signal E = HE1. $\overline{L}$ is present, where L indicates that the output sequence control unit is in state 1 or in state 2, which states will be defined further, and corresponds to the reading of a character of of a tabulation address from the buffer;
state 2: acknowledgment signal ACK from the buffer to the exterior control unit controls the cancellation of strobe signal SE, and, when the latter is out
return to state 0.

FIG. **12** shown the flow diagram of unit **316.**

When signal OKS is present (which means that there is at least one data recorded in buffer **301**) the output sequence control unit controls the transfer of data recorded at address AS **301** into an 8 bits output register **314.**

As already indicated, these data are either "print codes" i.e. codes giving rise to character printing (they are essentially character codes), or "function codes" such as, tabulation, line feed, all of the function codes giving rise to a forced return of the head to the rest position.

The data at output of register **314** are decoded in decoder **318.** If a character code is recognized by the latter, it increments a character counter **310** the content CC of which must not exceed the number, 133, of characters per line. If it is a function code that is recognized, counter **316** is reset to zero.

If, at a given instant, the buffer is empty ($\overline{OKS}$) and if the last code read out from the buffer was not a function code, the content CC of character counter **310** which is ≠ 0 is memorized in a counter decounter **312** the count of "+" input of which is coupled to counter **310** and the decount or "—" input is coupled to the output of buffer **301;** MCC represents the value stored in counter-decounter **312.** Simultaneously counter **310** is reset to zero and the code FCR (forced return of the head) is placed by means of a carriage return signal generator **311** in register **314** from where it is fed to the print logic. (Codes CR and FCR are similar, the letter F being only used here for indicating that the head return control is not generated by an input data instruction but elaborated by the control unit).

Signal CR is also generated by generator **402** (a coder generating an 8 bit signal code) when the content CC of counter **310** is equal to N + 1, N being the maximum number of characters print on a line, for example N = 133.

When signal OKS appears again (i.e. when at least one further data has been recorded in buffer **301**), this data is fed to register **314.**

If it is not a function data, the content of counter-decounter **312** is read out.

If it differs from zero, the print logic will receive a number of spacing orders equal to the content MCC of counter-decounter **312,** before the print control signal is appplied to the print logic.

This circuit allows for tabulating at any desired address on a line. Tabulation code HT, memorized before the next character, enables the memorization in counter-decounter **312** of number of spaces to be tabulated from the beginning of the line to the next printed character.

When a signal appears at the output of buffer **301** it triggers the "—" input of counter-decounter **312,** thus initiating the de-counting of the latter until its reset to zero, during which the counter-decounter **312** sends to register **314** spaces signals ESP which are applied to the print logic, thus giving rise to the displacement of the head along the anvil, no printing operation being then carried out. To this end a flip-flop **319** is set to "1" state by decoder **318** when the code HT is recognized. Flip-flop **319,** when in state 1, triggers sequence unit **317** which then increments counter **303** so as to skip in buffer **301** the address AD of the tabulation and to reset the flip-flop to zero.

Output sequence control unit is built up by three bistable devices HL_1, HL_2, HL_3; it may be triggered to eight different states according to the following table.

HL_3	HL_2	HL_1	State
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

-continued

HL_3	HL_2	HL_1	State
1	1	0	6
1	1	1	7

Only seven states are utilized (0, 1, 2, 3, 4, 6 and 7) according to the flow diagram shown in FIG. **12.**

The time chart of FIG. **14** illustrates the operation of sequence control unit **316** and **317.**

In this figure the numerals within circle indicate the state of the unit concerned, according to the tables hereinbefore given.

Starting from the top of the figure

Line 1 represents the pulses H from the master clock **503.**

Line 2 represents signal SE. It is applied by the exterior control device at any time together with a data information, and lasts until acknowledgment signal ACK from the buffer to the exterior control device has been registered by the latter.

The first clock pulse appearing after the beginning of signal SE triggers unit **316** from the state (0) shown in line **3** to the state (1) shown line **4.** State (1) lasts until signal $\overline{L}$ triggers it to the state (3) shown line **5.** It is recalled that signal $\overline{L}$ indicates that no reading operation is being carried out at this time. State (3) corresponds to a writing time into the buffer. When the writing is achieved, signal ACK triggers the unit **316** to state (2), shown line **6.**

Line **7** shows the portion of time (W) necessary for the writing: it is the sum of the time allotted to state (1) during which the address is stabilized and that to state (3) during which the writing proper is effected. When the writing is achieved signal OKS may appear (line **8**). Then, the next clock pulse triggers the sequence control unit from state (0) (line **9**) to state (1) or to state (2) (line **10**) according to whether a tabulation data has been recognized (state 2) or not (state 1). The next clock pulse triggers the unit to state (3) (line **11**) during which various functions are carried out as precedingly indicated and as illustrated in the flow diagram of FIG. **13.**

If there is a signal CI (i.e. if a character data has been decoded), the next clock pulse triggers unit **317** to state (7). The acknowledgment signal PEC (line **13**) from the print logic triggers unit **317** to state (5). Next clock pulse starts state (4) during which signal CRF if any is recognized.

At line **16** are shown the respective times allotted to the writing in the buffer and to the reading of the latter.

In order to facilitate the complete comprehension of the functioning of the device, one will examine in detail three specific cases chosen among those which present themselves in practice.

FIRST CASE

At the moment when the print is terminated, it is considered that the x characters constituting the text are all stored in the buffer **301** (i.e. OKS = 1 during all the edition process, and that only the last character corresponds to a "function" as recognized by an appropriate decoder **318** connected to the output of register **314**).

At the time of the passage of the sequence control unit **317** in state (1), the register **314** is loaded by the character to be printed. During state 3, the incrementation of the counter **303** is solely carried out since MCC = 0. During state 7, the print control CI is sent to the printer by the sequence control unit **317** and the counter **310** is incremented. This time ends when the acknowledgment signal PEC has been received by the sequence control unit **317.** From the state 4, the sequence control unit **317** evolves towards the time 0 as in the case considered, no signal CRF is applied to the sequence control unit **317** (which is the case, either when the contents of the counter **310** are CC = 0, or when, OKS being present, CC is different from the maximum number of characters that the printer may print in a single line).

The cycle of the output sequence control unit **317** is pursued in synchronism with the printer, and permits the striking of the $x - 1$ characters.

The last character being a function, the 10th cycle of the sequence control unit **317** causes, the latter being in state 7, the resetting to zero of the counter **310** by the sequence control unit **317.** Once the function is executed, the sequence control unit **317** comes back to the state 0 to wait a new output authorization signal OKS.

SECOND CASE

It is considered that, when x characters are printed, OKS = 0, although the line comprises $x + y$ characters, and that only the $(x + y)$th is a recognized "function".

For the printer comprising **132** characters per line, the counter **310** then supplies a signal CRF indicating a forced return of the head, either when its content CC = 132, or when, in the absence of OKS, CC is different from zero. For the $x - 1$ characters, the functioning is identical to the one of the first case.

When, for the xth character, the sequence control unit **317** passes through the state 4, the signal CRF is present. The sequence control unit **317** is arranged so that, under these conditions, the transition from state 4 to state 6 is achieved. At state 6, the code "return carriage" CR is forced in the register **314** and the contents CC are memorized in auxiliary counter **312.**

The forced return of the printing head is achieved by the printer during the course of the following times 7 and 5. During state 4, signal CRF is no longer present (since, now, CC = 0) and as a result, the sequence control unit **317** evolves towards the state 0.

The printing head having come back to rest, when new characters are introduced in the register **301,** OKS is validated thus permitting the generation of spaces by passing x times to the state 3 with the condition MCC $\neq$ 0. These x spaces once generated, the printing of y characters is carried out as in the first case.

THIRD CASE

The case of the tabulation is considered, with the presence of OKS during all the operation (which occurs, in the most general cases, during a tabulation). As explained above, register **301** contains a first text, say A, to be edited, A being followed by the tabulation code HT furnished by the decoder **318,** in turn followed by the tabulation address AD and a second text, say B.

The edition of the text A is carried out through the evolution of the sequence control unit **317** according to the cycle 0, 1, 3, 7, 5, 4, 0. When the code HT arrives in the register **314,** signal CR is tranferred in this register and the tabulation flip-flop **319** is set to 1. This flip-flop thus memorizes the code HT and authorizes the passage of the sequence control unit **317** from the state

0 to the state 2. The sequence control unit **317** is arranged for memorizing in that state the tabulation address (RAM → MCC) and to advance the counter **303** so as to skip in the memory **301** the address AD and to reset the flip-flop **319** to zero. This flip-flop being reset, the sequence control unit realizes the transitions through the times 0, 1, 3.

By passing to the state 3, since the condition RP ≠ FONC and MCC ≠ **0** is validated, the counter **312** counts down and spaces are executed until MCC becomes nil (this is carried out by evolution of the sequence control unit **317** along the cycle 0, 1, 3, 7, 5, 4, 0). When MCC = 0, the edition of the text B is carried out from the address AD + 1.

FIG. **13** represents a possible mode of utilization of the device.

The following circuits have been shown:

Block **15** represents the control unit (ref. FIG. **2**) associated circuits (which are of the type illustrated in FIG. **3**), intended for the memorization of characters to be edited.

Block P represents the printer (mechanism and print logic **12**) (ref. FIG. **1** and **2**).

A keyboard **403** permits the generation of the different characters to be edited as well as signals SE, CI and the function data instruction applied to input **14.**

A distant computer **404** towards which may eventually be dispatched the messages generated from the keyboard **403.**

Two transmit receive equipment **405, 406,** including modulation means are disposed, in this eventuality, at the extreme ends of the line **407** (a telephone line, for example).

The interrupted lines of FIG. **15** correspond to a functioning of the type exclusively pseudo-incremental; the continuous lines correspond to a functioning which can include, in addition, a possibility of teleprinting, the computer then supplying signals SE, CI together with the data input signals for the printer.

In FIG. **15,** the main modes of operation to be described below have been put into evidence and illustrate the versatility of utilization of the device.

(a) and (d): local utilization of the "typewriter" type.

(c) and (d): utilization as an output terminal;

(a) (b) and (d): utilization as teleprinter terminal with a copy in "local";

(b) (c) and (d): utilization as a teleprinter.

FIG. **16** represents other utilization possibilities of the device. The same notations, as in FIG. **15,** have been used in FIG. **16.** In addition to the possibilities of operating in the local mode characterized by a connection of the keyboard **403** to the logic circuit **401** and to the FIN generator **402** both in control unit **15,** through the links (a) and (d) and to the possibilities of a dialogue with the computer **404,** as already mentioned, FIG. **16** puts into evidence a utilization possibility of the "display" type: the informations destined for the computer **404** are introduced from the keyboard **403** in the logic circuit **401** following the link (a), but can only be transmitted towards the computer **404** after validation by a special key of the keyboard (line a): they then take up the link (e) and come back through the links (c) and (d).

In the different utilization cases, the disclosed buffer device permits operation — even though the acquisition speed of characters is below the printer nominal printing rate — to achieve the printing of a line of characters by conferring to the printing head several successive translation movements, separated from each other by a return of the printing head to the beginning of the same line. Its use thus confers to the series printers, and particularly of the needles type, a very great versatility of utilization.

The arrows and references in FIG. **14** aim to better show the correspondence between states and signals.

We claim:

1. A control unit for controlling a printer (P) of the type comprising a print logic (**12**) having a data input, a constant drive mechanism (**11**), an anvil (**2**) and a printing head (**1**), selectively driven by said mechanism through energization of a clutch (**10**), parallel to said anvil and automatically returned to a rest position upon deenergization of said clutch by means of a biasing device (**6**), said control unit being inserted between said data input and said print logic, and comprising:

a register (**16,314**), having an output coupled to said print logic, and an input, for storing momentarily a single data;

a buffer (**101, 301**) having an input line for sequentially receiving digitally coded data and an output line for sequentially transmitting digitally coded data to said register;

buffer input address means (**17**) permanently defining the address in the buffer of the last character entered on said input line;

buffer output address means (**18**) permanently defining the address in the buffer of the first character which is ready for transfer on said ouput line;

comparator means (**19**) permanently comparing said first mentioned address with the buffer maximum address and with said second mentioned address;

sequence control means (**20**) authorizing, depending on the result of said comparison, the entry of a character on the input line or the transfer of a character on the ouput line;

means for memorizing the position reached by the printing head each time the said addresses coincide, for then controlling the return of the printing head at the rest position, and for controlling, when new characters are entered after such a coincidence, a rapid space motion of the printing head along the anvil until the said memorized position is passed.

2. A control unit as claimed in claim **1,** wherein said input and output address means include respectively a first and a second counters (**302, 303**) respectively incremented by one each time a character is entered on said input line and each time a character is edited.

3. A control unit as claimed in claim **1,** wherein said means for memorizing the position reached by the printing head include a third counter (**310**) incremented by one for each translation of the printing head by an elementary step and a counter-decounter (**312**), in which the contents of the third counter are transferred at each of the said coincidences, the content of the counter-decounter being decreased by one for each of said elementary steps, the control unit further comprising means for authorizing the edition of the first characters memorized in the buffer when the content of the counter-decounter is nil.

4. A control unit as claimed in claim **2,** further comprising means for detecting a tabulation code, and means (fip-flop **319,** decoder **318,** counter **310,** counter-decounter **312**) for increasing the count of the second counter and preventing the edition of any character until the said count passes the tabulation address.

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