



(51) International Patent Classification:

B06B 1/02 (2006.01) *H02M 3/158* (2006.01)
H01L 41/04 (2006.01) *B06B 1/06* (2006.01)

(21) International Application Number:

PCT/GB2021/052210

(22) International Filing Date:

26 August 2021 (26.08.2021)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

17/092,613 09 November 2020 (09.11.2020) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(54) Title: DRIVER CIRCUITRY

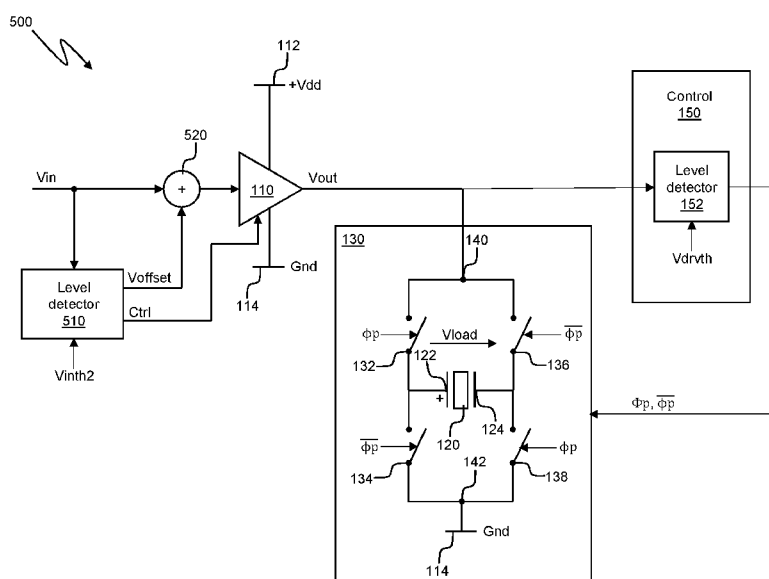


Figure 6

(57) **Abstract:** The present disclosure relates to circuitry for driving a load. The circuitry comprises driver circuitry configured to generate a drive signal, based on an input signal to the driver circuitry, for driving the load, and commutator circuitry for coupling the driver circuitry to the load. The commutator circuitry is configured to alternate between commutation states in response to a level of the drive signal meeting a drive signal threshold or in response to a level of the input signal meeting a first input signal threshold. The circuitry is configured to apply an offset to the input signal when the input signal is below a second input signal threshold so as to increase a minimum level of the drive signal above the drive signal threshold or to increase a minimum level of the input signal above the first input signal threshold.



(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

DRIVER CIRCUITRY

Field of the Invention

5 The present disclosure relates to driver circuitry, and in particular to driver circuitry for capacitive loads. Examples of capacitive loads include piezoelectric transducers, MEMS transducers and electrostatic transducers.

Background

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Piezoelectric transducers are increasingly being seen as a viable alternative to transducers such as speakers and resonant actuators for providing audio and/or haptic outputs in devices such as mobile telephones, laptop and tablet computers and the like, due to their thin form factor, which may be beneficial in meeting the demand for increasing functionality in such devices without significantly increasing their size. Piezoelectric transducers are also increasingly finding application as transducers for ultrasonic sensing and range-finding systems.

Summary

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According to a first aspect, the invention provides circuitry for driving a load, the circuitry comprising:

driver circuitry configured to generate a drive signal, based on an input signal to the driver circuitry, for driving the load; and

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commutator circuitry for coupling the driver circuitry to the load, wherein the commutator circuitry is configured to alternate between commutation states in response to a level of the drive signal meeting a drive signal threshold or in response to a level of the input signal meeting a first input signal threshold,

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wherein the circuitry is configured to apply an offset to the input signal when the input signal is below a second input signal threshold so as to increase a minimum level of the drive signal above the drive signal threshold or to increase a minimum level of the input signal above the first input signal threshold.

The load may comprise a capacitive load.

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The load may comprise a piezoelectric transducer.

The second input signal threshold is dependent upon an expected maximum level of the drive signal.

- 5 The second input signal threshold may be such that the commutator circuitry remains in a single commutation state until the level of the drive signal is within 6dB of the expected maximum level of the drive signal.

The offset may be a fixed offset.

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Alternatively, the offset may be variable according to a level of the input signal.

The circuitry may further comprise level detector circuitry configured to detect a level of the input signal.

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The level detector circuitry may comprise envelope detector circuitry configured to detect an envelope of the input signal.

- 20 The circuitry may further comprise a summing node configured to receive the input signal and an offset signal output by the level detector circuitry and to output a signal to the driver circuitry.

The circuitry may further comprise control circuitry configured to control operation of the commutator circuitry.

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The control circuitry may comprise:

level detector circuitry configured to output a control signal to the commutator circuitry each time the level of the drive signal meets the drive signal threshold.

- 30 The control circuitry may comprise:

level detector circuitry configured to output a control signal to the commutator circuitry each time the level of the input signal meets the first input signal threshold.

- 35 The driver circuitry may be selectively configurable to generate a drive signal that is shaped to take into account the effect of commutation of the drive signal that occurs when the level of the drive signal meets the drive signal threshold.

The level detector circuitry may be configured to output a control signal to control the configuration of the driver circuitry based on the detected level of the input signal.

- 5 The circuitry may further comprise controllable compressor circuitry configured to apply a controllable gain to the input signal so as to control a rate of change of the offset applied to the input signal, the controllable gain based on a level of the input signal.

According to a second aspect, the invention provides circuitry for driving a load, the
10 circuitry comprising:

driver circuitry configured to generate a drive signal, based on an input signal to the driver circuitry, for driving the load;

commutator circuitry configured to commutate the drive signal between first and second terminals of the load,

- 15 wherein the circuitry is configured to prevent commutation of the drive signal when a level of the input signal is below a threshold.

According to a third aspect, the invention provides circuitry for driving a load, the circuitry comprising:

- 20 driver circuitry configured to generate a drive signal, based on an input signal to the driver circuitry, for driving the load;

level detector circuitry configured to detect a level of the drive signal or a level of the input signal; and

- commutator circuitry for supplying the drive signal to either a first terminal or a
25 second terminal of the load based on an output of the level detector circuitry,

wherein the circuitry is configured to apply an offset to the input signal when the level of the input signal is below a predetermined input signal threshold.

According to a fourth aspect, the invention provides circuitry for driving a load, the
30 circuitry comprising:

driver circuitry configured to generate a drive signal, based on an input signal to the driver circuitry, for driving the load,

wherein the circuitry is configured to apply an offset to the input signal, and

wherein the offset is a function of the input signal level.

The circuitry may further comprise level detector circuitry configured to detect a level of the input signal and to control the offset based on the detected level of the input signal.

5 The level detector circuitry may comprise envelope detector circuitry configured to detect an envelope of the input signal.

10 The circuitry may further comprise a summing node configured to receive the input signal and an offset signal output by the level detector circuitry and to output a signal to the driver circuitry.

The circuitry may further comprise controllable compressor circuitry configured to apply a controllable gain to the input signal so as to control a rate of change of the offset applied to the input signal, the controllable gain based on a level of the input signal.

15 According to a fifth aspect the invention provides an integrated circuit comprising the circuitry of any of the first to fourth aspects.

20 According to a sixth aspect the invention provides a device comprising the circuitry of any of the first to fourth aspects. The device may comprise, for example, a mobile telephone, a tablet or laptop computer, a gaming device, an accessory device, a headset, headphones, earphones, a smart speaker.

Brief Description of the Drawings

25 Embodiments of the invention will now be described, strictly by way of example only, with reference to the accompanying drawings, of which:

Figure 1 is a schematic diagram illustrating example circuitry for driving a load such as a piezoelectric transducer;
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Figures 2a and 2b illustrate different commutation states of the circuitry of Figure 1;

Figure 3 is a schematic diagram illustrating alternative example circuitry for driving a load such as a piezoelectric transducer;
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Figure 4 illustrates a drive signal, a control signal and a voltage across a load during operation of the circuitry of Figure 1 for a relatively large drive signal;

Figure 5 illustrates a drive signal, a control signal and a voltage across a load during
5 operation of the circuitry of Figure 1 for a relatively small drive signal;

Figure 6 is a schematic diagram illustrating example circuitry for driving a load such as a piezoelectric transducer according to the present disclosure;

10 Figure 7 illustrates a drive signal, a control signal and a voltage across a load during operation of the circuitry of Figure 6 for a relatively small drive signal;

Figure 8 is a schematic diagram illustrating alternative example circuitry for driving a load such as a piezoelectric transducer according to the present disclosure;

15 Figure 9 illustrates the application of a fixed DC offset to an input signal;

Figure 10 is a schematic diagram illustrating alternative example circuitry for driving a load such as a piezoelectric transducer according to an aspect of the present disclosure;
20 and

Figures 11a and 11b illustrate the application of a variable DC offset to an input signal.

Detailed Description

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Figure 1 is a schematic diagram illustrating example circuitry for driving a load such as a piezoelectric transducer or some other capacitive load such as a MEMS transducer or an electrostatic transducer. The circuitry, shown generally at 100 in Figure 1, includes driver circuitry 110, which in this example receives a power supply from positive (+V_{dd}) and ground (Gnd) power supply rails 112, 114. The driver circuitry 110 receives an input
30 signal V_{in} and generates a drive signal V_{out}, based on the input signal, for driving a piezoelectric transducer 120.

The circuitry 100 further includes commutator circuitry 130, which in the illustrated
35 example includes first to fourth controllable switches 132 – 138. The commutator circuitry 130 is coupled to control circuitry 150 so as to receive control signals ϕ_p , $\overline{\phi_p}$ for

controlling the operation of the controllable switches 132 – 138, as will be described in more detail below.

5 The first controllable switch 132 is coupled between a first node 140 of the commutator circuitry 130 and a first terminal 122 of the piezoelectric transducer 120. The first node 140 of the commutator circuitry 130 is coupled to an output of the driver circuitry 110 so as to receive the drive signal V_{out} .

10 The second controllable switch 134 is coupled between the first terminal 122 of the piezoelectric transducer 120 and the ground voltage supply rail 114.

The third controllable switch 136 is coupled between the first node 150 of the commutator circuitry 130 and a second terminal 124 of the piezoelectric transducer 120.

15 The fourth controllable switch 138 is coupled between the second terminal 124 of the piezoelectric transducer 120 and the ground voltage supply rail 114.

20 By selectively opening and closing the controllable switches 132 – 138, one of the first and second terminals 122, 124 of the piezoelectric transducer 120 can be coupled to the output of the driver circuitry 110, and the other of the first and second terminals 122, 124 of the piezoelectric transducer 120 can be coupled to the ground voltage supply rail 114.

25 As shown in **Figure 2a**, when the control signal ϕ_p causes the first and fourth switches 132, 138 to close, the control signal $\overline{\phi_p}$ (which is the inverse of the control signal ϕ_p) causes the second and third switches 134, 136 to open, thus coupling the first terminal 122 of the piezoelectric transistor 122 to the output of the driver circuitry 110 so as to receive the drive signal V_{out} , and the second terminal 124 to the ground supply voltage rail 114. Thus in the configuration or commutation state shown in Figure 2a the voltage V_{load} across the piezoelectric transducer is equal to V_{out} .

30 As shown in **Figure 2b**, when the control signal ϕ_p causes the first and fourth switches 132, 138 to open, the control signal $\overline{\phi_p}$ causes the second and third switches 134, 136 to close, thus coupling the first terminal 122 of the piezoelectric transistor 122 to the ground supply voltage rail 114, and the second terminal 124 to the output of the driver circuitry 110 so as to receive the drive signal V_{out} . Thus in the configuration or

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commutation state shown in Figure 2a the voltage V_{load} across the piezoelectric transducer is equal to $-V_{out}$.

The control circuitry 150 may comprise, for example, level detector circuitry 152
5 configured to receive the drive signal V_{out} and a drive signal threshold V_{drvth} , and to output the control signals ϕ_p and $\overline{\phi_p}$ each time the level of the drive signal V_{out} meets or crosses the drive signal threshold V_{drvth} . The values of the control signals ϕ_p and $\overline{\phi_p}$ alternate each time the level of the drive signal V_{out} meets or crosses the drive signal threshold V_{drvth} such that, for example, the first time the level of the drive signal V_{out}
10 meets or crosses the drive signal threshold V_{drvth} , the value of the control signal ϕ_p is low or logic 0 and the value of the control signal $\overline{\phi_p}$ is high or logic 1, and the second time the level of the drive signal V_{out} meets or crosses the drive signal threshold V_{drvth} , the value of the control signal ϕ_p is high or logic 1 and the value of the control signal $\overline{\phi_p}$ is low or logic 0.

15

The operation of the controllable switches 132 – 138 is thus controlled by the control circuitry 150 based on a level of the drive signal V_{out} , such that each time the level of the drive signal V_{out} meets or crosses the drive signal threshold value, which in this example is 0 volts, the commutator circuitry 130 couples the output of the driver circuitry
20 110 to a different one of the first and second terminals 122, 124 of the piezoelectric transducer 120.

For example, if in a first phase of operation the first and fourth switches 132, 138 are closed and the second and third switches 134, 136 are open (i.e. the commutator circuitry
25 130 adopts the commutation state shown in Figure 2a), in a second phase of operation, which is triggered when the level of the drive signal V_{out} meets or crosses the drive signal threshold value, the second and third switches 134, 136 are closed and the first and fourth switches 132, 138 are opened (i.e. the commutator circuitry 130 adopts the commutation state shown in Figure 2b). In a subsequent third phase of operation, which
30 is triggered the next time the level of the drive signal V_{out} meets or crosses the drive signal threshold value, the first and fourth switches 132, 138 are again closed and the second and third switches 134, 136 are again opened (i.e. the commutator circuitry 130 again adopts the commutation state shown in Figure 2a).

Thus, the commutator circuitry 130 is configured to commutate the drive signal V_{out} between the first and second terminals 122, 124 of the piezoelectric transducer 120 on alternate drive signal threshold crossings of the drive signal V_{out} .

- 5 In an alternative arrangement, shown generally at 200 in **Figure 3**, the level detector circuitry 152 is configured to receive the input signal V_{in} and a first input signal threshold V_{inth1} , and to output the control signals ϕ_p and $\overline{\phi_p}$ each time the level of the input signal V_{in} meets or crosses the first input signal threshold V_{inth1} . The values of the control signals ϕ_p and $\overline{\phi_p}$ alternate each time level of the input signal V_{in} meets or crosses the
- 10 first input signal threshold V_{inth1} such that, for example, the first time the level of the input signal V_{in} meets or crosses the first input signal threshold V_{inth1} , the value of the control signal ϕ_p is low or logic 0 and the value of the control signal $\overline{\phi_p}$ is high or logic 1, and the second time the level of the input signal V_{in} meets or crosses the first input signal threshold V_{inth1} , the value of the control signal ϕ_p is high or logic 1 and the value
- 15 of the control signal $\overline{\phi_p}$ is low or logic 0.

The operation of the controllable switches 132 – 138 in the alternative arrangement of Figure 3 is thus controlled by the control circuitry 150 based on a level of the input signal V_{in} , such that each time the level of the input signal V_{in} meets or crosses the first input

20 signal threshold value V_{inth1} , which in this example is 0 volts, the commutator circuitry 130 couples the output of the driver circuitry 110 to a different one of the first and second terminals 122, 124 of the piezoelectric transducer 120.

For example, if in a first phase of operation the first and fourth switches 132, 138 are

25 closed and the second and third switches 134, 136 are open (i.e. the commutator circuitry 130 adopts the commutation state shown in Figure 2a), in a second phase of operation, which is triggered when the level of the input signal V_{in} meets or crosses the first input signal threshold value V_{inth1} , the second and third switches 134, 136 are closed and the first and fourth switches 132, 138 are opened (i.e. the commutator circuitry 130 adopts

30 the commutation state shown in Figure 2b). In a subsequent third phase of operation, which is triggered the next time the level of the input signal V_{in} meets or crosses the first input signal threshold value V_{inth1} , the first and fourth switches 132, 138 are again closed and the second and third switches 134, 136 are again opened (i.e. the commutator circuitry 130 again adopts the commutation state shown in Figure 2a).

Thus, the commutator circuitry 130 is configured to commutate the drive signal V_{out} between the first and second terminals 122, 124 of the piezoelectric transducer 120 on alternate first input signal threshold crossings of the input signal V_{in} . The first input signal threshold V_{inth1} is determined or selected such that the commutation of the drive signal V_{out} based on the level of the input signal V_{in} has the same effect as commutation of the drive signal V_{out} based on the level of the drive signal V_{out} in the arrangement shown in Figure 2. For example, if the drive signal threshold V_{drvth} in the arrangement of Figure 2 is 0v, then the same commutation effect can be achieved in the arrangement of Figure 3 by setting the first input signal threshold V_{inth1} to 0v. However, if the drive signal threshold V_{drvth} in the arrangement of Figure 2 has a value other than 0v, then the same commutation effect can be achieved in the arrangement of Figure 3 by setting the first input signal threshold V_{inth1} to a value equivalent V_{drvth} scaled to take into account any gain applied by the driver circuitry 110.

As will be appreciated by those of ordinary skill in the art, the commutation arrangements 100, 200 shown in Figures 1 and 3 have the effect of doubling the effective voltage swing across the piezoelectric transducer 120. This effect is illustrated in **Figure 4**, which shows examples of the driver circuitry drive signal V_{out} (trace 310), the control signal ϕ_p (trace 320) and the voltage V_{load} across the piezoelectric transducer 120 (trace 330) of the circuitry 100 over time.

As can be seen in Figure 4, during a first phase of operation of the circuitry 100 (from 0 to 20 μ s) in which the drive signal V_{out} has a positive value, the control signal ϕ_p is high, such that the commutator circuitry 130 adopts the commutation state or configuration shown in Figure 2a, and the voltage V_{load} across the piezoelectric transducer 120 follows the drive signal V_{out} , since $V_{load} = V_{out}$.

At around 20 μ s the level of the drive signal V_{out} falls to 0V. At this point the control signal ϕ_p goes low, such that the circuitry 100 enters a second phase of operation in which the commutator circuitry 130 adopts the commutation state or configuration shown in Figure 2b, and the voltage V_{load} across the piezoelectric transducer 120 is inverted with respect to the drive signal V_{out} , since $V_{load} = -V_{out}$.

At around 40 μ s the level of the drive signal V_{out} again falls to 0V. At this point the control signal ϕ_p goes high again, such that the circuitry 100 enters a third phase of operation in which the commutator circuitry 130 returns to the commutation state or configuration

shown in Figure 2a, and the voltage V_{load} across the piezoelectric transducer 120 again tracks the drive signal V_{out} , since $V_{load} = V_{out}$.

Thus, the voltage swing of the voltage V_{load} across the piezoelectric transducer 120 over the first and second phases of operation of the circuitry 100 is effectively twice what it would be if no commutation of the output voltage V_{out} were to occur (assuming that the magnitude of V_{out} is equal in the first and second phases).

This effective doubling of the voltage swing across the piezoelectric transducer 120 is useful where large displacements of the piezoelectric transducer 120 are required, as such displacements can be produced using relatively small driver circuitry output signals.

Where smaller displacements of the piezoelectric transducer 120 are required, commutation of the drive signal V_{out} is not necessary, because the desired displacement can be produced using a smaller voltage swing across the piezoelectric transducer 120.

However, as the control circuitry 150 of the circuitry 100 of Figure 1 triggers commutation each time the drive signal V_{out} meets the drive signal threshold, commutation still occurs in the circuitry 100 even when it is not required.

This is illustrated in **Figure 5**, which shows examples of a driver circuitry drive signal V_{out} (trace 410) that is smaller than the example shown at 310 in Figure 4, the control signal ϕ_p (trace 420) and the voltage V_{load} across the piezoelectric transducer 120 (trace 430) of the circuitry 100 over time. As can be seen, the control signal ϕ_p is the same for the smaller driver circuit output signal 410 as for the larger signal 310, which leads to a swing of the voltage V_{load} across the piezoelectric transducer 120 over the first and second phases of operation of the circuitry 100 that is effectively twice what it would be if no commutation of the output voltage V_{out} were to occur (assuming that the magnitude of V_{out} is equal in the first and second phases).

This unnecessary commutation leads to unnecessary switching losses, power consumption and noise.

Figure 6 is a schematic diagram illustrating example circuitry for driving a load (in this example a piezoelectric transducer, but it is to be understood that the circuitry illustrated is equally suited to driving another load such as a MEMS transducer or an electrostatic

transducer) according to the present disclosure. The circuitry, shown generally at 500 in Figure 6, includes a number of elements in common with the circuitry 100 of Figure 1. Such common elements are denoted by common reference numerals in Figures 1 and 6 and will not be described again in detail here. Although in the example shown in Figure 6 the level detector circuitry 152 of the control circuitry 150 is shown as receiving the drive signal V_{out} and the drive signal threshold V_{drvth} , as in the arrangement shown in Figure 1, it will be appreciated by those skilled in the art that the level detector circuitry 152 could equally receive the input signal V_{in} and the first input signal threshold V_{inth1} , as described above with reference to Figure 3.

10

The circuitry 500 includes second level detector circuitry 510 and a summing node 520. The summing node 520 is configured to receive, at a first input thereof, the input signal V_{in} , and at a second input thereof an offset signal V_{offset} output by the second level detector circuitry 510. An output of the summing node 520 is coupled to an input of the driver circuitry 110, such that the summing node outputs a signal $V_{in} + V_{offset}$ to the driver circuitry 110. As will be recalled, the output V_{out} of the driver circuitry 110 is based on the signal input to the driver circuitry 110, and thus in the example illustrated in Figure 5 the drive signal V_{out} is based on the signal $V_{in} + V_{offset}$ that is input to the driver circuitry 110.

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The second level detector circuitry 510, which may comprise, for example, envelope detector circuitry, is configured to receive the input signal V_{in} and to detect a level, e.g. an envelope, of the input signal V_{in} , and to compare the detected level of the input signal V_{in} to a second input signal threshold V_{inth2} . If the detected input signal level is equal to or greater than the second input signal threshold V_{inth2} , the second level detector circuitry 510 outputs no offset signal V_{offset} (or equivalently, outputs an offset signal V_{offset} of value 0 volts). If, however, the detected input signal level is less than the second input signal threshold V_{inth2} , the second level detector circuitry 510 outputs a positive DC offset signal V_{offset} , which is added to the input signal V_{in} by the summing node 520.

30

The purpose of the DC offset signal V_{offset} is to raise the level of the drive signal V_{out} such that a minimum level of the drive signal V_{out} is greater than the drive signal threshold V_{drvth} that triggers commutation of the drive signal V_{out} , or equivalently (where commutation is based on the level of the input signal V_{in} , as in the arrangement shown in Figure 3) to raise the level of the input signal V_{in} such that a minimum level of

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the input signal V_{in} is greater than the first input signal threshold V_{inth1} that triggers commutation of the drive signal V_{out} . By raising the level of the output or input signal in this way, commutation can be effectively disabled for input signals V_{in} for which commutation is not necessary to achieve a desired displacement of the piezoelectric transducer 120, thereby avoiding unnecessary commutation and the attendant switching losses, power consumption and noise.

For example, where the input signal V_{in} is an audio signal, the DC offset signal V_{offset} can be applied as a function of the volume of the input audio signal. Thus if the level of the input signal V_{in} is lower than the second input signal threshold V_{inth2} , the DC offset signal can be applied to the input signal V_{in} to effectively disable commutation of the drive signal V_{out} . If the level of the input signal V_{in} increases to the extent that it meets or exceeds the second input signal threshold V_{inth2} , the DC offset signal V_{offset} is no longer applied to the input signal V_{in} and thus commutation of the drive signal V_{out} is enabled. If the level of the input signal V_{in} subsequently falls below the second input signal threshold V_{inth2} , the DC offset signal can again be applied to the input signal V_{in} , thus again effectively disabling commutation of the drive signal V_{out} .

The DC offset signal V_{offset} may be of a fixed level. Using a fixed DC offset ensures that the minimum level of the drive signal V_{out} is always greater than the drive signal threshold and thus does not trigger commutation. However, this can lead to a large difference between the minimum level of the drive signal V_{out} and the drive signal threshold, which can increase power consumption unnecessarily.

Thus it may be preferable for the DC offset signal V_{offset} to be variable according to the detected level of the input signal V_{in} . This allows the DC offset signal V_{offset} to be tailored to ensure that the minimum level of the drive signal V_{out} is just above the drive signal threshold V_{drvth} , so as to avoid unnecessary commutation of the output signal, without unnecessarily increasing power consumption.

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The second input signal threshold V_{inth2} may be set such that commutation is prevented until the drive signal V_{out} is within 6dB of an expected maximum or full-scale level of the drive signal V_{out} , i.e. the input signal threshold V_{inth} may be set such that commutation is prevented (e.g. the commutator circuitry 130 remains in a single commutation state) when a level, e.g. an amplitude or envelope, of the drive signal V_{out} is below approximately 50% of an expected full scale level of the drive signal V_{out} . Thus the

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second input signal threshold V_{inH2} will be dependent upon the expected maximum or full-scale level or amplitude of the drive signal V_{out} , which will be dependent on the particular application of the circuitry 500. For example, if the circuitry 500 is for use in a parking sensor system, the expected full scale amplitude of V_{out} may be greater than if
5 the circuitry is for use in an audio device.

Figure 7 illustrates the effect of the offset signal V_{offset} on the drive signal V_{out} , the control signal ϕ_p and the voltage V_{load} across the piezoelectric transducer 120 (trace 430) of the circuitry 100 over time. As can be seen from trace 610, the drive signal V_{out}
10 never reaches 0 volts, and so the drive signal threshold is never met. The effect of this is that the control signal ϕ_p (trace 620) remains high, such that commutation does not occur, and the voltage V_{load} (trace 630) across the piezoelectric transducer 120 tracks the driver output voltage V_{out} .

It will be noted that in Figure 7 the drive signal V_{out} has a different shape than the drive signal V_{out} in Figures 4 and 5, in that trace 610 of Figure 7 shows an example drive signal having positive and negative half-cycles about a DC offset of approximately 0.5v, whereas traces 310 and 410 of Figures 4 and 5 respectively show example drive signals having only positive half-cycles with no DC offset. This is because in the examples
20 illustrated in Figures 4 and 5 the driver circuitry 110 is configured to output a drive signal V_{out} that is shaped to take into account the effect of the commutation of the drive signal V_{out} , in order to achieve a desired signal V_{load} across the piezoelectric transducer 120. In contrast, as commutation does not occur in the example illustrated in Figure 7, the drive signal V_{out} need not take into account the effect of commutation, and thus the drive
25 signal V_{out} can be the same shape as the desired signal V_{load} across the piezoelectric transducer 120.

In the circuitry 500 of Figure 6, the driver circuitry 110 maybe selectively configurable to shape the drive signal to take into account the effect of the commutation of the drive
30 signal V_{out} that occurs at high input signal levels (i.e. when the input signal V_{in} is equal to or greater than the input signal threshold V_{inH}).

Thus, in addition to the positive DC offset signal V_{offset} , the second level detector circuitry 510 may also output a control signal $Ctrl$ to the driver circuitry 110 if the detected
35 input signal level is less than the input signal threshold V_{inH} , to adjust a configuration of the driver circuitry 110 such that the driver circuitry 110 does not shape the drive signal

Vout to take into account the effect of the commutation of the drive signal Vout. If the detected input signal level is equal to or greater than the input signal threshold V_{inth} , the second level detector circuitry 510 may not output the control signal Ctrl, such that the configuration of the driver circuitry 110 is not adjusted and thus the driver circuitry 110
5 outputs a shaped drive signal Vout, as in the examples illustrated in Figures 4 and 5. In some examples, instead of providing a separate control signal Ctrl, the DC offset signal Voffset may be used as a control signal to adjust the configuration of the driver circuitry 110 such that shaping of the drive signal Vout is not performed. For example, the DC offset signal Voffset could be output to the driver circuitry 110 as the control signal Ctrl.
10 Alternatively, the driver circuitry 110 may be configured to detect the DC offset signal Voffset in the signal $V_{in}+V_{offset}$ that is input to the driver circuitry 110, and to adjust the configuration of the driver circuitry 110 to disable shaping of the drive signal Vout if the DC offset signal is detected in this way.

15 When the level of the input signal V_{in} changes quickly, there should be a correspondingly quick change in the DC offset signal Voffset, in order to switch between commutating and non-commutating operation of the circuitry 500 with minimal deviation of the signal Vload across the piezoelectric transducer 120 from the desired signal Vload. However, where the input signal V_{in} is an audio signal for generating an audible output at the
20 piezoelectric transducer 120, a quick change in the DC offset signal Voffset will give rise to audible artefacts in the audible output of the piezoelectric transducer 120.

Figure 8 is a schematic diagram illustrating further example circuitry for driving a load (in this example a piezoelectric transducer, but again it will be appreciated that the
25 circuitry is equally suited to driving another load such as a MEMS transducer or an electrostatic transducer) according to the present disclosure, which is configured to mitigate the effects of quick changes in the level of the input signal V_{in} . The circuitry, shown generally at 700 in Figure 8, includes a number of elements in common with the circuitry 500 of Figure 6. Such common elements are denoted by common reference
30 numerals in Figures 6 and 8 and will not be described again in detail here. Although in the example shown in Figure 8 the level detector circuitry 152 of the control circuitry 150 is shown as receiving the drive signal Vout and the drive signal threshold V_{drvth} , as in the arrangement shown in Figure 1, it will be appreciated by those skilled in the art that the level detector circuitry 152 could equally receive the input signal V_{in} and the first
35 input signal threshold V_{inth1} , as described above with reference to Figure 3.

The circuitry 700 includes controllable compressor circuitry 710, which is configured to apply a controllable gain to the input signal V_{in} to adjust its signal level and to output a level-adjusted version V_{in}' of the input signal V_{in} to the second level detector circuitry 510 and the summing node 520, in order to prevent clipping of the drive signal V_{out} , thus
5 avoiding generating audible artefacts in the audible signal output by the piezoelectric transducer 120.

The gain applied by the compressor circuitry 710 is adaptive, depending upon the level of the input signal V_{in} .

10

Thus, where the input signal level increases from a level that is lower than the input signal threshold V_{inth} to a level that exceeds the input signal threshold V_{inth} , the compressor circuitry 710 may apply gain to the input signal V_{in} to reduce its level. Thus instead of falling to zero in a single step, the DC offset V_{offset} output by the second level
15 detector circuitry 510 is reduced over time (at a rate that is lower than an audio frequency range). As the DC offset V_{offset} falls, the compressor circuitry 710 continues to adjust the gain applied to the input signal V_{in} , based on the level of the input signal V_{in} , thus controlling the DC offset that is applied in order to prevent clipping of the drive signal V_{out} whilst still maximising the signal level of the signal that is input to the driver circuitry
20 110.

Similarly, where the input signal level falls from a level that is greater than the input signal threshold V_{inth} to a level that is less than the input signal threshold V_{inth} , the compressor circuitry 710 may apply gain to the input signal V_{in} to increase its level. Thus instead of
25 increasing to a maximum DC offset value in a single step, the DC offset V_{offset} output by the second level detector circuitry 510 is increased over time (at a rate that is lower than an audio frequency range). As the DC offset V_{offset} increases, the compressor circuitry 710 continues to adjust the gain applied to the input signal V_{in} , based on the level of the input signal V_{in} , thus controlling the DC offset that is applied in order to
30 prevent clipping of the drive signal V_{out} whilst still maximising the signal level of the signal that is input to the driver circuitry 110.

In this way the DC offset signal V_{offset} output by the second level detector circuitry 510 can be reduced or increased gradually in a manner that avoids introducing audible
35 artefacts in the audible signal that is generated and output by the piezoelectric transducer 120 in response to the drive signal V_{out} .

In an alternative approach, instead of adjusting the gain applied by the compressor circuitry 710 as the level of the input signal V_{in} increases, the gain applied by the compressor circuitry 710 may be adjusted only when the drive signal V_{out} meets the drive signal threshold V_{drvth} , such that the level of the input signal V_{in} is reduced in response to the drive signal V_{out} meeting the drive signal threshold V_{drvth} .

As will be apparent from the foregoing discussion, the circuitry of the present disclosure allows commutation of the drive signal output by the driver circuitry 110 to be effectively disabled at small output signal levels to avoid unnecessary switching losses, power consumption and noise, whilst also permitting commutation to take place for drive signals that require a higher voltage swing across the piezoelectric transducer, e.g. where a relatively large transducer displacement is required.

As discussed above, the DC offset signal V_{offset} applied to the input signal V_{in} may be variable according to the detected level of the input signal V_{in} . This allows the DC offset signal V_{offset} to be tailored to ensure that the minimum level of the drive signal V_{out} is just above the drive signal threshold V_{drvth} , so as to avoid unnecessary commutation of the output signal, without unnecessarily increasing power consumption.

More generally, in circuitry for driving a piezoelectric transducer (or indeed another load that is capable of handling a DC offset, e.g. a capacitive load such as a MEMS transducer or an electrostatic transducer), it may be desirable to apply a bias voltage (i.e. a fixed DC offset) to an input signal that is received by driver circuitry which generates, based on the input signal, a drive signal.

For example, in driver circuitry (e.g. the driver circuitry 110) that receives its power supply from positive (+Vdd) and 0v or ground (Gnd) supply rails, it is common to add a fixed DC offset (e.g. a bias voltage) to an input signal, to reduce the risk of distortion in the output of the driver circuitry caused by clipping of the input signal.

Typically the DC offset or bias voltage is set to a value equal to the mid-point between Gnd and +Vdd, i.e. $V_{dd}/2$, as shown in **Figure 9**, as this provides sufficient headroom to avoid the effects of clipping. However, such an approach results in unnecessary power consumption at smaller (i.e. less than full-scale) input signal levels.

Figure 10 is a schematic diagram illustrating alternative example circuitry for driving a load such as a piezoelectric transducer, a MEMs transducer or an electrostatic transducer according to an aspect of the present disclosure.

5 The circuitry, shown generally at 900 in Figure 109, includes driver circuitry 910, which in this example receives a power supply from positive (+Vdd) and ground (Gnd) power supply rails 912, 914. The driver circuitry 910 is configured to generate a drive signal Vout, based on an input signal Vin, for driving a load such as a piezoelectric transducer 120 which is coupled between an output of the driver circuitry 910 and the ground supply
10 rail 914.

The circuitry 900 further includes level detector circuitry 920 and a summing node 930. The summing node 930 is configured to receive, at a first input thereof, the input signal Vin, and at a second input thereof an offset signal Voffset output by the level detector
15 circuitry 920. An output of the summing node 930 is coupled to an input of the driver circuitry 910, such that the summing node 930 outputs a signal $V_{in} + V_{offset}$ to the driver circuitry 910. As the output Vout of the driver circuitry 910 is based on the signal input to the driver circuitry 910, the drive signal Vout is based on the signal $V_{in} + V_{offset}$ that is input to the driver circuitry 910.

20

The level detector circuitry 920, which may comprise, for example, envelope detector circuitry, is configured to receive the input signal Vin and to detect a level (e.g. an envelope or a volume), of the input signal Vin and to output a DC offset Voffset as a function of the detected input signal level. Thus the level detector circuitry 920 controls
25 the level of the DC offset based on the detected level (e.g. the envelope or volume) of the input signal.

Thus, instead of applying a fixed DC offset or bias voltage to the input signal, the level of the DC offset Voffset output by the level detector circuitry 920 and applied to the input
30 signal Vin can vary, dependent upon a parameter of the input signal (e.g. a level, envelope or volume of the input signal), such that for smaller input signals a lower DC offset can be applied than for larger input signals, whilst still providing a DC offset that is sufficient to avoid clipping.

35 This is illustrated in **Figures 11a** and **11b**, which show that the DC offset Voffset output by the level detector circuitry 920 and applied to the input signal Vin varies as a function

of the input signal V_{in} . In the examples shown in Figures 11a and 11b the input signal V_{in} is small, and the level of the DC offset output by the level detector circuitry 920 is just high enough in each example to prevent clipping of the input signal. Thus power consumption is reduced (in comparison with the example shown in Figure 9) as the DC offset applied to the input signal V_{in} is no higher than is necessary.

When the level of the input signal V_{in} changes quickly, there should be a correspondingly quick change in the DC offset signal V_{offset} . However, where the input signal V_{in} is an audio signal for generating an audible output at the piezoelectric transducer 920, a quick change in the DC offset signal V_{offset} will give rise to audible artefacts in the audible output of the piezoelectric transducer 920.

In order to mitigate the effects of quick changes in the level of the input signal V_{in} , the circuitry 900 may include controllable compressor circuitry 940, which is configured to apply a controllable gain to the input signal V_{in} to adjust its signal level and to output a level-adjusted version V_{in}' of the input signal V_{in} to the level detector circuitry 920 and the summing node 930, in order to prevent clipping of the drive signal V_{out} , thus avoiding generating audible artefacts in the audible signal output by the piezoelectric transducer 920.

The gain applied by the compressor circuitry 940 is adaptive, depending upon, for example, the level of the input signal V_{in} or the rate of change of the level of the input signal V_{in} .

Thus, where the input signal level falls from a level that is greater than some threshold to a level that is less than the threshold, or at a rate that exceeds a threshold rate, the compressor circuitry 940 may apply gain to the input signal V_{in} to increase its level. Thus instead of reducing the DC offset V_{offset} output by the level detector circuitry 920 in a single step, the DC offset V_{offset} output by level detector circuitry 920 is reduced over time (at a rate that is lower than an audio frequency range, e.g. at a rate of 10Hz or less). As the DC offset V_{offset} decreases, the compressor circuitry 940 continues to adjust the gain applied to the input signal V_{in} , based on the level of the input signal V_{in} , thus controlling the DC offset that is applied in order to prevent.

Similarly, where the input signal level increases from a level that is lower than the threshold to a level that exceeds the threshold, the compressor circuitry 940 may apply

gain to the input signal V_{in} to reduce its level. Thus instead of increasing the DC offset V_{offset} to a final level appropriate to the new input signal level in a single step, the DC offset V_{offset} output by the level detector circuitry 920 is increased over time (again at a rate that is lower than an audio frequency range, e.g. at a rate of 10Hz or less). As the

5 DC offset V_{offset} increases, the compressor circuitry 940 continues to adjust the gain applied to the input signal V_{in} , based on the level of the input signal V_{in} , thus controlling the DC offset that is applied in order to prevent clipping.

In this way the DC offset signal V_{offset} output by the level detector circuitry 920 can be

10 increased or reduced gradually in a manner that avoids introducing audible artefacts in the audible signal that is generated and output by the piezoelectric transducer 920 in response to the drive signal V_{out} .

Although the invention has been described in the context of a system in which the load

15 to be driven is a piezoelectric transducer, it will be appreciated that the principles described above are equally applicable to any system that drives a load that is capable of handling a DC offset, in particular capacitive loads such as (but not limited to) MEMS transducers or electrostatic transducers.

Embodiments may be implemented as an integrated circuit which in some examples could be a codec or audio DSP or similar. Embodiments may be incorporated in an electronic device, which may for example be a portable device and/or a device operable with battery power. The device could be a communication device such as a mobile telephone or smartphone or similar. The device could be a computing device such as a

25 notebook, laptop or tablet computing device. The device could be a wearable device such as a smartwatch. The device could be a device with voice control or activation functionality such as a smart speaker. In some instances the device could be an accessory device such as a headset, headphones, earphones, earbuds or the like to be used with some other product.

30

The skilled person will recognise that some aspects of the above-described apparatus and methods, for example the discovery and configuration methods may be embodied as processor control code, for example on a non-volatile carrier medium such as a disk, CD- or DVD-ROM, programmed memory such as read only memory (Firmware), or on a

35 data carrier such as an optical or electrical signal carrier. For many applications, embodiments will be implemented on a DSP (Digital Signal Processor), ASIC

(Application Specific Integrated Circuit) or FPGA (Field Programmable Gate Array). Thus the code may comprise conventional program code or microcode or, for example code for setting up or controlling an ASIC or FPGA. The code may also comprise code for dynamically configuring re-configurable apparatus such as re-programmable logic gate arrays. Similarly the code may comprise code for a hardware description language such as Verilog™ or VHDL (Very high speed integrated circuit Hardware Description Language). As the skilled person will appreciate, the code may be distributed between a plurality of coupled components in communication with one another. Where appropriate, the embodiments may also be implemented using code running on a field- (re)programmable analogue array or similar device in order to configure analogue hardware.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word “comprising” does not exclude the presence of elements or steps other than those listed in a claim, “a” or “an” does not exclude a plurality, and a single feature or other unit may fulfil the functions of several units recited in the claims. Any reference numerals or labels in the claims shall not be construed so as to limit their scope.

CLAIMS

1. Circuitry for driving a load, the circuitry comprising:
 - 5 driver circuitry configured to generate a drive signal, based on an input signal to the driver circuitry, for driving the load; and
 - commutator circuitry for coupling the driver circuitry to the load, wherein the commutator circuitry is configured to alternate between commutation states in response to a level of the drive signal meeting a drive signal threshold or in response to a level of
 - 10 the input signal meeting a first input signal threshold,
 - wherein the circuitry is configured to apply an offset to the input signal when the input signal is below a second input signal threshold so as to increase a minimum level of the drive signal above the drive signal threshold or to increase a minimum level of the input signal above the first input signal threshold.
- 15 2. Circuitry according to claim 1, wherein the load comprises a capacitive load.
3. Circuitry according to claim 1, wherein the load comprises a piezoelectric transducer.
- 20 4. Circuitry according to claim 1, wherein the second input signal threshold is dependent upon an expected maximum level of the drive signal.
5. Circuitry according to claim 4, wherein the second input signal threshold is such
- 25 that the commutator circuitry remains in a single commutation state until the level of the drive signal is within 6dB of the expected maximum level of the drive signal.
6. Circuitry according to claim 1, wherein the offset is a fixed offset.
- 30 7. Circuitry according to claim 1, wherein the offset is variable according to a level of the input signal.
8. Circuitry according to claim 1, further comprising level detector circuitry configured to detect a level of the input signal.

9. Circuitry according to claim 8, wherein the level detector circuitry comprises envelope detector circuitry configured to detect an envelope of the input signal.
10. Circuitry according to claim 8, further comprising a summing node configured to
5 receive the input signal and an offset signal output by the level detector circuitry and to output a signal to the driver circuitry.
11. Circuitry according to claim 1, further comprising control circuitry configured to control operation of the commutator circuitry.
- 10 12. Circuitry according to claim 11, wherein the control circuitry comprises:
level detector circuitry configured to output a control signal to the commutator circuitry each time the level of the drive signal meets the drive signal threshold.
- 15 13. Circuitry according to claim 11, wherein the control circuitry comprises:
level detector circuitry configured to output a control signal to the commutator circuitry each time the level of the input signal meets the first input signal threshold.
- 20 14. Circuitry according to claim 8, wherein the driver circuitry is selectively configurable to generate a drive signal that is shaped to take into account the effect of commutation of the drive signal that occurs when the level of the drive signal meets the drive signal threshold.
- 25 15. Circuitry according to claim 14, wherein the level detector circuitry is configured to output a control signal to control the configuration of the driver circuitry based on the detected level of the input signal.
- 30 16. Circuitry according to claim 1 further comprising controllable compressor circuitry configured to apply a controllable gain to the input signal so as to control a rate of change of the offset applied to the input signal, the controllable gain based on a level of the input signal.
17. An integrated circuit comprising the circuitry of claim 1.

18. A device comprising the circuitry of claim 1, wherein the device comprises a mobile telephone, a tablet or laptop computer, a gaming device, an accessory device, a headset, headphones, earphones, a smart speaker.
- 5 19. Circuitry for driving a load, the circuitry comprising:
driver circuitry configured to generate a drive signal, based on an input signal to the driver circuitry, for driving the load;
commutator circuitry configured to commutate the drive signal between first and second terminals of the load,
- 10 wherein the circuitry is configured to prevent commutation of the drive signal when a level of the input signal is below a threshold.
20. Circuitry for driving a load, the circuitry comprising:
driver circuitry configured to generate a drive signal, based on an input signal to
- 15 the driver circuitry, for driving the load;
level detector circuitry configured to detect a level of the drive signal or a level of the input signal; and
commutator circuitry for supplying the drive signal to either a first terminal or a second terminal of the load based on an output of the level detector circuitry,
- 20 wherein the circuitry is configured to apply an offset to the input signal when the level of the input signal is below a predetermined input signal threshold.

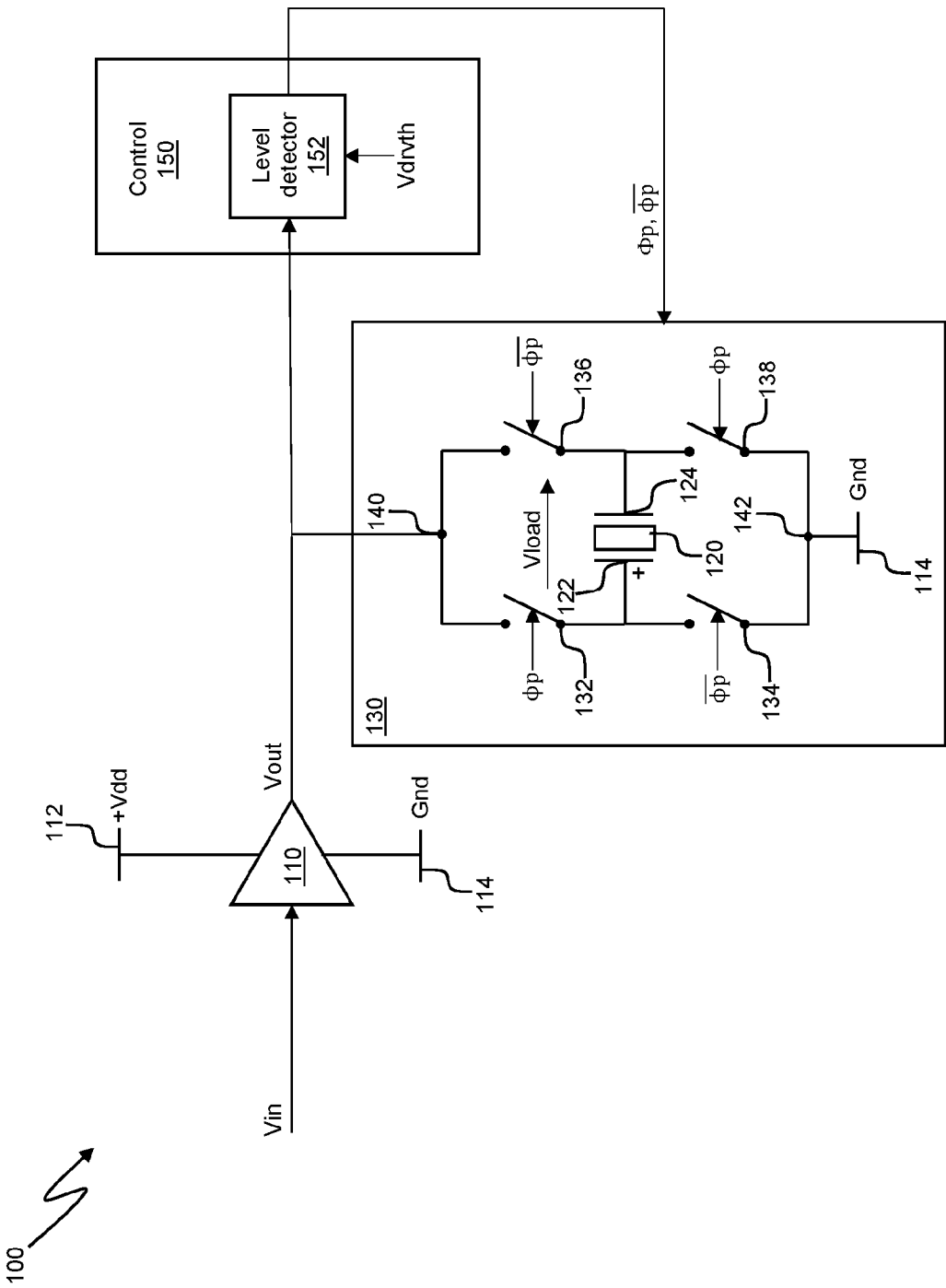


Figure 1

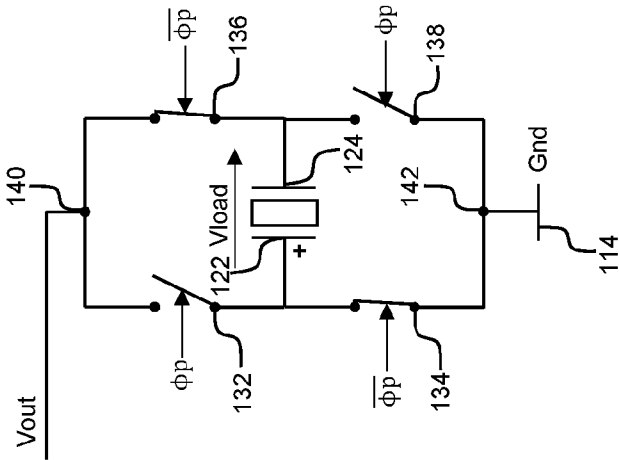


Figure 2b

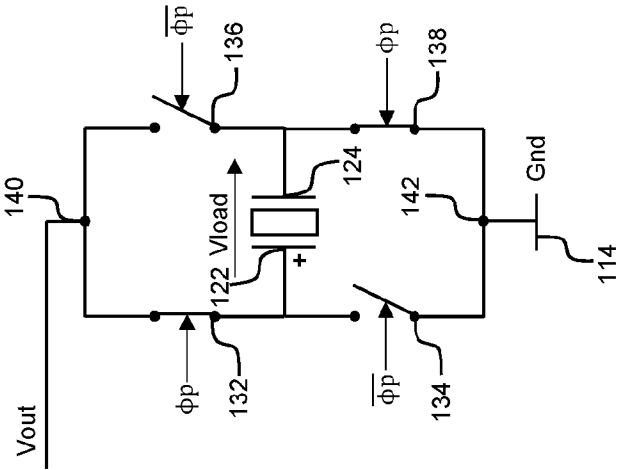


Figure 2a

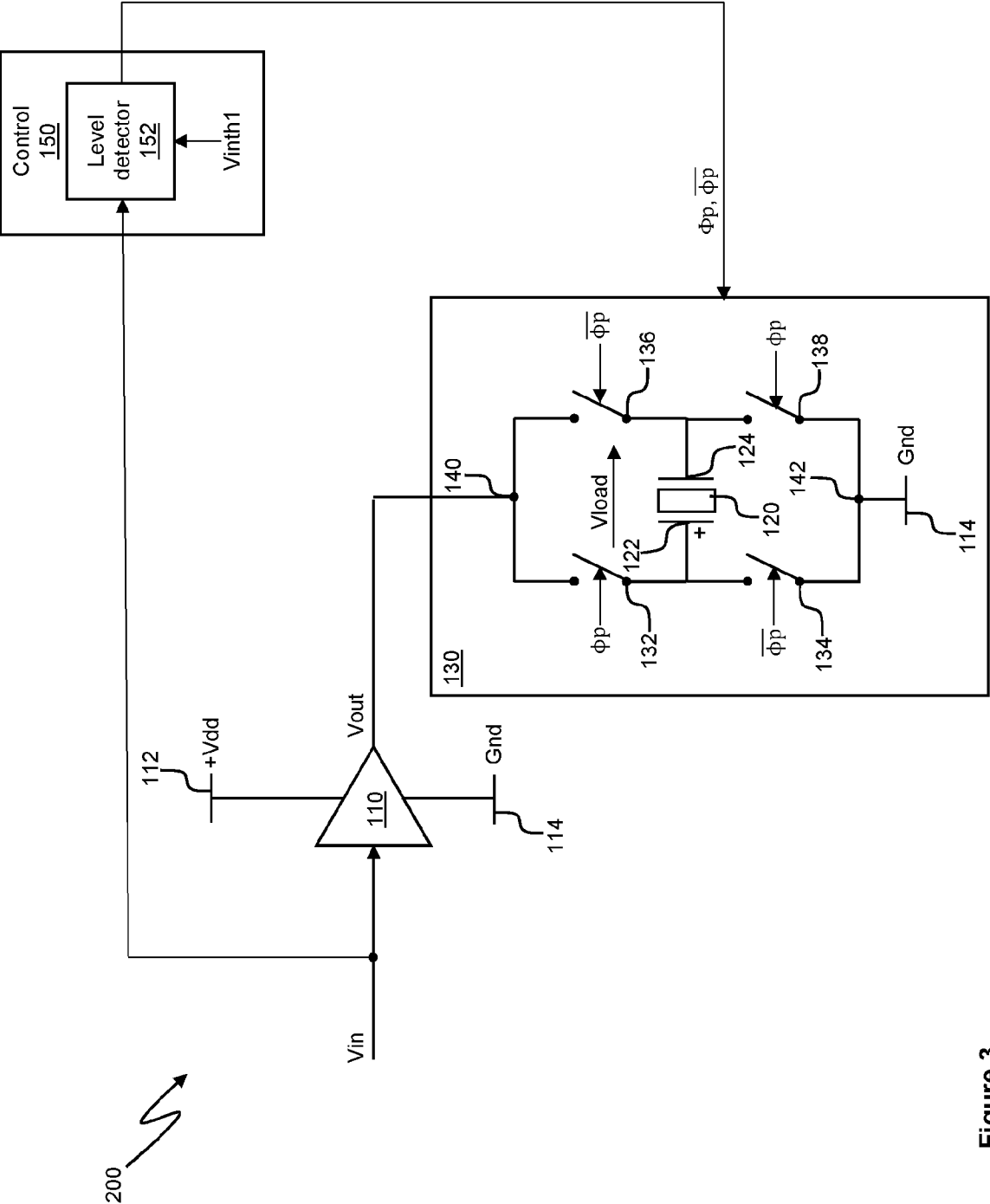


Figure 3

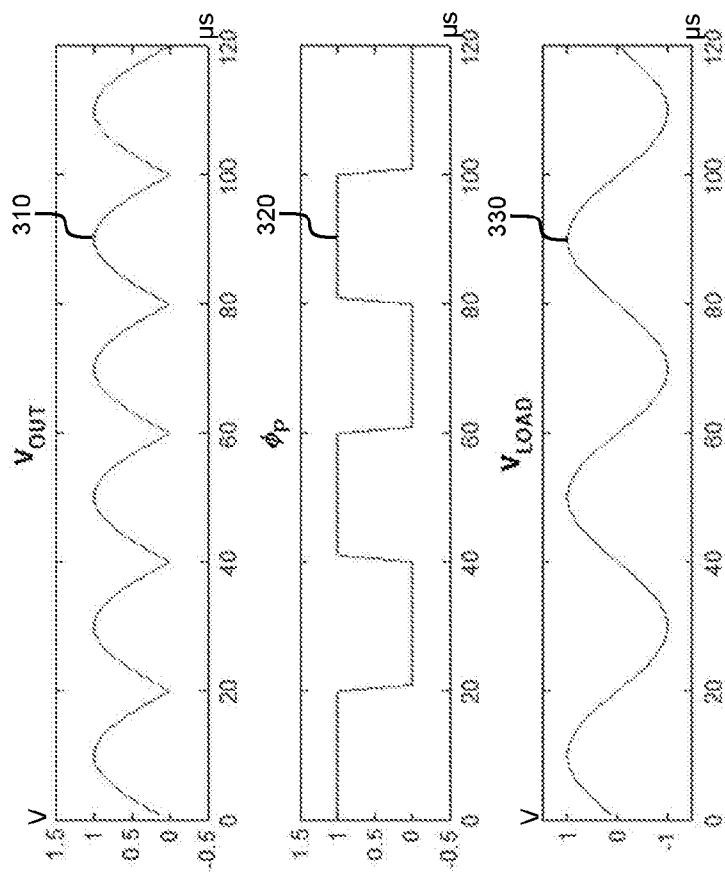


Figure 4

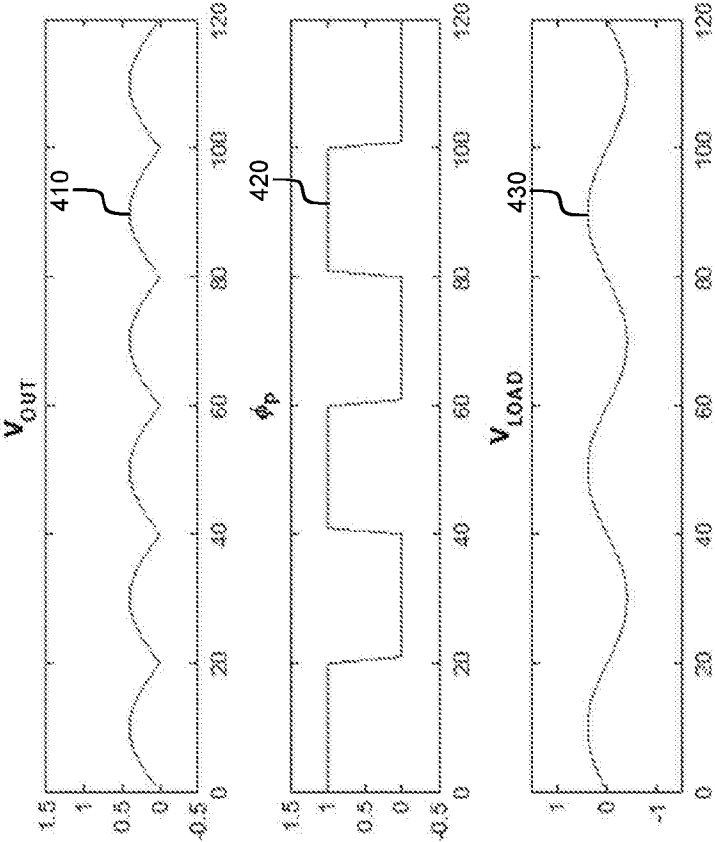


Figure 5

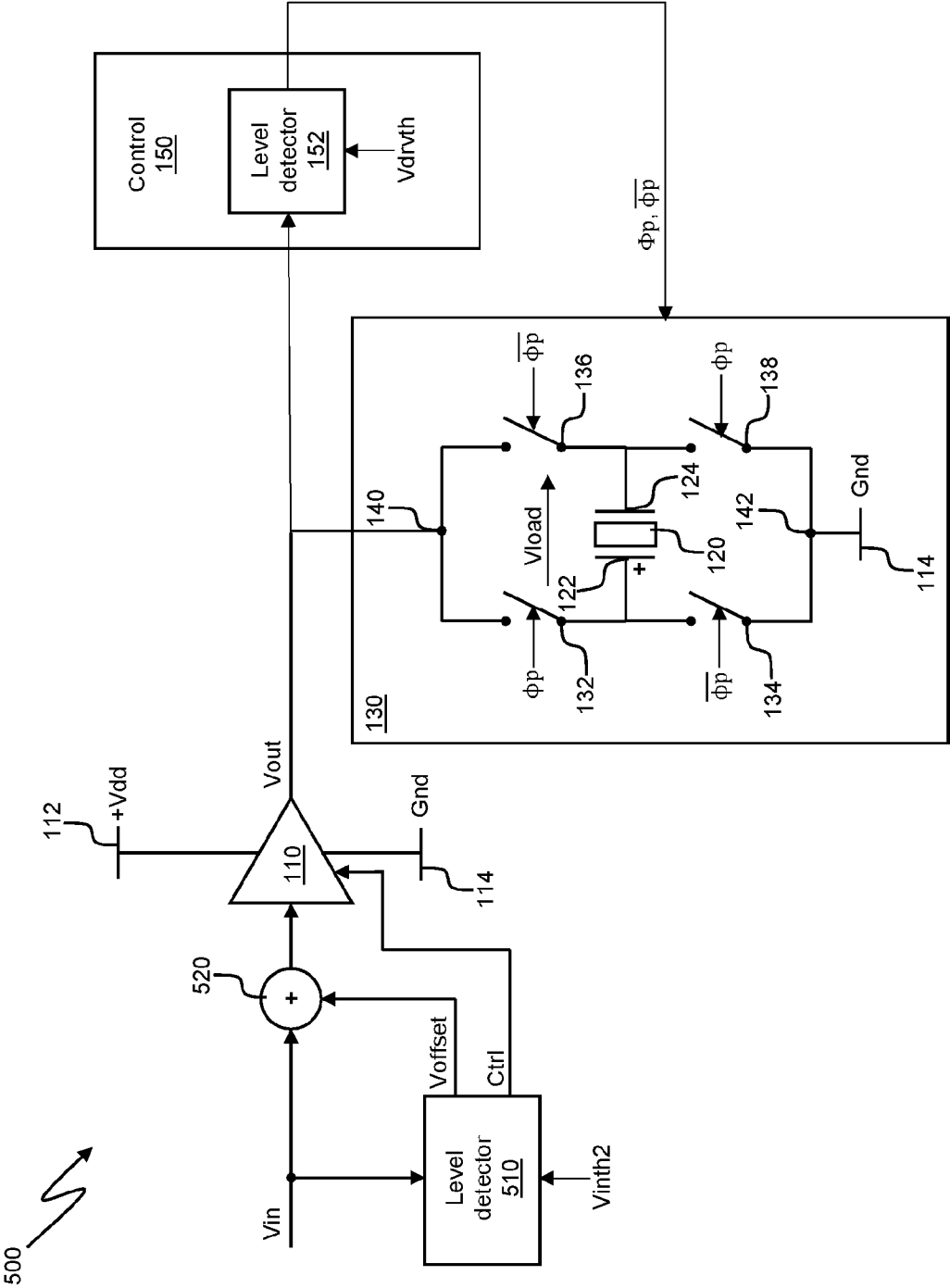


Figure 6

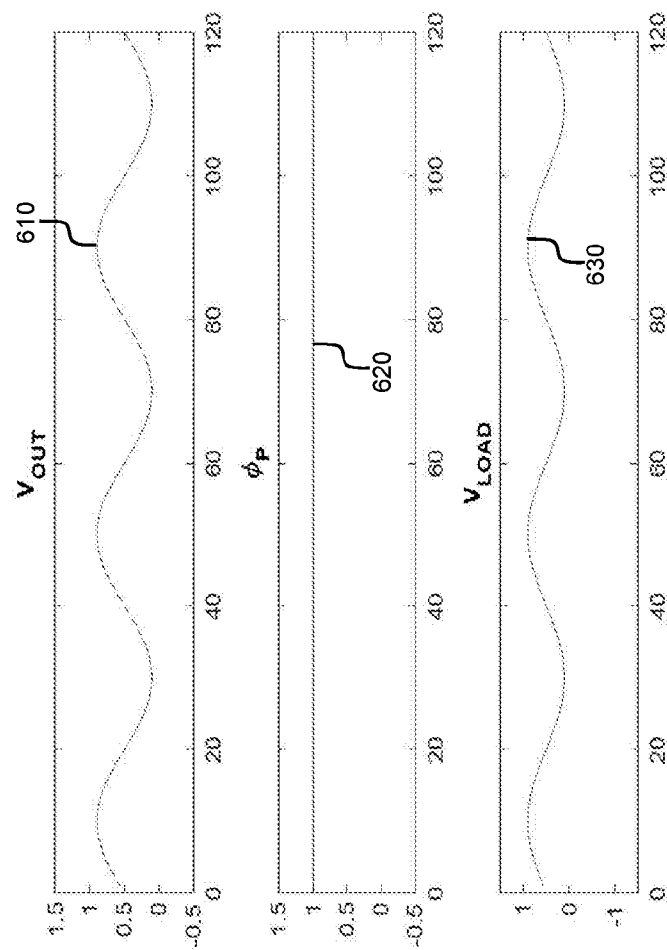


Figure 7

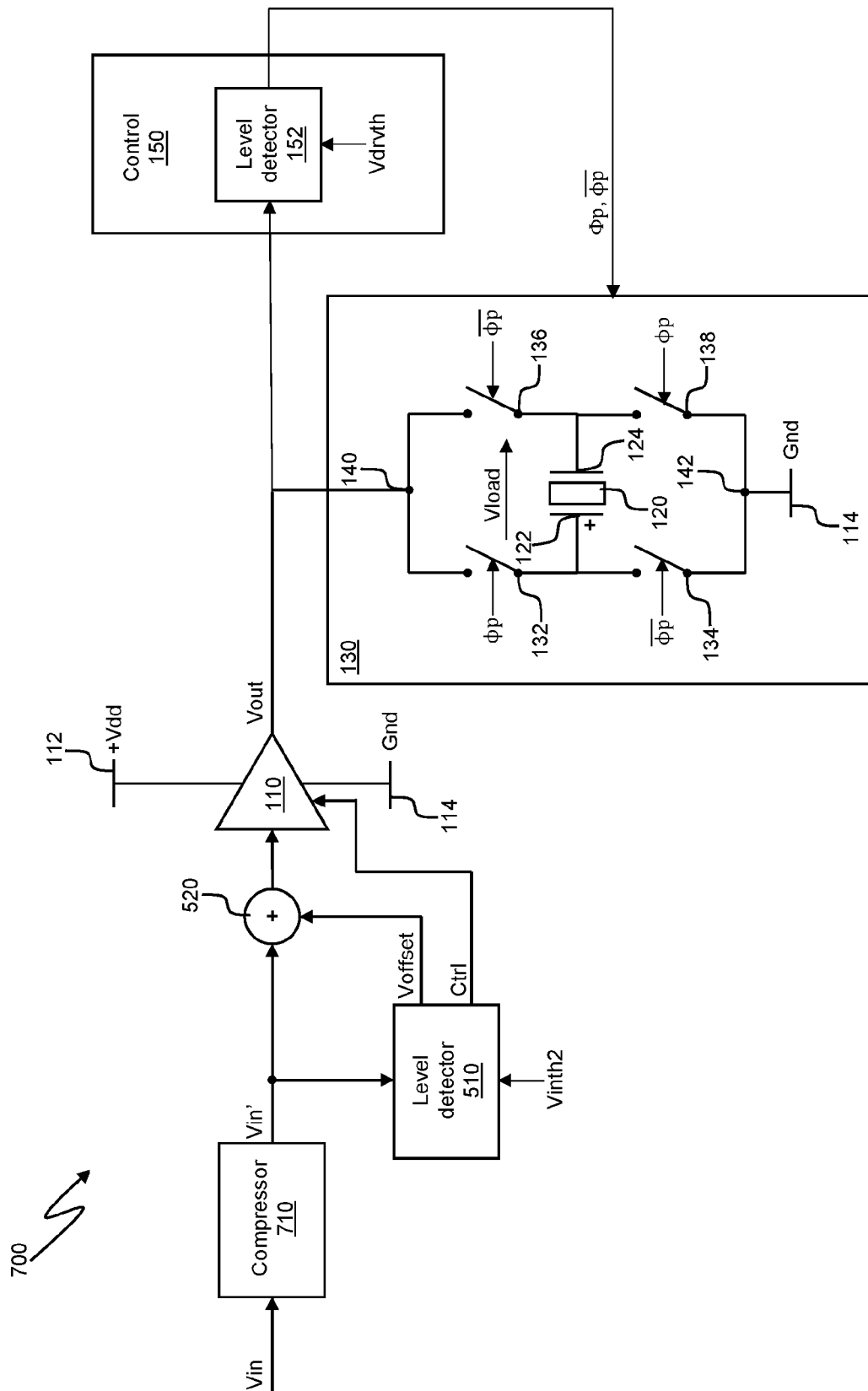


Figure 8

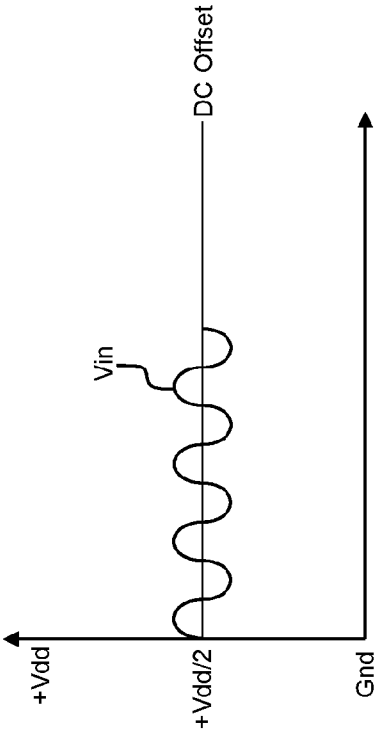


Figure 9

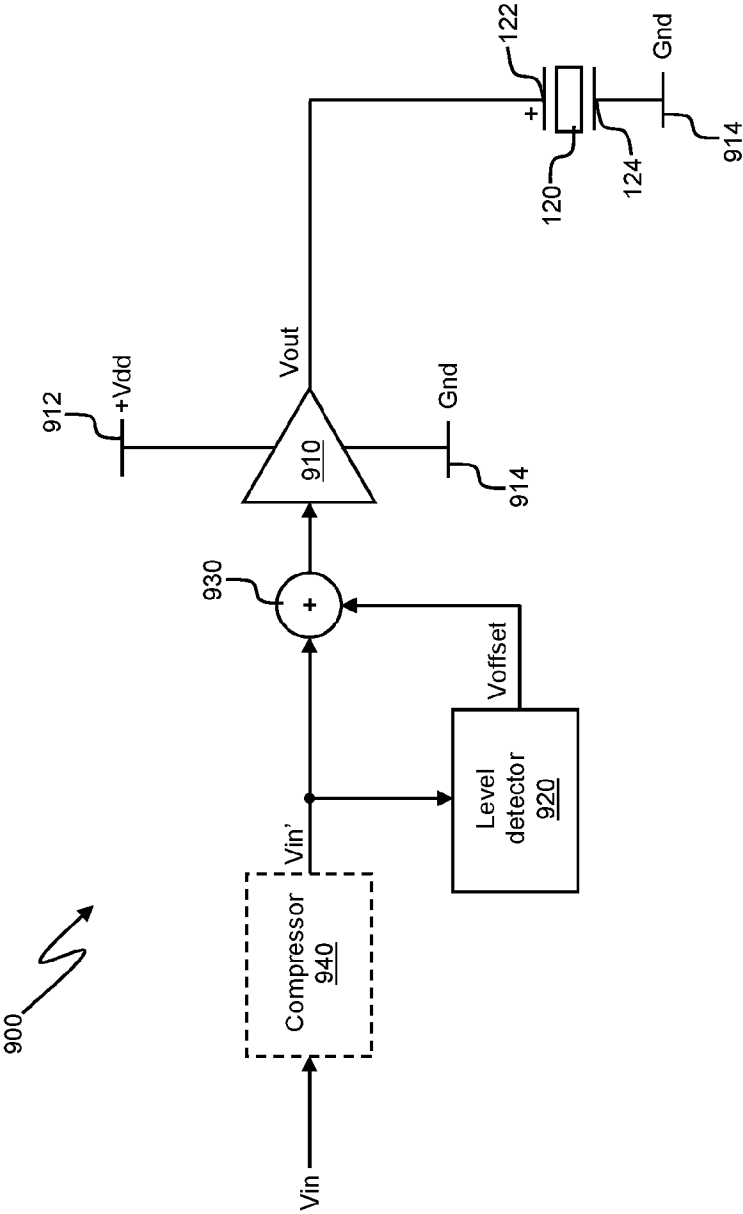


Figure 10

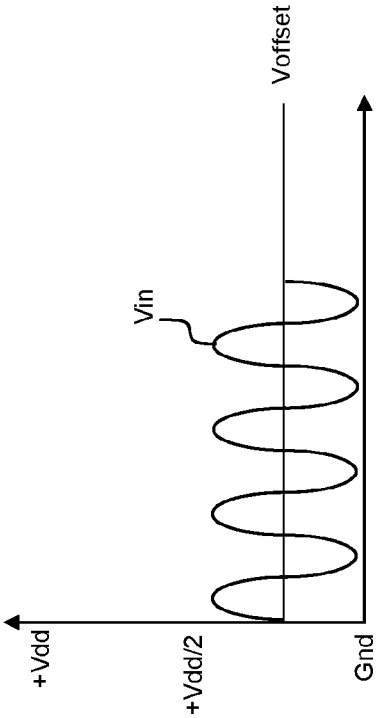


Figure 11b

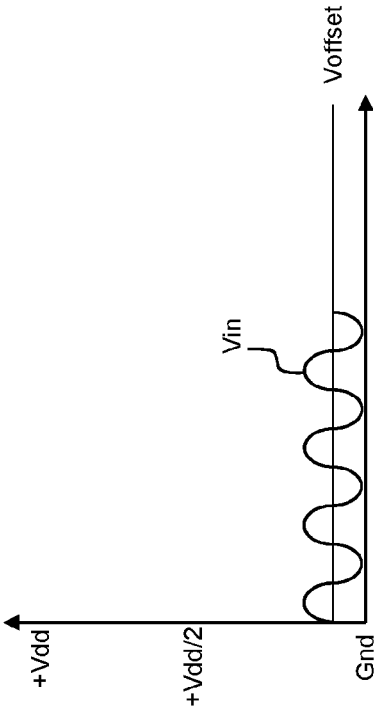


Figure 11a

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2021/052210

A. CLASSIFICATION OF SUBJECT MATTER INV. B06B1/02 H01L41/04 H02M3/158 B06B1/06 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) B06B H02N H01L H02M		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2020/244171 A1 (CHAPUT SIMON [CA] ET AL) 30 July 2020 (2020-07-30) paragraphs [0075], [0119] - [0140]; figures 1,2,3,20-24 -----	19,20 1-18
X A	US 2013/334987 A1 (GARG MAYANK [US] ET AL) 19 December 2013 (2013-12-19) paragraphs [0001] - [0043]; figures 2,3,11 -----	19 1-18,20
X A	EP 3 098 950 A1 (EATON CORP [US]) 30 November 2016 (2016-11-30) paragraphs [0001] - [0033]; figure 1 -----	19 1-18,20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents :		
"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 11 November 2021		Date of mailing of the international search report 19/11/2021
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Gassmann, Martin

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2021/052210

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