United States Patent

Drage et al.

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[54] NUMBER POSITIONING DISPLAY FOR ELECTRONIC CALCULATING MACHINES

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[51] **Int. Cl.** **G06f 7/46**

[58] **Field of Search** ..... 235/160, 159, 164; 328/37; 340/324 R

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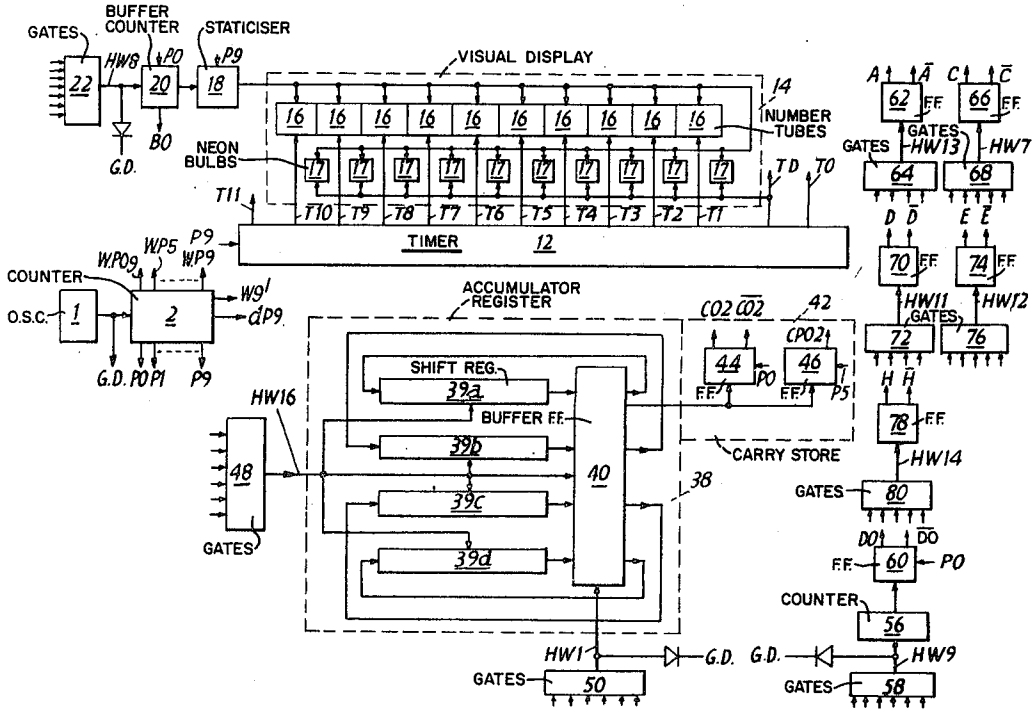
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Primary Examiner—Eugene G. Botz
Assistant Examiner—Jerry Smith
Attorney—Laurence R. Brown

[57] **ABSTRACT**

A calculating system employing a numerical display is described with a plurality of number display tubes each having a corresponding register for storing the number to be displayed. Numbers may be transferred from one register stage to another and the value of each of the digits is determined to present the highest significant digit at a predetermined stage by way of transfer in the stages.

7 Claims, 10 Drawing Figures



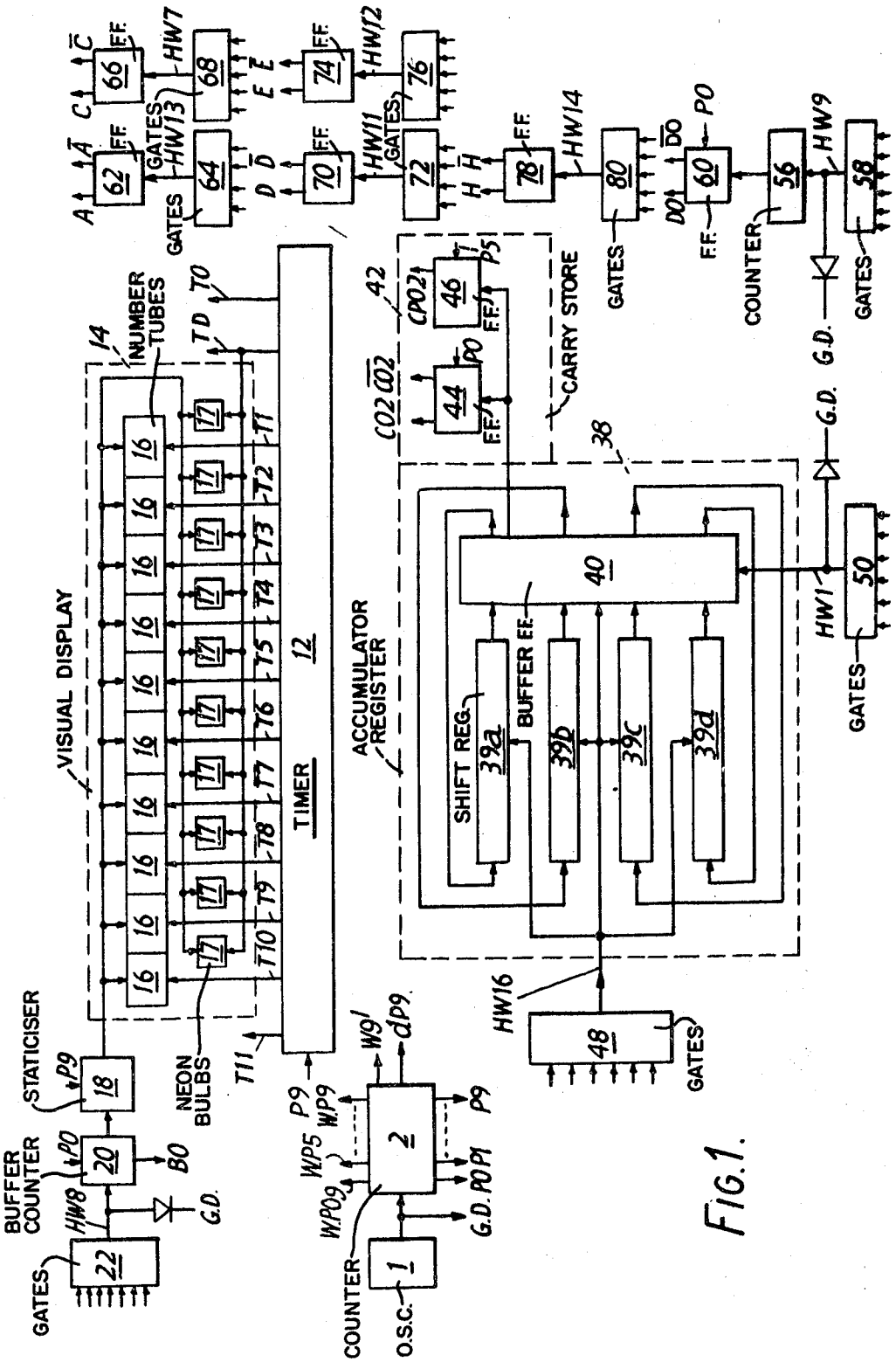

VISUAL DISPLAY
NUMBER TUBES
TIMER
ACCUMULATOR REGISTER
SHIFT REG.
BUFFER EE
CARRY STORE
STATICISER
NEON BULBS
BUFFER COUNTER
COUNTER
O.S.C.
GATES
F.F.
G.D.

FIG. 1.

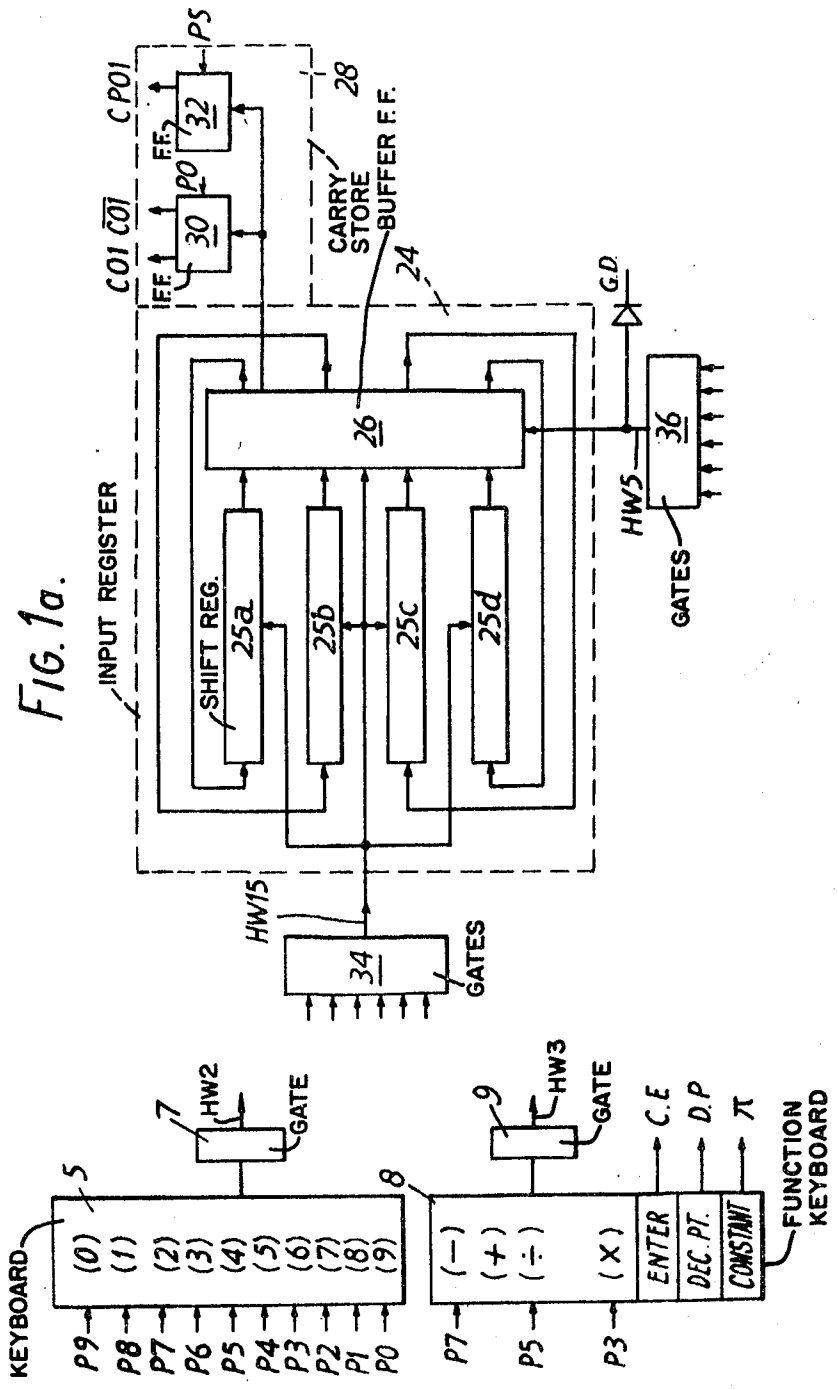

INPUT REGISTER
SHIFT REG.
25a
25b
25c
25d
26
CARRY STORE BUFFER F.F.
28
24
C01 C01
I.F.F.
30
P0
F.F.
32
C P01
P5
G.D
36
HW5
GATES
HW15
34
GATES
KEYBOARD
5
(0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
P9
P8
P7
P6
P5
P4
P3
P2
P1
P0
7
HW2
GATE
8
9
HW3
GATE
(−)
(+)
(÷)
(X)
P7
P5
P3
ENTER
DEC. PT.
CONSTANT
C.E
D.P
π
FUNCTION KEYBOARD

FIG. 1a.

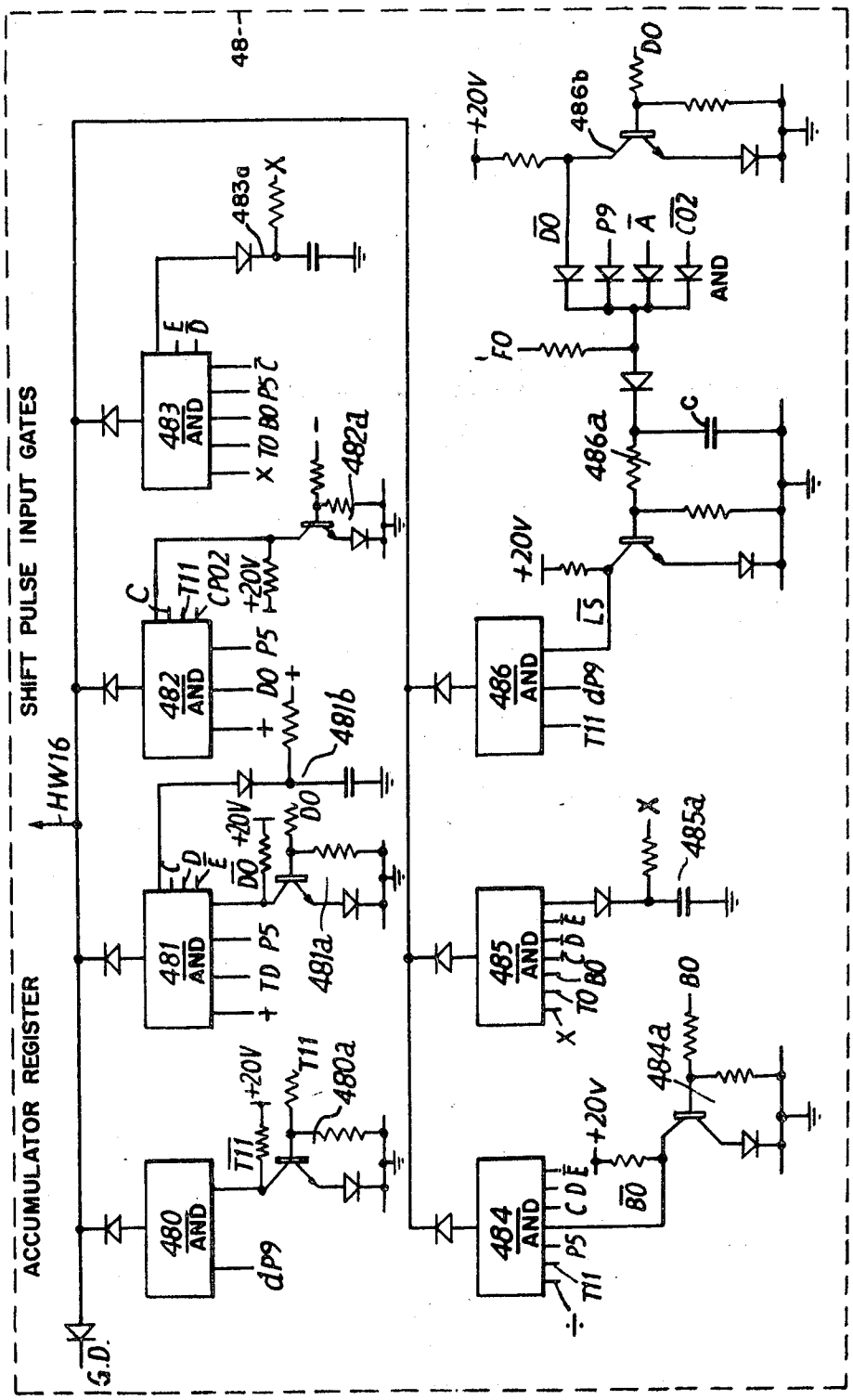

ACCUMULATOR REGISTER
SHIFT PULSE INPUT GATES
48
HW16
S.D.
480 AND
481 AND
482 AND
483 AND
484 AND
485 AND
486 AND
486a
486b
+20V
T11
CP02
P5
T0
B0
dP9
LS
FO
P9
C02
AND

FIG. 2.

FIG. 3.

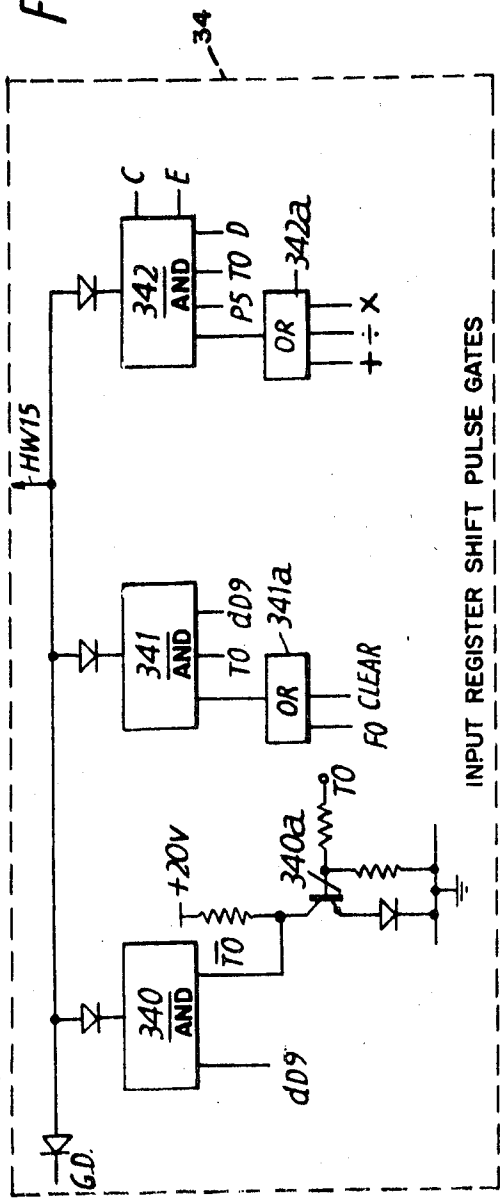

34
INPUT REGISTER SHIFT PULSE GATES
HW15
G.D.
340 AND
341 AND
342 AND
OR
OR
dD9
TO dD9
P5 TO D
FO CLEAR
+20V
340a
341a
342a
+ ÷ X

FIG. 4.

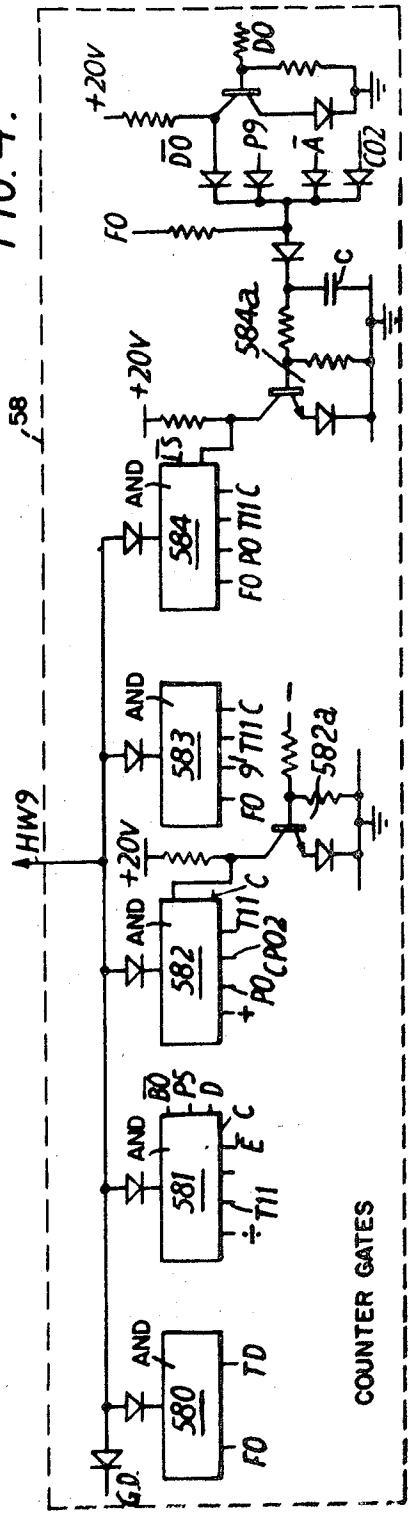

58
COUNTER GATES
HW9
G.D.
580
581
582
583
584
AND
+20V
584a
582a
FO
TD
÷T11
+P0 CP02
FO P0 T11C
FO P9 T11C
P9
A
CO2
DO

FIG. 5

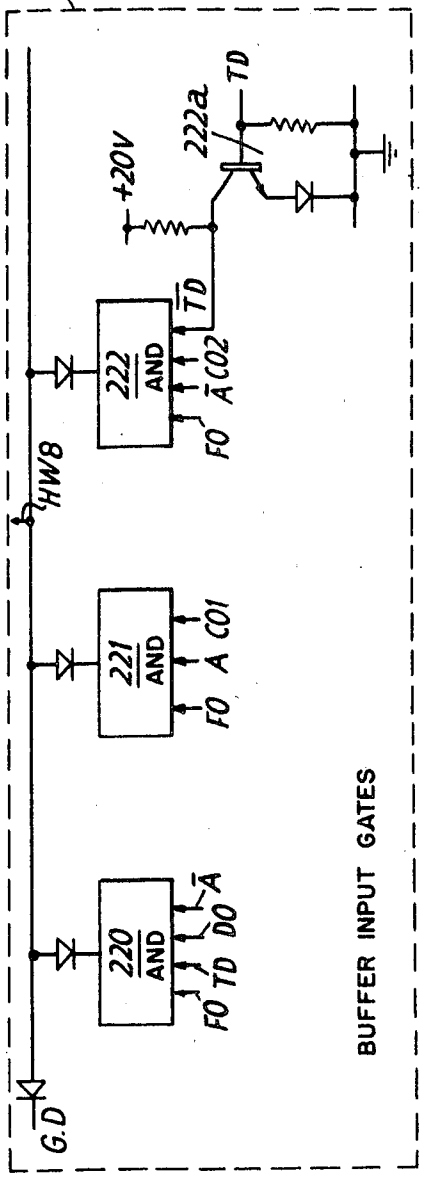
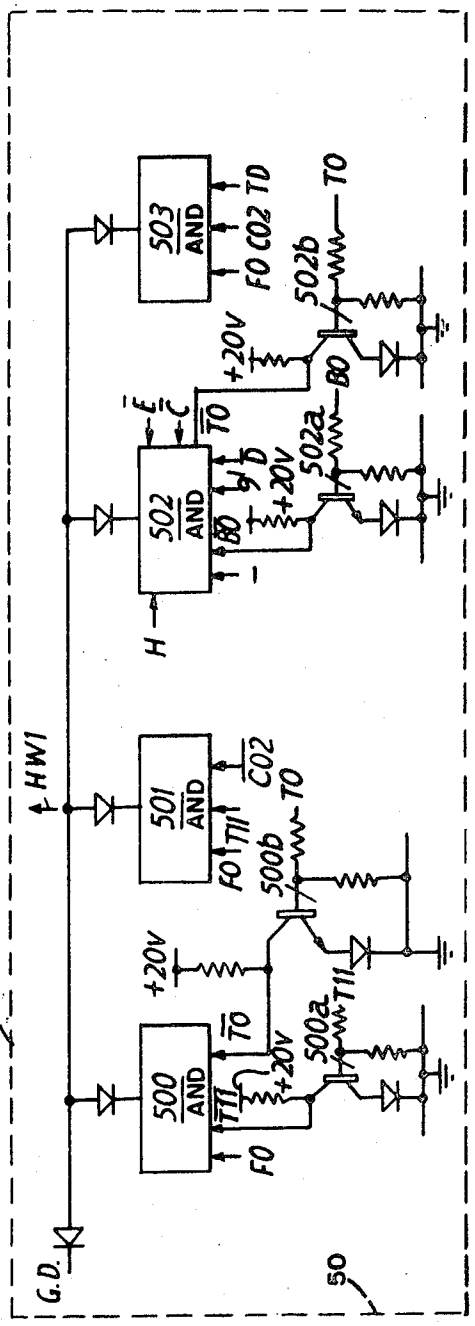
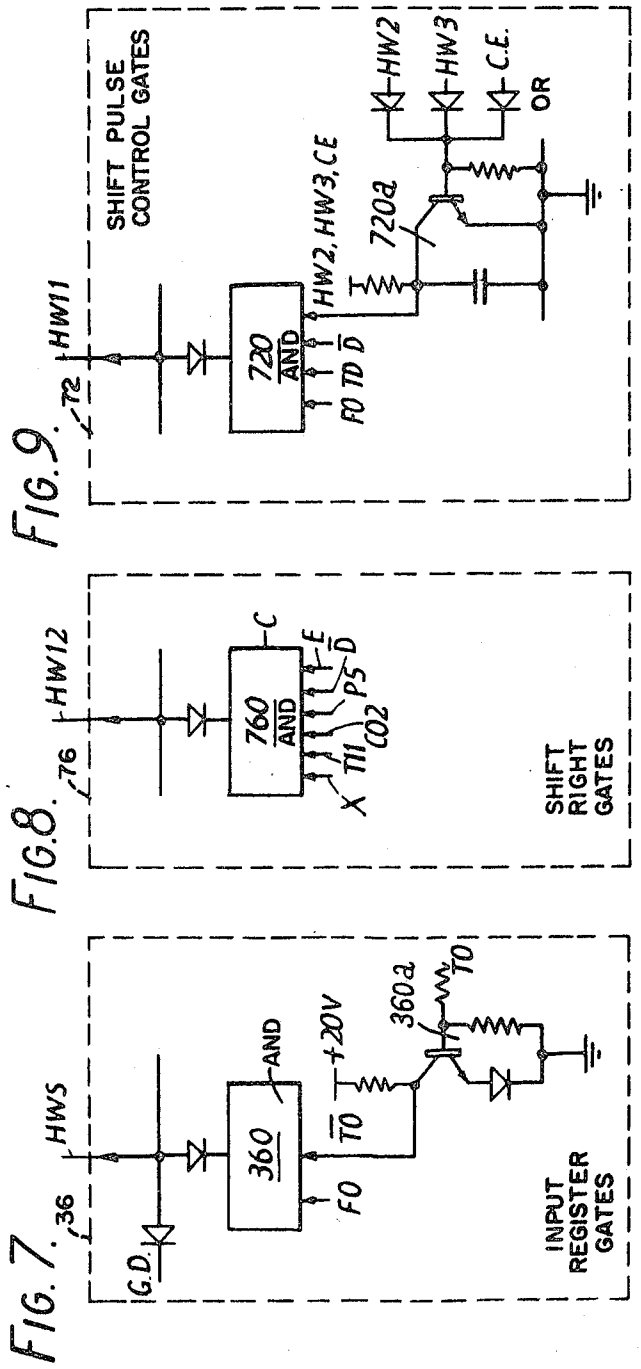

22
BUFFER INPUT GATES
G.D
HW8
220 AND
FO TD DO Ā
221 AND
FO A CO1
222 AND
FO Ā CO2 TD
+20V
222a
TD

FIG. 6.


ACCUMULATOR REGISTER INPUT GATES
50
G.D
HW1
500 AND
FO T11 T0
501 AND
FO T11 CO2 T0
502 AND
H E C T0 B1 B0
503 AND
FO CO2 TD
+20V
500a
500b
502a
502b
T11
T0
B0
B1


FIG. 7.
36
HWS
G.D.
360
AND
FO
T0
+20V
360a
T0
INPUT REGISTER GATES
FIG. 8.
76
HW12
760
AND
C
E
D
P5
T11
C02
X
SHIFT RIGHT GATES
FIG. 9.
72
HW11
720
AND
FO T0 D
HW2, HW3, CE
720a
HW2
HW3
C.E.
OR
SHIFT PULSE CONTROL GATES

NUMBER POSITIONING DISPLAY FOR ELECTRONIC CALCULATING MACHINES

This machine has reference to calculating machines and has particular reference to number store registers having associated display apparatus used for the storage and display of digit numbers representative of trains of digit pulses applied to the number store register. Such a number store register comprises a plurality of register stages, each register stage serving to store a digit number representative of the train of digit pulses applied to it. The display apparatus associated with the number stored register comprises a plurality of number tubes, each of which is associated with a number store register stage so that it can give a visual indication of the numerical content of this number store register stage.

It has been known hitherto that number store registers of calculating machines have the disadvantage that the position of the visual indication of numbers stored in the number store register have been affected by the previous arithmetical operations performed upon the numbers stored in the number store register.

If the direction of entry of numbers stored is from left to right, when the highest significant digit of the numerical result of an arithmetical operations is of a higher order than the highest significant digit of the two constituent numbers, the highest significant digit of the numerical result will "overflow" from the number store register and will not be available for visual display with the rest of the numerical result.

If the direction of entry of numbers stored in the number store register is from right to left, the highest significant digit of the result of an arithmetical operation, when greater than the highest significant digit of the constituents, moves towards the left. This method of number entry requires the provision of many more store addresses than are normally needed to ensure that the highest significant digit is not lost during any leftward movements.

An object of this invention is to provide an improved calculating machine.

According to another aspect of the invention there is provided a calculating machine comprising a number store register having a plurality of register stages for storing digit pulses representative of the digits of a number entered in the number store register; a multistage display device for displaying the digits of the number stored in the number store register, each stage in the display device being associated with a register stage; a means for transferring the digit pulse representative of the number from one register stage to another of the plurality of register stages; and a means for detecting the presence of a digit pulse of predetermined value at a particular register stage and thereupon operating the transfer means so that the highest significant digit pulse of the number entered in the register is displayed at a predetermined stage in the display device.

A constructional embodiment made in accordance with the invention will now be described, by way of example, with reference to the accompanying drawings wherein:

FIGS. 1 and 1A show a block diagram of part of an electronic calculating machine made according to the invention;

FIG. 2 shows part of the set of gates **48** shown in FIG. 1 in greater detail;

FIG. 3 shows part of the set of gates **34** shown in FIG. 1 in greater detail;

FIG. 4 shows part of the set of gates **58** shown in FIG. 1 in greater detail;

FIG. 5 shows part of the set of gates **22** shown in FIG. 1 in greater detail;

FIG. 6 shows part of the set of gates **50** shown in FIG. 1 in greater detail;

FIG. 7 shows part of the set of gates **36** shown in FIG. 1 in greater detail;

FIG. 8 shows part of the set of gates **76** shown in FIG. 1 in greater detail; and

FIG. 9 shows part of the set of gates **72** shown in FIG. 1 in greater detail.

The FIG. 1 shows an electronic calculating machine made according to the present invention. In FIG. 1 a master oscillator **1** generates free-running oscillator pulses GD which are "on" at +12 v. and "off" at 0 v. The oscillator **1** is connected to an input decade **2** which is connected as a Johnson ring circuit. The input decade **2** divides the master oscillator pulses GD into sequential groups of 10 pulses, viz **P0, P1, P2, P3, P4, P5, P6, P7, P8** and **P9**. The output pulses **P0** to **P9** from the input decade **2** are internally gated to give waveforms **P0, P5** and **P9**, a waveform 9^1 and a waveform $dP9$.

"Waveform **P0**" is up (at +12 v.) from the back edge of the **P9** pulse to the back edge of the **P0** pulse.

"Waveform **P5**" is up from the back edge of **P4** pulse to the back edge of **P5** pulse.

"Waveform **P9**" is up from the back edge of **P8** pulse to the back edge of **P9** pulse.

"Waveform 9^1" is up from the back edge of **P0** pulse to the back edge of **P9** pulse.

"Waveform $dP9$" is up from the back edge of **P9** pulse to the front edge of PO pulse.

The calculating machine has a digit keyboard **5** having 10 normally open digit key switches (not shown) representing the digits 0–9 respectively, which switches are closed when the corresponding keys (not shown) are depressed. The normally open contact of the digit key switches (not shown) representing the digits 0–9 respectively are connected to the pulses **P9** to **P0** respectively and the connections to the movable contact of the digit key switches are connected to a gate circuit **7** which has an output to a highway **HW2**. When a digit key (not shown) is depressed to close the corresponding digit key switch, a train of pulses of number equal to the digit corresponding to the digit key depressed, is repetitively transmitted along the highway **HW2** until the depressed digit key is released.

The calculating machine also has a function keyboard **8** which has function key switches (not shown) marked with the following symbols +, −, ×, , "decimal point," "constant," and "enter." The function key switches (not shown) marked +, −, × and , which control the arithmetical functions of addition, subtraction, multiplication and division are similar to the digit key switches and are connected in a similar way to a gate circuit **9**. The output from the gate circuit **9** is connected to a highway **HW3**. When a main function key is closed by depression of a main function key a function signal is transmitted along the highway **HW3**. The four function signals transmitted along highway **HW3** are:

on depression of the + key, up at the back edge of **P7**, down at the back edge of **P0**;

on depression of the − key, up at the back edge of **P7**, down at the back edge of **P0**;

on depression of the × key, up at the back edge of **P3**, down at the back edge of **P0**;

on depression of the key, up at the back edge of **P5**, down at the back edge of **P0**.

The entry key transmits a "CE" signal along the line C.E. when the entry key is depressed. The decimal point key transmits a "DP" signal along the line D.P. when the decimal point key is depressed, and the constant transmits a "constant" signal along the line π when the constant key is depressed.

The timer circuit **12**, which is a seven-position Johnson ring circuit is internally interconnected to have 13 count states which are labeled in order of ascending count states TO TD, **T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11**. The timer circuit **12** is driven continuously by **P9** pulses from the input decade **2** so that the count state outputs are sequentially and continuously generated and each count state output lasts from the back of the P9 pulse to the back edge of the next **P9** pulse.

A visual display **14** includes 10 number tube circuits each having a number tube **16** and 10 decimal point neon bulbs **17**. The anodes of the number tubes **16** are each connected in sequence to a positive potential under the control of the outputs **T10** to **T1** respectively of the timer circuit **12**. The highest significant digit in a displayed number is positioned in

the left-hand number tube, which is controlled by the output T10, by means of circuits hereinafter described.

One connection to each of the neon bulbs 17 is connected together and these are connected to a source of positive potential under the control of the output TD of the timer circuit 12. The cathodes of the 10 number tubes 16 which are shaped to the same digit are connected together. The other connections of the neon bulbs 17 are connected to the bunched cathode connections with the neon bulb 17 at the left-hand end connected to the bunched cathode connections showing the digit 0, the next neon bulb being connected to the one digit cathodes and so on until the 10th neon bulb is connected to the nine digit cathodes.

The 10 bunched cathode connections are connected to the outputs of a row of bistables or flip-flop circuits (FF) which form a staticizer 18. The inputs of the staticizer 18 are connected to the outputs of a buffer 20 in form of a decade counter which is internally interconnected so as to convert a train of pulses into the binary-coded-decimal equivalent on the outputs of the decade counter. The input of the buffer 20 is connected by a highway HW8 to a set of gates 22, part of which is shown in FIG. 5. The contents of the buffer 20 is cleared from the buffer 20 into the staticizer 18 at the front edge of each P0 pulse and the staticizer 18 is cleared, i.e., the digit 0 line is energized, at the back edge of each P9 pulse. The buffer 20 has an output B0 which is energized, i.e., goes to a positive potential, when the buffer 20 stores a digit 0 so that the number cleared from the buffer 20 stays in the staticizer 18 for nearly the duration of an output from the timer circuit 12.

The number tube connected to the output T2 displays the units digit, the number tube connected to the output T3 displays the 10s digit and so on. The position of the decimal point is given by a train of pulses loaded into the buffer 20 when the output TD of the timer circuit 12 is energized and is entered into the staticizer 18 and is displayed by the neon bulb 17 at the position corresponding to the number of pulses in the train, when the next output T1 of the time circuit is energized. Similarly, if for example the digit four is to be displayed at the 10s position, a train of four pulses is entered into the buffer 20 when the output of the time circuit is energized and the binary coded-decimal equivalent of the digit four appears on the output of the buffer 20. This output is transferred to the staticizer 18 at the pulse P0 and the digit four is displayed on that number tube 16 which is switched on when the output T3 of the timer circuit 12 is energized. The digit four is cleared from the staticizer 18 when the pulse P9 occurs at the end of the time in which the output T3 is energized. The frequency at which the outputs from the timer circuit 12 are energized are such that the digits appearing on the number tubes 16 and the decimal point appearing on a neon bulb 17 appear to be stationary because of the persistance effect of ocular vision.

A input register 24 has four shift registers 25*a*, 25*b*, 25*c* and 25*d* each having 12 digit stages. The input and output of the four shift register 25*a*, and 25*b*, 25*c* and 25*d* are each connected in a loop with a shift register buffer 26 in the form of four bistable circuits which are internally interconnected to form a decade counter and which act as the 13th digit stage. The shift pulse input to four shift registers 25*a*, 25*b*, 25*c* and 25*d* and the shift register buffer 26 are connected by a highway HW15 to a set of gates 34 part of which is hereinafter described (FIG. 3). The set of gates 34 provide shift pulses *d*P9 to the four shift registers 25*a*, 25*b*, 25*c* and 25*d* and to the shift register buffer 26 so that the binary-coded-decimal digits in the four shift register circulate through the shift register buffer 26 and back to the input of the shift registers respectively.

A carry pulse output on a bistable circuit of the shift register buffer 26 is energized when the digit in the shift register buffer buffer 26 goes from the count of nine to the count of zero is connected to the input of a carry store 28 which comprises a first bistable circuit 30 having the outputs CO1 and $\overline{CO1}$ and a second bistable circuit 32 having the output CP01. The set connections from the first bistable circuit 30 and the second bistable circuit 32 are connected to the carry pulse output of the shift register buffer 26. The first bistable circuit 30 is reset so that the output $\overline{CO1}$ is energized i.e., is at a positive potential by a pulse PO. The second bistable circuit 32 is reset so that the output CPO1 is not energized by a pulse P5. A set of gates 36, partly hereinafter described (FIG. 7), are connected by a highway HW5 to the input of the shift register buffer 26.

An accumulator register 38 has four 12-stage shift registers 30*a*, 39*b*, 39*c* and 39*d*, a shift register buffer 40 and a carry store 42 as previously described for input register 24. The shift pulse inputs of the four shift registers 39*a*, 39*b*, 39*c* and 39*d* and the shift register buffer 40 are connected by a highway HW16 to a set of gates 48 partly hereinafter described (FIG. 2). The carry pulse output of the shift register buffer 40 is connected to the set input to the carry store 42 which comprises first bistable circuit 44 having the outputs C02 and $\overline{C02}$ and a second bistable circuit 46 having an output CP02. The first bistable circuit 44 is reset so that the output $\overline{C02}$ is energized by a pulse P0 and the second bistable circuit is reset so that the output CP02 is not energized by a pulse P5. The shift register buffer 40 is connected by a highway HW1 to a set of gates 50, partly hereinafter described (FIG. 6).

Thus in the input register 24 and the accumulator register the shift registers and the shift register buffers form 13 stage loops around which pulse patterns circulate in synchronism with the energized outputs of the timer circuit 12. If the input register or accumulator register receives 13 shift pulses, the digit in the units or T1 digit stage of the input register 24 or accumulator register 38 is in the shift register buffer 26 or 40 respectively when the output T1 of the timer circuit 12 is energized. Similarly the 10s or T2 digit stage of the input register 24 or accumulator register 38 is in the shift register buffer 26 or 40 respectively when the output T2 of the timer circuit 12 is energized, and so on.

If one shift pulse to a register is suppressed, so that the register only receives 12 shift pulses, then the number in the register is moved one place to the left with respect to the outputs of the timer circuit 12.

If an extra shift pulse is gated into a register with the pulse P5, the number in the register is moved one place to the right with respect to the outputs of the timer circuit 12.

A decimal counter 56, which is a four-bistable ripple-through counter internally interconnected so as to have 10 count states, has its output connected to the set input of an output bistable circuit 60. The input of the decimal counter 56 is connected by a highway HW9 to a set of gates 58, partly hereinafter described (FIG. 4). The output bistable circuit 60 has the outputs D0 and $\overline{DO}$. The output bistable circuit 60 is set so that the output D0 is energized when the count in the decade counter 56 goes to or passes through the zero count state; the output bistable circuit 60 is reset so that the output $\overline{D0}$ is energized by the next P0 pulse.

The decimal counter 56 holds the count corresponding to the position of the decimal point digit of a number stored in the accumulator register 38. This decimal point digit is held separately form the other digits because the accumulator register 38 is used for calculation of products and quotients, and the whole accumulator register 38 is required for holding partial products or partial remainders during the calculation. Also, the answer in the accumulator register 38 may need to be repositioned in accordance with the present invention so as to display the most significant digit in the left-hand number tube 16 of the visual display 14, and this is more easily done if the decimal point digit is held separately.

A bistable circuit 62 having the outputs A and $\overline{A}$ has the input connected by a highway 13 to a set of gates 64. A bistable circuit 66 having the outputs C and $\overline{C}$ has the input connected by a highway HW7 to a set of gates 68. A bistable circuit 70 having the outputs D and $\overline{D}$ has the input connected by a highway HW11 to a set of gates 72, partly hereinafter described (FIG. 9). A bistable circuit 74 having outputs E and $\overline{E}$ has the input connected by a highway HW12 to a set of gates

76, partly hereinafter described (FIG. 8). A bistable circuit 78 having the outputs H and $\overline{H}$ has the input connected by a highway HW14 to a set of gates 80.

The bistable circuit 62 controls which register has its number displayed by the visual display 14; if the bistable circuit 62 is set so that output A is energized the number stored in the input register 24 is displayed; if the bistable circuit 62 is set so that the output $\overline{A}$ is energized the number stored in the accumulator register 38 is displayed.

The bistable circuit 66 controls the time at which the input register can shift with respect to the accumulator register so that the four arithmetic functions can be performed by the calculating machine. If the bistable circuit 66 is set so that the output C is energized, shift can take place; if the bistable circuit 66 is reset so that the output $\overline{C}$ is energized the registers are held so that shift cannot take place.

The bistable circuit 70 together with the bistable circuit 66 controls the number of shift pulses sent through the set of gates 34 and 48 to the input register 24 and the accumulator register 38 respectively. The control operation is more fully described hereinafter.

The bistable circuit 74 has a control function during a multiplication operation as hereinafter described.

The FIGS. 2–9 show in greater detail, part of some of the set of gates shown in FIG. 1. Unless otherwise indicated in the description the circuits shown are AND-logic-circuit gates.

The FIG. 2 shows in detail part of the set of gates 48 shown in FIG. 1. The set of gates 48 includes the AND-gates 480 to 486, the transistor invertor circuits 480*a*, 481*a*, 482*a*, and 484*a*, the time delay circuits 481*b*, 483*a* and 485*a* and the circuits 486*a* and 486*b*. The circuit 486*b* comprises a transistor invertor circuit whose input is connected to the output D0 of the output bistable 60 and whose output is connected to an AND-logic gate. The output of the AND gate is connected to a capacitor C and to transistor invertor circuits 486*a*.

The FIG. 3 shows in detail part of the set of gates 34 shown in FIG. 1. The circuit in the Figure comprise the AND-gates 340 to 342, the OR-gates 341*a* and 342*a* and the transistor invertor circuit 340*a* for the output T0 of the timer circuit 12.

The FIG. 4 shows in detail part of the set of gates 58 shown in FIG. 1. The circuits in the Figure comprise the AND-gates 580 to 584, the transistor invertor circuit 582*a* for the "subtract" output from the decade counter circuit 10, and the circuit 584*a*, which is identical to the circuit 486*a* shown in FIG. 2.

The FIG. 5 shows in detail part of the set of gates 22 shown in FIG. 1. The circuits in the Figure comprise the AND-gates 220 to 222 and the invertor circuit 222*a* for the output TD of the timer circuit 12.

The FIG. 6 shows in detail part of the set of gates 50 shown in FIG. 1. The circuits in the Figure comprise the AND-gates 500 to 503, and the transistor invertor circuits 500*a*, 500*b*, 502*a* and 502*b* for the outputs T11 and T0 of the timer circuit 12 and the output B0 of the buffer 20.

The FIG. 7 shows in detail part of the set of gates 36 shown in FIG. 1. The circuits in the Figure comprise an AND-gate 360 and a transistor invertor circuit 360*a* for the output T0 of the timer circuit 12.

The FIG. 8 shows in detail part of the set of gates 76 shown in FIG. 1. The circuit shown in the Figure comprises an AND-gate 760.

The FIG. 9 shows in detail part of the set of gates 72 shown in FIG. 1. The circuits shown in the Figure comprise an AND-gate 720 and circuit 720*a* which is an OR gate connected to the input of a transistor invertor circuit.

The gate 480 (FIG. 2) supplies 12 shift pulses *d*P9 and the gate 486 supplies the 13th shift pulse if the input $\overline{LS}$ is energized, so that the shift pulses to the accumulator register 38 and the outputs of the timer circuit 12 occur in synchronism.

The method of number alignment to connect the effect of the overflow of the highest significant digit into the T11 digit stage as a result of a calculation will now be described for each of the arithmetic operations of multiplication, division, addition and subtraction in turn.

The calculating machine has other circuitry (not shown) which is interconnected with the parts of the calculating machine shown so that numbers can be entered into the input register 24 and accumulator register 38 through the digit keyboard 5, which numbers are used to perform arithmetic calculations selected from those on the function keyboard 8.

The answer to a calculation is stored in and circulates around the accumulator register 38 and is displayed when the inputs marker F0 on gates 220 etc., are energized. A digit is shifted into the shift register buffer 40 of the accumulator register 38 by a *d*P9 pulse which occurs at the same time as the next output of the timer circuit 12 is energized. The gate 500 (FIG. 6) is energized for the outputs T1, TD and T2 to T10 of the timer circuit 12 and allows 10 oscillator GD pulses (corresponding to the pulses P0 to P9) to circulate the digit in the shift register buffer 40. At the same time the gate 222 is shut (since the first bistable circuit 44 was reset by the first pulse P0) and does not allow oscillator GD pulses to pass into the buffer 20. When the digit in the shift register buffer 40 goes through 0, a pulse is passed to the first bistable circuit 44 and the second bistable 46 so that the outputs C02 and CP02 are energized. When the input C02 is energized the gate 222 allows a number of oscillator pulses GD equal to the digit in the shift register buffer 40 to enter the buffer 20. As previously described, the digit in the buffer 20 is cleared into the staticizer 18 at the next P0 pulse (which also resets the first bistable circuit 44) and the digit is displayed on the visual display 14.

In the multiplication operation the number in the accumulator register 38 is the multiplier and the number in the input register is the multiplicand. The product is stored in the accumulator register 38. The multiplication process consists of entering the 10s complement of the least significant digit in the accumulator register 38 into the buffer 20. The number in the input register 24 is added into the accumulator register 38 and on each addition the number in the buffer 20 is increased by one increment. When the buffer 20 reaches the zero count state, i.e., B0 is energized, after a number of additions equal to the least significant figure originally in the accumulator register, the input register 24 shifts one place to left and the 10s complement of the next highest significant digit of the number in the accumulator register 38 is entered into the buffer 20. This sequence is repeated until the product has been built up in the accumulation register 38 by successive addition of partial products.

If the highest significant figure of the product or partial product spills into the T11 digit stage of the accumulator, when the T11 digit stage is energized the signal B0 and the signal C02 are together energized so that the gate 760 is energized to reset the E bistable circuit 74 to energize the output $\overline{E}$. The signal E is an input to the gate 485 and as a result of the energizing of output E by the gate 760, the gate 485 passes the 14th shift pulse to the accumulator register 38 to cause the accumulator register to shift one digit stage to the right.

In the division operation, the number in the accumulator register 38 is the dividend and the number in the input register 24 is the divisor. The quotient is stored in the accumulator register. The division operation takes place with the input register shifted to the right with respect to the accumulator. The division process consists of transferring the most significant digit of dividend (plus one) to the buffer and then successively subtracting the divisor from the dividend until the dividend goes negative. The divisor is then added back to the dividend and a right shift operation takes place. As the division operation continues the quotient is built up digit by digit from the highest significant figure of the accumulator register. Cases of division may occur where the first digit of the divisor is some way down the input register 24 and, in this case, the calculating machine would try to calculate a first digit of quotient greater than 9 and would spill its answer to the left into the T11 digit stage of the accumulator register. This case is guarded against by having a condition in the division routine that the first quotient digit is 0 (this digit is held at T11 and is not displayed). The first digit of dividend held at T11 is 0,

therefore, the first subtraction of the divisor should drive the buffer **20** to 0 (so that the output BO is energized) if the above condition is satisfied. If the condition is not satisfied then the gate **484** (FIG. 2) is energized to add an extra, 14th, shift pulse at **P5** to shift the accumulator register **38** to the right and the division routine begins again. Eventually the first quotient digit will be 0 and the division process proper can continue.

In the addition operation, the number in the input register **24** is added to the number in the accumulator register **38**. The answer is displayed in the accumulator register. The number are aligned before addition by relative shifting of the input and accumulator register by a number of shifts equal to the difference between the decimal point count.

If, when the numbers are added together, there is a carry into the **T11** stage of the accumulator, the output **CP02** of the carry store is energized to **T11**. The gate **482** is energized to pass a **P5** pulse as the 14th shift pulse to the accumulator register so as to cause the accumulator register **38** to shift one digit stage to the right with respect to the timer circuit **12**. The gate **582** is energized to pass a **P0** pulse to the decimal point counter to move the decimal point one space to the right.

The subtraction operation is similar to the addition operation and is done by the usual method of complementary addition. The right shift operation for the subtraction operation is identical with the right shift operation previously described for the addition operation.

When the arithmetical calculation is completed the result of the calculation is stored in the accumulator register **38** and is displayed by the number tube circuit **16** in the visual display **14** when the display signal **F0** is energized. The gate **480** supplies 12 shift pulses during the periods the outputs **T0** to **T10** are energized and the gate **486**, if the input $\overline{LS}$ is energized supplies the 13th shift pulse during the period that the output **T11** is energized so that the digit stages of the accumulator register **38** are in step with the outputs **T0** to **T11** from the timer circuit **12**. Also, at the time the output **T11** is energized the gate **583** controls the transmission of nine oscillator pulses GD to the decimal point counter **56**, and the gate **584**, if the input $\overline{LS}$ is energized, supplies a 10th pulse to the decimal point counter **56** at the time of the pulse **P0** so that the decimal point count in the decimal point counter is circulated at the time the output **T11** is energized. The outputs $\overline{LS}$ are the outputs of the circuits **486***a* and **584***a*. These circuits are an AND gate with the inputs display input **F0**, $\overline{DO}$ **P9**, $\overline{A}$ and $\overline{C02}$ and the output connected to a capacitor C and connected to a transistor invertor gate. When all the inputs to the AND gate are energized, the output of the AND gate charges up the capacitor C to a voltage which lasts long enough to bias the transistor invertor gate into conduction so that the outputs $\overline{LS}$ would be near 0 voltage, during the period when the next "T" output is energized. Thus if the AND gate charged up the capacitor C during the time the **T10** output of the timer circuit **12** is energized, the output $\overline{LS}$ of the circuits **486***a* and **584***a* would be near 0 voltage and so keep the gates **486** and **584** shut, during the time the output **T11** of the timer circuit **12** is energized.

The gates **486** and **584** and the circuits **486***a* and **584***a* are used to cause a left shift operation to position the highest significant figure of the result of a calculation at the left hand or **T10** number tube circuit **16** of the visual display **14** so as to make the maximum use of the number tube circuits of the visual display **14**. The two situations where a left shift would be used is, if as a result of, say, a subtraction operation a resultant was displayed which either was greater than unity but has zeros at the most significant end of the number tube circuits before the decimal point position.

Thus the essential requirements for a left shift are (a) the decimal point count is not at the zero position at the left hand and, i.e., the output $\overline{DO}$ is energized, and (b) the accumulator carry store output is 0 when the output **T10** is energized, i.e., $\overline{C02}$ is energized. Thus if the conditions (a) and (b) are fulfilled and the signal $\overline{A}$ is energized to display the accumulator register **38**, the AND gates of the circuit **486***a* and **584***a* charge up the capacitor C during the time the output **T10** is energized. The charged capacitor C inhibits the gate **486** and **584** during the time of the next shift pulse when the output **T11** is energized so that only 12 shift pulses and nine decimal point pulses pass to the accumulator register **38** and the decimal point counter **56** respectively. The result is a shift of one position left of the number and its decimal point. This action is repeated until either of the two conditions (a) and (b) is no longer fulfilled.

What we claim is:

1. A calculating machine comprising a number store register having a plurality of register stages for storing digit pulses representative of the digits of a number entered in the number store register; a multistage display device for displaying the digits of the number stored in the number store register, each stage in the display device being designated to display a particular digit of a number stored in the register stages; shifting means for transferring the digit pulses representative of the number from one register stage to another of the plurality of register stages; means for detecting the presence of a digit pulse of predetermined value at a particular register stage, display timer transfer means causing the digit pulse of the number entered in the particular register stage to be displayed at a predetermined stage in the display device designated for that digit of the number in the number store register; a circuit connecting the stages of the number store register to form an endless loop shift register circuit; said transfer means comprising a first set of AND gates, and a circuit connecting at least one input of said gates to the number store register and to a particular stage of the display device to display the highest significant digit of the number stored in the register at a predetermined display device stage.

2. A calculating machine according to claim **1**, wherein the calculating machine further includes a master oscillator; and input decade counter with 11 outputs connected to the output of the master oscillator to divide the continuously generated oscillator pulses into a continuous sequence of trains of 10 pulses which appear on 10 outputs respectively with each train of pulses being separated from the next train of pulses by a shift pulse which appears on a shift pulse output; and a timer circuit in said display timer transfer means having a number of outputs equal to the number of stages in the number store register, the input of the timer circuit being connected to the output of the one input of said gates to the number store register and to a particular stage of the display device to display the highest significant digit of the number stored in the register at a predetermined display device stage. 0

3. A calculating machine according to claim **2**, wherein the stages of the multistage display device include number tube circuits, the anodes of the number tubes are connected in sequence to a source of electric potential under the control of the outputs of the timer circuit at a frequency such that numbers appear steady by the persistence effect of ocular vision, a circuit connecting the cathodes of the number tubes shaped to the same digit together as groups of cathodes; and wherein the calculating machine further includes a buffer counter having 10 count state outputs including a 0 count state output; a group of four bistable circuits and whose inputs are connected to the outputs of the count state and whose outputs are connected to the groups of cathodes so that the 10 count states are connected to correspond with the groups of cathodes shaped to the digit corresponding to the count state respectively; and a third set of AND gates and accompanying circuit connecting at least one input of a gate of the third set of gates to enter a train of pulses equal in number to the number of the digit in the shift register buffer into the buffer when one of the outputs of the timer circuit is energized.

4. A calculating machine according to claim **2** including circuit means causing during one cycle of the timer circuit the number of shift pulses transmitted to the number store register to be one less than the number of stages so that the decimal point and the number move one stage to the right, and causing this to be repeated for each cycle of the timer circuit until

either the decimal point count reaches zero or until at the next higher stage after the predetermined stage a nonzero digit is presented in the predetermined stage of the visual display.

5. A calculating machine according to claim 1, wherein a stage of the number store register is internally interconnected as a decade counter to form a shift register buffer; and wherein the calculating machine further includes a carry store whose input is connected to an output of the shift register buffer, and a circuit including a second set of AND gates connected to control the passage of a train of 10 pulses from the input decade counter into the shift register buffer to circulate the digit stored in the counter so that when the digit passes through the zero digit valve a pulse is emitted from the decade counter to energize a carry output of the carry store.

6. A calculating machine according to claim 1 including sensing means having an input from the output of the timer circuit which corresponds to a stage on the visual register one stage higher than the predetermined stage in the visual display for the highest significant digit of the number entered in the number store register and means responsive to said sensing means to shift the position of the highest significant digit one stage down the display device.

7. A calculating machine according to claim 6, wherein the display device includes 10 neon bulbs to represent the position of the decimal point in the number displayed on the visual display, means connecting one conductor of each of the neon bulbs to an output of the timer circuit, means connecting the other conductor of each neon bulb in in ascending order of a 10 count state respectively, means providing a 10 count state with the zero count state corresponding to the decimal point at the highest significant digit end of the visual display, and a decimal point decade counter having an output which is energized when the decimal point count is zero, and a further set of AND gates and corresponding circuit means connecting the latter AND gate outputs to the input of the decimal point counter, connecting one input of at least some of these gates to the output of the timer circuit which corresponds to a stage on the visual register one stage higher than the predetermined stage in the visual display for the highest significant digit of the number entered in the number store register, and connecting at least one input of one of these gates to the output of the timer circuit which is connected to the decimal point neon bulbs.

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