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(54) Title: CORROSION RESISTANT ELECTRODE FOR A SEMICONDUCTOR LIGHT EMITTING LIGHT DEVICE AND METHOD FOR MANUFACTURING THE SAME

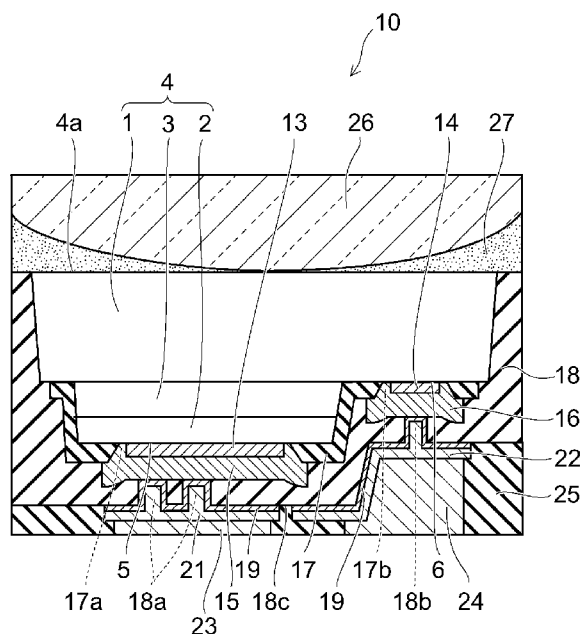


FIG. 1

(57) Abstract: According to one embodiment, a semiconductor light emitting device includes a semiconductor layer (4), an insulating film (17), a p-side contact electrode (13), an n-side contact electrode (14), a p-side metal protective film (17), and an n-side metal protective film. The semiconductor layer includes a light emitting layer (13). A second surface of the semiconductor layer is formed on a side opposite to the first surface. The second surface has a light emitting portion including the light emitting layer and a non-light emitting portion not including the light emitting layer. The p-side contact electrode is provided in contact with the light emitting portion inside a first opening of the insulating film. The n-side contact electrode is provided in contact with the non-light emitting portion inside a second opening of the insulating film. The p-side metal protective film covers a top surface and a side surface of the p-side contact electrode. The n-side metal protective film covers a top surface and a side surface of the n-side contact electrode.



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Description

Title of Invention: CORROSION RESISTANT ELECTRODE FOR A SEMICONDUCTOR LIGHT EMITTING LIGHT DEVICE AND METHOD FOR MANUFACTURING THE SAME

Field

[0001] Embodiments described herein relate generally to a semiconductor light emitting device and a method for manufacturing the same.

Background

[0002] In wafer-level LED (Light Emitting Diode) packaging technology in which the packaging process is performed collectively in the wafer state, processes of forming a semiconductor layer including a light emitting layer, etc., and contact electrodes having ohmic contact with the semiconductor layer are performed; and subsequently, processes of forming interconnect layers, a resin layer, a phosphor layer, etc., are performed. In the case where there are many processes after the forming of the contact electrodes or in the case where such processes are many steps, chemical liquids, etc., used in such processes may corrode the contact electrodes.

Citation List

Patent Literature

[0003] PTL 1: JP-A 2010-141176
PTL 2: JP-A 2004-103975

Brief Description of Drawings

[0004] FIG. 1 is a schematic cross-sectional view of a semiconductor light emitting device of an embodiment.

FIGS. 2A to 9B are schematic cross-sectional views illustrating a method for manufacturing the semiconductor light emitting device of the embodiment.

FIG. 10 is a schematic cross-sectional view of a semiconductor light emitting device of another embodiment.

FIG. 11 is a schematic cross-sectional view of a semiconductor light emitting device of yet another embodiment.

FIG. 12 is a schematic cross-sectional view of a semiconductor light emitting device of still yet another embodiment.

FIGS. 13A and 13B are schematic views illustrating the planar layout of the main components of the semiconductor light emitting device of the embodiment.

Detailed Description

[0005] According to one embodiment, a semiconductor light emitting device includes a semiconductor layer, an insulating film, a p-side contact electrode, an n-side contact electrode, a p-side metal protective film, and an n-side metal protective film.

The semiconductor layer includes a light emitting layer, a first surface, and a second surface. The second surface is formed on a side opposite to the first surface. The second surface has a light emitting portion including the light emitting layer and a non-light emitting portion not including the light emitting layer. The insulating film is provided on the second surface. The insulating film has a first opening connecting with the light emitting portion and a second opening connecting with the non-light emitting portion. The p-side contact electrode is provided in contact with the light emitting portion inside the first opening. The n-side contact electrode is provided in contact with the non-light emitting portion inside the second opening. The p-side metal protective film covers a top surface and a side surface of the p-side contact electrode. The n-side metal protective film covers a top surface and a side surface of the n-side contact electrode.

[0006] Embodiments will now be described with reference to the drawings. Similar components in the drawings are marked with like reference numerals.

[0007] FIG. 1 is a schematic cross-sectional view of a semiconductor light emitting device 10 of the embodiment.

[0008] The semiconductor light emitting device 10 includes a semiconductor layer 4. The semiconductor layer 4 includes a first surface 4a and a second surface formed in an uneven configuration on a side opposite to the first surface 4a. Electrodes, interconnect layers, and resin layers are provided on the second surface side. Light is emitted to the outside mainly from the first surface 4a on the side opposite to the second surface.

[0009] The semiconductor layer 4 includes a first semiconductor layer 1 and a second semiconductor layer 2. Both the first semiconductor layer 1 and the second semiconductor layer 2 include, for example, III-V nitride semiconductor. The first semiconductor layer 1 includes, for example, a foundation buffer layer, an n-type layer, etc.; and the n-type layer functions as a lateral-direction path of current. The second semiconductor layer 2 has a stacked structure in which a light emitting layer (an active layer) 3 is interposed between an n-type layer and a p-type layer.

[0010] The second surface of the semiconductor layer 4 is patterned into an uneven configuration. The second surface includes a light emitting portion 5 formed in a protruding configuration that includes the light emitting layer 3, and a non-light emitting portion 6 that does not include the light emitting layer 3.

[0011] A p-side contact electrode 13 is provided on the top surface of the second semiconductor layer 2 which is the top surface of the light emitting portion 5. An n-side contact electrode 14 is provided on the top surface of the first semiconductor layer 1 which is the top surface of the non-light emitting portion 6.

[0012] The p-side contact electrode 13 includes, for example, a first nickel (Ni) film provided on the top surface of the second semiconductor layer 2, a silver (Ag) film

provided on the first nickel film, and a second nickel film provided on the silver film.

- [0013] The first nickel film has ohmic contact with the top surface of the second semiconductor layer 2 which is, for example, a III-V nitride semiconductor. The reflectance of the silver is 98% with respect to light of 600 nm or more, 98% with respect to light near 500 to 600 nm, and 97% with respect to light near 450 to 500 nm; and the silver has high reflectance for wavelengths in the visible region. The second nickel film prevents sulfidization of the silver film during the plating and the wet etching described below.
- [0014] The n-side contact electrode 14 includes, for example, a first titanium (Ti) film provided on the top surface of the first semiconductor layer 1, an aluminum (Al) film provided on the first titanium film, a tantalum (Ta) film provided on the aluminum film, a second titanium film provided on the tantalum film, and a platinum (Pt) film provided on the second titanium film.
- [0015] The first titanium film has ohmic contact with the top surface of the first semiconductor layer 1 which is, for example, III-V nitride semiconductor. The tantalum film functions as a barrier metal that prevents the alloying of the metals thereon and thereunder.
- [0016] There are cases where the area of the light emitting portion 5 is larger than the area of the non-light emitting portion 6; and there are cases where the surface area of the light emitting portion 5 is less than the surface area of the non-light emitting portion 6. There are cases where the area of the p-side contact electrode 13 provided in the light emitting portion 5 is larger than the area of the n-side contact electrode 14 provided in the non-light emitting portion 6; and there are cases where the area of the p-side contact electrode 13 provided in the light emitting portion 5 is less than the area of the n-side contact electrode 14 provided in the non-light emitting portion 6. In the semiconductor light emitting device 10 illustrated in FIG. 1, the area of the light emitting portion 5 is larger than the area of the non-light emitting portion 6.
- [0017] An insulating film 17 is provided on the second surface of the semiconductor layer 4. The insulating film 17 is an inorganic film such as, for example, a silicon oxide film. The insulating film 17 covers a portion of the top surface of the light emitting portion 5 and a portion of the top surface of the non-light emitting portion 6. The insulating film 17 also covers the side surface of the light emitting portion 5 having the protruding configuration.
- [0018] The insulating film 17 has a first opening 17a and a second opening 17b. The first opening 17a connects with the top surface of the light emitting portion 5; and the second opening 17b connects with the top surface of the non-light emitting portion 6.
- [0019] An inner wall of the first opening 17a is tilted with respect to the top surface of the light emitting portion 5. Specifically, the opening area of the first opening 17a

increases from the top surface side of the light emitting portion 5 toward the top surface side of the insulating film 17. In other words, the cross section of the first opening 17a in FIG. 1 is formed in a trapezoidal configuration.

- [0020] Similarly, an inner wall of the second opening 17b is tilted with respect to the top surface of the non-light emitting portion 6. Specifically, the opening area of the second opening 17b increases from the top surface side of the non-light emitting portion 6 toward the top surface side of the insulating film 17. In other words, the cross section of the second opening 17b in FIG. 1 is formed in a trapezoidal configuration.
- [0021] The p-side contact electrode 13 has ohmic contact with the top surface of the light emitting portion 5 (the top surface of the second semiconductor layer 2) inside the first opening 17a. The n-side contact electrode 14 has ohmic contact with the top surface of the non-light emitting portion 6 (the top surface of the first semiconductor layer 1) inside the second opening 17b.
- [0022] The planar size of the bottom face of the first opening 17a on the light emitting portion 5 side is larger than the planar size of the p-side contact electrode 13; and the inner wall of the first opening 17a is separate from the side surface of the p-side contact electrode 13.
- [0023] The planar size of the bottom face of the second opening 17b on the non-light emitting portion 6 side is larger than the planar size of the n-side contact electrode 14; and the inner wall of the second opening 17b is separate from the side surface of the n-side contact electrode 14.
- [0024] The insulating film 17 is thicker than the p-side contact electrode 13; and the depth of the first opening 17a is larger than the thickness of the p-side contact electrode 13. The insulating film 17 is thicker than the n-side contact electrode 14; and the depth of the second opening 17b is larger than the thickness of the n-side contact electrode 14.
- [0025] A p-side metal protective film 15 is provided on the top surface and the side surface of the p-side contact electrode 13. The p-side metal protective film 15 is provided also on the top surface of the light emitting portion 5 in the gap between the inner wall of the first opening 17a and the side surface of the p-side contact electrode 13. The p-side metal protective film 15 is provided also on the inner wall of the first opening 17a to fill the gap. A portion of the p-side metal protective film 15 also is provided to rise onto the top surface of the insulating film 17 around the first opening 17a.
- [0026] In other words, the p-side metal protective film 15 has a planar size larger than those of the p-side contact electrode 13 and the first opening 17a, and covers the top surface and the side surface of the p-side contact electrode 13.

FIG. 13A illustrates an example of the planar layout of the main components of the semiconductor light emitting device 10. FIG. 13B illustrates another specific example of the planar layout.

As illustrated in FIGS. 13A and 13B, the p-side metal protective film 15 covers all around the p-side contact electrode 13 or the entire side surface of the p-side contact electrode 13.

[0027] In FIG. 1, the p-side metal protective film 15 includes, for example, a first titanium (Ti) film, a platinum (Pt) film provided on the first titanium film, a gold (Au) film provided on the platinum film, and a second titanium film provided on the gold film in order from the p-side contact electrode 13 side.

[0028] Of these films, the gold film, which does not undergo reactions such as oxidization and sulfidization, is thickest. The second titanium film has excellent adhesion with an insulating layer (e.g., polyimide) 18 described below. A nickel (Ni) film or a molybdenum (Mo) film may be used instead of the second titanium film.

[0029] An n-side metal protective film 16 is provided on the top surface and the side surface of the n-side contact electrode 14. The n-side metal protective film 16 is provided also on the top surface of the non-light emitting portion 6 in the gap between the inner wall of the second opening 17b and the side surface of the n-side contact electrode 14. The n-side metal protective film 16 is provided also on the inner wall of the second opening 17b to fill the gap. A portion of the n-side metal protective film 16 is also provided to rise onto the top surface of the insulating film 17 around the second opening 17b.

[0030] In other words, the n-side metal protective film 16 has a planar size larger than those of the n-side contact electrode 14 and the second opening 17b, and covers the top surface and the side surface of the n-side contact electrode 14. As illustrated in FIGS. 13A and 13B, the n-side metal protective film 16 covers the entire side surface of the n-side contact electrode 14. The n-side metal protective film 16 is thicker than the n-side contact electrode 14.

[0031] In FIG. 1, the n-side metal protective film 16 includes, for example, a first titanium (Ti) film, a platinum (Pt) film provided on the first titanium film, a gold (Au) film provided on the platinum film, and a second titanium film provided on the gold film in order from the n-side contact electrode 14 side.

[0032] Of these films, the gold film, which does not undergo reactions such as oxidization and sulfidization, is thickest. The second titanium film has excellent adhesion with the insulating layer (e.g., polyimide) 18 described below. A nickel (Ni) film or a molybdenum (Mo) film may be used instead of the second titanium film.

[0033] A portion of the p-side metal protective film 15 and a portion of the n-side metal protective film 16 are covered with the insulating layer 18. The insulating layer 18 also covers the insulating film 17 and the side surface of the first semiconductor layer 1. The insulating layer 18 is, for example, a resin such as polyimide having excellent patternability of ultra-fine openings. Alternatively, an inorganic substance such as silicon oxide, silicon nitride, etc., may be used as the insulating layer 18.

- [0034] The insulating layer 18 has a first via 18a that reaches the p-side metal protective film 15 and a second via 18b that reaches the n-side metal protective film 16. The insulating layer 18 includes an interconnect surface 18c on the side opposite to the p-side metal protective film 15 and the n-side metal protective film 16. A p-side re-interconnect layer 21 and an n-side re-interconnect layer 22 are provided apart from each other on the interconnect surface 18c.
- [0035] The p-side re-interconnect layer 21 is provided also inside the first via 18a and is electrically connected to the p-side metal protective film 15 and the p-side contact electrode 13. The n-side re-interconnect layer 22 is provided also inside the second via 18b and is electrically connected to the n-side metal protective film 16 and the n-side contact electrode 14. The p-side re-interconnect layer 21 and the n-side re-interconnect layer 22 are made of, for example, copper (Cu).
- [0036] A metal film 19 is provided between the p-side re-interconnect layer 21 and the p-side metal protective film 15, and between the p-side re-interconnect layer 21 and the insulating layer 18. The metal film 19 includes a copper (Cu) film and a titanium (Ti) film provided in order from the p-side re-interconnect layer 21 side. The metal film 19 is provided also between the n-side re-interconnect layer 22 and the n-side metal protective film 16, and between the n-side re-interconnect layer 22 and the insulating layer 18.
- [0037] A p-side metal pillar 23 is provided on the surface of the p-side re-interconnect layer 21 on the side opposite to the p-side metal protective film 15. The metal film 19, the p-side re-interconnect layer 21, and the p-side metal pillar 23 are included in the p-side interconnect layer of the embodiment.
- [0038] An n-side metal pillar 24 is provided on the surface of the n-side re-interconnect layer 22 on the side opposite to the n-side metal protective film 16. The metal film 19, the n-side re-interconnect layer 22, and the n-side metal pillar 24 are included in the n-side interconnect layer of the embodiment.
- [0039] A resin layer 25 is provided as a second insulating layer on the interconnect surface 18c of the insulating layer 18, between the p-side re-interconnect layer 21 and the n-side re-interconnect layer 22, and between the p-side metal pillar 23 and the n-side metal pillar 24.
- [0040] The surface of the p-side metal pillar 23 on the side opposite to the p-side re-interconnect layer 21 is exposed from the resin layer 25 and functions as the p-side external terminal for the mounting. The surface of the n-side metal pillar 24 on the side opposite to the n-side re-interconnect layer 22 is exposed from the resin layer 25 and functions as the n-side external terminal for the mounting. The p-side external terminal and the n-side external terminal are bonded with a bonding agent such as solder, another metal, electrically conductive material, etc., to pads formed in the mounting

substrate. The p-side external terminal and the n-side external terminal are formed in the same surface; and the mounting surface of the semiconductor light emitting device 10 is a substantially flat surface.

- [0041] It is possible to supply current with a more uniform distribution to the light emitting portion 5 as the area of the p-side contact electrode 13 increases. The current distribution of the light emitting portion 5 depends on the positions and the number of the first vias 18a. The first via 18a may be connected to the p-side metal protective film 15 at a position away from the region where the p-side metal pillar 23 spreads.
- [0042] The p-side re-interconnect layer 21 and the p-side metal pillar 23 can be formed using a low-resistance metal such as, for example, copper. The heat conduction and the heat dissipation of the p-side re-interconnect layer 21 and the p-side metal pillar 23 increase and it is possible to efficiently release the heat of the light emitting portion 5 as the planar sizes of the p-side re-interconnect layer 21 and the p-side metal pillar 23 increase.
- [0043] The area of the surface of the n-side re-interconnect layer 22 on the side opposite to the n-side metal protective film 16 is larger than the area of the n-side contact electrode 14. Thereby, an electrode structure drawn out to a wider region can be realized via the n-side re-interconnect layer 22 for the n-side contact electrode 14 provided in the non-light emitting portion 6 which is narrower than the light emitting portion 5.
- [0044] The first semiconductor layer 1 is electrically connected to the n-side metal pillar 24 via the n-side contact electrode 14, the n-side metal protective film 16, the metal film 19, and the n-side re-interconnect layer 22. The second semiconductor layer 2 that includes the light emitting layer 3 is electrically connected to the p-side metal pillar 23 via the p-side contact electrode 13, the p-side metal protective film 15, the metal film 19, and the p-side re-interconnect layer 21.
- [0045] The p-side interconnect layer which includes the p-side re-interconnect layer 21 and the p-side metal pillar 23 is thicker than the p-side contact electrode 13. The n-side interconnect layer which includes the n-side re-interconnect layer 22 and the n-side metal pillar 24 is thicker than the n-side contact electrode 14. The p-side metal pillar 23 is thicker than the p-side re-interconnect layer 21; and the n-side metal pillar 24 is thicker than the n-side re-interconnect layer 22. The p-side metal pillar 23, the n-side metal pillar 24, and the resin layer 25 filled between the p-side metal pillar 23 and the n-side metal pillar 24 increase the mechanical strength of the semiconductor light emitting device 10.
- [0046] Copper, gold, nickel, silver, etc., can be used as the materials of the p-side re-interconnect layer 21, the n-side re-interconnect layer 22, the p-side metal pillar 23, and the n-side metal pillar 24. Of these, good thermal conductivity, high migration resistance, and excellent adhesion with the insulating materials are obtained when copper

is used.

- [0047] The resin layer 25 reinforces the p-side metal pillar 23 and the n-side metal pillar 24. It may be desirable for the resin layer 25 to have a coefficient of thermal expansion near to or the same as that of the mounting substrate. Examples of such a resin layer 25 include, for example, an epoxy resin, a silicone resin, a fluorocarbon resin, etc.
- [0048] According to the embodiment, it is possible to maintain the mechanical strength by the p-side metal pillar 23, the n-side metal pillar 24, and the resin layer 25 being thick even in the case where the semiconductor layer 4 is thin and there is no substrate to support the semiconductor layer 4.
- [0049] Stress applied to the semiconductor layer 4 via the solder, etc., in the state in which the semiconductor light emitting device 10 is mounted to the mounting substrate can be mitigated by being absorbed by the p-side metal pillar 23 and the n-side metal pillar 24.
- [0050] A lens 26 and a phosphor layer 27 are provided on the first surface 4a of the semiconductor layer 4 as a transparent body which is transparent to the light emitted from the light emitting layer 3. The lens 26 is provided on the phosphor layer 27. Alternatively, the phosphor layer 27 may be provided on the lens 26. A structure may be used in which only the phosphor layer 27 or only the lens 26 is provided on the first surface 4a.
- [0051] The phosphor layer 27 includes a transparent resin and a phosphor dispersed in the transparent resin. The phosphor layer 27 is capable of absorbing the light emitted from the light emitting layer 3 and emitting a wavelength-converted light. Therefore, the semiconductor light emitting device 10 is capable of emitting a mixed light of the light from the light emitting layer 3 and the wavelength-converted light of the phosphor layer 27.
- [0052] For example, white, lamp, etc., can be obtained as the mixed color of a blue light from the light emitting layer 3 and a yellow light which is the wavelength-converted light of the phosphor layer 27 in the case where the light emitting layer 3 is III-V nitride semiconductor and the phosphor is a yellow phosphor configured to emit the yellow light. The phosphor layer 27 may have a configuration including multiple types of phosphors (e.g., a red phosphor configured to emit red light and a green phosphor configured to emit green light).
- [0053] The light emitted from the light emitting layer 3 is emitted to the outside mainly from the first surface 4a via the phosphor layer 27 and the lens 26.
- [0054] In the semiconductor light emitting device 10 of the embodiment, the surfaces of the p-side contact electrode 13 other than the surface contacting the second semiconductor layer 2 are covered with the p-side metal protective film 15. Similarly, the surfaces of the n-side contact electrode 14 other than the surface contacting the first semiconductor

layer 1 are covered with the n-side metal protective film 16.

[0055] The p-side metal protective film 15 and the n-side metal protective film 16 protect the p-side contact electrode 13 and the n-side contact electrode 14 from the chemical liquids, etc., used in the processes described below performed after the formation of these contact electrodes. The p-side metal protective film 15 and the n-side metal protective film 16 include mainly, for example, gold (Au) which does not undergo reactions such as oxidization and sulfidization.

The lower surface of the p-side metal protective film 15 (the surface on the p-side re-interconnect layer 21 side) has a dish-like configuration; and the edge portion is raised higher than the central portion. The lower surface of the p-side metal protective film 15 has a concave configuration. Therefore, it is easier to protect the p-side contact electrode 13 because the distance of the interface along which chemical liquids, etc., are conveyed is long. Because the lower surface of the p-side metal protective film 15 has a concave configuration, the chemical liquids do not easily overflow outside the portion having the concave configuration.

The lower surface of the n-side metal protective film 16 (the surface on the n-side re-interconnect layer 22 side) has a dish-like configuration; and the edge portion is raised higher than the central portion. The lower surface of the n-side metal protective film 16 has a concave configuration. Therefore, it is easier to protect the n-side contact electrode 14 because the distance of the interface along which the chemical liquids, etc., are conveyed is long. Because the lower surface of the n-side metal protective film 16 has a concave configuration, the chemical liquids do not easily overflow outside the portion having the concave configuration.

The edges of the p-side metal protective film 15 and the n-side metal protective film 16 are raised because the peripheries of the edges of the p-side metal protective film 15 and the n-side metal protective film 16 go up (extend) onto the insulating film 17.

[0056] Gold does not easily form an ohmic contact with the semiconductor layer 4 which is, for example, III-V nitride semiconductor. Accordingly, the p-side contact electrode 13 and the n-side contact electrode 14 include a metal that has good ohmic contact with the semiconductor layer 4. Even in the case where such a metal easily undergoes a reaction such as oxidization, sulfidization, etc., degradation of the p-side contact electrode 13 and the n-side contact electrode 14 and an increase of the resistance of the p-side contact electrode 13 and the n-side contact electrode 14 can be prevented because the top surface and the side surface of the p-side contact electrode 13 are covered with the p-side metal protective film 15 and the top surface and the side surface of the n-side contact electrode 14 are covered with the n-side metal protective film 16. As a result, a deterioration of the characteristics of the semiconductor light emitting device 10 can be prevented.

- [0057] A method for manufacturing the semiconductor light emitting device 10 of the embodiment will now be described with reference to FIG. 2A to FIG. 9B. In the drawings illustrating the processes described below, a region of a portion of the wafer state is illustrated.
- [0058] FIG. 2A illustrates a stacked body in which the semiconductor layer 4 including the first semiconductor layer 1 and the second semiconductor layer 2 is formed on a major surface of a substrate 8. The first semiconductor layer 1 is formed on the major surface of the substrate 8; and the second semiconductor layer 2 that includes the light emitting layer 3 is formed on the first semiconductor layer 1. The surface of the first semiconductor layer 1 contacting the substrate 8 becomes the first surface 4a of the semiconductor layer 4.
- [0059] In the case where the first semiconductor layer 1 and the second semiconductor layer 2 are, for example, III-V nitride semiconductors, these can be deposited on, for example, a sapphire substrate, a Si substrate using MOCVD (Metal Organic Chemical Vapor Deposition).
- [0060] The first semiconductor layer 1 includes, for example, a foundation buffer layer and an n-type GaN layer. The second semiconductor layer 2 includes the light emitting layer (the active layer) 3 and a p-type GaN layer. The light emitting layer 3 may be configured to emit blue, violet, bluish-violet, ultraviolet light, etc.
- [0061] Then, a portion of the first semiconductor layer 1 is exposed by removing a portion of the second semiconductor layer 2 as illustrated in FIG. 2B by, for example, RIE using a not-illustrated resist. The portion where the first semiconductor layer 1 is exposed becomes the non-light emitting portion 6 which does not include the light emitting layer 3. The second semiconductor layer 2 that remains in the protruding configuration becomes the light emitting portion 5 which includes the light emitting layer 3.
- [0062] Continuing as illustrated in FIG. 3A, the insulating film 17 is formed on the entire surface of the second surface of the semiconductor layer 4 which includes the light emitting portion 5 and the non-light emitting portion 6. The insulating film 17 is, for example, a silicon oxide film.
- [0063] Then, as illustrated in FIG. 3B, a resist mask 51 is formed on the insulating film 17; and the insulating film 17 is selectively etched using the resist mask 51 as a mask. An opening 51a is made in the resist mask 51. The first opening 17a is made in the insulating film 17 below the opening 51a. The first opening 17a reaches the top surface of the light emitting portion 5 (the top surface of the second semiconductor layer 2).
- [0064] Continuing, the p-side contact electrode 13 is formed on the top surface of the light emitting portion 5 inside the first opening 17a. At this time, the resist mask 51 used during the etching that made the first opening 17a remains; and the p-side contact

electrode 13 is formed by, for example, vapor deposition using the resist mask 51 as a mask.

[0065] The etching of the insulating film 17 progresses not only in the film thickness direction but also in the surface direction. Accordingly, the width of the first opening 17a made in the insulating film 17 becomes larger than the width of the opening 51a of the resist mask 51. The portion of the insulating film 17 facing the first opening 17a has a tapered configuration. The p-side contact electrode 13 is formed substantially directly under the opening 51a of the resist mask 51. Accordingly, a gap is made between the inner wall of the first opening 17a and the side surface of the p-side contact electrode 13.

[0066] Then, as illustrated in FIG. 4A, a resist mask 61 is formed on the insulating film 17 and the p-side contact electrode 13; and the insulating film 17 is selectively etched using the resist mask 61 as a mask. An opening 61a is made in the resist mask 61. The second opening 17b is made in the insulating film 17 below the opening 61a. The second opening 17b reaches the front surface of the non-light emitting portion 6 (the front surface of the first semiconductor layer 1).

[0067] Continuing, the n-side contact electrode 14 is formed on the front surface of the non-light emitting portion 6 inside the second opening 17b. At this time, the resist mask 61 used during the etching that made the second opening 17b remains; and the n-side contact electrode 14 is formed by, for example, vapor deposition using the resist mask 61 as a mask.

[0068] The etching of the insulating film 17 progresses not only in the film thickness direction but also in the surface direction. Accordingly, the width of the second opening 17b made in the insulating film 17 becomes larger than the width of the opening 61a of the resist mask 61. The portion of the insulating film 17 facing the second opening 17b has a tapered configuration. The n-side contact electrode 14 is formed substantially directly under the opening 61a of the resist mask 61. Accordingly, a gap is made between the inner wall of the second opening 17b and the side surface of the n-side contact electrode 14.

[0069] The second opening 17b may be made first; and the n-side contact electrode 14 may be formed before the p-side contact electrode 13.

[0070] The number of processes can be reduced by using the same resist mask 51 for the etching of the first opening 17a and the formation of the p-side contact electrode 13. Similarly, the number of processes can be reduced by using the same resist mask 61 for the etching of the second opening 17b and the formation of the n-side contact electrode 14.

[0071] It is conceivable to simultaneously make the first opening 17a and the second opening 17b. Then, in the case where the materials of the p-side contact electrode 13

and the n-side contact electrode 14 are different, one selected from the first opening 17a and the second opening 17b may be covered with a resist mask; and in this state, the p-side contact electrode 13 or the n-side contact electrode 14 is formed in the other opening. However, in the case where the opening is made and subsequently covered with the resist mask, an organic film may undesirably remain on the bottom face of the opening. This may lead to an increase of the contact resistance between the contact electrodes and the semiconductor layer.

[0072] In the embodiment, the contact electrode is formed continuing from the etching of the opening using the same resist mask. Therefore, the bottom face of the opening is not covered with the resist mask. Therefore, the contact electrode can be formed on the exposed surface as-is after the etching; and the increase of the contact resistance can be suppressed.

[0073] The first opening 17a and the second opening 17b may be made simultaneously; the resist mask used in the etching of these openings may remain as-is; and the p-side contact electrode 13 and the n-side contact electrode 14 may be formed simultaneously from the same material continuing from the etching.

[0074] Then, after removing the resist mask used for the etching of the insulating film 17 and the formation of the contact electrode, a resist mask 52 is formed on the insulating film 17 as illustrated in FIG. 4B. An opening 52a and an opening 52b are made in the resist mask 52.

The resist mask 52 is formed such that a portion of the insulating film 17 is exposed from the opening 52a and the opening 52b of the resist mask 52. In FIG. 4B, the resist mask 52 is formed such that the inner wall of the first opening 17a, the inner wall of the second opening 17b, and the flat portion (the top surface) of the insulating film 17 are exposed.

[0075] Then, the p-side metal protective film 15 and the n-side metal protective film 16 are formed using the resist mask 52 as a mask. The p-side metal protective film 15 and the n-side metal protective film 16 are formed simultaneously using, for example, vapor deposition.

[0076] One opening 52a made in the resist mask 52 is made over the first opening 17a made in the insulating film 17; and the width of the opening 52a is wider than the width of the first opening 17a. The top surface of the p-side contact electrode 13 is exposed at the bottom portion of the opening 52a. The p-side metal protective film 15 is formed on the bottom portion of the opening 52a. Accordingly, the p-side metal protective film 15 covers the top surface of the p-side contact electrode 13.

[0077] As described above, a gap is made between the inner wall of the first opening 17a and the side surface of the p-side contact electrode 13. The gap also is exposed at the bottom portion of the opening 52a. Accordingly, the p-side metal protective film 15

fills the gap and covers the side surface of the p-side contact electrode 13.

[0078] The p-side metal protective film 15 covers the step-like portion that extends from the inner wall of the first opening 17a over the top surface of the insulating film 17; and the planar size of the p-side metal protective film 15 is larger than the planar size of the p-side contact electrode 13. The inner wall of the first opening 17a is separate from the side surface of the p-side contact electrode 13. Therefore, the entire side surface of the p-side contact electrode 13 in the thickness direction is exposed in the state prior to the forming of the p-side metal protective film 15. Accordingly, the p-side metal protective film 15 can reliably cover all of the exposed surfaces of the p-side contact electrode 13. At this time, the p-side metal protective film 15 has a concave configuration.

[0079] One other opening 52b made in the resist mask 52 is made on the second opening 17b made in the insulating film 17; and the width of the opening 52b is wider than the width of the second opening 17b. The top surface of the n-side contact electrode 14 is exposed at the bottom portion of the opening 52b. The n-side metal protective film 16 is formed on the bottom portion of the opening 52b. Accordingly, the n-side metal protective film 16 covers the top surface of the n-side contact electrode 14.

[0080] As described above, a gap is made between the inner wall of the second opening 17b and the side surface of the n-side contact electrode 14. The gap also is exposed at the bottom portion of the opening 52b. Accordingly, the n-side metal protective film 16 fills the gap and covers the side surface of the n-side contact electrode 14.

[0081] The n-side metal protective film 16 covers the step-like portion that extends from the inner wall of the second opening 17b over the top surface of the insulating film 17; and the planar size of the n-side metal protective film 16 is larger than the planar size of the n-side contact electrode 14. The inner wall of the second opening 17b is separate from the side surface of the n-side contact electrode 14. Therefore, the entire side surface of the n-side contact electrode 14 in the thickness direction is exposed in the state prior to the forming of the n-side metal protective film 16. Accordingly, the n-side metal protective film 16 can reliably cover all of the exposed surfaces of the n-side contact electrode 14. At this time, the n-side metal protective film 16 has a concave configuration.

[0082] Then, the resist mask 52 used for the formation of the p-side metal protective film 15 and the n-side metal protective film 16 is removed (FIG. 5A).

[0083] Continuing as illustrated in FIG. 5B, a trench 62 piercing the first semiconductor layer 1 is made to reach the substrate 8 by, for example, Reactive Ion Etching (RIE) using a resist mask 53. An opening 53a is made in the resist mask 53; and the trench 62 is made under the opening 53a.

[0084] The trench 62 is made in the dicing region formed in, for example, a lattice configuration on the substrate 8 in the wafer state. The trench 62 also is made in, for

example, a lattice configuration and separates the semiconductor layer 4 into multiple chips on the substrate 8.

- [0085] The resist used when forming the p-side contact electrode 13, the n-side contact electrode 14, the p-side metal protective film 15, and the n-side metal protective film 16 can be easily coated onto the second surface side which has no large unevenness in the case where the trench 62 is made after forming the p-side contact electrode 13, the n-side contact electrode 14, the p-side metal protective film 15, and the n-side metal protective film 16.
- [0086] Prior to the forming of the resist mask 53, the insulating film 17 of the dicing region is removed as illustrated in FIG. 5A. During the etching that makes the trench 62, the resist mask 53 is consumed also in the surface direction. In other words, the width of the opening 53a widens from the position illustrated by the solid line to the position illustrated by the double dot-dash line. The insulating film 17 of the dicing region is removed beforehand such that the insulating film 17 is not exposed by the widening of the opening 53a at this time.
- [0087] In the case where the insulating film 17 of the dicing region is undesirably exposed by the consumption of the resist mask 53, the insulating film 17 substantially becomes the etching mask thereafter; and as illustrated by the broken line in FIG. 5B, a step easily forms undesirably in the side wall of the trench 62 (the side surface of the first semiconductor layer 1). This step may cause cracks to occur in the semiconductor layer 4 when removing the substrate 8 described below by laser lift-off or chemical wet etching off.
- [0088] The problem recited above can be avoided by removing the insulating film 17 beforehand such that the insulating film 17 is not exposed inside the opening 53a of the resist mask 53 that was widened during the etching.
- [0089] The trench 62 may be made prior to the forming of the p-side contact electrode 13, the n-side contact electrode 14, the p-side metal protective film 15, and the n-side metal protective film 16.
- [0090] Then, the resist mask 53 is removed (FIG. 6A).
- [0091] Continuing as illustrated in FIG. 6B, all of the exposed portions on the second surface side are covered with the insulating layer 18; and the first via 18a and the second via 18b are made in the insulating layer 18. The first via 18a reaches the p-side metal protective film 15. The second via 18b reaches the n-side metal protective film 16. The insulating layer 18 is filled into the trench 62.
- [0092] An organic material such as, for example, photosensitive polyimide, benzocyclobutene, etc., can be used as the insulating layer 18. In such a case, it is possible to directly perform the exposure and the development of the insulating layer 18 without using a resist. Alternatively, an inorganic film such as a silicon nitride film, a silicon

oxide film, etc., may be used as the insulating layer 18. In the case of an inorganic film, the first via 18a and the second via 18b are obtained by etching after the resist is patterned.

[0093] The outermost surfaces of the p-side metal protective film 15 and the n-side metal protective film 16 are films such as, for example, titanium (Ti), nickel (Ni), molybdenum (Mo), etc., which have good adhesion with polyimide.

[0094] Then, the metal film 19 is formed on the top surface of the insulating layer 18 (the interconnect surface 18c) as illustrated in FIG. 7A. The metal film 19 is formed also on the inner wall and the bottom portion of the first via 18a and the inner wall and the bottom portion of the second via 18b. The metal film 19 functions as a power supply layer for the plating to be performed next.

[0095] As the metal film 19, for example, a titanium (Ti) film is formed first by sputtering; and subsequently, a copper (Cu) film is formed on the titanium film by sputtering.

[0096] Sputter etching or milling is performed on the top surface of the p-side metal protective film 15 exposed at the first via 18a and the top surface of the n-side metal protective film 16 exposed at the second via 18b prior to the formation of the metal film 19. Thereby, insulating film residue and oxides on the top surfaces of the metal protective films 15 and 16, which cause the contact resistance between the metal protective films 15 and 16, and the interconnect layers provided thereon to increase, are removed.

[0097] By forming the titanium (Ti) film, the nickel (Ni) film, or the molybdenum (Mo) film of the outermost surface of the metal protective films 15 and 16 thinly with, for example, 1 - 20 nm, the removal of the film of the outermost surface of the metal protective films 15 and 16 by the sputter etching or the milling recited above is easy.

[0098] A clean surface of the gold (Au) is exposed at the outermost surface of the p-side metal protective film 15 and the outermost surface of the n-side metal protective film 16 by the sputter etching or the milling recited above. The metal film 19 is formed by forming a titanium (Ti) film, which has excellent adhesion with gold, on the clean surface of the gold (Au) and by forming a copper (Cu) film on the titanium film. Thereby, the adhesion can be improved between the metal film 19, which is the power supply layer for the plating, and the metal protective films 15 and 16. The metal film 19 is unnecessary in the case where the interconnect layers are not formed using plating.

[0099] Then, a resist (not illustrated) is formed selectively on the metal film 19; and Cu electroplating is performed using the metal film 19 as the power supply layer.

[0100] Thereby, the p-side re-interconnect layer 21 and the n-side re-interconnect layer 22 are formed as illustrated in FIG. 7B. The p-side re-interconnect layer 21 and the n-side re-interconnect layer 22 are made of, for example, a copper material formed simul-

taneously using plating. Or, the p-side re-interconnect layer 21 and the n-side re-interconnect layer 22 may be formed by forming a metal film using sputtering and/or vapor deposition and subsequently patterning the unnecessary portions by etching or lift-off using a resist.

- [0101] The p-side re-interconnect layer 21 is formed inside the first via 18a and on the metal film 19 around the first via 18a, and is electrically connected to the p-side metal protective film 15 via the metal film 19. The n-side re-interconnect layer 22 is formed inside the second via 18b and on the metal film 19 around the second via 18b and is electrically connected to the n-side metal protective film 16 via the metal film 19.
- [0102] Then, as illustrated in FIG. 7B, a resist 54 is formed selectively; and Cu electroplating is performed using the metal film 19 as the power supply layer. Thereby, the p-side metal pillar 23 and the n-side metal pillar 24 are formed. The p-side metal pillar 23 is formed on the p-side re-interconnect layer 21; and the n-side metal pillar 24 is formed on the n-side re-interconnect layer 22.
- [0103] The p-side metal pillar 23 and the n-side metal pillar 24 are made of a copper material formed simultaneously using plating. Or, the p-side metal pillar 23 and the n-side metal pillar 24 may be formed by forming a metal film using sputtering and/or vapor deposition and subsequently patterning the unnecessary portions by etching or lift-off using a resist.
- [0104] When forming the metal film 19 described above, the coverability of differences in levels degrades easily at the portions where the difference in levels of the underlying insulating layer 18 (portions 80 and 90 enclosed with the broken line in FIG. 7A) is large; and breakage of the metal film 19 occurs easily at the portions 80 and 90.
- [0105] In the case where breakage occurs in the metal film 19, permeation of the plating liquid is allowed from the location of such breakage. In FIG. 7B, the permeation path of the plating liquid is illustrated by a thick line 100.
- [0106] In the embodiment, the top surface and the side surface of the p-side contact electrode 13 are covered with the p-side metal protective film 15; and the top surface and the side surface of the n-side contact electrode 14 are covered with the n-side metal protective film 16. The p-side metal protective film 15 and the n-side metal protective film 16 include mainly gold (Au) which has poor reactivity such as oxidation and sulfidization. Accordingly, even in the case where the permeation of the plating liquid is allowed, the permeating plating liquid is blocked by the p-side metal protective film 15 and the n-side metal protective film 16 and does not reach the p-side contact electrode 13 and the n-side contact electrode 14. As a result, corrosion of the p-side contact electrode 13 and the n-side contact electrode 14 can be prevented.
- [0107] As described above, the inner wall of the first opening 17a and the inner wall of the second opening 17b made in the insulating film 17 are tapered surfaces that are not

perpendicular to the second surface but tilted with respect to the second surface.

Therefore, the coverability of differences in levels of the inner wall of the first opening 17a by the p-side metal protective film 15 and the coverability of differences in levels of the inner wall of the second opening 17b by the n-side metal protective film 16 can be good. As a result, the p-side contact electrode 13 and the n-side contact electrode 14 can be reliably protected from the plating liquid by avoiding the breakage of the p-side metal protective film 15 and the breakage of the n-side metal protective film 16.

[0108] By the p-side metal protective film 15 being thicker than the p-side contact electrode 13, the breakage of the p-side metal protective film 15 occurs less easily. Similarly, by the n-side metal protective film 16 being thicker than the n-side contact electrode 14, the breakage of the n-side metal protective film 16 occurs less easily.

[0109] The resist 54 used as the plating mask of the p-side metal pillar 23 and the n-side metal pillar 24 is removed using, for example, a chemical liquid. Then, as illustrated in FIG. 8A, the exposed portions of the metal film 19 are removed by wet etching using the p-side re-interconnect layer 21, the n-side re-interconnect layer 22, the p-side metal pillar 23, and the n-side metal pillar 24 as a mask. Thereby, the electrical connection between the p-side re-interconnect layer 21 and the n-side re-interconnect layer 22 via the metal film 19 is divided.

[0110] At this time, even in the case where permeation of the chemical liquid used for the removal of the resist 54 and the wet etching of the metal film 19 is allowed, the permeating chemical liquid is blocked by the p-side metal protective film 15 and the n-side metal protective film 16 and does not reach the p-side contact electrode 13 and the n-side contact electrode 14. As a result, the corrosion of the p-side contact electrode 13 and the n-side contact electrode 14 can be prevented.

[0111] Then, as illustrated in FIG. 8B, the resin layer 25 is formed as a second insulating layer on the insulating layer 18. The resin layer 25 covers the side surface of the p-side re-interconnect layer 21 and the side surface of the n-side re-interconnect layer 22 and fills between the p-side re-interconnect layer 21 and the n-side re-interconnect layer 22. Also, the resin layer 25 covers the side surface of the p-side metal pillar 23 and the side surface of the n-side metal pillar 24 and fills between the p-side metal pillar 23 and the n-side metal pillar 24.

[0112] The p-side metal pillar 23 and the n-side metal pillar 24, which function as the external terminals, are separated by a distance such that the p-side metal pillar 23 and the n-side metal pillar 24 are not shorted to each other by the solder, etc., when mounting to the mounting substrate.

[0113] Then, the substrate 8 is removed (FIG. 9A). The substrate 8 may be removed using, for example, laser lift-off, chemical wet etching. Specifically, laser light is irradiated from the back surface side of the substrate 8 toward the first semiconductor layer 1.

The laser light has a wavelength that is transmissive with respect to the substrate 8 and in the absorption region of the first semiconductor layer 1.

- [0114] When the laser light reaches the interface between the substrate 8 and the first semiconductor layer 1, the first semiconductor layer 1 proximal to the interface decomposes by absorbing the energy of the laser light. For example, in the case where the first semiconductor layer 1 is GaN, the first semiconductor layer 1 decomposes into gallium (Ga) and nitrogen gas. By this decomposition reaction, a micro gap is made between the substrate 8 and the first semiconductor layer 1; and the substrate 8 and the first semiconductor layer 1 separate.
- [0115] The irradiation of the laser light is performed over the entire wafer by performing multiply for every set region; and the substrate 8 is removed.
- [0116] Because the stacked body described above formed on the major surface of the substrate 8 is reinforced by the p-side metal pillar 23, the n-side metal pillar 24, and the resin layer 25 which are thicker than the semiconductor layer 4, it is possible to maintain the wafer state even in the case where there is no substrate 8.
- [0117] The first surface 4a of the semiconductor layer 4 from which the substrate 8 is removed is cleaned. The gallium (Ga) adhered to the first surface 4a is removed using, for example, hydrochloric acid, etc.
- [0118] If necessary, the first surface 4a is etched using, for example, a KOH (potassium hydroxide) aqueous solution, TMAH (tetramethylammonium hydroxide), etc. Thereby, an unevenness (frost) is formed in the first surface 4a due to the difference of the etching rates that depend on the crystal plane orientation. Alternatively, the unevenness may be formed in the first surface 4a by performing the etching after the patterning using the resist. The light extraction efficiency can be increased by the unevenness being formed in the first surface 4a.
- [0119] Then, as illustrated in FIG. 9B, the phosphor layer 27 and the lens 26 are formed on the first surface 4a and on the insulating layer 18 of the dicing region.
- [0120] The process of forming the phosphor layer 27 includes, for example, a process of supplying a liquid transparent resin having dispersed phosphor particles using a method such as printing, potting, molding, compression molding, etc., and a subsequent process of thermal curing. The transparent resin is transmissive to the light emitted from the light emitting layer 3 and the light emitted by the phosphor; and, for example, a material such as a silicone resin, an acrylic resin, liquid glass, etc., may be used.
- [0121] The lens 26 is transparent to the light emitted from the light emitting layer 3; and, for example, a silicone resin, an acrylic resin, glass, etc., may be used.
- [0122] Then, the resin layer 25, the insulating layer 18, the phosphor layer 27, and the lens 26 are cut at the position of the trench 62 to singulate into the multiple semiconductor

light emitting device 10. For example, the cutting is performed using a dicing blade. Alternatively, the cutting may be performed using laser irradiation.

- [0123] When dicing, the substrate 8 is already removed. Further, damage to the semiconductor layer 4 during the dicing can be avoided because the semiconductor layer 4 does not exist in the trench 62 which is the dicing region.
- [0124] The singulated semiconductor light emitting device 10 may have a single-chip structure including one semiconductor layer 4 or a multi-chip structure including multiple semiconductor layers 4.
- [0125] It is unnecessary to perform the interconnect and the packaging for every singulated individual device and it becomes possible to drastically reduce the production costs because each of the processes described above up to prior to the dicing is performed collectively in the wafer state. The interconnect and the packaging are already completed in the singulated state. Therefore, the productivity can be increased; and as a result, price reductions become easy.
- [0126] According to the embodiment, the p-side metal protective film 15 and the n-side metal protective film 16 protect the p-side contact electrode 13 and the n-side contact electrode 14 from the chemical liquids, etc., used in the processes performed after the formation of these contact electrodes. The p-side metal protective film 15 and the n-side metal protective film 16 also protect the p-side contact electrode 13 and the n-side contact electrode 14 from the sulfur, etc., in the air that permeates into the insulating layer 18. As a result, the corrosion and the increased resistance of the p-side contact electrode 13 and the n-side contact electrode 14 can be prevented.
- [0127] As illustrated in FIG. 10, it is unnecessary for the inner wall of the bottom portion of the first opening 17a on the second semiconductor layer 2 side to be separate from the side surface of the p-side contact electrode 13. Similarly, it is unnecessary for the inner wall of the bottom portion of the second opening 17b on the first semiconductor layer 1 side to be separate from the side surface of the n-side contact electrode 14.
- [0128] In such a case as well, a gap can be made between the inner wall of the first opening 17a and the side surface of the p-side contact electrode 13 by forming the inner wall of the first opening 17a as a tapered surface. The side surface of the p-side contact electrode 13 can be covered with the p-side metal protective film 15 by filling the p-side metal protective film 15 into the gap.
- [0129] Similarly, a gap can be made between the inner wall of the second opening 17b and the side surface of the n-side contact electrode 14 by forming the inner wall of the second opening 17b as a tapered surface. The side surface of the n-side contact electrode 14 can be covered with the n-side metal protective film 16 by filling the n-side metal protective film 16 into the gap.
- [0130] As illustrated in FIG. 1, the entire side surface of the p-side contact electrode 13 can

be reliably covered with the p-side metal protective film 15 by the inner wall of the bottom portion of the first opening 17a on the second semiconductor layer 2 side being separate from the side surface of the p-side contact electrode 13.

[0131] Similarly, the entire side surface of the n-side contact electrode 14 can be reliably covered with the n-side metal protective film 16 by the inner wall of the bottom portion of the second opening 17b on the first semiconductor layer 1 side being separate from the side surface of the n-side contact electrode 14.

[0132] Also, as illustrated in FIG. 11, the substrate 8 may thinly remain on the first surface 4a. The substrate 8 can be polished using, for example, a grinder for polishing a semiconductor wafer back face, etc.

[0133] The substrate 8 is, for example, a sapphire substrate and is transmissive to the light emitted from the nitride semiconductor-type light emitting layer. In such a case, because there is no phosphor layer, light having the same wavelength as the light emitted from the light emitting layer is emitted to the outside from the semiconductor light emitting device. The mechanical strength can be increased and a structure having high reliability is possible by leaving the substrate 8.

[0134] Further, as illustrated in FIG. 12, the phosphor layer 27 may be formed on the substrate 8. By leaving the substrate 8, it is possible to stably maintain the semiconductor layer 4 without providing the p-side interconnect layer, the n-side interconnect layer, and the resin layer. In such a case, the p-side metal protective film 15 functions as the p-side external terminal; and the n-side metal protective film 16 functions as the n-side external terminal. In other words, the p-side metal protective film 15 and the n-side metal protective film 16 are bonded to pads of the mounting substrate with solder, etc.

It is not always necessary for any of the substrate 8, the lens 26, and the phosphor layer 27 to be on the first surface 4a.

[0135] The red phosphor layer, the yellow phosphor layer, the green phosphor layer, and the blue phosphor layer described below can be used as the phosphor layer described above.

[0136] The red phosphor layer can contain, for example, a nitride-based phosphor of $\text{CaAlSiN}_3\text{:Eu}$ or a SiAlON-based phosphor.

[0137] In the case where a SiAlON-based phosphor is used,



can be used (where M is at least one type of metal element excluding Si and Al, and it may be desirable for M to be at least one selected from Ca and Sr; R is a light emission center element, and it may be desirable for R to be Eu; and x, a1, b1, c1, and d1 satisfy the following relationships: x is larger than 0 and 1 or less, a1 is larger than 0.6 and less than 0.95, b1 is larger than 2 and less than 3.9, c1 is larger than 0.25 and

less than 0.45, and d1 is larger than 4 and less than 5.7).

[0138] By using the SiAlON-based phosphor of Compositional Formula (1), the temperature characteristics of the wavelength conversion efficiency can be improved; and the efficiency in the high current density region can be increased further.

[0139] The yellow phosphor layer can contain, for example, a silicate-based phosphor of $(\text{Sr}, \text{Ca}, \text{Ba})_2\text{SiO}_4:\text{Eu}$.

[0140] The green phosphor layer can contain, for example, a halophosphate-based phosphor of $(\text{Ba}, \text{Ca}, \text{Mg})_{10}(\text{PO}_4)_6\text{Cl}_2:\text{Eu}$ or a SiAlON-based phosphor.

[0141] In the case where a SiAlON-based phosphor is used,
 $(\text{M}_{1-x}, \text{R}_x)_{a2}\text{AlSi}_{b2}\text{O}_{c2}\text{N}_{d2}$ Compositional Formula (2)
 can be used (where M is at least one type of metal element excluding Si and Al, and it may be desirable for M to be at least one selected from Ca and Sr; R is a light emission center element, and it may be desirable for R to be Eu; and x, a2, b2, c2, and d2 satisfy the following relationships: x is larger than 0 and 1 or less, a2 is larger than 0.93 and less than 1.3, b2 is larger than 4.0 and less than 5.8, c2 is larger than 0.6 and less than 1, and d2 is larger than 6 and less than 11).

[0142] By using the SiAlON-based phosphor of Compositional Formula (2), the temperature characteristics of the wavelength conversion efficiency can be improved; and the efficiency in the high current density region can be increased further.

[0143] The blue phosphor layer can contain, for example, an oxide-based phosphor of $\text{BaMgAl}_{10}\text{O}_{17}:\text{Eu}$.

[0144] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the invention.

Claims

- [Claim 1] A semiconductor light emitting device, comprising:
a semiconductor layer including a light emitting layer, a first surface, and a second surface, the second surface being formed on a side opposite to the first surface, the second surface having a light emitting portion including the light emitting layer and a non-light emitting portion not including the light emitting layer;
an insulating film provided on the second surface, the insulating film having a first opening connecting with the light emitting portion and a second opening connecting with the non-light emitting portion;
a p-side contact electrode provided in contact with the light emitting portion inside the first opening;
an n-side contact electrode provided in contact with the non-light emitting portion inside the second opening;
a p-side metal protective film covering a top surface and a side surface of the p-side contact electrode; and
an n-side metal protective film covering a top surface and a side surface of the n-side contact electrode.
- [Claim 2] The device of claim 1, wherein the p-side metal protective film is thicker than the p-side contact electrode.
- [Claim 3] The device of claim 1, wherein the n-side metal protective film is thicker than the n-side contact electrode.
- [Claim 4] The device of claim 1, wherein the p-side metal protective film oxidizes or sulfidizes less easily than the p-side contact electrode.
- [Claim 5] The device of claim 1, wherein the n-side metal protective film oxidizes or sulfidizes less easily than the n-side contact electrode.
- [Claim 6] The device of claim 1, wherein
the p-side metal protective film covers an exposed surface including the top surface and the side surface of the p-side contact electrode, and
the n-side metal protective film covers an exposed surface including the top surface and the side surface of the n-side contact electrode.
- [Claim 7] The device of claim 1, wherein
the p-side metal protective film has a planar size larger than a planar size of the first opening, and
the n-side metal protective film has a planar size larger than a planar size of the second opening.
- [Claim 8] The device of claim 1, wherein an inner wall of the first opening is

tilted with respect to a top surface of the light emitting portion to cause an opening surface area of the first opening to increase from the top surface side of the light emitting portion toward a top surface side of the insulating film.

[Claim 9] The device of claim 1, wherein an inner wall of the second opening is tilted with respect to a top surface of the non-light emitting portion to cause an opening area of the second opening to increase from the top surface side of the non-light emitting portion toward a top surface side of the insulating film.

[Claim 10] The device of claim 1, wherein
a gap is made between an inner wall of the first opening and the side surface of the p-side contact electrode, and
the p-side metal protective film is provided also on a bottom face of the first opening in the gap.

[Claim 11] The device of claim 1, wherein
a gap is made between an inner wall of the second opening and the side surface of the n-side contact electrode, and
the n-side metal protective film is provided also on a bottom face of the second opening in the gap.

[Claim 12] The device of claim 1, further comprising:
a first insulating layer provided on the insulating film, the p-side metal protective film, and the n-side metal protective film, the first insulating layer having a first via communicating with the p-side metal protective film and a second via communicating with the n-side metal protective film;
a p-side interconnect layer provided inside the first via and on a surface of the first insulating layer on a side opposite to the p-side metal protective film, the p-side interconnect layer being electrically connected to the p-side metal protective film;
an n-side interconnect layer provided inside the second via and on a surface of the first insulating layer on a side opposite to the n-side metal protective film, the n-side interconnect layer being electrically connected to the n-side metal protective film; and
a second insulating layer provided at least between the p-side interconnect layer and the n-side interconnect layer.

[Claim 13] The device of claim 12, wherein
the p-side interconnect layer includes a p-side re-interconnect layer provided on the first insulating layer side and a p-side metal pillar

provided on a top surface of the p-side re-interconnect layer, the p-side metal pillar being thicker than the p-side re-interconnect layer, and the n-side interconnect layer includes an n-side re-interconnect layer provided on the first insulating layer side and an n-side metal pillar provided on a top surface of the n-side re-interconnect layer, the n-side metal pillar being thicker than the n-side re-interconnect layer.

[Claim 14] The device of claim 12, wherein a area of a surface of the n-side interconnect layer on a side opposite to the n-side metal protective film is greater than a area of the n-side contact electrode.

[Claim 15] The device of claim 12, wherein the p-side interconnect layer is thicker than the p-side contact electrode.

[Claim 16] The device of claim 12, wherein the n-side interconnect layer is thicker than the n-side contact electrode.

[Claim 17] The device of claim 1, further comprising a transparent body provided on the first surface, the transparent body being transparent to light emitted from the light emitting layer.

[Claim 18] A semiconductor light emitting device, comprising:
a semiconductor layer including a light emitting layer, a first surface, and a second surface, the second surface being formed on a side opposite to the first surface, the second surface having a light emitting portion including the light emitting layer and a non-light emitting portion not including the light emitting layer;
an insulating film provided on the second surface, the insulating film having a first opening connecting with the light emitting portion and a second opening connecting with the non-light emitting portion;
a p-side contact electrode provided in contact with the light emitting portion inside the first opening;
an n-side contact electrode provided in contact with the non-light emitting portion inside the second opening;
a p-side metal protective film covering a top surface and a side surface of the p-side contact electrode, a portion of the p-side metal protective film being provided on the insulating film, a top surface of the p-side metal protective film having a concave configuration, the p-side metal protective film being configured to oxidize or sulfidize less easily than the p-side contact electrode; and
an n-side metal protective film covering a top surface and a side surface of the n-side contact electrode, a portion of the n-side metal protective film being provided on the insulating film, a top surface of the n-side

metal protective film having a concave configuration, the n-side metal protective film being configured to oxidize or sulfidize less easily than the n-side contact electrode,
an inner wall of the first opening of the insulating film and an inner wall of the second opening of the insulating film having tapered configurations narrower toward the semiconductor layer.

[Claim 19]

A method for manufacturing a semiconductor light emitting device, comprising:

forming an insulating film on a second surface of a semiconductor layer, the insulating film having a first opening and a second opening, the semiconductor layer including a light emitting layer, a first surface, and the second surface, the second surface being formed on a side opposite to the first surface, the second surface having a light emitting portion including the light emitting layer and a non-light emitting portion not including the light emitting layer, the first opening connecting with the light emitting portion, the second opening connecting with the non-light emitting portion;

forming a p-side contact electrode on a top surface of the light emitting portion inside the first opening;

forming an n-side contact electrode on a top surface of the non-light emitting portion inside the second opening;

forming a p-side metal protective film on a top surface and a side surface of the p-side contact electrode; and

forming an n-side metal protective film on a top surface and a side surface of the n-side contact electrode.

[Claim 20]

The method of claim 19, wherein the first opening and the second opening are made by selective etching of the insulating film using a resist mask, and the p-side contact electrode and the n-side contact electrode are formed subsequently using the same resist mask.

[Claim 21]

The method of claim 19, further comprising:

forming a first insulating layer on the insulating film, the p-side metal protective film, and the n-side metal protective film, the first insulating layer having a first via communicating with the p-side metal protective film and a second via communicating with the n-side metal protective film;

forming a p-side interconnect layer inside the first via and on a surface of the first insulating layer on a side opposite to the p-side metal protective film; and

forming an n-side interconnect layer inside the second via and on a surface of the first insulating layer on a side opposite to the n-side metal protective film.

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FIG. 1

[Fig. 2]

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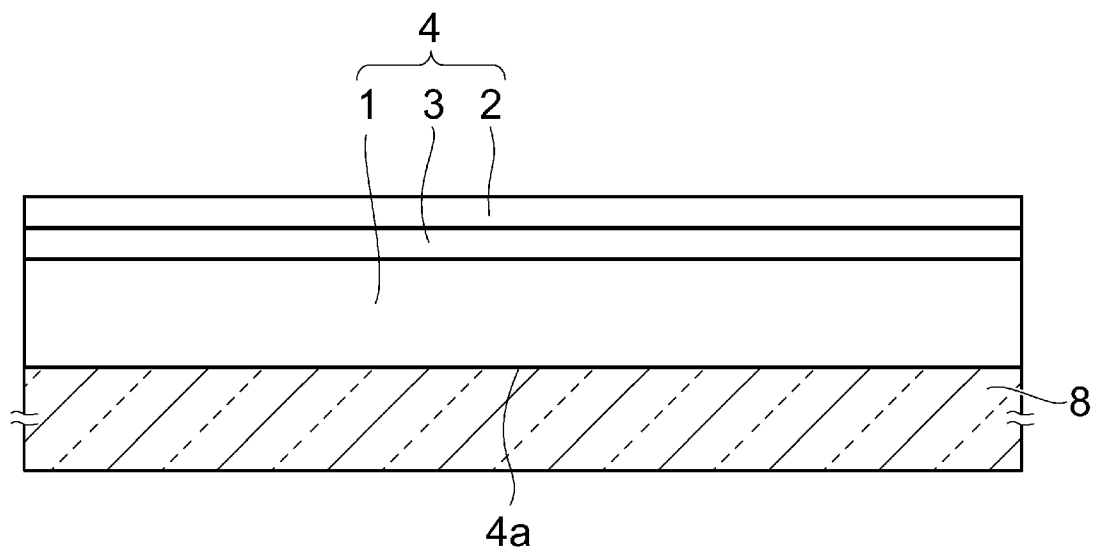


FIG. 2A

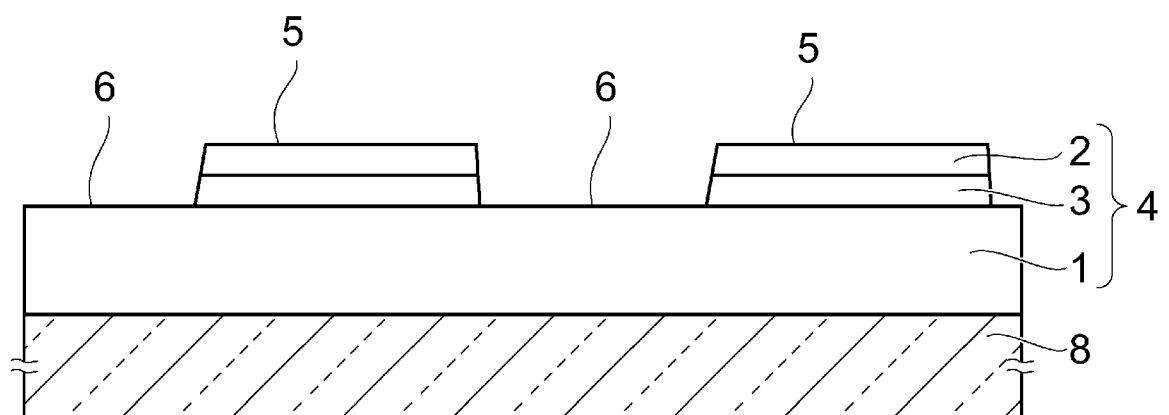


FIG. 2B

[Fig. 3]

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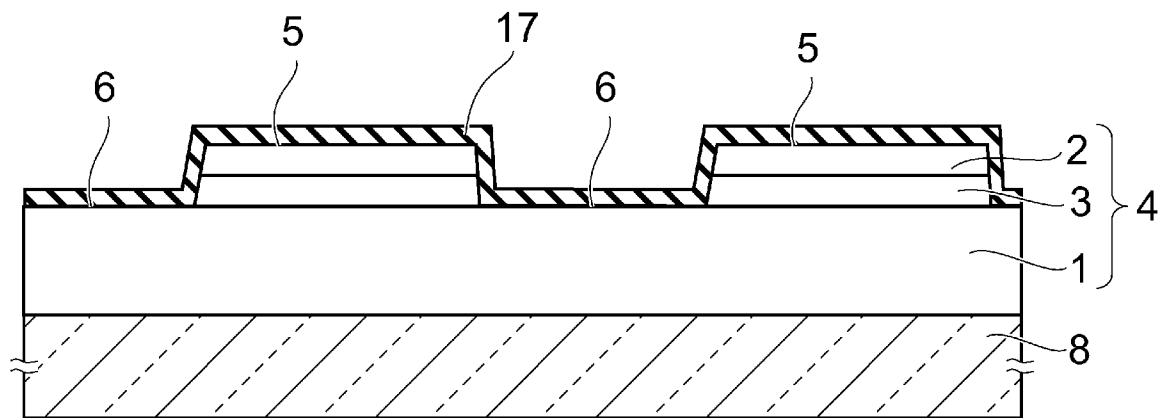


FIG. 3A

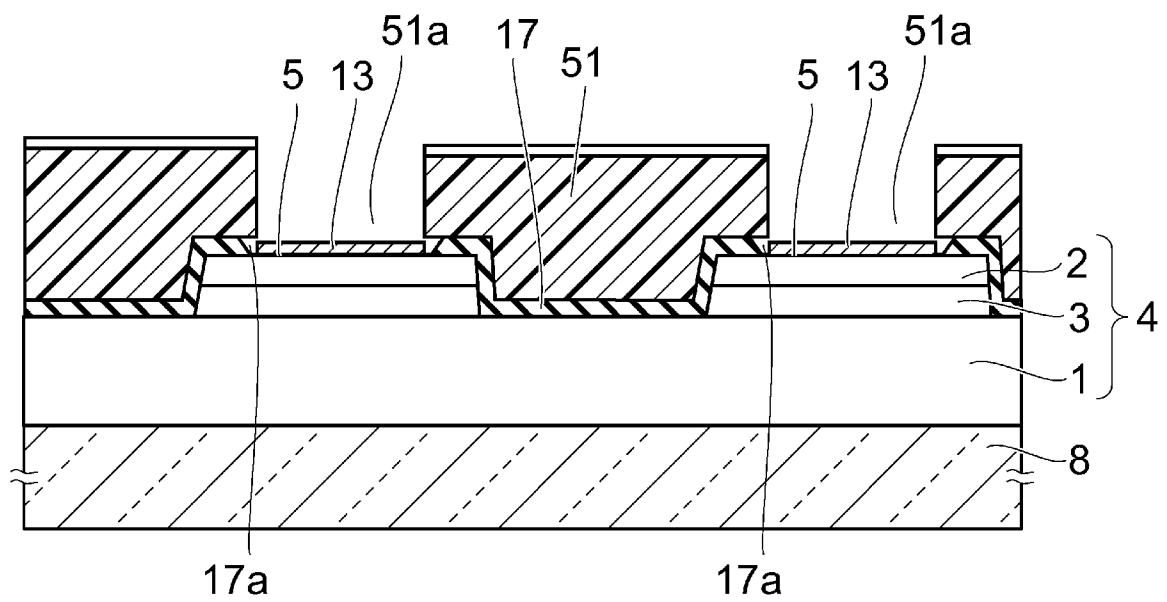


FIG. 3B

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[Fig. 5]

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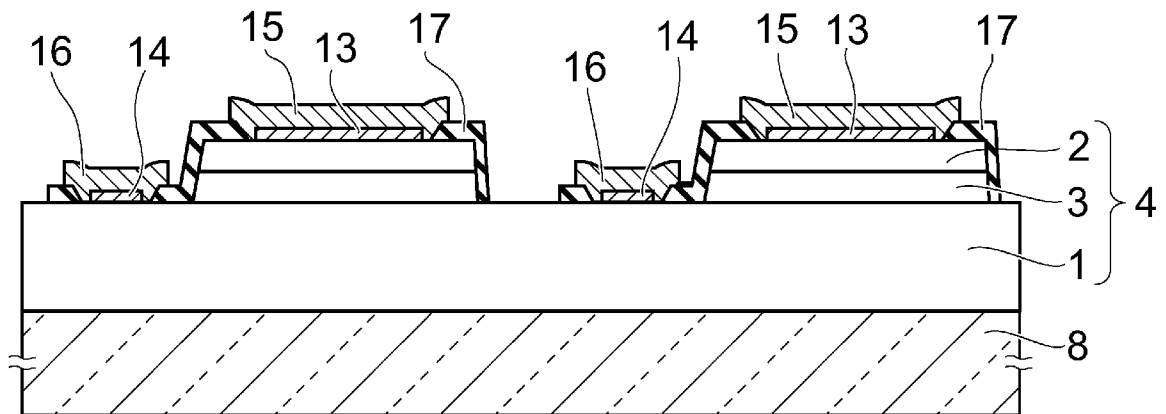


FIG. 5A

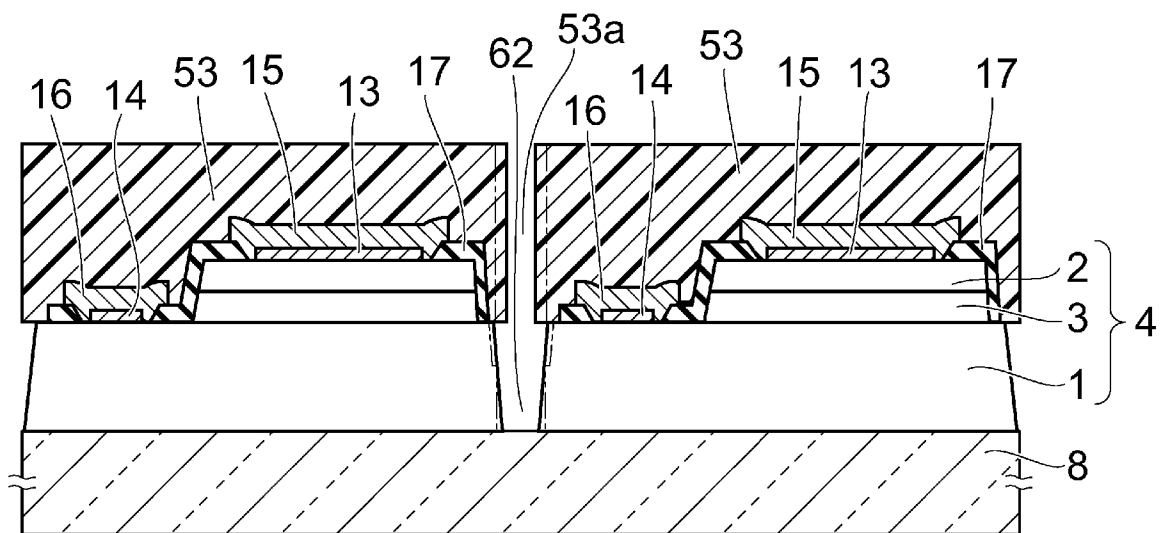


FIG. 5B

[Fig. 6]

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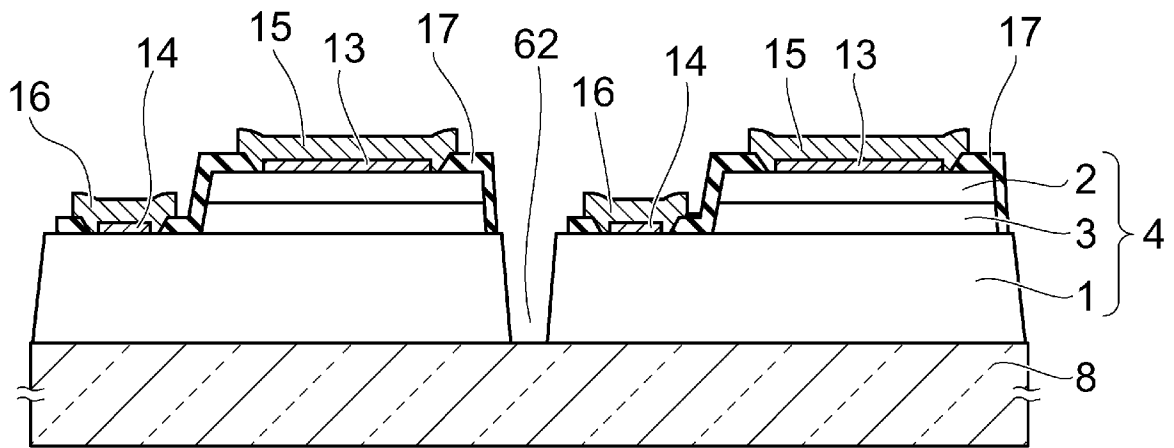


FIG. 6A

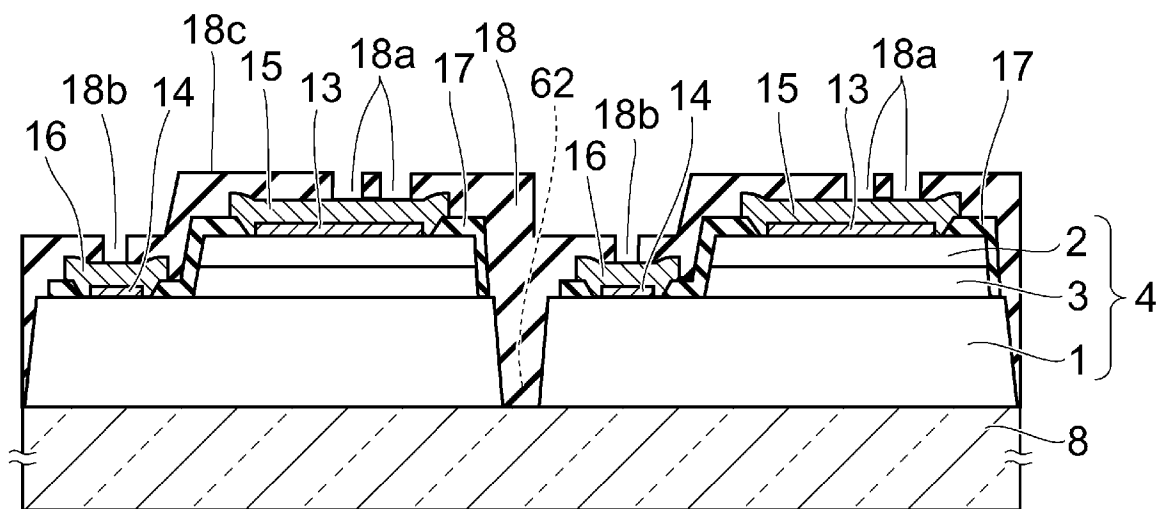


FIG. 6B

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[Fig. 10]

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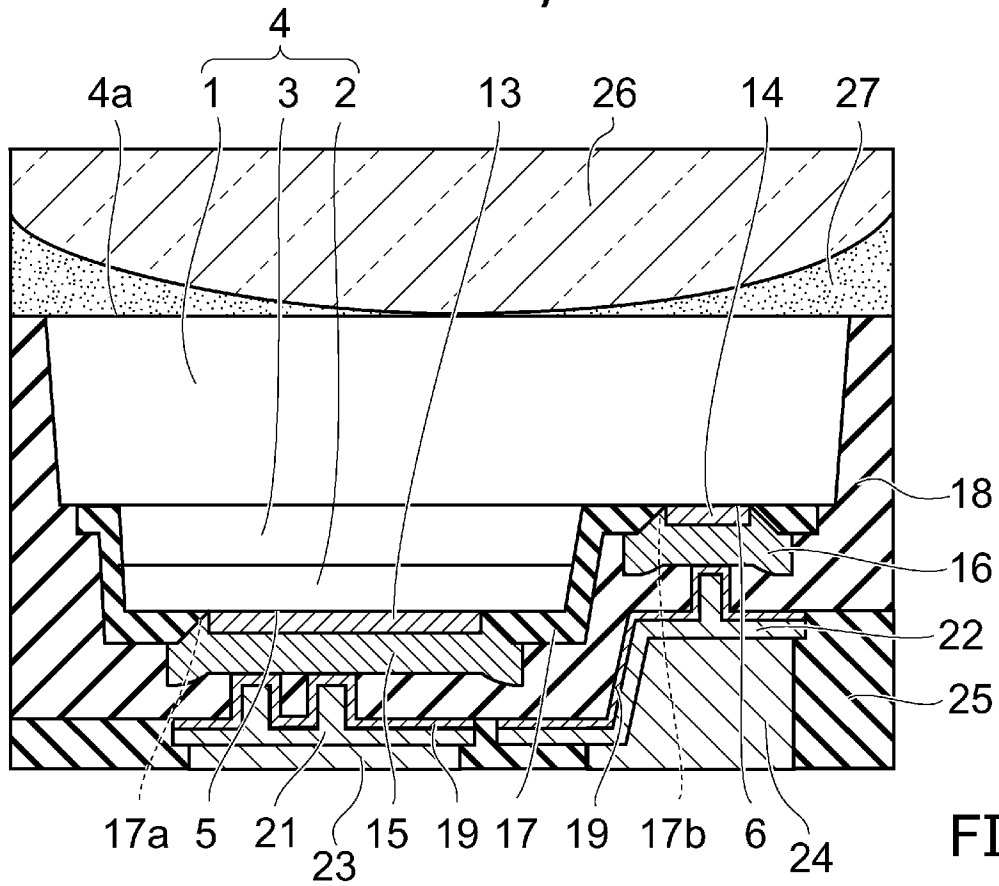


FIG. 10

[Fig. 11]

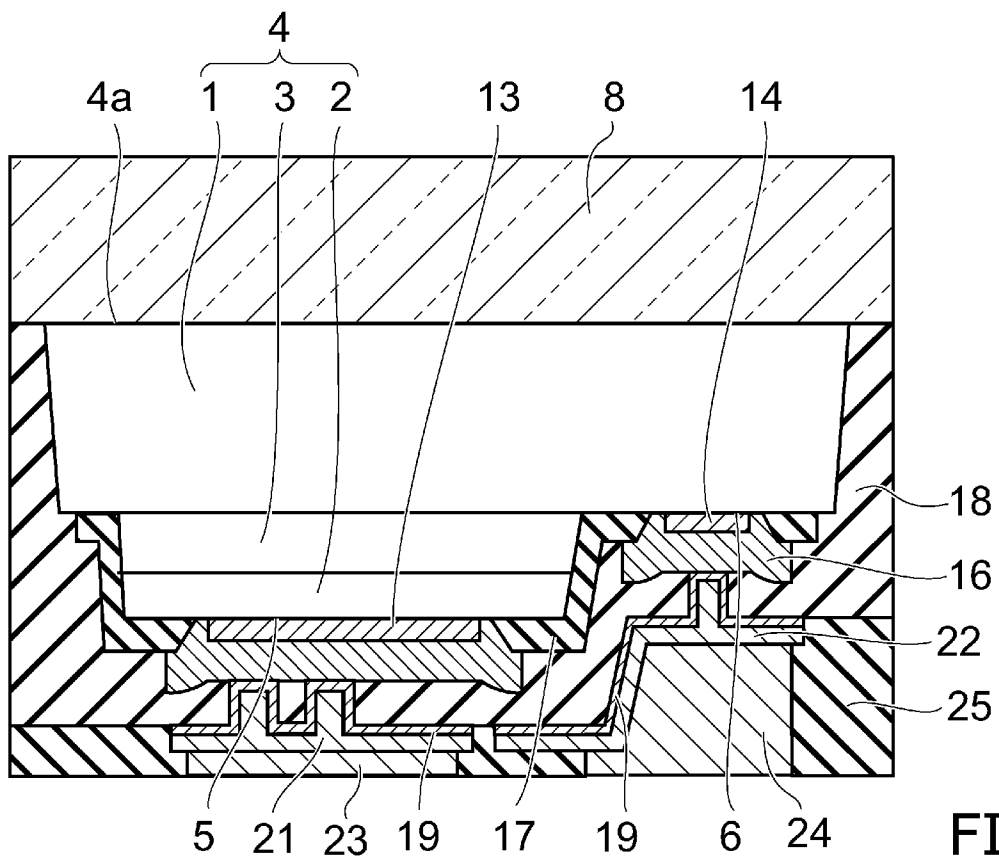


FIG. 11

[Fig. 12]

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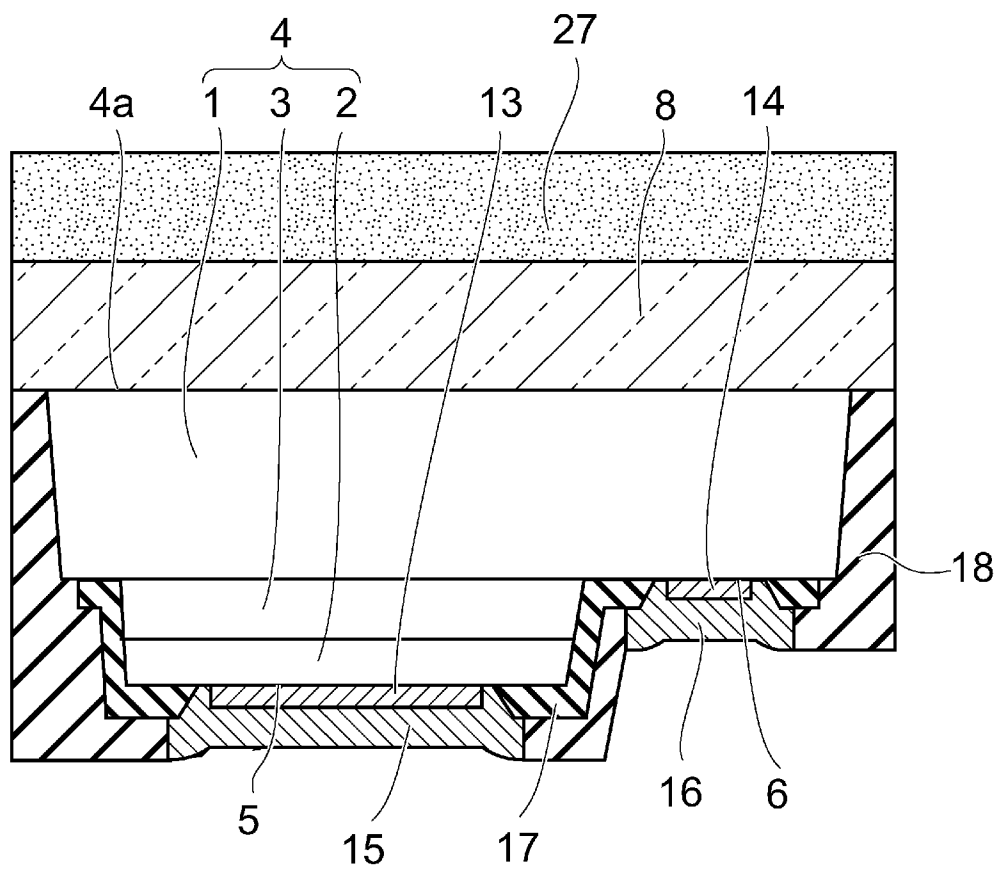


FIG. 12

[Fig. 13]

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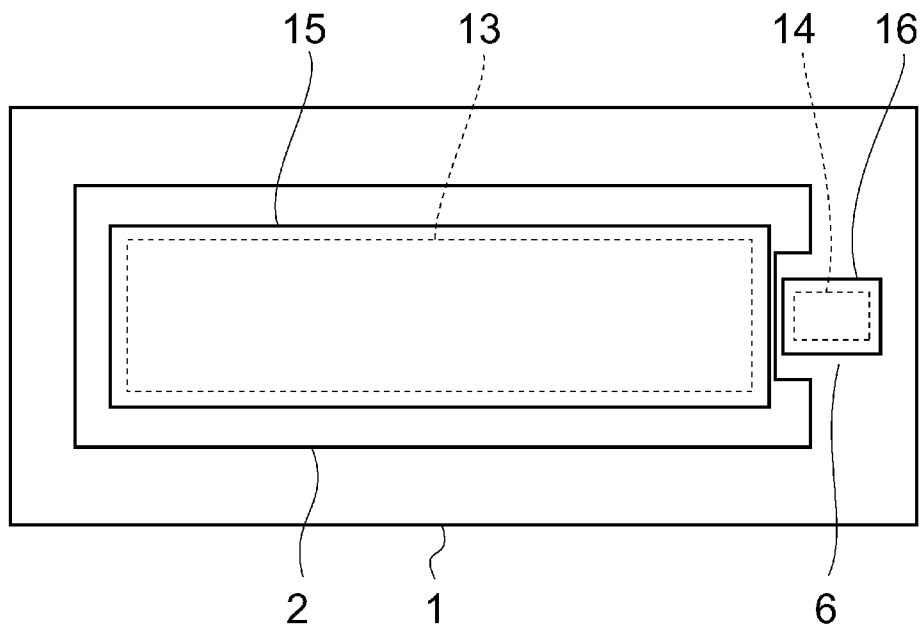


FIG. 13A

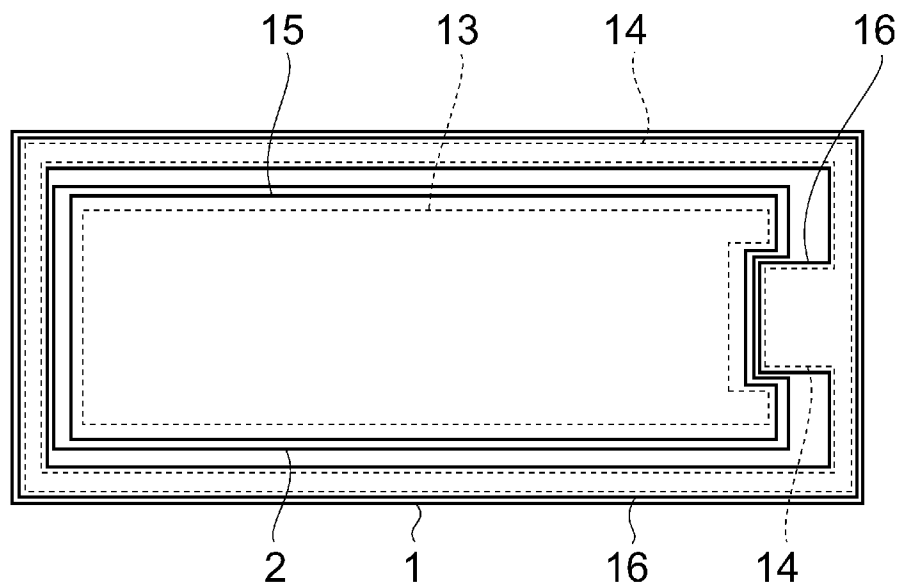


FIG. 13B

Box No. IV Text of the abstract (Continuation of item 5 of the first sheet)

According to one embodiment, a semiconductor light emitting device includes a semiconductor layer (4), an insulating film (17), a p-side contact electrode (13), an n-side contact electrode (14), a p-side metal protective film (17), and an n-side metal protective film. The semiconductor layer includes a light emitting layer (13). A second surface of the semiconductor layer is formed on a side opposite to the first surface. The second surface has a light emitting portion including the light emitting layer and a non-light emitting portion not including the light emitting layer. The p-side contact electrode is provided in contact with the light emitting portion inside a first opening of the insulating film. The n-side contact electrode is provided in contact with the non-light emitting portion inside a second opening of the insulating film. The p-side metal protective film covers a top surface and a side surface of the p-side contact electrode. The n-side metal protective film covers a top surface and a side surface of the n-side contact electrode.

INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2011/004536

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L33/40

ADD. H01L33/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/207480 A1 (KOBAYASHI TOSHIMASA [JP] ET AL) 6 November 2003 (2003-11-06)	1-11, 17-20
Y	abstract; figures 8,19-21 paragraphs [0052] - [0054] paragraph [0087]	12-16,21
Y	----- US 2003/230754 A1 (STEIGERWALD DANIEL A [US] ET AL) 18 December 2003 (2003-12-18) abstract; figures 6,7	12-16,21
A	----- US 2011/018013 A1 (MARGALITH TAL [US] ET AL) 27 January 2011 (2011-01-27) abstract; figure 6 paragraph [0059]	12,14,21
A	----- US 2003/222270 A1 (UEMURA TOSHIYA [JP]) 4 December 2003 (2003-12-04) ----- -/-	1-21



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

22 November 2011

Date of mailing of the international search report

01/12/2011

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Fax: (+31-70) 340-3016

Authorized officer

Heising, Stephan

INTERNATIONAL SEARCH REPORT

International application No

PCT/JP2011/004536

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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International application No

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