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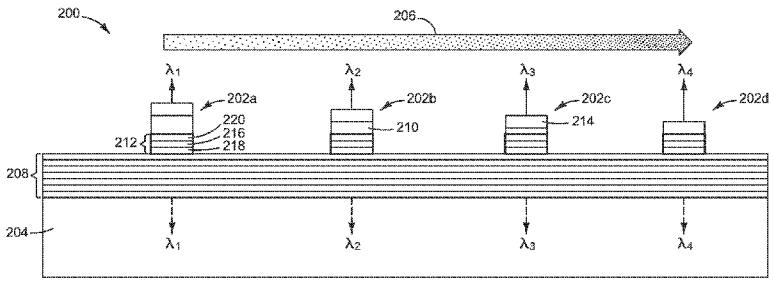


FIG. 2

(57) Abstract: An array of monolithic wavelength division multiplexing (WDM) vertical cavity surface emitting lasers (VCSELs) with spatially varying gain peak and Fabry Perot wavelength is provided. Each VCSEL includes a lower distributed Bragg reflector (DBR), a Fabry Perot tuning/current spreading layer, and a structure comprising a multiple quantum well (MQW) layer sandwiched between a lower separate confinement heterostructure (SCH) layer and an upper SCH layer. The structure is sandwiched between the DBR and the Fabry Perot tuning/ current spreading layer. Each MQW experiences a different amount of quantum well intermixing and concomitantly a different wavelength shift. Each VCSEL further includes a top mirror on the Fabry Perot tuning/current spreading layer. A method is also provided for manufacturing the array.

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MONOLITHIC WDM VCSELS WITH SPATIALLY VARYING GAIN PEAK AND FABRY PEROT WAVELENGTH

BACKGROUND

[0001] A datacenter is a facility used to house computer systems and associated components, such as telecommunications and storage systems. To handle increasing volumes of data, optical fiber is replacing copper wire. Due to the digital processing needed to make a copper solution work, a copper transceiver may consume up to 5-6 W of power. This is almost ten times as much as a fiber optic transceiver that consumes only 0.5 to 1 W.

[0002] VCSELs (Vertical Cavity Surface Emitting Lasers) are a type of semiconductor laser diode with laser beam emission perpendicular from the wafer surface, contrary to conventional edge-emitting semiconductor lasers (also in-plane lasers) which emit from surfaces formed by cleaving the individual chip out of a wafer. VCSELs may be used as a light source for optical fiber data transmission.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIGS. 1A-1B depict a schematic view of quantum well intermixing (QWI) band diagrams for both an as-grown VCSEL band (FIG. 1A) and a post-QWI VCSEL band (FIG. 1B), according to an example.

[0004] FIG. 2 is a side elevation view, depicting monolithic WDM (Wavelength Division Multiplexing) VCSELs with a spatially varying gain peak, according to an example.

[0005] FIG. 3 is a flow chart, depicting a method of manufacturing an array of monolithic WDM VCSELs with QWI, according to an example.

[0006] FIGS. 4A-4F are each a side-elevational view, illustrating a method for manufacturing an array of monolithic WDM VCSELs with QWI, according to an example.

[0007] FIGS. 5A-5F are each a side-elevational view, illustrating another method for manufacturing an array of monolithic WDM VCSELs with QWI, according to an example.

[0008] FIG. 6 is a side-elevational view, depicting a bottom emitting VCSEL structure, according to an example.

DETAILED DESCRIPTION

[0009] Once an optical fiber infrastructure is installed in datacenters, it is a daunting task to add more fibers to accommodate increasing bandwidth demands. Wavelength division multiplexing (WDM) is a means to increase the bandwidth density without increasing fiber count. Typical VCSEL-based WDM transmitters are composed of discrete VCSEL dies that emit light at unique wavelengths. This may translate to increased transmitter packaging complexity and cost.

[0010] In accordance with the teachings herein, monolithic WDM VCSEL arrays may use quantum well intermixing (QWI). Each VCSEL may include a bottom distributed Bragg reflector (DBR), a top mirror, and a laser cavity therebetween. The laser cavity may include a multiple quantum well (MQW) layer sandwiched between a lower separate confinement heterostructure (SCH) layer and an upper SCH layer. The multiple quantum well layer is made of alternating quantum well and barrier layers. Each VCSEL further includes a Fabry Perot tuning/current spreading layer as part of the laser cavity. In some cases, the Fabry Perot tuning/current spreading layer may have a length that varies from one VCSEL to another. In other cases, the Fabry Perot tuning/current spreading layer may be the same length for all VCSELS, but the top mirror may have different structures from one VCSEL to the next. Each VCSEL is formed with a different amount of quantum well intermixing and consequently experiences a different lasing wavelength shift.

[0011] By "quantum well intermixing" is meant a modification of the band gaps of the gain medium in the laser structure. The QWI allows a shift in the wavelength at which the gain is maximum. The Fabry Perot tuning/current spreading layer controls the resonant wavelength of the laser cavity.

[0012] While the QWI may not need to be impurity-free, the presence of impurities may lead to reliability issues, increased optical loss, and compromise VCSEL performance. QWI enables spatially tuning of the gain peak across the VCSEL array, so that each VCSEL or sets of VCSELs emit light at discrete wavelengths.

[0013] The teachings herein have the potential to more efficiently utilize datacenter optical fiber infrastructure, increase the bandwidth density of bundled optical connections, and reduce the packaging cost and complexity of VCSEL based WDM transmitters.

[0014] Impurity-free quantum well intermixing allows blue-shifting the emission wavelength of quantum well gain media in VCSELs without creating

unwanted defects that can lead to high optical loss, performance, and reliability concerns.

[0015] A linear array of VCSELs may be fabricated, each VCSEL in the array emitting a different wavelength. Alternatively, the VCSELs may be arranged in two-dimensional arrays where each row emits a specific wavelength.

[0016] The VCSELs may be fabricated as top emitters or substrate side emitters and patterned with under bump metals and/or solder bumps for direct solder attachment to interposers, organic substrates, or PCBs. The VCSELS may alternatively be fabricated as bottom emitters, through the substrate.

[0017] FIGS. 1A-1B are each a schematic view of the energy band diagrams 100, 150 of a quantum well gain medium, in an as-grown state (FIG. 1A) and after quantum well intermixing (FIG. 1B). In FIG. 1A, there is a distance, denoted by arrow 102, separating a hole energy level 104 in valence band 106 from an electron energy level 108 in conduction band 110. Light λ_1, denoted by arrow 112, is at a longer wavelength and is termed "red".

[0018] In FIG. 1B, after quantum well intermixing, the distance 102' between the hole energy level 104' and the electron energy level 108' may be increased by quantum well intermixing, as described in greater detail below. Light λ_2, denoted by arrow 112', is at a shorter wavelength and is termed "blue" or "blue-shifted".

[0019] FIGS. 1A-1B may be viewed as showing the energy band diagrams of two VCSELs gain media side by side, one in which no QWI has taken place and one in which QWI has taken place. By controlling the extent of QWI, more VCSELs may be placed side by side, each VCSEL emitting a different wavelength of light. The VCSEL gain media may incorporate multiple quantum wells. In this case, QWI will shift the gain peak of each quantum well in the gain media.

[0020] FIG. 2 illustrates an example of a top emitting (or bottom emitting) WDM VCSEL array with spatially varying gain and Fabry Perot peak wavelength. FIG. 2 is a side elevational view of a configuration, or array, 200 of four VCSELs 202a, 202b, 202c, 202d, having been processed so that there is an increasing blue shift going from left to right of the Figure. Each VCSEL 202a, 202b, 202c, 202d is supported on a common substrate 204 and emits a different wavelength of light λ_1, λ_2, λ_3, λ_4, respectively. As shown by arrow 206, the array 200 has a spatially increasing blue shift. Specifically, the array 200 has spatially increasing blue-shifted gain media and decreasing effective laser cavity length.

[0021] As pictured, the array 200 may be a one-dimensional array of four VCSELs. Alternatively, the array 200 may be a row of four VCSELs in a two-dimensional array of VCSELs. While FIG. 2 depicts an array of four VCSELs, there may be fewer or more VCSELs in the array 200.

[0022] Each VCSEL 202a-202d may include a broadband lower distributed Bragg reflector 208 (common to all VCSELs 202a-202d), Fabry Perot tuning/current spreading layer 210, and a cavity and gain media 212 between the DBR 208 and the Fabry Perot tuning/current spreading layer 210, sometimes referred to herein as the Fabry Perot layer 210. A top mirror 214 may be formed on top of the Fabry Perot layer 210.

[0023] The Fabry Perot layer 210 serves as a wavelength filter, only allowing one particular wavelength to resonate inside the cavity. The Fabry Perot layer may be longest at the first VCSEL, since the cavity may be increasingly shorter for subsequent VCSELs. Spatial adjustment of the Fabry Perot layer ensures optimum offset between the cold cavity resonant wavelength and the intermixed MQW gain peak for optimum over-temperature performance. The cavity and gain media 212 in each case may include a multiple quantum well (MQW) layer 216 sandwiched between a lower separate confinement heterostructure (SCH) layer 218 and an upper SCH layer 220. The top mirror 214 serves as an upper mirror in the cavity, which includes the gain medium (the multiple quantum wells) 216, the SCH layers 218, 220, and the Fabry Perot layer 210.

[0024] The substrate 204 may be a III-V material, such as gallium arsenide (GaAs). The lower DBR 208 may be formed of alternating layers of, but not limited to, GaAs and aluminum gallium arsenide (AlGaAs). The lower and upper SCH layers 218, 220 may be AlGaAs. The MQW 216 may be alternating layers (not shown) of, but not limited to, GaAs and AlGaAs. It will be appreciated that various compositions of $Al_xGa_{1-x}As$, where x = 0 to 1, may be employed, since all such compositions are lattice-matched to GaAs. Alternative materials may be employed in the MQW such as indium gallium arsenide (InGaAs) and indium gallium phosphide (InGaP) and gallium arsenide phosphide (GaAsP). The Fabry Perot tuning/current spreading layer 210 may be AlGaAs, GaAs, or alternating layers thereof.

[0025] Examples of structures that may be used as top mirror 214 include, but are not limited to, semiconductor Bragg reflectors, dielectric Bragg reflectors, dielectric (such as SiO_2) enhanced metal hybrid mirrors, transparent conductive oxide or nitride enhanced metal hybrid mirrors, high contrast gratings, suspended reflectors, and combinations thereof.

[0026] Since the variation in wavelength progresses in an orderly fashion from the spaced-apart VCSELs, this configuration 200 is called "monolithic WDM VCSELs with spatially varying gain peak". The configuration 200 is considered to be monolithic, since all VCSELs are fabricated on the same substrate, but for the amount of intermixing in the MQW and, potentially, the design of the top mirror. The point defects to induce intermixing may be introduced by creating a stress mismatch on a surface of the cap layers and propagating the point defects toward the MQW.

[0027] The array 200 is considered to be wavelength division multiplexing because of the different wavelengths emitted by the array of VCSELs.

[0028] A method of manufacturing an array of monolithic WDM VCSELs with QWI is provided. Each VCSEL may include a multiple quantum well and emitting light at a different wavelength from the others. The method may include creating point defects, such as vacancies, above the multiple quantum well

layer, wherein different concentrations of point defects induce different amounts of intermixing between the quantum well and barrier materials and different wavelengths of light.

[0029] The method 300 of manufacturing the array of VCSELs is illustrated in FIG. 3 and is as follows:

grow 305 a half cavity VCSEL epitaxial wafer;

perform 310 selective quantum well intermixing;

form 315 top mirrors;

fabricate 320 VCSELs.

[0030] By "grow a half cavity VCSEL epitaxial wafer" is meant forming the lower DBR layers 208 on the substrate 204, followed by forming the cavity and gain media 212, and the Fabry Perot tuning/current spreading layer 210, and then a sacrificial layer.

[0031] By "perform selective quantum well intermixing" is meant forming a patternable layer (such as SrF_2) on the sacrificial layer, patterning the patternable layer (by wet or dry etching, for example), blanket coating the patterned layer with a stress-inducing layer (such as SiO_2), and performing rapid thermal annealing to induce quantum well mixing in the MQW layer 216. The pattern selected may be such that the more area covered by the patterned layer, the less stress that can be induced in the MQW layer 216. That is, there may be less quantum well intermixing on the left side of the device in FIG. 2, and progressively more QWI proceeding across to the right side.

[0032] Due to the mismatch in crystal structure or coefficient of thermal expansion (CTE) between the stress-inducing layer and the sacrificial layer, point defects (not shown) may be generated in the sacrificial layer. In an example, the sacrificial layer may be GaAs. Heating, such as by rapid thermal annealing (RTA), may cause Ga to diffuse from the GaAs sacrificial layer into the stress-inducing layer, leaving behind point defects such as vacancies. Heating may drive the vacancies through the Fabry Perot layer 210 and upper SCH

layer 220 toward the MQW 216 and induce intermixing between the quantum well and barrier layer materials. The RTA may be performed at a temperature within a range of about 600° to 1000°C for a time within a range of about 10 sec to several minutes.

[0033] By "form top mirrors" is meant stripping off the blanket coat, the patterned layer, and the sacrificial layer, progressively thinning the Fabry Perot layer 210 across the surface from left to right (or progressively thickening the Fabry Perot layer 210 from right to left), with thicker portions aligned with less intermixing in the MQW 216, and forming the top mirror 214 onto the Fabry Perot layer 210. The top mirror conforms to the progressively thinned Fabry Perot layer 210. Alternatively, by "form top mirrors" is meant providing different structures for each top mirror 214.

[0034] By "fabricate VCSELs" is meant forming the array 200 of VCSELs, in which individual VCSELs 202a-2-2d may be formed by etching and wet oxidation. A lower contact (not shown) may be formed on the lower DBR 208 surface or substrate 204. A top contact (not shown) may be formed on the top mirror or Fabry Perot layer 210.

[0035] FIGS. 4A-4F and FIGS. 5A-5F each illustrate an example method for manufacturing an array of VCSELs. In both examples, an array 200 of four VCSELs 202a-202d (FIG. 4F) or an array 200' of four VCSELs 202a'-202d', with reference to FIG. 2, may be fabricated. It may be appreciated that more, or less, than four VCSELs may be made by these methods.

[0036] These example methods are provided for teaching one skilled in the art for manufacturing an array of VCSELs. However, examples of other methods may also be devised; such methods are considered to fall within the scope of the appended claims.

[0037] Turning now to FIGS. 4A-4F, a first example method starts in FIG. 4A with providing a substrate 204, with reference to FIG. 2. The lower DBR 208 may be formed on the top of the substrate 204. The lower SCH layer 218, the quantum wells and barriers for the MQW 216, and the upper confinement layer

220 may each be formed in turn over the lower DBR 208. The Fabry Perot layer 210 may be formed on top of the upper confinement layer 220. A sacrificial cap layer 402 may be formed on the top of the Fabry Perot layer 210. The sacrificial cap layer 402 may be of GaAs or AlGaAs, and may be removed in a later stage of the method. The thickness of the sacrificial cap layer 402 may be in the range of about 10 to 200 nm. In other approaches, the upper SCH layer 220 may be replaced with or include a thin etch stop layer, such as, but not limited to, AlAs, AlGaAs, InGaP, and capped with the GaAs sacrificial cap layer 402.

[0038] In FIG. 4B, selectively intermixing the quantum wells may be achieved by covering the top surface of the sacrificial cap layer 402 with a patternable layer 404 and patterning this layer to form areas 406a, 406b, 406c, 406d where a blue shift is desired. The thickness of the patternable layer 404 may be in the range of about 50 to 200 nm. An example of the patternable layer 404 is SrF_2, which can be patterned to expose the different areas 406a-406d. In patterning, a higher percent of SrF_2 is left in places where less blue shift is desired. For example, the four areas may be covered as follows to provide a blue shift across the surface: 100% (406a), 75% (406b), 50% (406c), and 0% (406d), where 100% coverage leads to lower blue shift and 0% coverage leads to greater blue shift. The patterning may be performed using a linewidth pattern in which the linewidths may be in the range 1 to 200 μm.

[0039] In FIG. 4C, the entire structure may be blanket-coated with a stress-inducing layer 408 such as of SiO_2, followed by heating to perform the quantum well intermixing. The heating may be performed by rapid thermal annealing (RTA).

[0040] Due to the mismatch in crystal structure or coefficient of thermal expansion (CTE) between the stress-inducing layer 408 and the sacrificial layer 402, point defects (not shown) may be generated in the sacrificial layer. Heating, such as by rapid thermal annealing (RTA), may cause Ga to diffuse from the Ga-containing sacrificial layer 402 into the stress-inducing layer 408, leaving behind point defects such as vacancies. Heating may then drive the vacancies

through the upper SCH layer 220 toward the MQW 216 and induce intermixing between the quantum well and barrier layer materials. The RTA may be performed at a temperature within a range of about 600° to 1000°C for a time within a range of about 10 sec to several minutes.

[0041] The presence of the point defects may induce intermixing in the MQW 216 and may cause a change in the energy hole level 104 and the electron energy level 108, resulting in an increase in the distance 102' between the hole energy level 104' and the electron energy level 108' (see FIG. 1), thereby blue-shifting the gain peak, and therefore the light emitted from a VCSEL formed locally from those areas covered by the stress-inducing layer. In general, the more point defects, the greater the blue shift. The number of point defects or the extent of quantum well intermixing to provide a specific wavelength shift may be established empirically, and may depend on the design of the epitaxial layers and the properties of the sacrificial cap layer 402, the patternable layer 404, and the stress-inducing layer 408.

[0042] There are a number of different ways to control the concentration of point defects. For example, stress mismatch between the stress-inducing layer 408 and the sacrificial GaAs cap layer 402 may be altered in progressing across the substrate from the original, unstressed MQW region (from left to right in FIG. 4C). Increasing the stress increases the point defect concentration, which in turn causes a greater blue-shifting of the emitted light.

[0043] Alternatively, and as shown in FIGS. 4B-4C, a material with a lower Ga diffusion coefficient, such as SrF_2 404, can be patterned below the SiO_2 layer 408 to spatially control the concentration of point defects, and therefore, the blue shift. In this case, only a single RTA heating step is required. Another method is to pattern or modify the thickness of the SiO_2 layer 408 to control the concentration of vacancies formed in the Ga-containing layer 402.

[0044] The stress-inducing layer 408 may be a material that is lattice-mismatched or CTE (coefficient of thermal expansion)-mismatched with the sacrificial layer 402, here, GaAs or AlGaAs. Further, Ga is to be able to diffuse

through the material. Examples of such materials include, but are not limited to, SiO_2, SiO_x, silicon oxynitride, and Si_xN_y. The diffusion of Ga into SrF_2 is less than into SiO_2.

[0045] The shading of MQW layer 216 has been altered from its original shading, shown in FIGS. 4A-4B, to reflect the fact that each section of the MQW layer 216, corresponding to the patterned stress-inducing regions 406a-406d, has been successively blue-shifted, due to the quantum well intermixing.

[0046] Next, as shown in FIG. 4D, the stress-inducing layer 408, the patternable layer 404 and the sacrificial Ga-containing cap layer 402 may be removed. Removal of the sacrificial cap layer 402 may be desired, since the cap layer may have excess defects that contribute to optical loss, poor laser performance, and poor growth surface on which to form the top mirror 214. The Fabry Perot layer 210 may be successively thinned in going from left to right, so that the Fabry Perot layer 210 is thickest in the 406a region and thinnest in the 406d region. The Fabry Perot layer may be provisioned with etch stop layers (not shown). Etch stop layers in combination with selective etching techniques can be used for precise laser cavity thickness control. Alternatively, the Fabry Perot layer 210 can be increased from right to left by adding material.

[0047] Next, as shown in FIG. 4E, the top mirror 214 may be deposited on the Fabry Perot layer 210. The deposition may be conformal, to follow the stepped contour of the Fabry Perot layer 210. The top mirror 214 may be deposited to a thickness within a range of 0.1 to 10 μm. Deposition of the top mirror 214 may be performed by, but not limited to, any of metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), plasma-enhanced chemical vapor deposition (PECVD), sputtering, electron beam evaporation, thermal evaporation, or combinations thereof.

[0048] Finally, as shown in FIG. 4F, an array 200 of VCSELs 202a, 202b, 202c, 202d is formed. The individual VCSELs 202a-202d may be formed by etching and wet oxidation. An oxide aperture (not shown in FIG. 4F, but depicted in FIG. 6) may be added to each VCSEL 202a-202d. The arrangement of

P-ohmic and N-ohmic contacts (not shown) may depend on the type of mirror 214 and the choice between top or bottom emission.

[0049] An example of a completed VCSEL 202a-202d may include the doped or semi-insulating GaAs substrate 204, on which is formed the lower Bragg reflector 208 of multiple periods of n-AlGaAs/AlAs/GaAs. On the lower Bragg reflector 208 may be formed the lower SCH layer 218 of AlGaAs. On the lower SCH layer 218 may be formed the multiple quantum well layer 216, formed of alternating layers of a quantum wells of InGaAs and barriers of AlGaAs. On the multiple quantum well layer 216 may be formed the upper confinement layer 220, formed of AlGaAs. On the upper confinement layer 220 may be formed the Fabry Perot layer 210, formed of AlGaAs, AlAs, GaAs, or alternating layers thereof. On the Fabry Perot layer 210 may be formed the top mirror 214. The materials/structures for the top mirror 214 are discussed above.

[0050] Turning now to FIGS. 5A-5F, a second example method starts in FIG. 5A with providing a substrate 204, with reference to FIG. 2. FIG. 5A is essentially identical to FIG. 4A. As in FIG. 4A, the lower DBR 208 may be formed on the top of the substrate 204. The lower SCH layer 218, the quantum wells and barriers for the MQW 216, and the upper confinement layer 220 may each be formed in turn over the lower DBR 208. The Fabry Perot layer 210 may be formed on top of the upper confinement layer 220. A sacrificial cap layer 402 may be formed on the top of the Fabry Perot layer 210. The sacrificial cap layer 402 may be of GaAs or AlGaAs, and may be removed in a later stage of the method. The thickness of the sacrificial cap layer 402 may be in the range of about 10 to 200 nm. In other approaches, the upper SCH layer 220 may be replaced or include with a thin etch stop layer, such as, but not limited to, AlAs, AlGaAs, InGaP, and capped with the GaAs sacrificial cap layer 402.

[0051] In FIG. 5B, which is essentially identical to FIG. 4B, selectively intermixing the quantum wells may be achieved by covering the top surface of the sacrificial cap layer 402 with a patternable layer 404 and patterning this layer to form areas 406a, 406a, 406c, 406d where a blue shift is desired. The thickness

of the patternable layer 404 may be in the range of about 50 to 200 nm. An example of the patternable layer 404 is SrF_2, which can be patterned to expose the different areas 406a-406d. In patterning, a higher percent of SrF_2 is left in places where less blue shift is desired. For example, the four areas may be covered as follows to provide a blue shift across the surface: 100% (406a), 75% (406b), 50% (406c), and 0% (406d), where 100% coverage leads to lower blue shift and 0% coverage leads to greater blue shift. The patterning may be performed using a linewidth pattern in which the linewidths may in the range 1 to 200 μm.

[0052] In FIG. 5C, which is essentially identical to FIG. 4C, the entire structure may be blanket-coated with a stress-inducing layer 408 such as of SiO_2, followed by heating to perform the quantum well intermixing. The heating may be performed by rapid thermal annealing (RTA).

[0053] Due to the mismatch in crystal structure or coefficient of thermal expansion (CTE) between the stress-inducing layer 408 and the sacrificial layer 402, point defects (not shown) may be generated in the sacrificial layer. Heating, such as by rapid thermal annealing (RTA), may cause Ga to diffuse from the Ga-containing sacrificial layer 402 into the stress-inducing layer 408, leaving behind point defects such as vacancies. Heating may then drive the vacancies through the upper SCH layer 220 toward the MQW 216 and induce intermixing between the quantum well and barrier layer materials. The RTA may be performed at a temperature within a range of about 600° to 1000°C for a time within a range of about 10 sec to several minutes.

[0054] The presence of the point defects may induce intermixing in the MQW 216 and may cause a change in the energy hole level 104 and the electron energy level 108, resulting in an increase in the distance 102' between the hole energy level 104' and the electron energy level 108' (see FIG. 1), thereby blue-shifting the gain peak, and therefore the light emitted from a VCSEL formed locally from those areas covered by the stress-inducing layer. In general, the more point defects, the greater the blue shift. The number of point defects or

the extent of quantum well intermixing to provide a specific wavelength shift may be established empirically, and may depend on the design of the epitaxial layers and the properties of the sacrificial cap layer 402, the patternable layer 404 and the stress-inducing layer 408.

[0055] There are a number of different ways to control the concentration of point defects. For example, stress mismatch between the stress-inducing layer 408 and the sacrificial GaAs cap layer 402 may be altered in progressing across the substrate from the original, unstressed MQW region (from left to right in FIG. 5C). Increasing the stress increases the point defect concentration, which in turn causes a greater blue-shifting of the emitted light.

[0056] Alternatively, and as shown in FIGS. 5B-5C, a material with a lower Ga diffusion coefficient, such as SrF_2 404, can be patterned below the SiO_2 layer 408 to spatially control the concentration of point defects, and therefore, the blue shift. In this case, only a single RTA heating step is required. Another method is to pattern or modify the thickness of the SiO_2 layer 408 to control the concentration of vacancies formed in the Ga-containing layer 402.

[0057] The stress-inducing layer 408 may be a material that is lattice-mismatched or CTE (coefficient of thermal expansion)-mismatched with the sacrificial layer 402, here, GaAs or AlGaAs. Further, Ga is to be able to diffuse through the material. Examples of such materials include, but are not limited to, SiO_2, SiO_x, silicon oxynitride, and Si_xN_y. The diffusion of Ga into SrF_2 is less than into SiO_2.

[0058] The shading of MQW layer 216 has been altered from its original shading, shown in FIGS. 5A-5B, to reflect the fact that each section of the MQW layer 216, corresponding to the patterned stress-inducing regions 406a-406d, has been successively blue-shifted, due to the quantum well intermixing.

[0059] Next, as shown in FIG. 5D, the stress-inducing layer 408, the patternable layer 404, and the sacrificial Ga-containing cap layer 402 may be removed. Removal of the sacrificial cap layer 402 may be desired, since the cap

layer may have excess defects that contribute to optical loss, poor laser performance, and poor growth surface on which to form the top mirror 214.

[0060] Next, as shown in FIG. 5E, a plurality of top mirrors 214a-214d may be deposited on the Fabry Perot layer 210. Each top mirror 214a-214d is aligned with the stress-inducing regions 406a-406d. The top mirrors 214a-214d may be deposited to a thickness within a range of 0.1 to 10 μm. Deposition of the top mirror 214a-214d may be performed by, but not limited to, any of metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), plasma-enhanced chemical vapor deposition (PECVD), sputtering, electron beam evaporation, thermal evaporation, or combinations thereof. In this example method, different wavelengths may be achieved by employing different structures for the top mirrors 214a-214d. This may be accomplished by employing different reflectivities and different phase responses (phase resonance condition in the cavity) for each of the top mirror 214 structures. In an example, high contrast gratings may be employed, each with a different pattern. In an alternate example, dielectric DBR mirrors may be employed.

[0061] Finally, as shown in FIG. 5F, an array 200' of VCSELs 202a', 202b', 202c', 202d' is formed. The prime associated with each reference number is a recognition that the VCSEL structure is somewhat modified from FIG. 2.The individual VCSELs 202a'-202d' may be formed by etching and wet oxidation. An oxide aperture (not shown in FIG. 5F but depicted in FIG. 6) may be added to each VCSEL 202a-202d. The arrangement of P-ohmic and N-ohmic contacts (not shown) may depend on the type of mirror 214 and the choice between top or bottom emission.

[0062] An example of a completed VCSEL 202a'-202d' may be similar to that given above for VCSEL 202a-202d.

[0063] Shown above is an example in which the Fabry Perot tuning/current spreading layer 210 has a different thickness for each VCSEL in the array and in which the top mirror 214 has the same structure (FIGS. 4A-4F). Also

shown above is an example in which the Fabry Perot tuning/current spreading layer 210 has the same thickness for each VCSEL in the array and in which the top mirror 214 has a different structure for each VCSEL in the array (FIGS. 5A-5F). It may be appreciated that in yet another example, the Fabry Perot tuning/current spreading layer 210 may have a different thickness for each VCSEL in the array and the top mirror 214 may have a different structure for each VCSEL in the array.

[0064] The foregoing description has been primarily directed to a top emitting VCSEL. FIG. 6 depicts an example of a completed bottom emitting VCSEL 600. The bottom emitting VCSEL 600 may include the substrate 204, on which may be disposed the semiconductor DBR 208. The substrate may be n-type or semi-insulating. In contact with the DBR 208 may be the lower SCH layer 218, on which may be disposed the multiple quantum well 216. An upper SCH layer 220, including an oxide aperture structure 602 may be disposed on or offset above and/or below from the multiple quantum well 216. The Fabry Perot layer 210 may be disposed over the oxide aperture structure 602. The mirror layer 214 may be disposed on the Fabry Perot layer 210. The oxide aperture may be incorporated into the lower DBR 208, Fabry Perot layer 210, or mirror layer 214. In some embodiments, the oxide aperture may be formed prior to formation of the top mirror layer 214.

[0065] The oxide aperture structure 602 may be made up of two portions, a layer of AlGaAs, serving as the upper SCH 220, in which is formed a dielectric aperture 602a. The AlGaAs of the upper SCH 220 may be a high Al-containing composition, such as 98% Al. By patterning a mesa and exposing the upper SCH 220 sidewalls to water vapor at an elevated temperature, such as 400°C, AlGaAs may be converted into an aluminum oxide. The time of exposure may control how far into the SCH 220 the aluminum oxide ring 602a extends. The aluminum oxide ring 602a serves as a current blocking layer and optical confinement layer (since it has a lower index of refraction compared to that of AlGaAs), and may act to confine light in the horizontal direction.

[0066] In previous discussions, the Fabry Perot layer 210 primarily served as a tuning layer. In this example, it may serve an additional function as a current spreading layer, in which it spreads the current in the horizontal direction and reduces the resistance for the current to try to flow more uniformly through the oxide aperture structure 602. The current spreading function may be aided by doping the Fabry Perot layer 210 more heavily than in other examples. Alternatively, two regions 210a, 210b may be provided, with one region 210a primarily directed to tuning and the other region 210b primarily directed to current spreading. The dashed line separated these two layers is to show this alternative configuration. Doping in either example may be P-type and achieved with carbon.

[0067] Contact to the VCSEL 600 may be provided by an N-ohmic contact 604 disposed on the lower DBR 208. A P-ohmic contact 606 may be disposed on the Fabry Perot layer 210. Lenses (not shown) may be integrated on the backside 204a of the VCSEL 600. Light λ may be emitted from the bottom of the VCSEL 600.

[0068] The N-ohmic contact 604 may be provided using gold, germanium, and nickel. The P-ohmic contact 606 may be provided using titanium, platinum, and gold.

[0069] A cap layer 608 may be used to seal the mirror 214 and also provide additional reflectivity. The cap layer 608 may be, but not limited to, gold and the same material as the P-ohmic contact 606.

[0070] The preceding description has been presented to illustrate and describe examples of the principles described. This description is not intended to be exhaustive or to limit these principles to any precise form disclosed. Many modifications and variations are possible in light of the above teaching.

[0071] In the foregoing description, numerous details are set forth to provide an understanding of the examples disclosed herein. However, it will be un-

derstood that the examples may be practiced without these details. While a limited number of examples have been disclosed, it should be understood that there are numerous modifications and variations therefrom.

[0072] As used in the specification and claims herein, the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise.

[0073] As used in this specification and the appended claims, "approximately" and "about" mean a ±10% variance caused by, for example, variations in manufacturing processes.

[0074] In the foregoing detailed description, reference is made to the drawings accompanying this disclosure, which illustrate specific examples in which this disclosure may be practiced. The components of the examples can be positioned in a number of different orientations and any directional terminology used in relation to the orientation of the components is used for purposes of illustration and is in no way limiting. Directional terminology includes words such as "top," "bottom," "front," "back," "leading," "trailing," etc. Similar or equal elements in the Figures may be indicated using the same numeral.

[0075] It is to be understood that other examples in which this disclosure may be practiced exist, and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense. Instead, the scope of the present disclosure is defined by the appended claims. While a limited number of examples have been disclosed, it should be understood that there are numerous modifications and variations therefrom.

CLAIMS

What is claimed is:

1. An array of monolithic wavelength division multiplexing (WDM) vertical cavity surface emitting lasers (VCSELs) with spatially varying gain peak and Fabry Perot wavelength, each VCSEL including a lower distributed Bragg reflector (DBR), a Fabry Perot tuning/current spreading layer, and a structure comprising a multiple quantum well (MQW) layer sandwiched between a lower separate confinement heterostructure (SCH) layer and an upper SCH layer, the structure sandwiched between the DBR and the Fabry Perot tuning/current spreading layer, each MQW experiencing a different amount of quantum well intermixing and concomitantly a different wavelength shift,

wherein each VCSEL further includes a top mirror on the Fabry Perot tuning/current spreading layer.

2. The array of claim 1, in which the lower DBR comprises layers of GaAs and AlGaAs, the lower and upper SCH layers comprise GaAs and AlGaAs, and the MQW comprises layers of GaAs or InGaAs, and AlGaAs or InGaP or GaAsP.

3. The array of claim 1, in which the Fabry Perot tuning/current spreading layer comprises AlGaAs, GaAs, or alternating layers of AlGaAs and GaAs.

4. The array of claim 1, in which the top mirror comprises any of semiconductor Bragg reflectors, dielectric Bragg reflectors, dielectric enhanced metal hybrid mirrors, transparent conductive oxide or nitride enhanced metal hybrid mirrors, high contrast gratings, suspended reflectors, and combinations thereof.

5. The array of claim 1, in which the VCSELs are arranged in a linear fashion, each VCSEL having a larger quantum well intermixing in a particular direction, each VCSEL emitting light of a wavelength that is blue-shifted in the direction of larger quantum well intermixing.

6. The array of claim 5, in which the quantum well intermixing arises from a concentration of point defects generated by stress mismatch, with a greater number of point defects resulting in a larger quantum well intermixing.

7. The array of claim 1, in which the Fabry Perot tuning/current spreading layer has different thickness for each VCSEL in the array and in which the top mirror has the same structure or in which the Fabry Perot tuning/current spreading layer has the same thickness for each VCSEL in the array and in which the top mirror has a different structure for each VCSEL in the array or in which the Fabry Perot tuning/current spreading layer has a different thickness for each VCSEL in the array and in which the top mirror has a different structure for each VCSEL in the array.

8. The array of claim 1, further including appropriate ohmic contacts.

9. The array of claim 1, in which the VCSELs either emit light from the top side or from the bottom side.

10. A method of manufacturing an array of monolithic wavelength division multiplexed (WDM) vertical cavity surface emitting lasers (VCSELs) with spatially varying gain peak and Fabry Perot wavelength, the method including:

growing a half cavity VCSEL epitaxial wafer;

performing selective quantum well intermixing;

forming top mirrors; and

fabricating VCSELs.

11. The method of claim 10, in which growing a half cavity VCSEL epitaxial wafer comprises forming lower DBR layers on a substrate, followed by the gain media sandwiched by SCH layers, a Fabry Perot tuning/current spreading layer, and then a sacrificial layer.

12. The method of claim 11, in which performing selective quantum well intermixing comprises forming a patternable layer on the sacrificial layer, patterning the patternable layer, blanket coating the patterned layer with a stress-inducing layer, and performing rapid thermal annealing to induce quantum well mixing in a MQW layer.

13. The method of claim 12, in which the pattern selected is such that the more area covered by the patternable layer, the less stress that can be induced in the MQW layer.

14. The method of claim 12, in which forming top mirrors comprises stripping off the blanket coat, the patternable layer, and the sacrificial layer, and either progressively altering the thickness of the Fabry Perot tuning/current spreading layer across the surface, with thicker portions aligned with less intermixing in the MQW, and forming the top mirror on the Fabry Perot tuning/current spreading layer, wherein the top mirror conforms to the progressively altered Fabry Perot tuning/current spreading layer, or forming a plurality of top mirrors on the Fabry Perot tuning/current spreading layer, each top mirror to enable distinct Fabry Perot resonant wavelengths for each VCSEL.

15. The method of claim 14, in which fabricating VCSELs comprises forming the array of VCSELs, in which individual VCSELs are formed by etching and wet oxidation, followed by application of appropriate contacts.

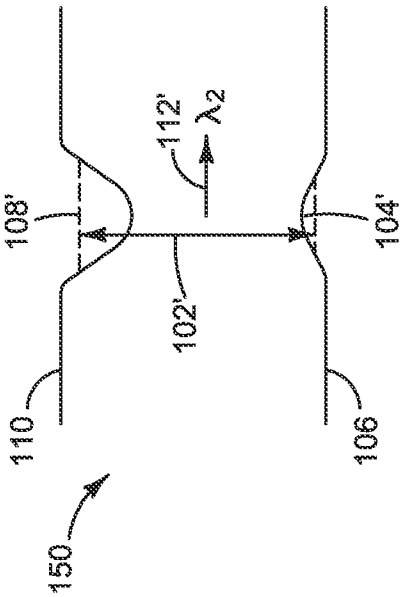

108'
112'
λ_2
104'
102'
110
106
150

FIG. 1B

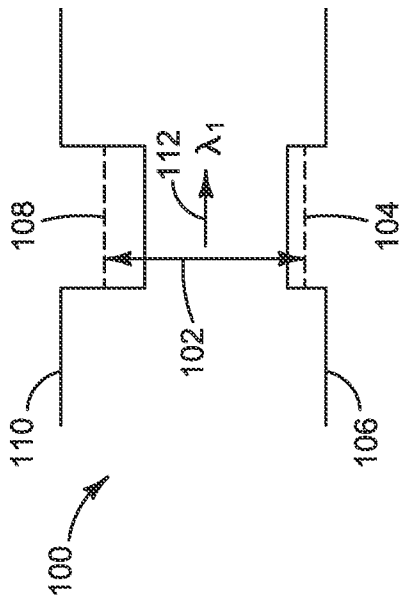

108
112
λ_1
104
102
110
106
100

FIG. 1A

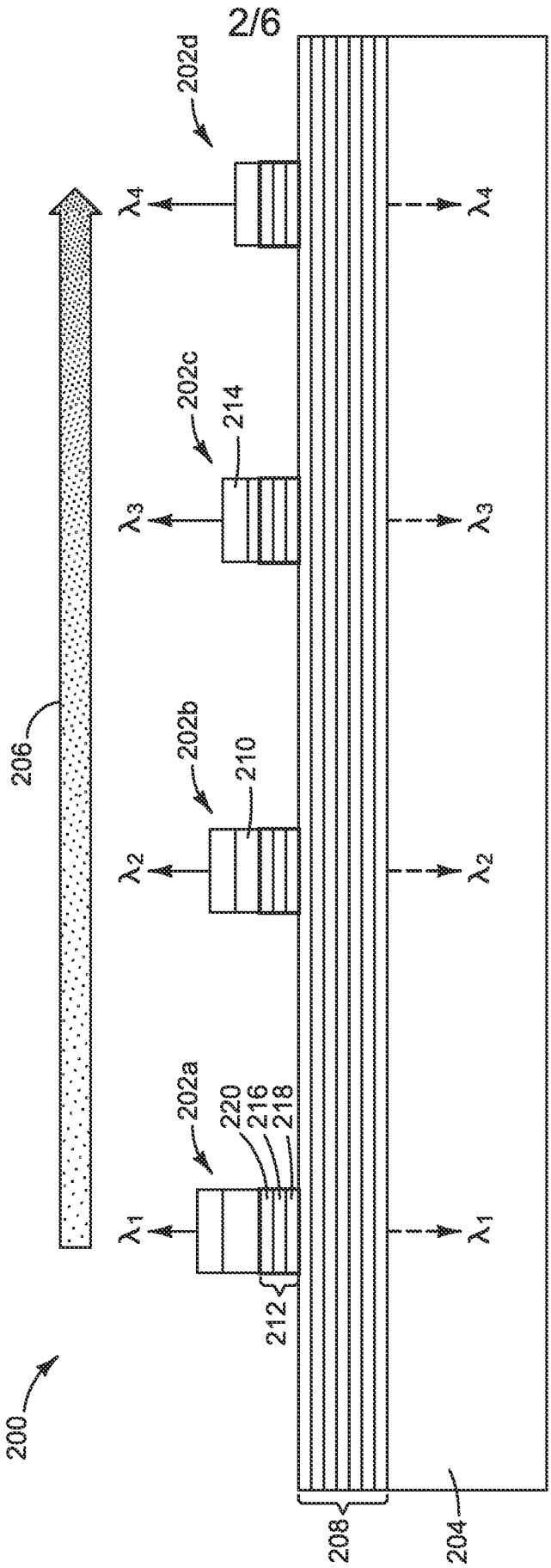

200
206
202a
220
216
218
212
202b
210
202c
214
202d
λ1
λ2
λ3
λ4
208
204

FIG. 2

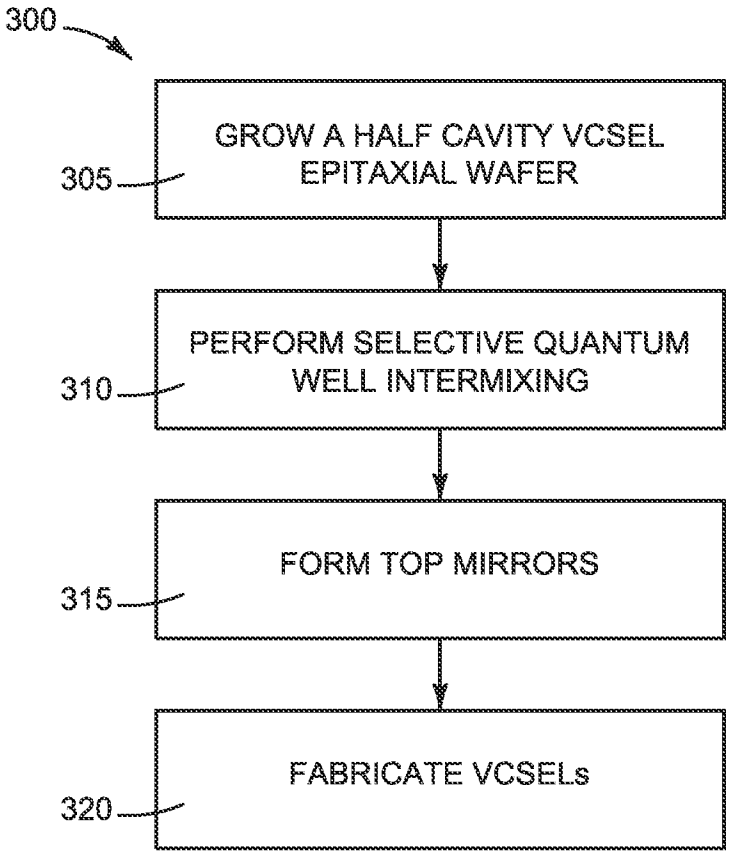

300
GROW A HALF CAVITY VCSEL EPITAXIAL WAFER
305
PERFORM SELECTIVE QUANTUM WELL INTERMIXING
310
FORM TOP MIRRORS
315
FABRICATE VCSELs
320

FIG. 3

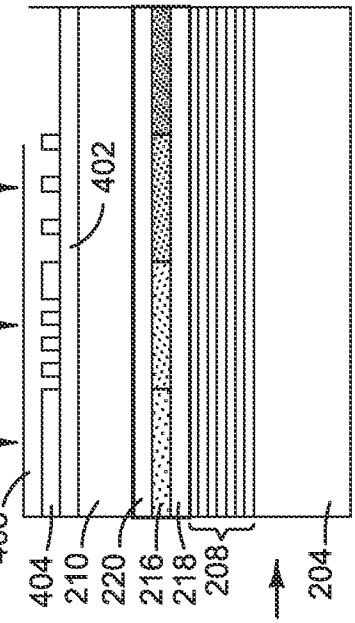


FIG. 4C

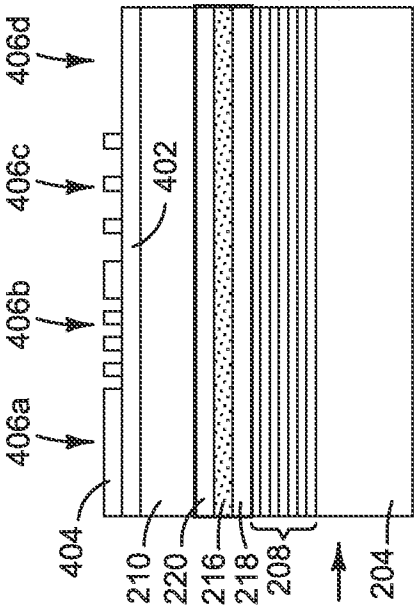


FIG. 4B

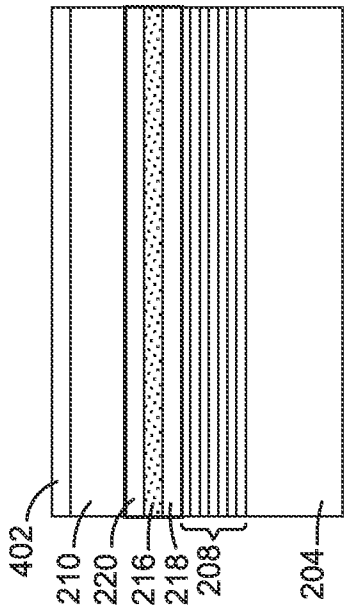


FIG. 4A

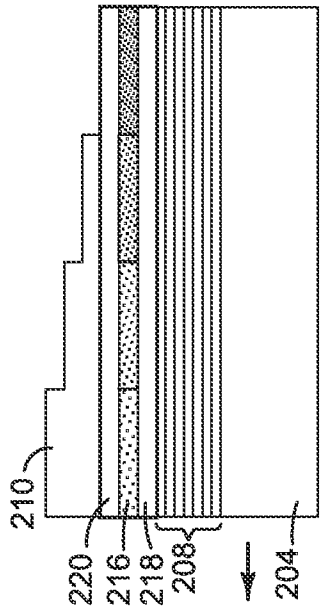


FIG. 4D

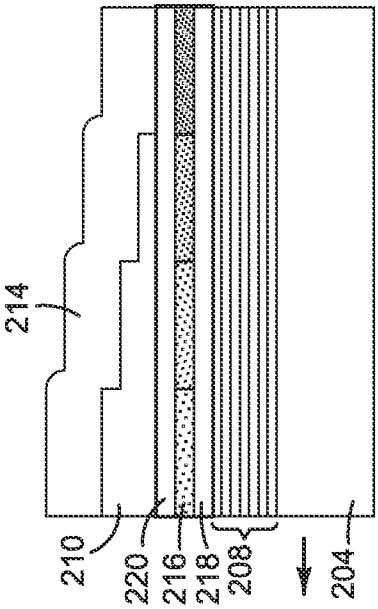


FIG. 4E

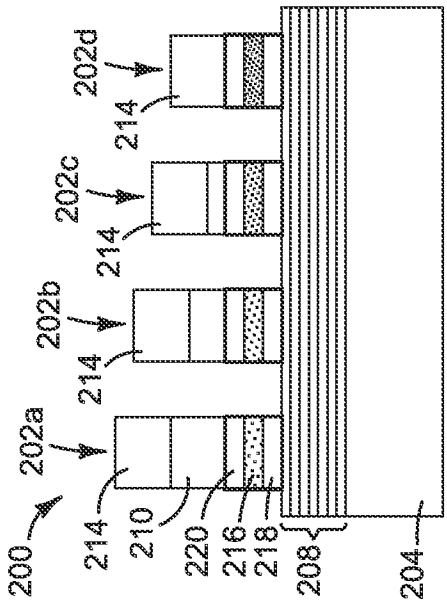


FIG. 4F

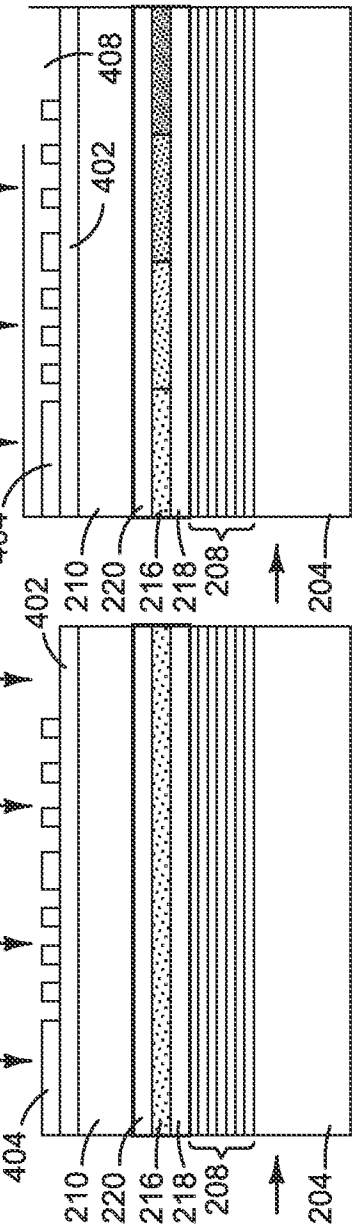


FIG. 5A

FIG. 5B

FIG. 5C

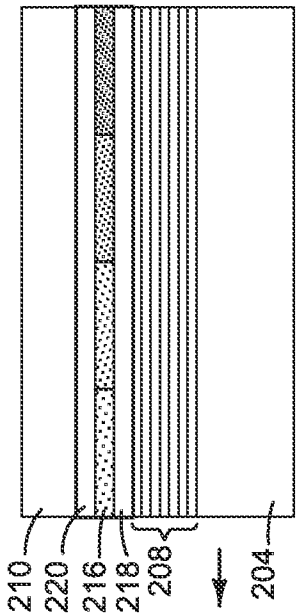


FIG. 5D

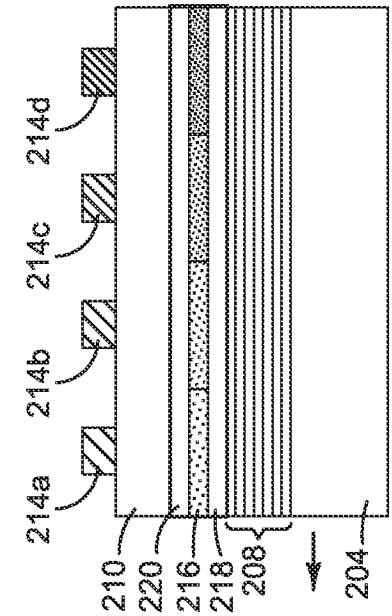


FIG. 5E

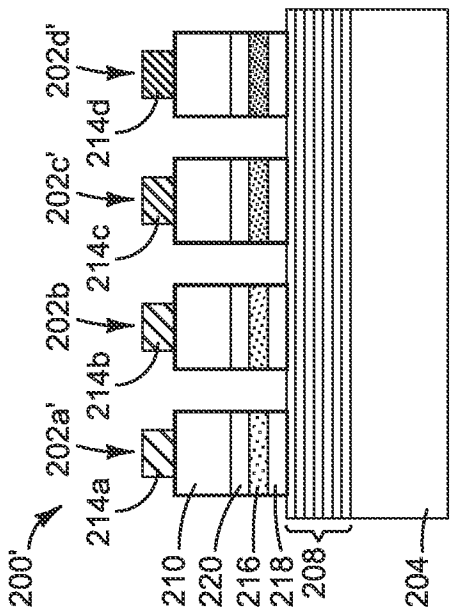


FIG. 5F

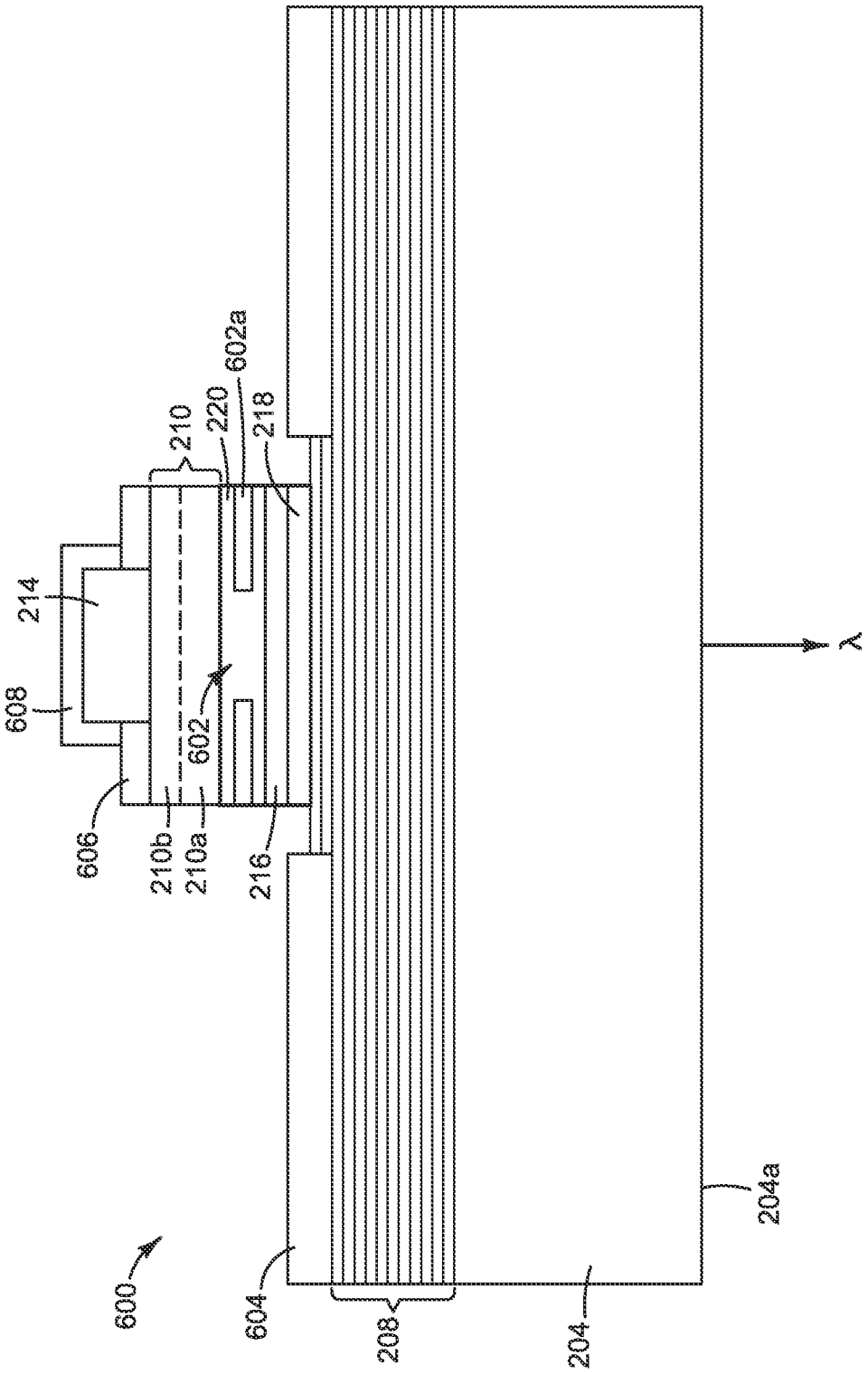

600
604
208
204
204a
λ
606
608
214
210b
210a
602
216
210
220
218
602a

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/034272

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/861(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/861; G02B 6/293; H01S 3/025; H01S 3/25; H01S 3/00; H01S 3/085; H01S 5/183

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:WDM, VCSEL, quantum well, wavelength division multiplexing, vertical cavity surface emitting laser

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003-0123507 A1 (TZU-YU WANG) 03 July 2003 See paragraphs [0006]-[0019], [0036]-[0041], claim 8 and figures 1, 4-7.	1,3-9
Y		2,10-15
Y	WO 00-69037 A2 (GORE ENTERPRISE HOLDINGS, INC.) 16 November 2000 See page 4, lines 19-21, page 6, lines 8-16 and Figure 2.	2,10-15
A	WO 98-14807 A1 (W.L. GORE & ASSOCIATES, INC.) 09 April 1998 See abstract, claims 1-14 and figure 1.	1-15
A	EP 0949728 A1 (HEWLETT-PACKARD COMPANY) 13 October 1999 See abstract, claim 1 and figure 2.	1-15
A	EP 0865123 A2 (MOTOROLA, INC.) 16 September 1998 See abstract, claim 1 and figure 4.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 March 2016 (04.03.2016)	**04 March 2016 (04.03.2016)**

Name and mailing address of the ISA/KR
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Telephone No. +82-42-481-8746

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/034272

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