(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 July 2018 (26.07.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/133574 A1

(51) International Patent Classification:
G09G 3/20 (2006.01)

(21) International Application Number:
PCT/CN2017/115082

(22) International Filing Date:
07 December 2017 (07.12.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
201710046234.3 20 January 2017 (20.01.2017) CN

(71) Applicants: **BOE TECHNOLOGY GROUP CO., LTD.** [CN/CN]; No. 10 Jiuxianqiao Rd., Chaoyang District, Beijing 100015 (CN). **HEFEI XINSHENG OPTO-ELECTRONICS TECHNOLOGY CO., LTD.** [CN/CN]; Xinzhan Industrial Park, Hefei, Anhui 230012 (CN).

(72) Inventors: **ZHANG, Miao**; No. 9 Dize Rd., BDA, Beijing 100176 (CN). **CHEN, Mo**; No. 9 Dize Rd., BDA, Beijing 100176 (CN). **SUN, Jing**; No. 9 Dize Rd., BDA, Beijing 100176 (CN). **FU, Wuxia**; No. 9 Dize Rd., BDA, Beijing 100176 (CN).

(74) Agent: **TEE&HOWE INTELLECTUAL PROPERTY ATTORNEYS**; Yuan CHEN, 10th Floor, Tower D, Minsheng Financial Center, 28 Jianguomennei Avenue, Dongcheng District, Beijing 100005 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,

(54) Title: PIXEL CIRCUIT, DRIVING METHOD THEREOF, ELECTROLUMINESCENT PANEL AND DISPLAY DEVICE

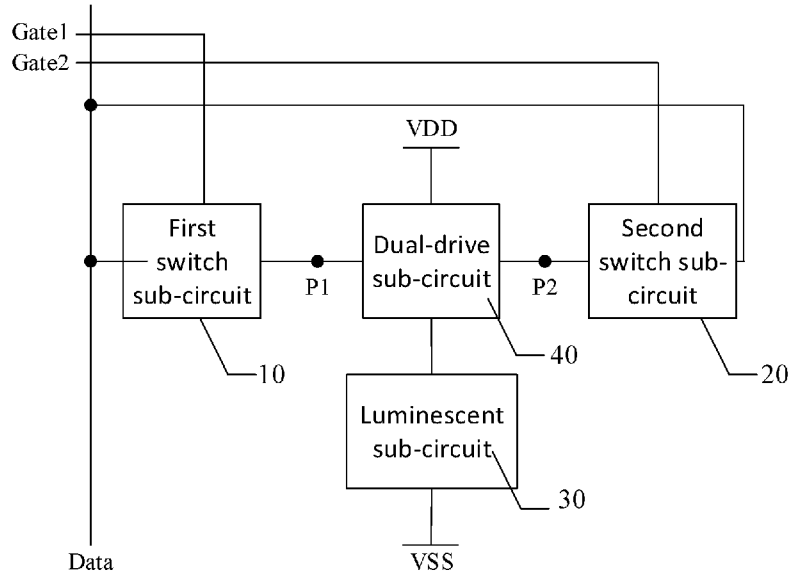

FIG. 2A

(57) Abstract: A pixel circuit, a method thereof, an electroluminescent panel, and a display device are provided. The pixel circuit includes a first switch sub-circuit, a second switch sub-circuit, a luminescent sub-circuit, and a dual-drive sub-circuit. Through improving the pixel circuit, a first driving terminal of the dual-drive sub-circuit connects to a first node, a second driving terminal of the dual-drive sub-circuit connects to the second node, when a first and a second gate line signal terminal input the gate line scanning signal alternatively, the first and the second switch sub-circuit are working alternatively, cause the first and the second driving terminal are working alternatively, thus to drive the luminescent sub-circuit to emit light. Therefore, the two driving terminals work alternatively to avoid the voltage instability due to threshold voltage shift caused by one driving terminal of the dual-drive sub-circuit works for a long time.

WO 2018/133574 A1

[Continued on next page]

SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

PIXEL CIRCUIT, DRIVING METHOD THEREOF, ELECTROLUMINESCENT PANEL AND DISPLAY DEVICE

FIELD OF THE DISCLOSURE

[0001] The disclosure relates to a luminescent technical field, and more particularly to a pixel circuit, a driving method thereof, an electroluminescent panel and a display device.

BACKGROUND

[0002] Organic Light Emitting Diode (OLED) can be classified to two types as passive matrix OLED (PMOLED) and active matrix OLED (AMOLED) according to the driving mode. AMOLED includes pixels arranged in matrix, and is belonged to active display type with high luminous efficacy, high contrast, wide view angle, and other advantages. AMOLED usually is used in high-definition display device with large size. A usual AMOLED pixel circuit is the current mode driving circuit when there is current flowing through OLED, and the OLED emits light. And changing the luminance of pixel grayscale can be achieved by controlling the amount of current flowing through the OLED itself.

SUMMARY

[0003] Embodiments of the disclosure provide a pixel circuit, including comprising: a first switch sub-circuit having a first signal control terminal coupled to a first gate line signal terminal, a first signal input terminal coupled to a data line signal terminal, and a first signal output terminal coupled to a first node, and configured to transmit a data signal provided by the data line signal terminal to the first node under controlling of a first gate line scanning signal input from the first gate line signal terminal; a second switch sub-circuit having a second signal control terminal coupled to a second gate line signal terminal, a second signal input terminal coupled to the data line signal terminal, and a second signal output terminal coupled to a second node, and configured to transmit the data signal provided by the data line signal terminal to the second node under controlling of a second gate line scanning signal input from the second gate line signal terminal; a dual-drive sub-circuit having a first driving terminal coupled to the first node, a second driving terminal coupled to the second node, a drive signal input terminal coupled to a first reference signal terminal, and a drive signal output terminal coupled to a luminescent sub-circuit, and configured to drive the luminescent sub-circuit to emit light based on a voltage level of the first node and a voltage level of the second node.

[0004] In an embodiment of the disclosure, the dual-drive sub-circuit comprises: a dual-gate thin film transistor comprising a first gate electrode, a second gate electrode, a source

electrode, and a drain electrode, wherein the first gate electrode is coupled to the first node, the second gate electrode is coupled to the second node, the source electrode is coupled to the first reference signal terminal, and the drain electrode is coupled to the second reference signal terminal; a first capacitor is coupled between the first node and the drain electrode of the dual-gate thin film transistor; a second capacitor is coupled between the second node and the drain electrode of the dual-gate thin film transistor.

[0005] In an embodiment of the disclosure, the first switch sub-circuit comprises a first thin film transistor; a gate electrode of the first thin film transistor is coupled to the first gate line signal terminal, a source electrode of the first thin film transistor is coupled to the data line signal terminal, a drain electrode of the first thin film transistor is coupled to the first node.

[0006] In an embodiment of the disclosure, the second switch sub-circuit comprises a second thin film transistor; a gate electrode of the second thin film transistor is coupled to the second gate line signal terminal, a source electrode of the second thin film transistor is coupled to the data line signal terminal, a drain electrode of the second thin film transistor is coupled to the second node.

[0007] In an embodiment of the disclosure, the luminescent sub-circuit comprises an organic light-emitting diode (OLED) having a first terminal coupled to the drive signal output terminal of the dual-drive sub-circuit and a second terminal coupled to a second reference signal terminal, the OLED being configured to emit light induced by a driving current provided by the dual-drive sub-circuit.

[0008] In an embodiment of the disclosure, the luminescent sub-circuit comprises an organic light-emitting diode (OLED) having a first terminal coupled to the drive signal input terminal of the dual-drive sub-circuit and a second terminal coupled to a first reference signal terminal, the OLED being configured to emit light induced by a driving current provided by the dual-drive sub-circuit.

[0009] In an embodiment of the disclosure, the first gate line scanning signal input from the first gate line signal terminal is a high level signal to control the data signal provided by the data line signal terminal transmitted to the first node in a first period and the second gate line scanning signal input from the second gate line signal terminal is a high level signal to control the data signal provided by the data line signal terminal transmitted to the second node in a second period, wherein the first period and the second period are time-sequential.

[0010] In one or more optional embodiments, the first period is a first frame and the second period is a second frame.

[0011] Embodiments of the disclosure further provide a driving method of the pixel circuit provided by the embodiment of the disclosure, includes: when the first gate line signal terminal inputs the gate line scanning signal, the first switch sub-circuit transmits a data signal provided by the data line signal terminal to the first node under the controlling of a gate line scanning signal provided by the first gate line signal terminal; the dual-drive sub-circuit drives the luminescent sub-circuit to emit light when a voltage of the first node is a voltage level of the data signal provided by the data line signal terminal; when the second gate line signal terminal inputs the gate line scanning signal, the second switch sub-circuit transmits the data signal provided by the data line signal terminal to the second node, under the controlling of a gate line scanning signal provided by the second gate line signal terminal; the dual-drive sub-circuit drives the luminescent sub-circuit to emit light when a voltage of the second node is the voltage level of the data signal provided by the data line signal terminal.

[0012] In an embodiment of the disclosure, further comprising: alternatively receiving the gate line scanning signal from the first gate line signal terminal and the second gate line signal terminal during a preset first time period.

[0013] In an embodiment of the disclosure, the first switch sub-circuit and the second switch sub-circuit are configured to work alternatively.

[0014] In an embodiment of the disclosure, the first driving terminal and the second driving terminal are configured to work alternatively on two frames separated by a preset time lag.

[0015] Embodiments of the disclosure further provide an electroluminescent panel, the electroluminescent panel a matrix of pixel circuits, each pixel circuit in the matrix comprising: a first switch sub-circuit having a first signal control terminal coupled to a first gate line signal terminal, a first signal input terminal coupled to a data line signal terminal, and a first signal output terminal coupled to a first node, and configured to transmit a data signal provided by the data line signal terminal to the first node under controlling of a first gate line scanning signal input from the first gate line signal terminal; a second switch sub-circuit having a second signal control terminal coupled to a second gate line signal terminal, a second signal input terminal coupled to the data line signal terminal, and a second signal output terminal coupled to a second node, and configured to transmit the data signal provided by the data line signal terminal to the second node under controlling of a second gate line scanning signal input from the second gate line signal terminal; a dual-drive sub-circuit having a first driving terminal coupled to the first node, a second driving terminal

coupled to the second node, a drive signal input terminal coupled to a first reference signal terminal, and a drive signal output terminal coupled to a luminescent sub-circuit, and configured to drive the luminescent sub-circuit to emit light based on a voltage level of the first node and a voltage level of the second node.

[0016] In an embodiment of the disclosure, the dual-drive sub-circuit comprises: a dual-gate thin film transistor comprising a first gate electrode, a second gate electrode, a source electrode, and a drain electrode, wherein the first gate electrode is coupled to the first node, the second gate electrode is coupled to the second node, the source electrode is coupled to the first reference signal terminal, and the drain electrode is coupled to the second reference signal terminal; a first capacitor is connected coupled between the first node and the drain electrode of the dual-gate thin film transistor; a second capacitor is connected coupled between the second node and the drain electrode of the dual-gate thin film transistor.

[0017] In an embodiment of the disclosure, the first switch sub-circuit comprises a first thin film transistor; a gate electrode of the first thin film transistor is coupled to the first gate line signal terminal, a source electrode of the first thin film transistor is coupled to the data line signal terminal, a drain electrode of the first thin film transistor is coupled to the first node.

[0018] In an embodiment of the disclosure, the second switch sub-circuit comprises a second thin film transistor; a gate electrode of the second thin film transistor is coupled to the second gate line signal terminal, a source electrode of the second thin film transistor is coupled to the data line signal terminal, a drain electrode of the second thin film transistor is coupled to the second node.

[0019] In an embodiment of the disclosure, further comprising a controller configured to apply a first high level signal in a first period to the first node via the first gate line signal terminal and apply a second high level signal in a second period to the second node via the second gate line signal terminal, wherein the first period and the second period are time-sequential.

[0020] In an embodiment of the disclosure, the first period is a first frame and the second period is a second frame.

[0021] Embodiments of the disclosure further provide a display device, the electroluminescent panel includes the electroluminescent pane provided by the embodiment of the disclosure. It is to be understood that both the foregoing general description and the following detailed description are exemplary only and are not restrictive of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIG. 1 is a structure diagram of a pixel circuit according to the related art.

[0023] FIG. 2A is a structure diagram of a pixel circuit according to one embodiment of the disclosure.

[0024] FIG. 2B is a structure diagram of a pixel circuit according to another embodiment of the disclosure.

[0025] FIG. 3A is a detail structure diagram of a pixel circuit according to another embodiment of the disclosure.

[0026] FIG. 3B is a detail structure diagram of a pixel circuit according to one embodiment of the disclosure.

[0027] FIG. 4 is a timing sequence diagram when the pixel circuit is working, corresponding to the pixel circuit shown in FIG. 3, according to one embodiment of the disclosure.

[0028] Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions and/or relative positioning of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of various examples of the present disclosure. Also, common but well-understood elements that are useful or necessary in a commercially feasible example are often not depicted in order to facilitate a less obstructed view of these various examples. It will further be appreciated that certain actions and/or steps may be described or depicted in a particular order of occurrence while those skilled in the art will understand that such specificity with respect to sequence is not actually required. It will also be understood that the terms and expressions used herein have the ordinary technical meaning as is accorded to such terms and expressions by persons skilled in the technical field as set forth above, except where different specific meanings have otherwise been set forth herein.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0029] The terminology used in the present disclosure is for the purpose of describing exemplary examples only and is not intended to limit the present disclosure. As used in the present disclosure and the appended claims, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It shall also be understood that the terms “or” and "and/or" used herein are intended to signify and include any or all possible combinations of one or more of the associated listed items, unless the context clearly indicates otherwise.

[0030] It shall be understood that, although the terms “first,” “second,” “third,” etc. may be used herein to describe various information, the information should not be limited by these terms. These terms are only used to distinguish one category of information from another. For example, without departing from the scope of the present disclosure, first information may be termed as second information; and similarly, second information may also be termed as first information. As used herein, the term "if" may be understood to mean "when" or "upon" or "in response to” depending on the context.

[0031] Reference throughout this specification to "one embodiment," "an embodiment," "exemplary embodiment," or the like in the singular or plural means that one or more particular features, structures, or characteristics described in connection with an example is included in at least one embodiment of the present disclosure. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment," "in an exemplary embodiment," or the like in the singular or plural in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics in one or more embodiments may be combined in any suitable manner.

[0032] In general, a basic structure of a typical AMOLED pixel circuit is a 2T1C structure as shown in FIG. 1, which includes two thin film transistors (TFTs) and one capacitor. When the pixel circuit is working, a gate scanning signal Gate1 input from a gate line signal terminal controls a switch thin film transistor T1 to turn on, a data signal Data input from a data line signal terminal is transmitted to a gate electrode of a drive thin film transistor T2 via the switch thin film transistor T1 and charges the capacitor C1. When the drive thin film transistor T2 is turned on, the OLED D is driven to emit light. Furthermore, under the effect of the capacitor, the voltage level of the gate electrode of the drive thin film transistor T2 can be maintained until the next picture is switched, which ensures the pictures are continuous.

[0033] However, because the drive thin film transistor T2 of the pixel circuit is effected at bias voltage status for a long time, a threshold voltage of the drive thin film transistor T2 would be shifted. The threshold shift may make the luminance of the OLED D changes undesirably and may cause various kinds of defect of the display.

[0034] Based on this background, how to suppress the threshold voltage of the drive thin film transistor from shifting, ensure the stability of the luminance of the grayscale, and prevent the occurrence of defect of display, are technical problems need to be resolved.

[0035] The disclosure has following beneficial effects. The disclosure provides a pixel circuit, a driving method thereof, an electroluminescent panel, and a display device. The pixel circuit includes the first switch sub-circuit, the second switch sub-circuit, the luminescent sub-circuit, and the dual-drive sub-circuit. The first driving terminal of the dual-drive sub-circuit is connected to the first node, the second driving terminal of the dual-drive sub-circuit is connected to the second node, the signal input terminal of the dual-drive sub-circuit is connected to the first reference signal terminal, and the signal output terminal of the dual-drive sub-circuit is connected to the first port of the luminescent sub-circuit. The second port of the luminescent sub-circuit is connected to the second reference signal terminal. The dual-drive sub-circuit is used to drive the luminescent sub-circuit to emit light under the controlling of the voltage level of the first node or the second node. Therefore, through improving the pixel circuit, the first driving terminal of the dual-drive sub-circuit connects to the first node, the second driving terminal of the dual-drive sub-circuit connects to the second node, when the first gate line signal terminal and the second gate line signal terminal input the gate line scanning signal alternatively, the first switch sub-circuit and the second switch sub-circuit are working alternatively, cause the first driving terminal and the second driving terminal of the dual-drive sub-circuit are working alternatively, thus to drive the luminescent sub-circuit to emit light. Therefore, through the two driving terminals work alternatively, avoiding the voltage instability due to one driving terminal of the dual-drive sub-circuit works for a long time, ensuring the stability of pixel grayscale luminance, eliminating the defect of display.

[0036] Embodiments of a pixel circuit, a driving method thereof, an electroluminescent panel, and a display device of the disclosure will be described in detail with reference to the accompanying drawings as follows.

[0037] As shown in FIG. 2A and FIG. 2B, the pixel circuit includes: a first switch sub-circuit 10, a second switch sub-circuit 20, a luminescent sub-circuit 30, and a dual-drive sub-circuit 40.

[0038] A signal control terminal of the first switch sub-circuit 10 is connected to a first gate line signal terminal Gate1, a signal input terminal of the first switch sub-circuit 10 is connected to a data line signal terminal (labeled as Data), a signal output terminal of the first switch sub-circuit 10 is connected to a first node P1. The first switch sub-circuit 10 is used to transmit a data signal provided by the data line signal terminal (labeled as Data) to the

first node P1, under the controlling of a gate line scanning signal input from the first gate line signal terminal Gate1.

[0039] A signal control terminal of the second switch sub-circuit 20 is connected to a second gate line signal terminal Gate2, a signal input terminal of the second switch sub-circuit 20 is connected to the data line signal terminal (labeled as Data), a signal output terminal of the second switch sub-circuit 20 is connected to a second node P2. The second switch sub-circuit 20 is used to transmit the data signal provided by the data line signal terminal (labeled as Data) to the second node P2, under the controlling of a gate line scanning signal input from the second gate line signal terminal Gate2.

[0040] As shown in FIG. 2A, a first driving terminal of the dual-drive sub-circuit 40 is connected to the first node P1, a second driving terminal of the dual-drive sub-circuit 40 is connected to the second node P2, a signal input terminal of the dual-drive sub-circuit 40 is connected to a first reference signal terminal VDD, and a signal output terminal of the dual-drive sub-circuit 40 is connected to a first port of the luminescent sub-circuit 30. A second port of the luminescent sub-circuit 30 is connected to a second reference signal terminal GND. The dual-drive sub-circuit 40 is used to drive the luminescent sub-circuit 30 to emit light under the controlling of a voltage level of the first node P1 or the second node P2.

[0041] As shown in FIG. 2B, a first driving terminal of the dual-drive sub-circuit 40 is connected to the first node P1, a second driving terminal of the dual-drive sub-circuit 40 is connected to the second node P2, a signal input terminal of the dual-drive sub-circuit 40 is connected to a first port of the luminescent sub-circuit 30, and a signal output terminal of the dual-drive sub-circuit 40 is connected to a second reference signal terminal GND. A second port of the luminescent sub-circuit 30 is connected to a first reference signal terminal VDD. The dual-drive sub-circuit 40 is used to drive the luminescent sub-circuit 30 to emit light under the controlling of a voltage level of the first node P1 or the second node P2.

[0042] The disclosure provides a new pixel circuit that includes the dual-drive sub-circuit 40. The first driving terminal of the dual-drive sub-circuit 40 connects to the first node P1 while the second driving terminal of the dual-drive sub-circuit 40 connects to the second node P2. When the first gate line signal terminal Gate1 and the second gate line signal terminal Gate2 input the gate line scanning signal alternatively, the first switch sub-circuit 10 and the second switch sub-circuit 20 are working alternatively, which cause the first driving terminal and the second driving terminal of the dual-drive sub-circuit 40 work alternatively to drive

the luminescent sub-circuit 30 to emit light. For example, the first gate line scanning signal input from the first gate line signal terminal Gate1 is a high level signal to control the data signal provided by the data line signal terminal (labeled as Data) transmitted to the first node in a first period and the second gate line scanning signal input from the second gate line signal terminal Gate2 is a high level signal to control the data signal provided by the data line signal terminal transmitted to the second node in a second period, wherein the first period and the second period are time-sequential. For example, the first period is a first frame and the second period is a second frame. For example, the first period is a first frame and the second period is a third frame. Therefore, the threshold voltage shift of the dual-drive sub-circuit 40 is greatly reduced by adopting two driving terminals work alternatively. The new pixel circuit avoids the voltage instability due to one driving terminal of the dual-drive sub-circuit 40 works for a long time, ensures the stability of pixel grayscale luminance, and eliminates the defect of display.

[0043] A detail implementation is provided clearly describe the two driving terminal of the dual-drive sub-circuit 40 how to work alternatively. As shown in FIG. 3A, the dual-drive sub-circuit 40 includes: a dual-gate thin film transistor Td, a first capacitor C1, and a second capacitor C2. The luminescent sub-circuit comprises an organic light-emitting diode (OLED) having a first terminal coupled to the drive signal output terminal of the dual-drive sub-circuit and a second terminal coupled to a second reference signal terminal GND, the OLED D being configured to emit light induced by a driving current provided by the dual-drive sub-circuit. For example, the first terminal of the OLED D is an anode and the second terminal of the OLED D is a cathode. As shown in FIG. 3B, The luminescent sub-circuit comprises an organic light-emitting diode (OLED) having a first terminal coupled to the drive signal input terminal of the dual-drive sub-circuit and a second terminal coupled to a first reference signal terminal VDD, the OLED D being configured to emit light induced by a driving current provided by the dual-drive sub-circuit. For example, the first terminal of the OLED D is a cathode and the second terminal of the OLED D is an anode.

[0044] As shown in FIG. 3A, a first gate electrode of the dual-gate thin film transistor Td is connected to the first node P1, a second gate electrode of the dual-gate thin film transistor Td is connected to the second node P2, a source electrode of the dual-gate thin film transistor Td is connected to the first reference signal terminal VDD, and a drain electrode of the dual-gate thin film transistor Td is connected to the anode of the OLED D.

[0045] The first capacitor C1 is connected between the first node P1 and the anode of the OLED D.

[0046] The second capacitor C2 is connected between the second node P2 and the anode of the OLED D.

[0047] As shown in FIG. 3B, a first gate electrode of the dual-gate thin film transistor Td is connected to the first node P1, a second gate electrode of the dual-gate thin film transistor Td is connected to the second node P2, a source electrode of the dual-gate thin film transistor Td is connected to the cathode of the OLED D, and a drain electrode of the dual-gate thin film transistor Td is connected to the second reference signal terminal GND, the anode of the OLED D is connected to the first reference signal terminal VDD.

[0048] The first capacitor C1 is connected between the first node P1 and the second reference terminal GND.

[0049] The second capacitor C2 is connected between the second node P2 and the second reference terminal GND.

[0050] In detail, the working principle of the dual-gate thin film transistor Td to suppress the threshold voltage to shift, can be described in combine with a threshold voltage shift experience formula as shown in below:

[0051] $\triangle V_{th} \propto |V_{gate}|^{\beta} t^{\gamma}$.

[0052] Therein, $\triangle V_{th}$ represents a shift value of the threshold voltage, V_{gate} represents the voltage of the gate electrode, t represents time, β and γ represent constant related to the character of the thin film transistor itself.

[0053] In the pixel circuit provided in the embodiment of the disclosure, take the first gate electrode of the dual-gate thin film transistor Td is working in a first frame and the second gate electrode of the dual-gate thin film transistor Td is working in a second frame adjacent to the first frame as example. The threshold voltage shift value of the first gate electrode of the dual-gate thin film transistor Td is equal to $k1 \times |V_{data1}|^{\beta 1} t^{\gamma 1}$, K1 is a constant. The threshold voltage shift value of the second gate electrode of the dual-gate thin film transistor Td is equal to $k2 \times |V_{data1}|^{\beta 1} t^{\gamma 1}$, K2 is a constant. A bias voltage of the first gate electrode in the first frame and a bias voltage of the second gate electrode in the second frame produce opposite effect to the channel of the thin film transistor, therefore, after two frame signals are applied completely, the threshold voltage shift value is $k1 \times |V_{data1}|^{\beta 1} t^{\gamma 1} - k2 \times |V_{data2}|^{\beta 2} t^{\gamma 2}$. In detail, the parameters β and γ can be adjusted to consistent with

each other, namely data1 is equal to data2, via manufacturing technology for manufacturing the thin film transistor, thus to make the threshold voltage shift value near to zero after the two frame signals are applied completely. Thus achieving the threshold voltage shift value of a couple of odd-even frames to be counteracted due to the first gate electrode and second gate electrode work alternatively, and avoiding the luminance to be changed due to the electrical property of the thin film transistor is changed.

[0054] Of course, the first gate electrode and second gate electrode work alternatively, are not limited in two consecutive frames, the first gate electrode and second gate electrode can work alternatively in two frames that are not adjacent, which are not limited by the examples in the disclosure.

[0055] In detail, the data signal provided by the data line signal terminal (labeled as Data) is a high level signal, the dual-gate thin film transistor Td is a N-type (N-channel) thin film transistor; or, the data signal provided by the data line signal terminal (labeled as Data) is a low level signal, the dual-gate thin film transistor Td is a P-type (P-channel) thin film transistor.

[0056] The detail structure of the dual-drive sub-circuit 40 as described above is just an example, when in implementation, the structure of the dual-drive sub-circuit 40 is not limited to the above structure of the example, and can be other structures known by the persons in related technical field.

[0057] The first reference signal terminal is a high level terminal, and the voltage of it can be voltage VDD, the second reference signal terminal is a low level terminal, and the voltage of it can be grounded voltage GND or VSS. Therein, VDD>GND>VSS.

[0058] In one implementation, in the pixel circuit provided in the embodiment of the disclosure, as shown in FIG. 3A and FIG. 3B, the first switch sub-circuit 10 may include a first thin film transistor T1.

[0059] A gate electrode of the first thin film transistor T1 is connected to the first gate line signal terminal Gate1, a source electrode of the first thin film transistor T1 is connected to the data line signal terminal (labeled as Data), a drain electrode of the first thin film transistor T1 is connected to the first node P1.

[0060] In one or more embodiments, the first thin film transistor T1 can transmit the data signal provided by the data line signal terminal (labeled as Data) to the first node P1, under the controlling of the gate line scanning signal input from the first gate line signal terminal Gate1.

[0061] Furthermore, the gate line scanning signal input from the first gate line signal terminal Gate1 is the high level signal, the first thin film transistor T1 is N-type thin film transistor; or, the gate line scanning signal input from the first gate line signal terminal Gate1 is the low level signal, the first thin film transistor T1 is P-type thin film transistor.

[0062] The detail structure of the first switch sub-circuit 10 as described above is just an example, the structure of the first switch sub-circuit 10 is not limited to the above structure of the example, and can be other structures known by a person having ordinary skill in related technical field.

[0063] In one implementation, in the pixel circuit provided in the embodiment of the disclosure, as shown in FIG. 3A and FIG. 3B, the second switch sub-circuit 20 may include a second thin film transistor T2.

[0064] A gate electrode of the second thin film transistor T2 is connected to the second gate line signal terminal Gate2, a source electrode of the second thin film transistor T2 is connected to the data line signal terminal (labeled as Data), a drain electrode of the second thin film transistor T2 is connected to the second node P2.

[0065] In one or more embodiments, the second thin film transistor T2 may transmit the data signal provided by the data line signal terminal (labeled as Data) to the second node P2, under the controlling of the gate line scanning signal input from the second gate line signal terminal Gate2.

[0066] Furthermore, the gate line scanning signal input from the second gate line signal terminal Gate2 is the high level signal when the second thin film transistor T2 is N-type thin film transistor. Alternatively, the gate line scanning signal input from the second gate line signal terminal Gate2 is the low level signal when the second thin film transistor T2 is P-type thin film transistor.

[0067] The detail structure of the second switch sub-circuit 20 as described above is just an example, the structure of the second switch sub-circuit 20 is not limited to the above structure of the example, and can be other structures known by the persons in related technical field.

[0068] Of course, the transistors referred in the above pixel circuit of the embodiment of the disclosure are not limited to thin film transistors, the transistors also can be metal-oxide-semiconductor field effect transistor (MOSFET). And the manufacturing technology of the source electrode and drain electrode of each thin film transistor (include the first thin film transistor, the second thin film transistor, and the dual-gate thin film

transistor Td) can be the same, and the name of the source electrode and drain electrode of each thin film transistor described above can be interchanged, namely the name of the source electrode and drain electrode of each thin film transistor can be changed according to the voltage direction for the thin film transistor.

[0069] In detail, in order to achieve light emitting function, in the pixel circuit provided in the disclosure, as shown in FIG. 3A and FIG. 3B, the luminescent sub-circuit 30 may include organic light emitting diode (OLED) D.

[0070] As shown in FIG. 3A, a first terminal of the OLED D is connected to the signal output terminal of the dual-gate thin film transistor Td, a second terminal of the OLED D is connected to the second reference signal terminal GND.

[0071] Of course, although the OLED D referred in the pixel circuit provided in the embodiment of the disclosure is active matrix electroluminescent component, the OLED D may be replaced by quantum light emitting diode (QLED) or other type of light emitting diode.

[0072] It is necessary to note that, the improvements of the pixel circuit provided by the embodiment of the disclosure, are not limited to the structure shown in FIG. 3A and FIG. 3B, the pixel circuit may be implemented with other structures, which are not limited in the disclosure.

[0073] The working process of the above pixel circuit provided in the disclosure is described below, in combination with the pixel circuit as shown in FIG.3A and working timing sequence diagram of the pixel circuit as shown in FIG. 4.

[0074] FIG. 4 is a timing sequence diagram of the pixel circuit provided in the one or more embodiments of the disclosure, where each frame of two consecutive frames is divided to two phases. The pixel circuit as shown in FIG. 3A, take each thin film transistor is N-type thin film transistor, the voltage of the first reference signal terminal is grounded voltage GND, and the voltage of the second reference signal terminal is VDD as example.

[0075] In the first phase as marked by t1, the first gate line signal terminal Gate1 inputs the gate line scanning signal, the first thin film transistor T1 is turned on and transmits the data signal VData1 provided by the data line signal terminal (labeled as Data) to the first node P1, and charges the first capacitor C1 simultaneously. At this time, the first gate electrode of the dual-gate thin film transistor Td is turned on and maintains the voltage of the cathode of the OLED D at low level, because the voltage of the anode of the OLED D is high level, thus driving the OLED D to emit light.

[0076] In the second phase as marked by t2, the first gate line signal terminal Gate1 stops inputting the gate line scanning signal, the first thin film transistor T1 is turned off, at this time, the first capacitor C1 is discharged, the first gate electrode of the dual-gate thin film transistor Td is turned on continuously, and maintains the voltage of the cathode of the OLED D at low level continuously, thus driving the OLED D to emit light continuously.

[0077] In the third phase as marked by t3, the second gate line signal terminal Gate2 inputs the gate line scanning signal, the second thin film transistor T2 is turned on and transmits the data signal VData2 provided by the data line signal terminal (labeled as Data) to the second node P2, and charges the second capacitor C2 simultaneously. At this time, the second gate electrode of the dual-gate thin film transistor Td is turned on and causes the voltage of the cathode of the OLED D at low level, thus driving the OLED D to emit light.

[0078] In the fourth phase as marked by t4, the second gate line signal terminal Gate2 stops inputting the gate line scanning signal, the second thin film transistor T2 is turned off, at this time, the second capacitor C2 is discharged. At this time, the second gate electrode of the dual-gate thin film transistor Td is turned on continuously, and maintains the voltage of the cathode of the OLED D at low level continuously, thus driving the OLED D to emit light continuously.

[0079] The above four phases may repeat themselves. The first two phases t1 and t2 may constitute a first frame. The last two phases t3 and t4 may constitute a second frame. The first two phases t1 and t2 may not be directly adjacent to the last two phases t3 and t4. In other words, the two frames may not be next to each other. For example, the first two phases t1 and t2 may constitute a first frame, the last two phases t3 and t4 may constitute a third frame.

[0080] When the next t1 phase comes, namely the first gate line signal terminal Gate1 inputs the gate line scanning signal again, the first thin film transistor T1 is turned on and the second thin film transistor T2 is turned off. Therefore, the dual-drive sub-circuit utilizes the first thin film transistor T1 and the second thin film transistor T2 to work alternatively. Accordingly, the first gate electrode and the second gate electrode of the dual-gate thin film transistor Td are caused to work alternatively, which avoids the threshold voltage to shift due to one gate electrode works for a long time. Therefore, the dual-drive sub-circuit ensures the stability of pixel grayscale luminance and eliminates the potential defect of display caused by threshold voltage shift.

[0081] Based on the same conception, the embodiments of the disclosure further provide a driving method for the above pixel circuit provided by the disclosure, the driving method may include:

[0082] When the first gate line signal terminal inputs the gate line scanning signal, the first switch sub-circuit transmits data signal provided by the data line signal terminal to the first node, under the controlling of gate line scanning signal provided by the first gate line signal terminal; the dual-gate thin film transistor drives the luminescent sub-circuit to emit light when the voltage of the first node is the voltage level of the data signal provided by the data line signal terminal.

[0083] When the second gate line signal terminal inputs the gate line scanning signal, the second switch sub-circuit transmits data signal provided by the data line signal terminal to the second node, under the controlling of gate line scanning signal provided by the second gate line signal terminal; the dual-gate thin film transistor drives the luminescent sub-circuit to emit light when the voltage of the second node is the voltage level of the data signal provided by the data line signal terminal.

[0084] Based on the same conception, the embodiments of the disclosure further provides a electroluminescent panel, the electroluminescent panel can include at least one pixel circuit provided by at least embodiments of the disclosure. The embodiments of the electroluminescent panel can refer to descriptions of the pixel circuit of the embodiments of the disclosure, here does not describe again.

[0085] Embodiments of the disclosure further provide an electroluminescent panel, the electroluminescent panel a matrix of pixel circuits, each pixel circuit in the matrix comprising: a first switch sub-circuit having a first signal control terminal coupled to a first gate line signal terminal, a first signal input terminal coupled to a data line signal terminal, and a first signal output terminal coupled to a first node, and configured to transmit a data signal provided by the data line signal terminal to the first node under controlling of a first gate line scanning signal input from the first gate line signal terminal; a second switch sub-circuit having a second signal control terminal coupled to a second gate line signal terminal, a second signal input terminal coupled to the data line signal terminal, and a second signal output terminal coupled to a second node, and configured to transmit the data signal provided by the data line signal terminal to the second node under controlling of a second gate line scanning signal input from the second gate line signal terminal; a dual-drive sub-circuit having a first driving terminal coupled to the first node, a second driving terminal

coupled to the second node, a drive signal input terminal coupled to a first reference signal terminal, and a drive signal output terminal coupled to a luminescent sub-circuit, and configured to drive the luminescent sub-circuit to emit light based on a voltage level of the first node and a voltage level of the second node.

[0086] In an embodiment of the disclosure, the dual-drive sub-circuit comprises: a dual-gate thin film transistor comprising a first gate electrode, a second gate electrode, a source electrode, and a drain electrode, wherein the first gate electrode is coupled to the first node, the second gate electrode is coupled to the second node, the source electrode is coupled to the first reference signal terminal, and the drain electrode is coupled to the second reference signal terminal; a first capacitor is connected coupled between the first node and the drain electrode of the dual-gate thin film transistor; a second capacitor is connected coupled between the second node and the drain electrode of the dual-gate thin film transistor.

[0087] In an embodiment of the disclosure, the first switch sub-circuit comprises a first thin film transistor; a gate electrode of the first thin film transistor is coupled to the first gate line signal terminal, a source electrode of the first thin film transistor is coupled to the data line signal terminal, a drain electrode of the first thin film transistor is coupled to the first node.

[0088] In an embodiment of the disclosure, the second switch sub-circuit comprises a second thin film transistor; a gate electrode of the second thin film transistor is coupled to the second gate line signal terminal, a source electrode of the second thin film transistor is coupled to the data line signal terminal, a drain electrode of the second thin film transistor is coupled to the second node.

[0089] In an embodiment of the disclosure, further comprising a controller configured to apply a first high level signal in a first period to the first node via the first gate line signal terminal and apply a second high level signal in a second period to the second node via the second gate line signal terminal, wherein the first period and the second period are time-sequential.

[0090] In an embodiment of the disclosure, the first period is a first frame and the second period is a second frame.

[0091] The embodiments of the disclosure further provides a display device, the display device can include the electroluminescent panel provided in the disclosure. The display device can be a mobile phone, a tablet computer, a television, a monitor, a portable computer, a digital camera, a navigator, and any devices and components including display

function. The embodiments of the display device can refer to descriptions of the electroluminescent panel of the disclosure, here does not describe again.

[0092] The embodiment of the disclosure provides a novel pixel circuit, a novel driving method thereof, an electroluminescent panel, and a display device. The pixel circuit includes the first switch sub-circuit, the second switch sub-circuit, the luminescent sub-circuit, and the dual-drive sub-circuit. The first driving terminal of the dual-drive sub-circuit is connected to the first node, the second driving terminal of the dual-drive sub-circuit is connected to the second node, the signal input terminal of the dual-drive sub-circuit is connected to the first reference signal terminal VDD, and the signal output terminal of the dual-drive sub-circuit is connected to the first port of the luminescent sub-circuit. The second port of the luminescent sub-circuit is connected to the second reference signal terminal. The dual-drive sub-circuit is used to drive the luminescent sub-circuit to emit light under the controlling of voltage level of the first node or the second node. Therefore, through improving the pixel circuit, the first driving terminal of the dual-drive sub-circuit connects to the first node, the second driving terminal of the dual-drive sub-circuit connects to the second node, when the first gate line signal terminal and the second gate line signal terminal input the gate line scanning signal alternatively, the first switch sub-circuit and the second switch sub-circuit are working alternatively, cause the first driving terminal and the second driving terminal of the dual-drive sub-circuit are working alternatively, thus to drive the luminescent sub-circuit to emit light. Therefore, through the two driving terminals work alternatively, avoiding the voltage instability due to one driving terminal of the dual-drive sub-circuit works for a long time, ensuring the stability of pixel grayscale luminance, eliminating the defect of display.

[0093] The disclosed above is merely example embodiments of the disclosure, which does not limit the protection scope of the disclosure. Equivalent modification within the spirit of the claims of the disclosure should be covered by the protected scope of the disclosure.

WHAT IS CLAIMED IS:

1. A pixel circuit in a luminescent panel, comprising:

a first switch sub-circuit having a first signal control terminal coupled to a first gate line signal terminal, a first signal input terminal coupled to a data line signal terminal, and a first signal output terminal coupled to a first node, and configured to transmit a data signal provided by the data line signal terminal to the first node under controlling of a first gate line scanning signal input from the first gate line signal terminal;

a second switch sub-circuit having a second signal control terminal coupled to a second gate line signal terminal, a second signal input terminal coupled to the data line signal terminal, and a second signal output terminal coupled to a second node, and configured to transmit the data signal provided by the data line signal terminal to the second node under controlling of a second gate line scanning signal input from the second gate line signal terminal;

a dual-drive sub-circuit having a first driving terminal coupled to the first node, a second driving terminal coupled to the second node, a drive signal input terminal coupled to a first reference signal terminal, and a drive signal output terminal coupled to a luminescent sub-circuit, and configured to drive the luminescent sub-circuit to emit light based on a voltage level of the first node and a voltage level of the second node.

2. The pixel circuit according to claim 2, wherein the dual-drive sub-circuit comprises:

a dual-gate thin film transistor comprising a first gate electrode, a second gate electrode, a source electrode, and a drain electrode, wherein the first gate electrode is coupled to the first node, the second gate electrode is coupled to the second node, the source electrode is coupled to the first reference signal terminal, and the drain electrode is coupled to the second reference signal terminal;

a first capacitor is coupled between the first node and the drain electrode of the dual-gate thin film transistor;

a second capacitor is coupled between the second node and the drain electrode of the dual-gate thin film transistor.

3. The pixel circuit according to claim 1, wherein the first switch sub-circuit comprises a first thin film transistor;

a gate electrode of the first thin film transistor is coupled to the first gate line signal terminal, a source electrode of the first thin film transistor is coupled to the data line signal terminal, a drain electrode of the first thin film transistor is coupled to the first node.

4. The pixel circuit according to claim 1, wherein the second switch sub-circuit comprises a second thin film transistor;

a gate electrode of the second thin film transistor is coupled to the second gate line signal terminal, a source electrode of the second thin film transistor is coupled to the data line signal terminal, a drain electrode of the second thin film transistor is coupled to the second node.

5. The pixel circuit of claim 1, wherein the luminescent sub-circuit comprises an organic light-emitting diode (OLED) having a first terminal coupled to the drive signal output terminal of the dual-drive sub-circuit and a second terminal coupled to a second reference signal terminal, the OLED being configured to emit light induced by a driving current provided by the dual-drive sub-circuit.

6. The pixel circuit of claim 1, wherein the luminescent sub-circuit comprises an organic light-emitting diode (OLED) having a first terminal coupled to the drive signal input terminal of the dual-drive sub-circuit and a second terminal coupled to a first reference signal terminal, the OLED being configured to emit light induced by a driving current provided by the dual-drive sub-circuit.

7. The pixel circuit according to claim 1, wherein the first gate line scanning signal input from the first gate line signal terminal is a high level signal to control the data signal provided by the data line signal terminal transmitted to the first node in a first period and the second gate line scanning signal input from the second gate line signal terminal is a high level signal to control the data signal provided by the data line signal terminal transmitted to the second node in a second period,

wherein the first period and the second period are time-sequential.

8. The pixel circuit according to claim 7, wherein the first period is a first frame and the second period is a second frame.

9. An electroluminescent panel comprising a matrix of pixel circuits, each pixel circuit in the matrix comprising:

a first switch sub-circuit having a first signal control terminal coupled to a first gate line signal terminal, a first signal input terminal coupled to a data line signal terminal, and a first signal output terminal coupled to a first node, and configured to transmit a data signal provided by the data line signal terminal to the first node under controlling of a first gate line scanning signal input from the first gate line signal terminal;

a second switch sub-circuit having a second signal control terminal coupled to a second gate line signal terminal, a second signal input terminal coupled to the data line signal terminal, and a second signal output terminal coupled to a second node, and configured to transmit the data signal provided by the data line signal terminal to the second node under controlling of a second gate line scanning signal input from the second gate line signal terminal;

a dual-drive sub-circuit having a first driving terminal coupled to the first node, a second driving terminal coupled to the second node, a drive signal input terminal coupled to a first reference signal terminal, and a drive signal output terminal coupled to a luminescent sub-circuit, and configured to drive the luminescent sub-circuit to emit light based on a voltage level of the first node and a voltage level of the second node.

10. The electroluminescent panel according to claim 9, wherein the dual-drive sub-circuit comprises:

a dual-gate thin film transistor comprising a first gate electrode, a second gate electrode, a source electrode, and a drain electrode, wherein the first gate electrode is coupled to the first node, the second gate electrode is coupled to the second node, the source electrode is coupled to the first reference signal terminal, and the drain electrode is coupled to the second reference signal terminal;

a first capacitor is connected coupled between the first node and the drain electrode of the dual-gate thin film transistor;

a second capacitor is connected coupled between the second node and the drain electrode of the dual-gate thin film transistor.

11. The electroluminescent panel according to claim 9, wherein the first switch

sub-circuit comprises a first thin film transistor;

a gate electrode of the first thin film transistor is coupled to the first gate line signal terminal, a source electrode of the first thin film transistor is coupled to the data line signal terminal, a drain electrode of the first thin film transistor is coupled to the first node.

12. The electroluminescent panel according to claim 9, wherein the second switch sub-circuit comprises a second thin film transistor;

a gate electrode of the second thin film transistor is coupled to the second gate line signal terminal, a source electrode of the second thin film transistor is coupled to the data line signal terminal, a drain electrode of the second thin film transistor is coupled to the second node.

13. The electroluminescent panel according to claim 9, further comprising a controller configured to apply a first high level signal in a first period to the first node via the first gate line signal terminal and apply a second high level signal in a second period to the second node via the second gate line signal terminal,

wherein the first period and the second period are time-sequential.

14. The electroluminescent panel according to claim 13, wherein the first period is a first frame and the second period is a second frame.

15. A driving method for driving the pixel circuit according to any one of claims 1-8, comprising:

when the first gate line signal terminal inputs a first gate line scanning signal, transmitting, by the first switch sub-circuit, a data signal provided by the data line signal terminal to the first node under the controlling of the first gate line scanning signal provided by the first gate line signal terminal;

wherein the dual-drive sub-circuit drives the luminescent sub-circuit to emit light when a voltage of the first node is a voltage level of the data signal provided by the data line signal terminal;

when the second gate line signal terminal inputs a second gate line scanning signal, transmitting, by the second switch sub-circuit, the data signal provided by the data line signal terminal to the second node, under the controlling of the gate line scanning signal

provided by the second gate line signal terminal;

wherein the dual-drive sub-circuit drives the luminescent sub-circuit to emit light when a voltage of the second node is the voltage level of the data signal provided by the data line signal terminal.

16. The driving method according to claim 15, further comprising:

alternatively receiving the gate line scanning signal from the first gate line signal terminal and the second gate line signal terminal during a preset first time period.

17. The driving method according to claim 15, wherein the first switch sub-circuit and the second switch sub-circuit are configured to work alternatively.

18. The driving method according to claim 15, wherein the first driving terminal and the second driving terminal are configured to work alternatively on two frames separated by a preset time lag.

19. A display device, wherein the display device comprises the electroluminescent panel according to any one of claims 9-14.

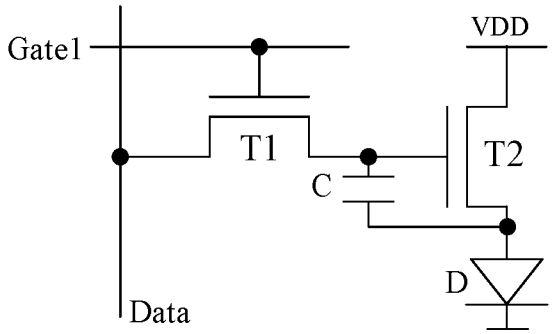

FIG. 1 (Related Art)

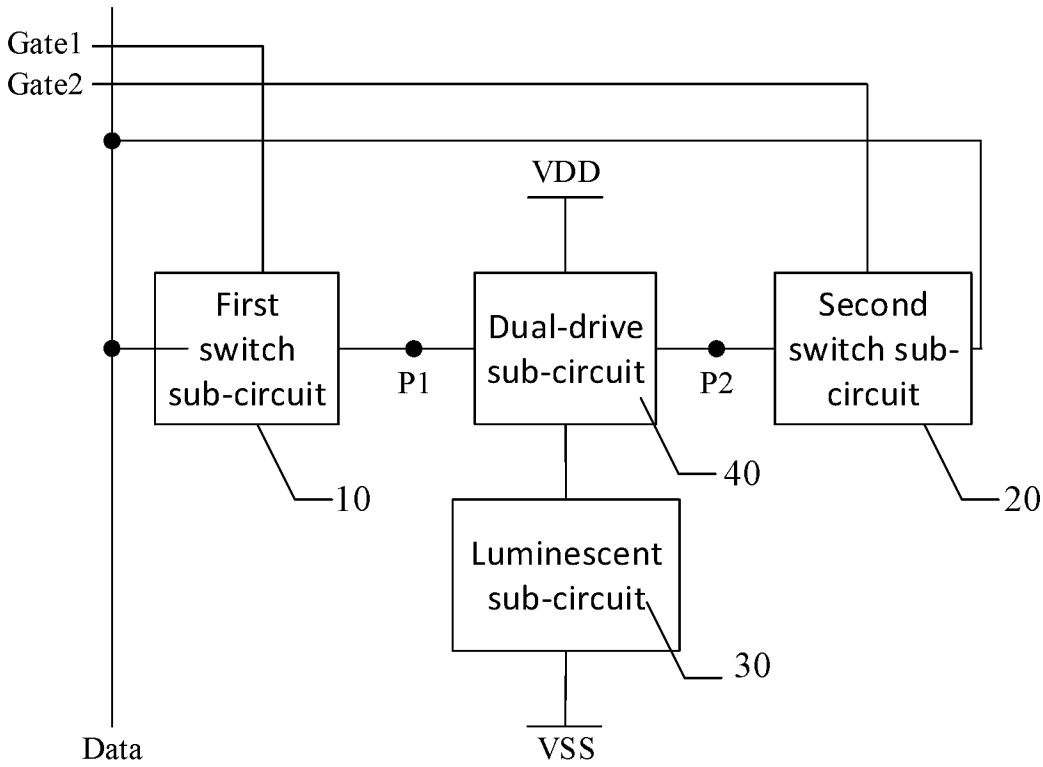

FIG. 2A

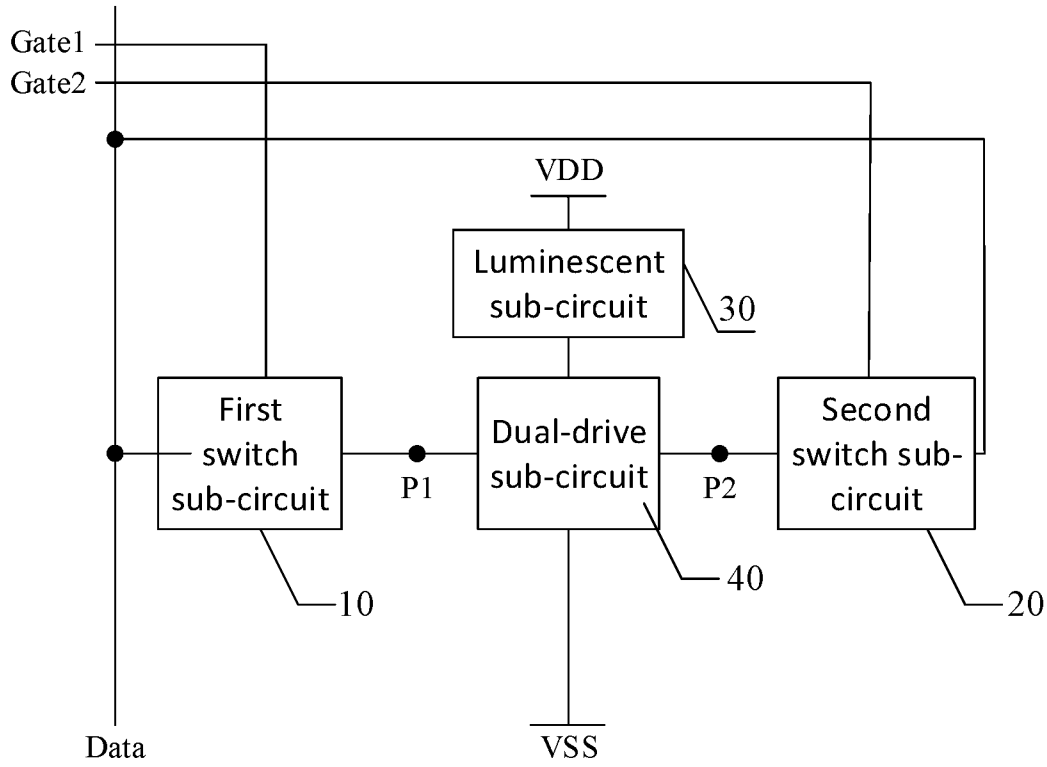
Gate1
Gate2
VDD
Luminescent sub-circuit
30
First switch sub-circuit
P1
Dual-drive sub-circuit
P2
Second switch sub-circuit
10
40
20
Data
VSS

FIG. 2B

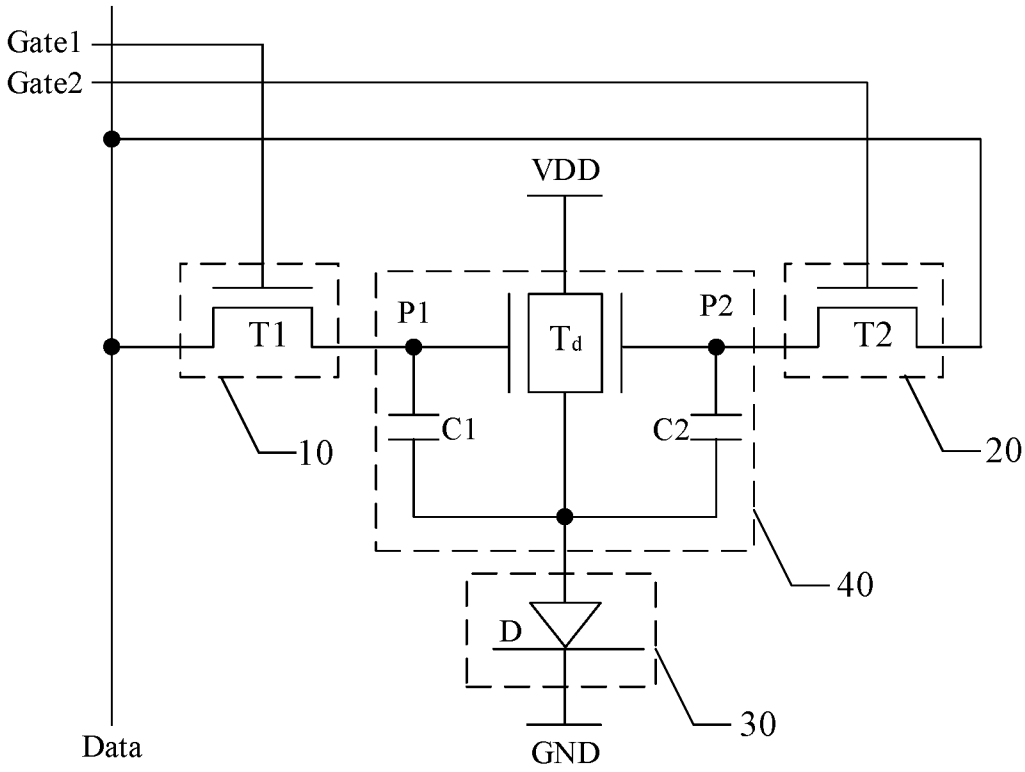

FIG. 3A

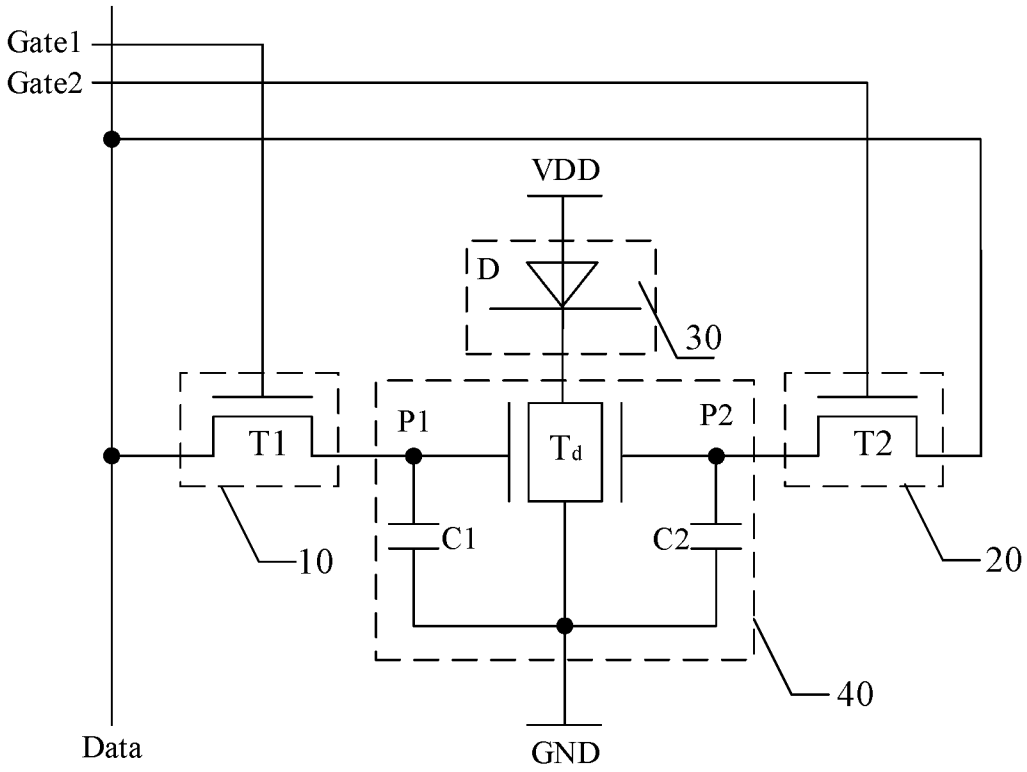
Gate1
Gate2
VDD
D
30
T1
P1
Td
P2
T2
10
C1
C2
20
40
Data
GND

FIG. 3B

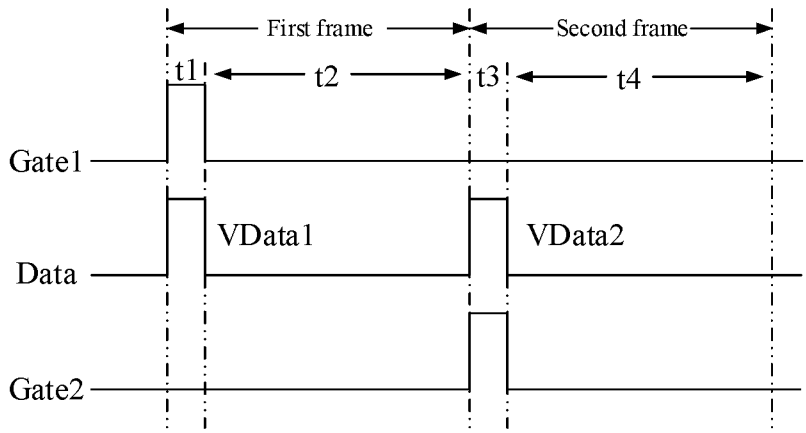
First frame
Second frame
t1
t2
t3
t4
Gate1
VData1
VData2
Data
Gate2

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/115082

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/20(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: pixel, circuit, driv???, alternat+, display, dual, emit, light, OLED, by turn?, first, second, current

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 106097959 A (BOE TECHNOLOGY GROUP CO., LTD.) 09 November 2016 (2016-11-09) description, paragraphs [0084]-[0086], [0090], figure 10	1-19
X	CN 101937647 A (UNIV. SHANGHAI JIAOTONG) 05 January 2011 (2011-01-05) description, paragraphs [0023]-[0033], figures 1-3	1-19
X	CN 1742308 A (KONINKL PHILIPS ELECTRONICS N.V.) 01 March 2006 (2006-03-01) description, page 8 to the paragraph 4 of page 10, figures 3-10	1-19
X	CN 103927991 A (HE, DONGYANG) 16 July 2014 (2014-07-16) description, paragraphs [0011]-[0016], figure 2	1-19
X	CN 104050927 A (HE, DONGYANG) 17 September 2014 (2014-09-17) description, paragraphs [0011]-[0016], figure 2	1-19
X	US 2006012587 A1 (STEVENSON, MATTHEW ET AL.) 19 January 2006 (2006-01-19) description, paragraph [0112], figure 10	1-19

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 February 2018	**05 March 2018**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**CHU,Xiaohui**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)53962577**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2017/115082

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	106097959	A	09 November 2016	None			
CN	101937647	A	05 January 2011	CN	101937647	B	05 September 2012
CN	1742308	A	01 March 2006	US	2006097965	A1	11 May 2006
				TW	200418074	A	16 September 2004
				KR	20050101183	A	20 October 2005
				JP	2006518473	A	10 August 2006
				EP	1590786	A1	02 November 2005
				GB	0301623	D0	26 February 2003
				US	8130173	B2	06 March 2012
				WO	2004066250	A1	05 August 2004
CN	103927991	A	16 July 2014	None			
CN	104050927	A	17 September 2014	None			
US	2006012587	A1	19 January 2006	US	7397448	B2	08 July 2008