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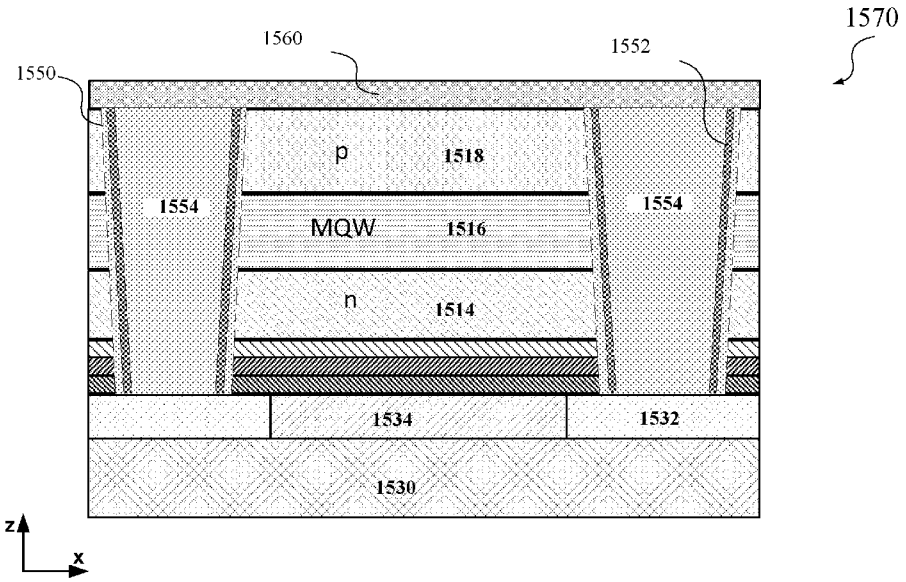

FIG. 15G

(57) Abstract: A common-anode micro-LED device includes an array of micro light-emitting diodes (micro-LEDs) characterized by a pitch less than 20 mm and including a first common anode for the first array of micro-LEDs, and a backplane wafer including pixel drive circuits configured to individually address micro-LEDs of the array of micro-LEDs through cathodes of the micro-LEDs. Each pixel drive circuit of the pixel drive circuits includes an analog current drive circuit connected to a cathode of a micro-LED of the first array of micro-LEDs, a storage circuit for storing pixel data, and a timing control circuit configured to control the analog current drive circuit based on the pixel data.

[Continued on next page]

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COMMON ANODE MICRO-LED SYSTEM ARCHITECTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of and priority to U.S. Provisional Application No. 63/306,817, filed February 4, 2022, entitled "COMMON ANODE MICRO-LED SYSTEM ARCHITECTURE,".

FIELD OF THE INVENTION

[0001] The present disclosure relates generally to micro-light emitting diodes (micro-LEDs). More specifically, this disclosure relates to common-anode micro-LED display devices and methods of fabricating the common-anode micro-LED display devices. Various inventive embodiments are described herein, including devices, systems, circuits, methods, processes, materials, and the like.

BACKGROUND

[0002] Light emitting diodes (LEDs) convert electrical energy into optical energy, and offer many benefits over other light sources, such as reduced size, improved durability, and increased efficiency. LEDs can be used as light sources in many display systems, such as televisions, computer monitors, laptop computers, tablets, smartphones, projection systems, and wearable electronic devices. Micro-LEDs ("μLEDs") based on III-V semiconductors, such as alloys of AlN, GaN, InN, AlGaInP, other ternary and quaternary nitride, phosphide, and arsenide compositions, and the like, have begun to be developed for various display applications due to their small size (e.g., with a linear dimension less than 100 μm, less than 50 μm, less than 10 μm, or less than 5 μm), high packing density (and hence higher resolution), and high brightness. For example, micro-LEDs that emit light of different colors (e.g., red, green, and blue) can be used to form the sub-pixels of a display system, such as a television or a near-eye display system.

SUMMARY

[0003] In accordance with a first aspect of the present disclosure, there is provided a display device comprising a first array of micro light-emitting diodes (micro-LEDs) characterized by a pitch less than 20 μm and including a first common anode for the first array of micro-LEDs; and a backplane wafer including pixel drive circuits configured to individually address micro-LEDs of the first array of micro-LEDs through cathodes of the micro-LEDs, each pixel drive circuit of the pixel drive circuits including an analog current drive circuit connected to a cathode of a micro-LED of the first array of micro-LEDs, a storage circuit for storing pixel data, and a timing control circuit configured to control the

analog current drive circuit based on the pixel data.

[0004] In some embodiments, each micro-LED of the first array of micro-LEDs includes a mesa structure that includes a reflector layer electrically coupled to the cathode of the micro-LED, an n-type semiconductor layer coupled to the reflector layer, an active region on the n-type semiconductor layer, and at least a portion of a p-type semiconductor layer on the active region. In some embodiments, the first common anode includes a transparent conductive layer on the p-type semiconductor layer. In some embodiments, the first common anode includes a metal layer in regions surrounding mesa structures of the first array of micro-LEDs, and the first array of micro-LEDs includes a plurality of p-contacts coupling the metal layer to the p-type semiconductor layer at a plurality of locations between the mesa structures of the first array of micro-LEDs. In some embodiments, the metal layer is on sidewalls of the mesa structures of the first array of micro-LEDs and regions between the mesa structures of the first array of micro-LEDs. In some embodiments, the active region includes GaN-based semiconductor materials or phosphide-based semiconductor materials.

[0005] In some embodiments, the cathode of the micro-LED is bonded to the backplane wafer. In some embodiments, the backplane wafer includes a first voltage regulator configured to output a first positive supply voltage to the timing control circuit, and a second voltage regulator configured to output a second positive supply voltage to the first common anode of the first array of micro-LEDs. In some embodiments, the first array of micro-LEDs is configured to emit light in a first wavelength range, the display device includes a second array of micro-LEDs that includes a second common anode and is configured to emit light in a second wavelength range, and the backplane wafer further includes a third voltage regulator configured to output a third positive supply voltage to the second common anode of the second array of micro-LEDs.

[0006] In some embodiments, the timing control circuit includes a pulse-width modulation (PWM) latch configured to generate PWM signals for controlling the analog current drive circuit, and a comparator configured to compare the pixel data with a counter value and generate a control signal to control the PWM latch. In some embodiments, the analog current drive circuit is on a indium-gallium-zinc-oxide (IGZO) layer. In some embodiments, the backplane wafer includes a common control circuit shared by two or more micro-LED of the first array of micro-LEDs. In some embodiments, the storage circuit for storing pixel data includes an analog data storage circuit, a digital data storage circuit, or a combination. In some embodiments, a pitch of the pixel drive circuits matches the pitch of the first array of micro-LEDs.

[0007] In accordance with a second aspect of the present disclosure, there is provided a display device comprising an array of pixels characterized by a pitch less than 20 μm, each pixel of the array of pixels comprising: a micro light-emitting diode (micro-LED) and a pixel drive circuit electrically connected to the micro-LED. The pixel drive circuit comprising an analog current drive circuit connected to a cathode of the micro-LED, a storage circuit for storing pixel data, and a timing control circuit configured to control the analog current drive circuit based on the pixel data, wherein anodes of micro-LEDs of the array of pixels are electrically shorted.

[0008] In some embodiments, the anodes of the micro-LEDs of the array of pixels are connected to a transparent conductive layer. In some embodiments, the anodes of the micro-LEDs of the array of pixels are connected to a metal layer in regions between the array of pixels. In some embodiments, the micro-LED includes GaN-based semiconductor materials or phosphide-based semiconductor materials. In some embodiments, the display device further comprises: a first voltage regulator configured to output a first positive supply voltage to the timing control circuit, and a second voltage regulator configured to output a second positive supply voltage to the anodes of the micro-LEDs of the array of pixels. In some embodiments, the timing control circuit includes a pulse-width modulation (PWM) latch configured to generate PWM signals for controlling the analog current drive circuit, and a comparator configured to compare the pixel data with a counter value and generate a control signal to control the PWM latch.

[0009] In accordance with a third aspect of the present disclosure, there is provided a method including obtaining a first wafer that includes a first substrate, a p-type semiconductor layer on the first substrate, an active layer on the p-type semiconductor layer, and an n-type semiconductor layer on the active layer; depositing a reflector layer on the n-type semiconductor layer; forming a first metal bonding layer on the reflector layer; bonding a second metal bonding layer on a backplane wafer to the first metal bonding layer; removing the first substrate to expose the p-type semiconductor layer; etching through the p-type semiconductor layer, the active layer, the n-type semiconductor layer, the reflector layer, the first metal bonding layer, and the second metal bonding layer to form an array of mesa structures for an array of micro-light emitting diodes; forming a passivation layer on sidewalls of the array of mesa structures; forming a sidewall reflector layer on the passivation layer; and depositing a common anode layer on the array of mesa structures, the common anode layer electrically coupled to the p-type semiconductor layer in each mesa structure of

the array of mesa structures.

[0010] In some embodiments of the method, the active layer includes GaN-based semiconductor materials, and obtaining the first wafer includes growing, on a growth substrate, the n-type semiconductor layer, the active layer, and the p-type semiconductor layer, bonding the first substrate to the p-type semiconductor layer, and removing the growth substrate. In some embodiments, the active layer includes phosphide-based semiconductor materials, and obtaining the first wafer includes growing, on the first substrate, the p-type semiconductor layer, the active layer, and the n-type semiconductor layer. The backplane wafer includes timing control circuits, a first voltage regulator configured to output a first positive supply voltage to the timing control circuits, and a second voltage regulator configured to output a second positive supply voltage to the common anode layer.

[0011] In accordance with a fourth aspect of the present disclosure, there is provided a method including obtaining a first wafer that includes a first substrate, a p-type semiconductor layer on the first substrate, an active layer on the p-type semiconductor layer, and an n-type semiconductor layer on the active layer; etching the n-type semiconductor layer, the active layer, and a portion of the p-type semiconductor layer to form a 2-D array of mesa structures; depositing a first dielectric layer on surfaces of the 2-D array of mesa structures; forming a plurality of p-contacts at regions between mesa structures of the 2-D array of mesa structures; depositing a metal layer on the first dielectric layer and the plurality of p-contacts; forming a patterned second dielectric layer on the metal layer; forming an array of n-contacts in the patterned second dielectric layer; forming a patterned third dielectric layer on the patterned second dielectric layer; forming p-electrodes and n-electrodes in the patterned third dielectric layer, the n-electrodes electrically connected to the array of n-contacts, and the p-electrodes electrically connected to the plurality of p-contacts; bonding the first wafer to a backplane wafer that includes electrical circuits, such that the electrical circuits are coupled to the p-electrodes and n-electrodes in the patterned third dielectric layer; and removing the first substrate to expose the p-type semiconductor layer.

[0012] In some embodiments of the method, the active layer includes GaN-based semiconductor materials, and obtaining the first wafer includes growing, on a growth substrate, the n-type semiconductor layer, the active layer, and the p-type semiconductor layer; bonding the first substrate to the p-type semiconductor layer; and remove the growth substrate. In some embodiments, the active layer includes phosphide-based semiconductor materials, and obtaining the first wafer includes growing, on the first substrate, the p-type semiconductor layer, the active layer, and the n-type semiconductor layer. In some

embodiments, the backplane wafer includes timing control circuits, a first voltage regulator configured to output a first positive supply voltage to the timing control circuits, and a second voltage regulator configured to output a second positive supply voltage to the p-electrodes.

[0013] This summary is neither intended to identify key or essential features of the claimed subject matter, nor is it intended to be used in isolation to determine the scope of the claimed subject matter. The subject matter should be understood by reference to appropriate portions of the entire specification of this disclosure, any or all drawings, and each claim. The foregoing, together with other features and examples, will be described in more detail below in the following specification, claims, and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Illustrative embodiments are described in detail below with reference to the following figures.

[0015] FIG. 1 is a simplified block diagram of an example of an artificial reality system environment including a near-eye display.

[0016] FIG. 2 is a perspective view of an example of a near-eye display in the form of a head-mounted display (HMD) device for implementing some of the examples disclosed herein.

[0017] FIG. 3 is a perspective view of an example of a near-eye display in the form of a pair of glasses for implementing some of the examples disclosed herein.

[0018] FIG. 4 illustrates an example of an optical see-through augmented reality system including a waveguide display.

[0019] FIG. 5A illustrates an example of a near-eye display device including a waveguide display.

[0020] FIG. 5B illustrates an example of a near-eye display device including a waveguide display.

[0021] FIG. 6 illustrates an example of an image source assembly in an augmented reality system.

[0022] FIG. 7A illustrates an example of a light emitting diode (LED) having a vertical mesa structure.

[0023] FIG. 7B is a cross-sectional view of an example of an LED having a parabolic mesa structure.

[0024] FIGS. 8A-8D illustrates an example of a method of hybrid bonding for arrays of LEDs.

[0025] FIG. 9 illustrates an example of an LED array with secondary optical components

fabricated thereon.

[0026] FIG. 10A illustrates an example of a method of die-to-wafer bonding for arrays of LEDs.

[0027] FIG. 10B illustrates an example of a method of wafer-to-wafer bonding for arrays of LEDs.

[0028] FIG. 11 is a simplified block diagram of an example of a micro-LED display device.

[0029] FIGS. 12A-12F illustrate an example of a method of fabricating a common-cathode micro-LED display device using alignment-free metal-to-metal bonding and post-bonding mesa formation processes.

[0030] FIG. 13 illustrates an example of a pixel of a common-cathode micro-LED display device.

[0031] FIG. 14 includes a simplified block diagram of an example of a common-cathode micro-LED display device.

[0032] FIGS. 15A-15G illustrate an example of a method of fabricating a common-anode GaN-based micro-LED display device.

[0033] FIGS. 16A-16F illustrate an example of a method of fabricating a common-anode phosphide-based micro-LED display device.

[0034] FIG. 17 illustrates an example of a common-anode micro-LED display device that may be fabricated using the method of FIGS. 15A-15G or the method of FIGS. 16A-16F.

[0035] FIGS. 18A and 18B illustrate an example of a common-anode micro-LED wafer including a plurality of mesa structures formed thereon.

[0036] FIGS. 19A and 19B illustrate an example of a common-anode micro-LED wafer with a bonding layer for bonding to a backplane wafer.

[0037] FIG. 20 illustrates an example of a pixel of a common-anode micro-LED display device.

[0038] FIG. 21 includes a simplified block diagram of an example of a common-anode micro-LED display device.

[0039] FIG. 22 includes a flowchart illustrating an example of a method of fabricating a common-anode micro-LED device.

[0040] FIG. 23 is a simplified block diagram of an electronic system of an example of a near-eye display.

[0041] The figures depict embodiments of the present disclosure for purposes of illustration only. One skilled in the art will readily recognize from the following description that alternative embodiments of the structures and methods illustrated may be employed without

departing from the principles, or benefits touted, of this disclosure.

[0042] In the appended figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a dash and a second label that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

DETAILED DESCRIPTION

[0043] This disclosure relates generally to micro-light emitting diodes (micro-LEDs). More specifically, this disclosure relates to common-anode micro-LED devices and methods of fabricating the common-anode micro-LED display devices. Various inventive embodiments are described herein, including devices, systems, circuits, methods, processes, materials, and the like.

[0044] LEDs with small pitches (e.g., less than about 20 μm, less than about 10 μm, less than about 5 μm, less than about 3 μm, or less than about 2 μm) may be used in high-resolution display systems. For example, augmented reality (AR) and virtual reality (VR) applications may use near-eye displays that include tiny light emitters such as micro-LEDs. Micro-LEDs in high-resolution display systems may be controlled by drive circuits that provide drive currents to the micro-LEDs based on pixel data of the display images, such that the micro-LEDs may emit light with appropriate intensities to form the display images. Micro-LEDs may be fabricated by epitaxially growing III-V semiconductor material layers on a growth substrate, whereas the drive circuits are generally fabricated on silicon wafers using processing technology developed for fabricating complementary metal-oxide-semiconductor (CMOS) integrated circuits. The wafer that includes CMOS drive circuits fabricated thereon is referred to herein as a backplane wafer or a CMOS backplane. Micro-LED arrays on a die or wafer may be bonded to the CMOS backplane, such that the individual micro-LEDs in the micro-LED arrays may be electrically connected to the corresponding pixel drive circuits and thus may become individually addressable to receive drive currents for driving the respective micro-LEDs.

[0045] Due to the small pitches of the micro-LED arrays and the small dimensions of individual micro-LEDs, it can be challenging to precisely align the bonding pads on the micro-LED arrays with the bonding pads on the drive circuits and form reliable bonding at the interfaces that may include both dielectric materials (e.g., SiO_2, SiN, or SiCN) and metal

(e.g., Cu, Au, Ti, or Al) bonding pads. In some implementations, to avoid precise alignment for the bonding, a micro-LED wafer may be bonded to a backplane wafer after the growth of the epitaxial layers and before the formation of individual micro-LEDs on the micro-LED wafer, where the micro-LED wafer and the backplane wafer may be bonded through metal-to-metal bonding of two solid metal bonding layers on the two wafers. No alignment is needed for bonding the solid metal bonding layers. After the bonding, the substrate of the micro-LED wafer may be removed, and the epitaxial layers and the metal bonding layers in the bonded wafer stack may be etched to form mesa structures for individual micro-LEDs. The etching process can have much higher alignment accuracy than the bonding process and thus may form individual micro-LEDs that align with the underlying pixel drive circuits.

[0046] In this process, the epitaxial layers on the micro-LED wafer may be grown by growing an n-type semiconductor layer (e.g., n-doped GaN layer) first, followed by an active region (light-emitting layers, such as quantum well layers) and a p-type semiconductor layer. A bonding layer may then be formed on the p-type semiconductor layer, and the micro-LED wafer may be bonded to the backplane wafer with the p-type semiconductor layer closer to the backplane wafer. When the micro-LED wafer is bonded to the backplane wafer with the p-type semiconductor layer closer to the backplane wafer, the micro-LEDs on the micro-LED wafer may have a common cathode and may be individually addressed through the anodes of the respective micro-LEDs. Driving the common-cathode micro-LEDs may require negative supply voltages at the common cathode, and the drive current may need to flow through multiple voltage supplies or voltage regulators. Therefore, the power rail design for the drive circuits may be complex, and the efficiency of the voltage supplies or voltage regulators may be low.

[0047] According to certain embodiments, a micro-LED display device may include common-anode micro-LEDs, and corresponding drive circuits that may include a voltage supply (e.g., a first voltage regulator) for supplying a positive voltage level to digital pixel drive circuits (e.g., timing control circuits) and another voltage supply (e.g., a second voltage regulator) for supplying a positive voltage level (and drive current) to the common anode of the micro-LEDs. In some embodiments, the micro-LED display device may include multiple arrays of micro-LEDs, where each array of micro-LEDs may emit light in a respective wavelength ranges (e.g., red, green, or blue light) and may have a common anode that receives a positive voltage level (and drive current) from a respective voltage supply. Thus, the drive circuits for the common-anode micro-LEDs may not need negative voltage levels and can have higher efficiency. In addition, the current driving transistors in the common-

anode micro-LED devices can be n-channel transistors that may have smaller sizes than p-channel transistors for driving the same current. Therefore, the common-anode pixel drive circuit can use a smaller semiconductor area and may be better suitable for, in particular, small micro-LEDs with in-pixel drive circuits.

[0048] In some embodiments, the micro-LED display device may include GaN-based micro-LEDs (e.g., including quantum wells formed by InGaN/GaN layers) and may be made, for example, by epitaxially growing a p-type semiconductor layer after growing an n-type semiconductor layer and active layers on a growth substrate, bonding a carrier substrate to the p-type semiconductor layer, removing the growth substrate to expose the n-type semiconductor layer, forming a solid metal bonding layer on the exposed n-type semiconductor layer, bonding the metal bonding layer formed on the n-type semiconductor layer to a metal bonding layer of a backplane wafer, removing the carrier substrate from the bonded wafer stack to expose the p-type semiconductor layer, etching the epitaxial layers and the metal bonding layers from the side of the p-type semiconductor layer to form mesa structures of singulated micro-LEDs, and depositing a common anode layer (e.g., a transparent conductive layer) on the p-type semiconductor layer.

[0049] In some embodiments, the micro-LED display device may include InGaP-based micro-LEDs (e.g., including quantum wells formed by InGaP/AlGaInP layers) and may be made, for example, by epitaxially growing an n-type semiconductor layer after growing a p-type semiconductor layer and active layers on a growth substrate, forming a metal bonding layer on the n-type semiconductor layer, bonding the metal bonding layer formed on the n-type semiconductor layer to a metal bonding layer of a backplane wafer, removing the growth substrate from the bonded wafer stack to expose the p-type semiconductor layer, etching the epitaxial layers and the metal bonding layers from the side of the p-type semiconductor layer to form mesa structures of singulated micro-LEDs, and depositing a common anode layer (e.g., a transparent conductive layer) on the p-type semiconductor layer.

[0050] In some embodiments, the micro-LED display device may be made, for example, by obtaining a layer stack that includes a p-type semiconductor layer, active layers, and an exposed n-type semiconductor layer as described above; etching the layer stack from the side of the n-type semiconductor layer to form individual mesa structures and expose regions of the p-type semiconductor layer; forming an array of p-contacts at the expose regions of the p-type semiconductor layer and a common anode layer (e.g., a contiguous metal layer) on the array of p-contacts; forming n-contacts on the n-type semiconductor layer of the mesa structures; forming bonding pads that are electrically connected to the p-contacts and n-

contacts; and aligning and bonding the bonding pads to bonding pads on a backplane wafer.

[0051] The micro-LEDs described herein may be used in conjunction with various technologies, such as an artificial reality system. An artificial reality system, such as a head-mounted display (HMD) or heads-up display (HUD) system, generally includes a display configured to present artificial images that depict objects in a virtual environment. The display may present virtual objects or combine images of real objects with virtual objects, as in virtual reality (VR), augmented reality (AR), or mixed reality (MR) applications. For example, in an AR system, a user may view both displayed images of virtual objects (e.g., computer-generated images (CGIs)) and the surrounding environment by, for example, seeing through transparent display glasses or lenses (often referred to as optical see-through) or viewing displayed images of the surrounding environment captured by a camera (often referred to as video see-through). In some AR systems, the artificial images may be presented to users using an LED-based display subsystem.

[0052] As used herein, the term "light emitting diode (LED)" refers to a light source that includes at least an n-type semiconductor layer, a p-type semiconductor layer, and a light emitting region (i.e., active region) between the n-type semiconductor layer and the p-type semiconductor layer. The light emitting region may include one or more semiconductor layers that form one or more heterostructures, such as quantum wells. In some embodiments, the light emitting region may include multiple semiconductor layers that form one or more multiple-quantum-wells (MQWs), each including multiple (e.g., about 2 to 6) quantum wells.

[0053] As used herein, the term "micro-LED" or "μLED" refers to an LED that has a chip where a linear dimension of the chip is less than about 200 μm, such as less than 100 μm, less than 50 μm, less than 20 μm, less than 10 μm, or smaller. For example, the linear dimension of a micro-LED may be as small as 6 μm, 5 μm, 4 μm, 2 μm, or smaller. Some micro-LEDs may have a linear dimension (e.g., length or diameter) comparable to the minority carrier diffusion length. However, the disclosure herein is not limited to micro-LEDs, and may also be applied to mini-LEDs and large LEDs.

[0054] As used herein, the term "bonding" may refer to various methods for physically and/or electrically connecting two or more devices and/or wafers, such as adhesive bonding, metal-to-metal bonding, metal oxide bonding, wafer-to-wafer bonding, die-to-wafer bonding, hybrid bonding, soldering, under-bump metallization, and the like. For example, adhesive bonding may use a curable adhesive (e.g., an epoxy) to physically bond two or more devices and/or wafers through adhesion. Metal-to-metal bonding may include, for example, wire

bonding or flip chip bonding using soldering interfaces (e.g., pads or balls), conductive adhesive, or welded joints between metals. Metal oxide bonding may form a metal and oxide pattern on each surface, bond the oxide sections together, and then bond the metal sections together to create a conductive path. Wafer-to-wafer bonding may bond two wafers (e.g., silicon wafers or other semiconductor wafers) without any intermediate layers and is based on chemical bonds between the surfaces of the two wafers. Wafer-to-wafer bonding may include wafer cleaning and other preprocessing, aligning and pre-bonding at room temperature, and annealing at elevated temperatures, such as about 250 °C or higher. Die-to-wafer bonding may use bumps on one wafer to align features of a pre-formed chip with drivers of a wafer. Hybrid bonding may include, for example, wafer cleaning, high-precision alignment of contacts of one wafer with contacts of another wafer, dielectric bonding of dielectric materials within the wafers at room temperature, and metal bonding of the contacts by annealing at, for example, 250-300 °C or higher. As used herein, the term "bump" may refer generically to a metal interconnect used or formed during bonding.

[0055] In the following description, for the purposes of explanation, specific details are set forth in order to provide a thorough understanding of examples of the disclosure. However, it will be apparent that various examples may be practiced without these specific details. For example, devices, systems, structures, assemblies, methods, and other components may be shown as components in block diagram form in order not to obscure the examples in unnecessary detail. In other instances, well-known devices, processes, systems, structures, and techniques may be shown without necessary detail in order to avoid obscuring the examples. The figures and description are not intended to be restrictive. The terms and expressions that have been employed in this disclosure are used as terms of description and not of limitation, and there is no intention in the use of such terms and expressions of excluding any equivalents of the features shown and described or portions thereof. The word "example" is used herein to mean "serving as an example, instance, or illustration." Any embodiment or design described herein as "example" is not necessarily to be construed as preferred or advantageous over other embodiments or designs.

[0056] **FIG. 1** is a simplified block diagram of an example of an artificial reality system environment 100 including a near-eye display 120 in accordance with certain embodiments. Artificial reality system environment 100 shown in FIG. 1 may include near-eye display 120, an optional external imaging device 150, and an optional input/output interface 140, each of which may be coupled to an optional console 110. While FIG. 1 shows an example of artificial reality system environment 100 including one near-eye display 120, one external

imaging device 150, and one input/output interface 140, any number of these components may be included in artificial reality system environment 100, or any of the components may be omitted. For example, there may be multiple near-eye displays 120 monitored by one or more external imaging devices 150 in communication with console 110. In some configurations, artificial reality system environment 100 may not include external imaging device 150, optional input/output interface 140, and optional console 110. In alternative configurations, different or additional components may be included in artificial reality system environment 100.

[0057] Near-eye display 120 may be a head-mounted display that presents content to a user. Examples of content presented by near-eye display 120 include one or more of images, videos, audio, or any combination thereof. In some embodiments, audio may be presented via an external device (*e.g.*, speakers and/or headphones) that receives audio information from near-eye display 120, console 110, or both, and presents audio data based on the audio information. Near-eye display 120 may include one or more rigid bodies, which may be rigidly or non-rigidly coupled to each other. A rigid coupling between rigid bodies may cause the coupled rigid bodies to act as a single rigid entity. A non-rigid coupling between rigid bodies may allow the rigid bodies to move relative to each other. In various embodiments, near-eye display 120 may be implemented in any suitable form-factor, including a pair of glasses. Some embodiments of near-eye display 120 are further described below with respect to FIGS. 2 and 3. Additionally, in various embodiments, the functionality described herein may be used in a headset that combines images of an environment external to near-eye display 120 and artificial reality content (*e.g.*, computer-generated images). Therefore, near-eye display 120 may augment images of a physical, real-world environment external to near-eye display 120 with generated content (*e.g.*, images, video, sound, etc.) to present an augmented reality to a user.

[0058] In various embodiments, near-eye display 120 may include one or more of display electronics 122, display optics 124, and an eye-tracking unit 130. In some embodiments, near-eye display 120 may also include one or more locators 126, one or more position sensors 128, and an inertial measurement unit (IMU) 132. Near-eye display 120 may omit any of eye-tracking unit 130, locators 126, position sensors 128, and IMU 132, or include additional elements in various embodiments. Additionally, in some embodiments, near-eye display 120 may include elements combining the function of various elements described in conjunction with FIG. 1.

[0059] Display electronics 122 may display or facilitate the display of images to the user

according to data received from, for example, console 110. In various embodiments, display electronics 122 may include one or more display panels, such as a liquid crystal display (LCD), an organic light emitting diode (OLED) display, an inorganic light emitting diode (ILED) display, a micro light emitting diode (μLED) display, an active-matrix OLED display (AMOLED), a transparent OLED display (TOLED), or some other display. For example, in one implementation of near-eye display 120, display electronics 122 may include a front TOLED panel, a rear display panel, and an optical component (*e.g.*, an attenuator, polarizer, or diffractive or spectral film) between the front and rear display panels. Display electronics 122 may include pixels to emit light of a predominant color such as red, green, blue, white, or yellow. In some implementations, display electronics 122 may display a three-dimensional (3D) image through stereoscopic effects produced by two-dimensional panels to create a subjective perception of image depth. For example, display electronics 122 may include a left display and a right display positioned in front of a user's left eye and right eye, respectively. The left and right displays may present copies of an image shifted horizontally relative to each other to create a stereoscopic effect (*i.e.*, a perception of image depth by a user viewing the image).

[0060] In certain embodiments, display optics 124 may display image content optically (*e.g.*, using optical waveguides and couplers) or magnify image light received from display electronics 122, correct optical errors associated with the image light, and present the corrected image light to a user of near-eye display 120. In various embodiments, display optics 124 may include one or more optical elements, such as, for example, a substrate, optical waveguides, an aperture, a Fresnel lens, a convex lens, a concave lens, a filter, input/output couplers, or any other suitable optical elements that may affect image light emitted from display electronics 122. Display optics 124 may include a combination of different optical elements as well as mechanical couplings to maintain relative spacing and orientation of the optical elements in the combination. One or more optical elements in display optics 124 may have an optical coating, such as an antireflective coating, a reflective coating, a filtering coating, or a combination of different optical coatings.

[0061] Magnification of the image light by display optics 124 may allow display electronics 122 to be physically smaller, weigh less, and consume less power than larger displays. Additionally, magnification may increase a field of view of the displayed content. The amount of magnification of image light by display optics 124 may be changed by adjusting, adding, or removing optical elements from display optics 124. In some

embodiments, display optics 124 may project displayed images to one or more image planes that may be further away from the user's eyes than near-eye display 120.

[0062] Display optics 124 may also be designed to correct one or more types of optical errors, such as two-dimensional optical errors, three-dimensional optical errors, or any combination thereof. Two-dimensional errors may include optical aberrations that occur in two dimensions. Example types of two-dimensional errors may include barrel distortion, pincushion distortion, longitudinal chromatic aberration, and transverse chromatic aberration. Three-dimensional errors may include optical errors that occur in three dimensions. Example types of three-dimensional errors may include spherical aberration, comatic aberration, field curvature, and astigmatism.

[0063] Locators 126 may be objects located in specific positions on near-eye display 120 relative to one another and relative to a reference point on near-eye display 120. In some implementations, console 110 may identify locators 126 in images captured by external imaging device 150 to determine the artificial reality headset's position, orientation, or both. A locator 126 may be a light-emitting diode (LED), a corner cube reflector, a reflective marker, a type of light source that contrasts with an environment in which near-eye display 120 operates, or any combination thereof. In embodiments where locators 126 are active components (*e.g.*, LEDs or other types of light emitting devices), locators 126 may emit light in the visible band (*e.g.*, about 380 nm to 750 nm), in the infrared (IR) band (*e.g.*, about 750 nm to 1 mm), in the ultraviolet band (*e.g.*, about 12 nm to about 380 nm), in another portion of the electromagnetic spectrum, or in any combination of portions of the electromagnetic spectrum.

[0064] External imaging device 150 may include one or more cameras, one or more video cameras, any other device capable of capturing images including one or more of locators 126, or any combination thereof. Additionally, external imaging device 150 may include one or more filters (*e.g.*, to increase signal to noise ratio). External imaging device 150 may be configured to detect light emitted or reflected from locators 126 in a field of view of external imaging device 150. In embodiments where locators 126 include passive elements (*e.g.*, retroreflectors), external imaging device 150 may include a light source that illuminates some or all of locators 126, which may retro-reflect the light to the light source in external imaging device 150. Slow calibration data may be communicated from external imaging device 150 to console 110, and external imaging device 150 may receive one or more calibration parameters from console 110 to adjust one or more imaging parameters (*e.g.*, focal length, focus, frame rate, sensor temperature, shutter speed, aperture, etc.).

[0065] Position sensors 128 may generate one or more measurement signals in response to motion of near-eye display 120. Examples of position sensors 128 may include accelerometers, gyroscopes, magnetometers, other motion-detecting or error-correcting sensors, or any combination thereof. For example, in some embodiments, position sensors 128 may include multiple accelerometers to measure translational motion (*e.g.*, forward/back, up/down, or left/right) and multiple gyroscopes to measure rotational motion (*e.g.*, pitch, yaw, or roll). In some embodiments, various position sensors may be oriented orthogonally to each other.

[0066] IMU 132 may be an electronic device that generates fast calibration data based on measurement signals received from one or more of position sensors 128. Position sensors 128 may be located external to IMU 132, internal to IMU 132, or any combination thereof. Based on the one or more measurement signals from one or more position sensors 128, IMU 132 may generate fast calibration data indicating an estimated position of near-eye display 120 relative to an initial position of near-eye display 120. For example, IMU 132 may integrate measurement signals received from accelerometers over time to estimate a velocity vector and integrate the velocity vector over time to determine an estimated position of a reference point on near-eye display 120. Alternatively, IMU 132 may provide the sampled measurement signals to console 110, which may determine the fast calibration data. While the reference point may generally be defined as a point in space, in various embodiments, the reference point may also be defined as a point within near-eye display 120 (*e.g.*, a center of IMU 132).

[0067] Eye-tracking unit 130 may include one or more eye-tracking systems. Eye tracking may refer to determining an eye's position, including orientation and location of the eye, relative to near-eye display 120. An eye-tracking system may include an imaging system to image one or more eyes and may optionally include a light emitter, which may generate light that is directed to an eye such that light reflected by the eye may be captured by the imaging system. For example, eye-tracking unit 130 may include a non-coherent or coherent light source (*e.g.*, a laser diode) emitting light in the visible spectrum or infrared spectrum, and a camera capturing the light reflected by the user's eye. As another example, eye-tracking unit 130 may capture reflected radio waves emitted by a miniature radar unit. Eye-tracking unit 130 may use low-power light emitters that emit light at frequencies and intensities that would not injure the eye or cause physical discomfort. Eye-tracking unit 130 may be arranged to increase contrast in images of an eye captured by eye-tracking unit 130 while reducing the overall power consumed by eye-tracking unit 130 (*e.g.*, reducing power consumed by a light

emitter and an imaging system included in eye-tracking unit 130). For example, in some implementations, eye-tracking unit 130 may consume less than 120 milliwatts of power.

[0068] Near-eye display 120 may use the orientation of the eye to, *e.g.*, determine an inter-pupillary distance (IPD) of the user, determine gaze direction, introduce depth cues (*e.g.*, blur image outside of the user's main line of sight), collect heuristics on the user interaction in the VR media (*e.g.*, time spent on any particular subject, object, or frame as a function of exposed stimuli), some other functions that are based in part on the orientation of at least one of the user's eyes, or any combination thereof. Because the orientation may be determined for both eyes of the user, eye-tracking unit 130 may be able to determine where the user is looking. For example, determining a direction of a user's gaze may include determining a point of convergence based on the determined orientations of the user's left and right eyes. A point of convergence may be the point where the two foveal axes of the user's eyes intersect. The direction of the user's gaze may be the direction of a line passing through the point of convergence and the mid-point between the pupils of the user's eyes.

[0069] Input/output interface 140 may be a device that allows a user to send action requests to console 110. An action request may be a request to perform a particular action. For example, an action request may be to start or to end an application or to perform a particular action within the application. Input/output interface 140 may include one or more input devices. Example input devices may include a keyboard, a mouse, a game controller, a glove, a button, a touch screen, or any other suitable device for receiving action requests and communicating the received action requests to console 110. An action request received by the input/output interface 140 may be communicated to console 110, which may perform an action corresponding to the requested action. In some embodiments, input/output interface 140 may provide haptic feedback to the user in accordance with instructions received from console 110. For example, input/output interface 140 may provide haptic feedback when an action request is received, or when console 110 has performed a requested action and communicates instructions to input/output interface 140. In some embodiments, external imaging device 150 may be used to track input/output interface 140, such as tracking the location or position of a controller (which may include, for example, an IR light source) or a hand of the user to determine the motion of the user. In some embodiments, near-eye display 120 may include one or more imaging devices to track input/output interface 140, such as tracking the location or position of a controller or a hand of the user to determine the motion of the user.

[0070] Console 110 may provide content to near-eye display 120 for presentation to the

user in accordance with information received from one or more of external imaging device 150, near-eye display 120, and input/output interface 140. In the example shown in FIG. 1, console 110 may include an application store 112, a headset tracking subsystem 114, an artificial reality engine 116, and an eye-tracking subsystem 118. Some embodiments of console 110 may include different or additional devices or subsystems than those described in conjunction with FIG. 1. Functions further described below may be distributed among components of console 110 in a different manner than is described here.

[0071] In some embodiments, console 110 may include a processor and a non-transitory computer-readable storage medium storing instructions executable by the processor. The processor may include multiple processing units executing instructions in parallel. The non-transitory computer-readable storage medium may be any memory, such as a hard disk drive, a removable memory, or a solid-state drive (*e.g.*, flash memory or dynamic random access memory (DRAM)). In various embodiments, the devices or subsystems of console 110 described in conjunction with FIG. 1 may be encoded as instructions in the non-transitory computer-readable storage medium that, when executed by the processor, cause the processor to perform the functions further described below.

[0072] Application store 112 may store one or more applications for execution by console 110. An application may include a group of instructions that, when executed by a processor, generates content for presentation to the user. Content generated by an application may be in response to inputs received from the user via movement of the user's eyes or inputs received from the input/output interface 140. Examples of the applications may include gaming applications, conferencing applications, video playback application, or other suitable applications.

[0073] Headset tracking subsystem 114 may track movements of near-eye display 120 using slow calibration information from external imaging device 150. For example, headset tracking subsystem 114 may determine positions of a reference point of near-eye display 120 using observed locators from the slow calibration information and a model of near-eye display 120. Headset tracking subsystem 114 may also determine positions of a reference point of near-eye display 120 using position information from the fast calibration information. Additionally, in some embodiments, headset tracking subsystem 114 may use portions of the fast calibration information, the slow calibration information, or any combination thereof, to predict a future location of near-eye display 120. Headset tracking subsystem 114 may provide the estimated or predicted future position of near-eye display 120 to artificial reality engine 116.

[0074] Artificial reality engine 116 may execute applications within artificial reality system environment 100 and receive position information of near-eye display 120, acceleration information of near-eye display 120, velocity information of near-eye display 120, predicted future positions of near-eye display 120, or any combination thereof from headset tracking subsystem 114. Artificial reality engine 116 may also receive estimated eye position and orientation information from eye-tracking subsystem 118. Based on the received information, artificial reality engine 116 may determine content to provide to near-eye display 120 for presentation to the user. For example, if the received information indicates that the user has looked to the left, artificial reality engine 116 may generate content for near-eye display 120 that mirrors the user's eye movement in a virtual environment. Additionally, artificial reality engine 116 may perform an action within an application executing on console 110 in response to an action request received from input/output interface 140, and provide feedback to the user indicating that the action has been performed. The feedback may be visual or audible feedback via near-eye display 120 or haptic feedback via input/output interface 140.

[0075] Eye-tracking subsystem 118 may receive eye-tracking data from eye-tracking unit 130 and determine the position of the user's eye based on the eye tracking data. The position of the eye may include an eye's orientation, location, or both relative to near-eye display 120 or any element thereof. Because the eye's axes of rotation change as a function of the eye's location in its socket, determining the eye's location in its socket may allow eye-tracking subsystem 118 to more accurately determine the eye's orientation.

[0076] **FIG. 2** is a perspective view of an example of a near-eye display in the form of an HMD device 200 for implementing some of the examples disclosed herein. HMD device 200 may be a part of, e.g., a VR system, an AR system, an MR system, or any combination thereof. HMD device 200 may include a body 220 and a head strap 230. FIG. 2 shows a bottom side 223, a front side 225, and a left side 227 of body 220 in the perspective view. Head strap 230 may have an adjustable or extendible length. There may be a sufficient space between body 220 and head strap 230 of HMD device 200 for allowing a user to mount HMD device 200 onto the user's head. In various embodiments, HMD device 200 may include additional, fewer, or different components. For example, in some embodiments, HMD device 200 may include eyeglass temples and temple tips as shown in, for example, FIG. 3 below, rather than head strap 230.

[0077] HMD device 200 may present to a user media including virtual and/or augmented views of a physical, real-world environment with computer-generated elements. Examples of the media presented by HMD device 200 may include images (e.g., two-dimensional (2D) or

three-dimensional (3D) images), videos (e.g., 2D or 3D videos), audio, or any combination thereof. The images and videos may be presented to each eye of the user by one or more display assemblies (not shown in FIG. 2) enclosed in body 220 of HMD device 200. In various embodiments, the one or more display assemblies may include a single electronic display panel or multiple electronic display panels (e.g., one display panel for each eye of the user). Examples of the electronic display panel(s) may include, for example, an LCD, an OLED display, an ILED display, a μLED display, an AMOLED, a TOLED, some other display, or any combination thereof. HMD device 200 may include two eye box regions.

[0078] In some implementations, HMD device 200 may include various sensors (not shown), such as depth sensors, motion sensors, position sensors, and eye tracking sensors. Some of these sensors may use a structured light pattern for sensing. In some implementations, HMD device 200 may include an input/output interface for communicating with a console. In some implementations, HMD device 200 may include a virtual reality engine (not shown) that can execute applications within HMD device 200 and receive depth information, position information, acceleration information, velocity information, predicted future positions, or any combination thereof of HMD device 200 from the various sensors. In some implementations, the information received by the virtual reality engine may be used for producing a signal (e.g., display instructions) to the one or more display assemblies. In some implementations, HMD device 200 may include locators (not shown, such as locators 126) located in fixed positions on body 220 relative to one another and relative to a reference point. Each of the locators may emit light that is detectable by an external imaging device.

[0079] **FIG. 3** is a perspective view of an example of a near-eye display 300 in the form of a pair of glasses for implementing some of the examples disclosed herein. Near-eye display 300 may be a specific implementation of near-eye display 120 of FIG. 1, and may be configured to operate as a virtual reality display, an augmented reality display, and/or a mixed reality display. Near-eye display 300 may include a frame 305 and a display 310. Display 310 may be configured to present content to a user. In some embodiments, display 310 may include display electronics and/or display optics. For example, as described above with respect to near-eye display 120 of FIG. 1, display 310 may include an LCD display panel, an LED display panel, or an optical display panel (e.g., a waveguide display assembly).

[0080] Near-eye display 300 may further include various sensors 350a, 350b, 350c, 350d, and 350e on or within frame 305. In some embodiments, sensors 350a-350e may include one or more depth sensors, motion sensors, position sensors, inertial sensors, or ambient light

sensors. In some embodiments, sensors 350a-350e may include one or more image sensors configured to generate image data representing different fields of views in different directions. In some embodiments, sensors 350a-350e may be used as input devices to control or influence the displayed content of near-eye display 300, and/or to provide an interactive VR/AR/MR experience to a user of near-eye display 300. In some embodiments, sensors 350a-350e may also be used for stereoscopic imaging.

[0081] In some embodiments, near-eye display 300 may further include one or more illuminators 330 to project light into the physical environment. The projected light may be associated with different frequency bands (e.g., visible light, infra-red light, ultra-violet light, etc.), and may serve various purposes. For example, illuminator(s) 330 may project light in a dark environment (or in an environment with low intensity of infra-red light, ultra-violet light, etc.) to assist sensors 350a-350e in capturing images of different objects within the dark environment. In some embodiments, illuminator(s) 330 may be used to project certain light patterns onto the objects within the environment. In some embodiments, illuminator(s) 330 may be used as locators, such as locators 126 described above with respect to FIG. 1.

[0082] In some embodiments, near-eye display 300 may also include a high-resolution camera 340. Camera 340 may capture images of the physical environment in the field of view. The captured images may be processed, for example, by a virtual reality engine (e.g., artificial reality engine 116 of FIG. 1) to add virtual objects to the captured images or modify physical objects in the captured images, and the processed images may be displayed to the user by display 310 for AR or MR applications.

[0083] **FIG. 4** illustrates an example of an optical see-through augmented reality system 400 including a waveguide display according to certain embodiments. Augmented reality system 400 may include a projector 410 and a combiner 415. Projector 410 may include a light source or image source 412 and projector optics 414. In some embodiments, light source or image source 412 may include one or more micro-LED devices described above. In some embodiments, image source 412 may include a plurality of pixels that displays virtual objects, such as an LCD display panel or an LED display panel. In some embodiments, image source 412 may include a light source that generates coherent or partially coherent light. For example, image source 412 may include a laser diode, a vertical cavity surface emitting laser, an LED, and/or a micro-LED described above. In some embodiments, image source 412 may include a plurality of light sources (e.g., an array of micro-LEDs described above), each emitting a monochromatic image light corresponding to a primary color (e.g., red, green, or blue). In some embodiments, image source 412 may include three two-dimensional arrays of

micro-LEDs, where each two-dimensional array of micro-LEDs may include micro-LEDs configured to emit light of a primary color (e.g., red, green, or blue). In some embodiments, image source 412 may include an optical pattern generator, such as a spatial light modulator. Projector optics 414 may include one or more optical components that can condition the light from image source 412, such as expanding, collimating, scanning, or projecting light from image source 412 to combiner 415. The one or more optical components may include, for example, one or more lenses, liquid lenses, mirrors, apertures, and/or gratings. For example, in some embodiments, image source 412 may include one or more one-dimensional arrays or elongated two-dimensional arrays of micro-LEDs, and projector optics 414 may include one or more one-dimensional scanners (e.g., micro-mirrors or prisms) configured to scan the one-dimensional arrays or elongated two-dimensional arrays of micro-LEDs to generate image frames. In some embodiments, projector optics 414 may include a liquid lens (e.g., a liquid crystal lens) with a plurality of electrodes that allows scanning of the light from image source 412.

[0084] Combiner 415 may include an input coupler 430 for coupling light from projector 410 into a substrate 420 of combiner 415. Combiner 415 may transmit at least 50% of light in a first wavelength range and reflect at least 25% of light in a second wavelength range. For example, the first wavelength range may be visible light from about 400 nm to about 650 nm, and the second wavelength range may be in the infrared band, for example, from about 800 nm to about 1000 nm. Input coupler 430 may include a volume holographic grating, a diffractive optical element (DOE) (e.g., a surface-relief grating), a slanted surface of substrate 420, or a refractive coupler (e.g., a wedge or a prism). For example, input coupler 430 may include a reflective volume Bragg grating or a transmissive volume Bragg grating. Input coupler 430 may have a coupling efficiency of greater than 30%, 50%, 75%, 90%, or higher for visible light. Light coupled into substrate 420 may propagate within substrate 420 through, for example, total internal reflection (TIR). Substrate 420 may be in the form of a lens of a pair of eyeglasses. Substrate 420 may have a flat or a curved surface, and may include one or more types of dielectric materials, such as glass, quartz, plastic, polymer, poly(methyl methacrylate) (PMMA), crystal, or ceramic. A thickness of the substrate may range from, for example, less than about 1 mm to about 10 mm or more. Substrate 420 may be transparent to visible light.

[0085] Substrate 420 may include or may be coupled to a plurality of output couplers 440, each configured to extract at least a portion of the light guided by and propagating within substrate 420 from substrate 420, and direct extracted light 460 to an eyebox 495 where an

eye 490 of the user of augmented reality system 400 may be located when augmented reality system 400 is in use. The plurality of output couplers 440 may replicate the exit pupil to increase the size of eyebox 495 such that the displayed image is visible in a larger area. As input coupler 430, output couplers 440 may include grating couplers (*e.g.*, volume holographic gratings or surface-relief gratings), other diffraction optical elements (DOEs), prisms, etc. For example, output couplers 440 may include reflective volume Bragg gratings or transmissive volume Bragg gratings. Output couplers 440 may have different coupling (*e.g.*, diffraction) efficiencies at different locations. Substrate 420 may also allow light 450 from the environment in front of combiner 415 to pass through with little or no loss. Output couplers 440 may also allow light 450 to pass through with little loss. For example, in some implementations, output couplers 440 may have a very low diffraction efficiency for light 450 such that light 450 may be refracted or otherwise pass through output couplers 440 with little loss, and thus may have a higher intensity than extracted light 460. In some implementations, output couplers 440 may have a high diffraction efficiency for light 450 and may diffract light 450 in certain desired directions (*i.e.*, diffraction angles) with little loss. As a result, the user may be able to view combined images of the environment in front of combiner 415 and images of virtual objects projected by projector 410.

[0086] **FIG. 5A** illustrates an example of a near-eye display (NED) device 500 including a waveguide display 530 according to certain embodiments. NED device 500 may be an example of near-eye display 120, augmented reality system 400, or another type of display device. NED device 500 may include a light source 510, projection optics 520, and waveguide display 530. Light source 510 may include multiple panels of light emitters for different colors, such as a panel of red light emitters 512, a panel of green light emitters 514, and a panel of blue light emitters 516. The red light emitters 512 are organized into an array; the green light emitters 514 are organized into an array; and the blue light emitters 516 are organized into an array. The dimensions and pitches of light emitters in light source 510 may be small. For example, each light emitter may have a diameter less than 2 μm (e.g., about 1.2 μm) and the pitch may be less than 2 μm (e.g., about 1.5 μm). As such, the number of light emitters in each red light emitters 512, green light emitters 514, and blue light emitters 516 can be equal to or greater than the number of pixels in a display image, such as 960×720, 1280×720, 1440×1080, 1920×1080, 2160×1080, or 2560×1080 pixels. Thus, a display image may be generated simultaneously by light source 510. A scanning element may not be used in NED device 500.

[0087] Before reaching waveguide display 530, the light emitted by light source 510 may be conditioned by projection optics 520, which may include a lens array. Projection optics 520 may collimate or focus the light emitted by light source 510 to waveguide display 530, which may include a coupler 532 for coupling the light emitted by light source 510 into waveguide display 530. The light coupled into waveguide display 530 may propagate within waveguide display 530 through, for example, total internal reflection as described above with respect to FIG. 4. Coupler 532 may also couple portions of the light propagating within waveguide display 530 out of waveguide display 530 and towards user's eye 590.

[0088] **FIG. 5B** illustrates an example of a near-eye display (NED) device 550 including a waveguide display 580 according to certain embodiments. In some embodiments, NED device 550 may use a scanning mirror 570 to project light from a light source 540 to an image field where a user's eye 590 may be located. NED device 550 may be an example of near-eye display 120, augmented reality system 400, or another type of display device. Light source 540 may include one or more rows or one or more columns of light emitters of different colors, such as multiple rows of red light emitters 542, multiple rows of green light emitters 544, and multiple rows of blue light emitters 546. For example, red light emitters 542, green light emitters 544, and blue light emitters 546 may each include N rows, each row including, for example, 2560 light emitters (pixels). The red light emitters 542 are organized into an array; the green light emitters 544 are organized into an array; and the blue light emitters 546 are organized into an array. In some embodiments, light source 540 may include a single line of light emitters for each color. In some embodiments, light source 540 may include multiple columns of light emitters for each of red, green, and blue colors, where each column may include, for example, 1080 light emitters. In some embodiments, the dimensions and/or pitches of the light emitters in light source 540 may be relatively large (e.g., about 3-5 μm) and thus light source 540 may not include sufficient light emitters for simultaneously generating a full display image. For example, the number of light emitters for a single color may be fewer than the number of pixels (e.g., 2560×1080 pixels) in a display image. The light emitted by light source 540 may be a set of collimated or diverging beams of light.

[0089] Before reaching scanning mirror 570, the light emitted by light source 540 may be conditioned by various optical devices, such as collimating lenses or a freeform optical element 560. Freeform optical element 560 may include, for example, a multi-facet prism or another light folding element that may direct the light emitted by light source 540 towards scanning mirror 570, such as changing the propagation direction of the light emitted by light

source 540 by, for example, about 90° or larger. In some embodiments, freeform optical element 560 may be rotatable to scan the light. Scanning mirror 570 and/or freeform optical element 560 may reflect and project the light emitted by light source 540 to waveguide display 580, which may include a coupler 582 for coupling the light emitted by light source 540 into waveguide display 580. The light coupled into waveguide display 580 may propagate within waveguide display 580 through, for example, total internal reflection as described above with respect to FIG. 4. Coupler 582 may also couple portions of the light propagating within waveguide display 580 out of waveguide display 580 and towards user's eye 590.

[0090] Scanning mirror 570 may include a microelectromechanical system (MEMS) mirror or any other suitable mirrors. Scanning mirror 570 may rotate to scan in one or two dimensions. As scanning mirror 570 rotates, the light emitted by light source 540 may be directed to a different area of waveguide display 580 such that a full display image may be projected onto waveguide display 580 and directed to user's eye 590 by waveguide display 580 in each scanning cycle. For example, in embodiments where light source 540 includes light emitters for all pixels in one or more rows or columns, scanning mirror 570 may be rotated in the column or row direction (e.g., x or y direction) to scan an image. In embodiments where light source 540 includes light emitters for some but not all pixels in one or more rows or columns, scanning mirror 570 may be rotated in both the row and column directions (e.g., both x and y directions) to project a display image (e.g., using a raster-type scanning pattern).

[0091] NED device 550 may operate in predefined display periods. A display period (e.g., display cycle) may refer to a duration of time in which a full image is scanned or projected. For example, a display period may be a reciprocal of the desired frame rate. In NED device 550 that includes scanning mirror 570, the display period may also be referred to as a scanning period or scanning cycle. The light generation by light source 540 may be synchronized with the rotation of scanning mirror 570. For example, each scanning cycle may include multiple scanning steps, where light source 540 may generate a different light pattern in each respective scanning step.

[0092] In each scanning cycle, as scanning mirror 570 rotates, a display image may be projected onto waveguide display 580 and user's eye 590. The actual color value and light intensity (e.g., brightness) of a given pixel location of the display image may be an average of the light beams of the three colors (e.g., red, green, and blue) illuminating the pixel location

during the scanning period. After completing a scanning period, scanning mirror 570 may revert back to the initial position to project light for the first few rows of the next display image or may rotate in a reverse direction or scan pattern to project light for the next display image, where a new set of driving signals may be fed to light source 540. The same process may be repeated as scanning mirror 570 rotates in each scanning cycle. As such, different images may be projected to user's eye 590 in different scanning cycles.

[0093] **FIG. 6** illustrates an example of an image source assembly 610 in a near-eye display system 600 according to certain embodiments. Image source assembly 610 may include, for example, a display panel 640 that may generate display images to be projected to the user's eyes, and a projector 650 that may project the display images generated by display panel 640 to a waveguide display as described above with respect to FIGS. 4-5B. Display panel 640 may include a light source 642 and a drive circuit 644 for light source 642. Light source 642 may include, for example, light source 510 or 540. Projector 650 may include, for example, freeform optical element 560, scanning mirror 570, and/or projection optics 520 described above. Near-eye display system 600 may also include a controller 620 that synchronously controls light source 642 and projector 650 (e.g., scanning mirror 570). Image source assembly 610 may generate and output an image light to a waveguide display (not shown in FIG. 6), such as waveguide display 530 or 580. As described above, the waveguide display may receive the image light at one or more input-coupling elements, and guide the received image light to one or more output-coupling elements. The input and output coupling elements may include, for example, a diffraction grating, a holographic grating, a prism, or any combination thereof. The input-coupling element may be chosen such that total internal reflection occurs with the waveguide display. The output-coupling element may couple portions of the total internally reflected image light out of the waveguide display.

[0094] As described above, light source 642 may include a plurality of light emitters arranged in an array or a matrix. Each light emitter may emit monochromatic light, such as red light, blue light, green light, infra-red light, and the like. While RGB colors are often discussed in this disclosure, embodiments described herein are not limited to using red, green, and blue as primary colors. Other colors can also be used as the primary colors of near-eye display system 600. In some embodiments, a display panel in accordance with an embodiment may use more than three primary colors. Each pixel in light source 642 may include three subpixels that include a red micro-LED, a green micro-LED, and a blue micro-LED. A semiconductor LED generally includes an active light emitting layer within multiple layers of semiconductor materials. The multiple layers of semiconductor materials may

include different compound materials or a same base material with different dopants and/or different doping densities. For example, the multiple layers of semiconductor materials may include an n-type material layer, an active region that may include hetero-structures (e.g., one or more quantum wells), and a p-type material layer. The multiple layers of semiconductor materials may be grown on a surface of a substrate having a certain orientation. In some embodiments, to increase light extraction efficiency, a mesa that includes at least some of the layers of semiconductor materials may be formed.

[0095] Controller 620 may control the image rendering operations of image source assembly 610, such as the operations of light source 642 and/or projector 650. For example, controller 620 may determine instructions for image source assembly 610 to render one or more display images. The instructions may include display instructions and scanning instructions. In some embodiments, the display instructions may include an image file (e.g., a bitmap file). The display instructions may be received from, for example, a console, such as console 110 described above with respect to FIG. 1. The scanning instructions may be used by image source assembly 610 to generate image light. The scanning instructions may specify, for example, a type of a source of image light (e.g., monochromatic or polychromatic), a scanning rate, an orientation of a scanning apparatus, one or more illumination parameters, or any combination thereof. Controller 620 may include a combination of hardware, software, and/or firmware not shown here so as not to obscure other aspects of the present disclosure.

[0096] In some embodiments, controller 620 may be a graphics processing unit (GPU) of a display device. In other embodiments, controller 620 may be other kinds of processors. The operations performed by controller 620 may include taking content for display and dividing the content into discrete sections. Controller 620 may provide to light source 642 scanning instructions that include an address corresponding to an individual source element of light source 642 and/or an electrical bias applied to the individual source element. Controller 620 may instruct light source 642 to sequentially present the discrete sections using light emitters corresponding to one or more rows of pixels in an image ultimately displayed to the user. Controller 620 may also instruct projector 650 to perform different adjustments of the light. For example, controller 620 may control projector 650 to scan the discrete sections to different areas of a coupling element of the waveguide display (e.g., waveguide display 580) as described above with respect to FIG. 5B. As such, at the exit pupil of the waveguide display, each discrete portion is presented in a different respective location. While each discrete section is presented at a different respective time, the presentation and scanning of

the discrete sections occur fast enough such that a user's eye may integrate the different sections into a single image or series of images.

[0097] Image processor 630 may be a general-purpose processor and/or one or more application-specific circuits that are dedicated to performing the features described herein. In one embodiment, a general-purpose processor may be coupled to a memory to execute software instructions that cause the processor to perform certain processes described herein. In another embodiment, image processor 630 may be one or more circuits that are dedicated to performing certain features. While image processor 630 in FIG. 6 is shown as a stand-alone unit that is separate from controller 620 and drive circuit 644, image processor 630 may be a sub-unit of controller 620 or drive circuit 644 in other embodiments. In other words, in those embodiments, controller 620 or drive circuit 644 may perform various image processing functions of image processor 630. Image processor 630 may also be referred to as an image processing circuit.

[0098] In the example shown in FIG. 6, light source 642 may be driven by drive circuit 644, based on data or instructions (e.g., display and scanning instructions) sent from controller 620 or image processor 630. In one embodiment, drive circuit 644 may include a circuit panel that connects to and mechanically holds various light emitters of light source 642. Light source 642 may emit light in accordance with one or more illumination parameters that are set by the controller 620 and potentially adjusted by image processor 630 and drive circuit 644. An illumination parameter may be used by light source 642 to generate light. An illumination parameter may include, for example, source wavelength, pulse rate, pulse amplitude, beam type (continuous or pulsed), other parameter(s) that may affect the emitted light, or any combination thereof. In some embodiments, the source light generated by light source 642 may include multiple beams of red light, green light, and blue light, or any combination thereof.

[0099] Projector 650 may perform a set of optical functions, such as focusing, combining, conditioning, or scanning the image light generated by light source 642. In some embodiments, projector 650 may include a combining assembly, a light conditioning assembly, or a scanning mirror assembly. Projector 650 may include one or more optical components that optically adjust and potentially re-direct the light from light source 642. One example of the adjustment of light may include conditioning the light, such as expanding, collimating, correcting for one or more optical errors (e.g., field curvature, chromatic aberration, etc.), some other adjustments of the light, or any combination thereof. The optical components of projector 650 may include, for example, lenses, mirrors, apertures, gratings, or

any combination thereof.

[0100] Projector 650 may redirect image light via its one or more reflective and/or refractive portions so that the image light is projected at certain orientations toward the waveguide display. The location where the image light is redirected toward the waveguide display may depend on specific orientations of the one or more reflective and/or refractive portions. In some embodiments, projector 650 includes a single scanning mirror that scans in at least two dimensions. In other embodiments, projector 650 may include a plurality of scanning mirrors that each scan in directions orthogonal to each other. Projector 650 may perform a raster scan (horizontally or vertically), a bi-resonant scan, or any combination thereof. In some embodiments, projector 650 may perform a controlled vibration along the horizontal and/or vertical directions with a specific frequency of oscillation to scan along two dimensions and generate a two-dimensional projected image of the media presented to user's eyes. In other embodiments, projector 650 may include a lens or prism that may serve similar or the same function as one or more scanning mirrors. In some embodiments, image source assembly 610 may not include a projector, where the light emitted by light source 642 may be directly incident on the waveguide display.

[0101] In semiconductor LEDs, photons are usually generated at a certain internal quantum efficiency through the recombination of electrons and holes within an active region (*e.g.*, one or more semiconductor layers), where the internal quantum efficiency is the proportion of the radiative electron-hole recombination in the active region that emits photons. The generated light may then be extracted from the LEDs in a particular direction or within a particular solid angle. The ratio between the number of emitted photons extracted from an LED and the number of electrons passing through the LED is referred to as the external quantum efficiency, which describes how efficiently the LED converts injected electrons to photons that are extracted from the device.

[0102] The external quantum efficiency may be proportional to the injection efficiency, the internal quantum efficiency, and the extraction efficiency. The injection efficiency refers to the proportion of electrons passing through the device that are injected into the active region. The extraction efficiency is the proportion of photons generated in the active region that escape from the device. For LEDs, and in particular, micro-LEDs with reduced physical dimensions, improving the internal and external quantum efficiency and/or controlling the emission spectrum may be challenging. In some embodiments, to increase the light extraction efficiency, a mesa that includes at least some of the layers of semiconductor materials may be formed.

[0103] **FIG. 7A** illustrates an example of an LED 700 having a vertical mesa structure. LED 700 may be a light emitter in light source 510, 540, or 642. LED 700 may be a micro-LED made of inorganic materials, such as multiple layers of semiconductor materials. The layered semiconductor light emitting device may include multiple layers of III-V semiconductor materials. A III-V semiconductor material may include one or more Group III elements, such as aluminum (Al), gallium (Ga), or indium (In), in combination with a Group V element, such as nitrogen (N), phosphorus (P), arsenic (As), or antimony (Sb). When the Group V element of the III-V semiconductor material includes nitrogen, the III-V semiconductor material is referred to as a III-nitride material. The layered semiconductor light emitting device may be manufactured by growing multiple epitaxial layers on a substrate using techniques such as vapor-phase epitaxy (VPE), liquid-phase epitaxy (LPE), molecular beam epitaxy (MBE), or metalorganic chemical vapor deposition (MOCVD). For example, the layers of the semiconductor materials may be grown layer-by-layer on a substrate with a certain crystal lattice orientation (e.g., polar, nonpolar, or semi-polar orientation), such as a GaN, GaAs, or GaP substrate, or a substrate including, but not limited to, sapphire, silicon carbide, silicon, zinc oxide, boron nitride, lithium aluminate, lithium niobate, germanium, aluminum nitride, lithium gallate, partially substituted spinels, or quaternary tetragonal oxides sharing the beta-$LiAlO_2$ structure, where the substrate may be cut in a specific direction to expose a specific plane as the growth surface.

[0104] In the example shown in FIG. 7A, LED 700 may include a substrate 710, which may include, for example, a sapphire substrate or a GaN substrate. A semiconductor layer 720 may be grown on substrate 710. Semiconductor layer 720 may include a III-V material, such as GaN, and may be p-doped (e.g., with Mg, Ca, Zn, or Be) or n-doped (e.g., with Si or Ge). One or more active layers 730 may be grown on semiconductor layer 720 to form an active region. Active layer 730 may include III-V materials, such as one or more InGaN layers, one or more AlInGaP layers, and/or one or more GaN layers, which may form one or more heterostructures, such as one or more quantum wells or MQWs. A semiconductor layer 740 may be grown on active layer 730. Semiconductor layer 740 may include a III-V material, such as GaN, and may be p-doped (e.g., with Mg, Ca, Zn, or Be) or n-doped (e.g., with Si or Ge). One of semiconductor layer 720 and semiconductor layer 740 may be a p-type layer and the other one may be an n-type layer. Semiconductor layer 720 and semiconductor layer 740 sandwich active layer 730 to form the light emitting region. For example, LED 700 may include a layer of InGaN situated between a layer of p-type GaN doped with magnesium and a layer of n-type GaN doped with silicon or oxygen. In some embodiments, LED 700

may include a layer of AlInGaP situated between a layer of p-type AlInGaP doped with zinc or magnesium and a layer of n-type AlInGaP doped with selenium, silicon, or tellurium.

[0105] In some embodiments, an electron-blocking layer (EBL) (not shown in FIG. 7A) may be grown to form a layer between active layer 730 and at least one of semiconductor layer 720 or semiconductor layer 740. The EBL may reduce the electron leakage current and improve the efficiency of the LED. In some embodiments, a heavily-doped semiconductor layer 750, such as a P^+ or P^{++} semiconductor layer, may be formed on semiconductor layer 740 and act as a contact layer for forming an ohmic contact and reducing the contact impedance of the device. In some embodiments, a conductive layer 760 may be formed on heavily-doped semiconductor layer 750. Conductive layer 760 may include, for example, an indium tin oxide (ITO) or Al/Ni/Au film. In one example, conductive layer 760 may include a transparent ITO layer.

[0106] To make contact with semiconductor layer 720 (e.g., an n-GaN layer) and to more efficiently extract light emitted by active layer 730 from LED 700, the semiconductor material layers (including heavily-doped semiconductor layer 750, semiconductor layer 740, active layer 730, and semiconductor layer 720) may be etched to expose semiconductor layer 720 and to form a mesa structure that includes layers 720-760. The mesa structure may confine the carriers within the device. Etching the mesa structure may lead to the formation of mesa sidewalls 732 that may be orthogonal to the growth planes. A passivation layer 770 may be formed on mesa sidewalls 732 of the mesa structure. Passivation layer 770 may include an oxide layer, such as a SiO_2 layer, and may act as a reflector to reflect emitted light out of LED 700. A contact layer 780, which may include a metal layer, such as Al, Au, Ni, Ti, or any combination thereof, may be formed on semiconductor layer 720 and may act as an electrode of LED 700. In addition, another contact layer 790, such as an Al/Ni/Au metal layer, may be formed on conductive layer 760 and may act as another electrode of LED 700.

[0107] When a voltage signal is applied to contact layers 780 and 790, electrons and holes may recombine in active layer 730, where the recombination of electrons and holes may cause photon emission. The wavelength and energy of the emitted photons may depend on the energy bandgap between the valence band and the conduction band in active layer 730. For example, InGaN active layers may emit green or blue light, AlGaN active layers may emit blue to ultraviolet light, while AlInGaP active layers may emit red, orange, yellow, or green light. The emitted photons may be reflected by passivation layer 770 and may exit LED 700 from the top (e.g., conductive layer 760 and contact layer 790) or bottom (e.g., substrate 710).

[0108] In some embodiments, LED 700 may include one or more other components, such as a lens, on the light emission surface, such as substrate 710, to focus or collimate the emitted light or couple the emitted light into a waveguide. In some embodiments, an LED may include a mesa of another shape, such as planar, conical, semi-parabolic, or parabolic, and a base area of the mesa may be circular, rectangular, hexagonal, or triangular. For example, the LED may include a mesa of a curved shape (e.g., paraboloid shape) and/or a non-curved shape (e.g., conic shape). The mesa may be truncated or non-truncated.

[0109] **FIG. 7B** is a cross-sectional view of an example of an LED 705 having a parabolic mesa structure. Similar to LED 700, LED 705 may include multiple layers of semiconductor materials, such as multiple layers of III-V semiconductor materials. The semiconductor material layers may be epitaxially grown on a substrate 715, such as a GaN substrate or a sapphire substrate. For example, a semiconductor layer 725 may be grown on substrate 715. Semiconductor layer 725 may include a III-V material, such as GaN, and may be p-doped (*e.g.*, with Mg, Ca, Zn, or Be) or n-doped (*e.g.*, with Si or Ge). One or more active layer 735 may be grown on semiconductor layer 725. Active layer 735 may include III-V materials, such as one or more InGaN layers, one or more AlInGaP layers, and/or one or more GaN layers, which may form one or more heterostructures, such as one or more quantum wells. A semiconductor layer 745 may be grown on active layer 735. Semiconductor layer 745 may include a III-V material, such as GaN, and may be p-doped (*e.g.*, with Mg, Ca, Zn, or Be) or n-doped (*e.g.*, with Si or Ge). One of semiconductor layer 725 and semiconductor layer 745 may be a p-type layer and the other one may be an n-type layer.

[0110] To make contact with semiconductor layer 725 (e.g., an n-type GaN layer) and to more efficiently extract light emitted by active layer 735 from LED 705, the semiconductor layers may be etched to expose semiconductor layer 725 and to form a mesa structure that includes layers 725-745. The mesa structure may confine carriers within the injection area of the device. Etching the mesa structure may lead to the formation of mesa side walls (also referred to herein as facets) that may be non-parallel with, or in some cases, orthogonal, to the growth planes associated with crystalline growth of layers 725-745.

[0111] As shown in FIG. 7B, LED 705 may have a mesa structure that includes a flat top. A dielectric layer 775 (e.g., SiO_2 or SiNx) may be formed on the facets of the mesa structure. In some embodiments, dielectric layer 775 may include multiple layers of dielectric materials. In some embodiments, a metal layer 795 may be formed on dielectric layer 775. Metal layer 795 may include one or more metal or metal alloy materials, such as aluminum (Al), silver (Ag), gold (Au), platinum (Pt), titanium (Ti), copper (Cu), or any combination

thereof. Dielectric layer 775 and metal layer 795 may form a mesa reflector that can reflect light emitted by active layer 735 toward substrate 715. In some embodiments, the mesa reflector may be parabolic-shaped to act as a parabolic reflector that may at least partially collimate the emitted light.

[0112] Electrical contact 765 and electrical contact 785 may be formed on semiconductor layer 745 and semiconductor layer 725, respectively, to act as electrodes. Electrical contact 765 and electrical contact 785 may each include a conductive material, such as Al, Au, Pt, Ag, Ni, Ti, Cu, or any combination thereof (e.g., Ag/Pt/Au or Al/Ni/Au), and may act as the electrodes of LED 705. In the example shown in FIG. 7B, electrical contact 785 may be an n-contact, and electrical contact 765 may be a p-contact. Electrical contact 765 and semiconductor layer 745 (e.g., a p-type semiconductor layer) may form a back reflector for reflecting light emitted by active layer 735 back toward substrate 715. In some embodiments, electrical contact 765 and metal layer 795 include same material(s) and can be formed using the same processes. In some embodiments, an additional conductive layer (not shown) may be included as an intermediate conductive layer between the electrical contacts 765 and 785 and the semiconductor layers.

[0113] When a voltage signal is applied across electrical contacts 765 and 785, electrons and holes may recombine in active layer 735. The recombination of electrons and holes may cause photon emission, thus producing light. The wavelength and energy of the emitted photons may depend on the energy bandgap between the valence band and the conduction band in active layer 735. For example, InGaN active layers may emit green or blue light, while AlInGaP active layers may emit red, orange, yellow, or green light. The emitted photons may propagate in many different directions, and may be reflected by the mesa reflector and/or the back reflector and may exit LED 705, for example, from the bottom side (e.g., substrate 715) shown in FIG. 7B. One or more other secondary optical components, such as a lens or a grating, may be formed on the light emission surface, such as substrate 715, to focus or collimate the emitted light and/or couple the emitted light into a waveguide.

[0114] One or two-dimensional arrays of the LEDs described above may be manufactured on a wafer to form light sources (e.g., light source 642). Drive circuits (e.g., drive circuit 644) may be fabricated, for example, on a silicon wafer using CMOS processes. The LEDs and the drive circuits on wafers may be diced and then bonded together, or may be bonded on the wafer level and then diced. Various bonding techniques can be used for bonding the LEDs and the drive circuits, such as adhesive bonding, metal-to-metal bonding, metal oxide bonding, wafer-to-wafer bonding, die-to-wafer bonding, hybrid bonding, and the like.

[0115] **FIGS. 8A-8D** illustrate an example of a method of hybrid bonding for arrays of LEDs according to certain embodiments. The hybrid bonding may generally include wafer cleaning and activation, high-precision alignment of contacts of one wafer with contacts of another wafer, dielectric bonding of dielectric materials at the surfaces of the wafers at room temperature, and metal bonding of the contacts by annealing at elevated temperatures. **FIG. 8A** shows a substrate 810 with passive or active circuits 820 manufactured thereon. As described above with respect to FIGS. 8A-8B, substrate 810 may include, for example, a silicon wafer. Circuits 820 may include drive circuits for the arrays of LEDs. A bonding layer may include dielectric regions 840 and contact pads 830 connected to circuits 820 through electrical interconnects 822. Contact pads 830 may include, for example, Cu, Ag, Au, Al, W, Mo, Ni, Ti, Pt, Pd, or the like. Dielectric materials in dielectric regions 840 may include SiCN, SiO_2, SiN, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, or the like. The bonding layer may be planarized and polished using, for example, chemical mechanical polishing, where the planarization or polishing may cause dishing (a bowl like profile) in the contact pads. The surfaces of the bonding layers may be cleaned and activated by, for example, an ion (e.g., plasma) or fast atom (e.g., Ar) beam 805. The activated surface may be atomically clean and may be reactive for formation of direct bonds between wafers when they are brought into contact, for example, at room temperature.

[0116] **FIG. 8B** illustrates a wafer 850 including an array of micro-LEDs 870 fabricated thereon as described above with respect to, for example, FIGS. 7A-8B. Wafer 850 may be a carrier wafer and may include, for example, GaAs, InP, GaN, AlN, sapphire, SiC, Si, or the like. Micro-LEDs 870 may include an n-type layer, an active region, and a p-type layer epitaxially grown on wafer 850. The epitaxial layers may include various III-V semiconductor materials described above, and may be processed from the p-type layer side to etch mesa structures in the epitaxial layers, such as substantially vertical structures, parabolic structures, conic structures, or the like. Passivation layers and/or reflection layers may be formed on the sidewalls of the mesa structures. P-contacts 880 and n-contacts 882 may be formed in a dielectric material layer 860 deposited on the mesa structures and may make electrical contacts with the p-type layer and the n-type layers, respectively. Dielectric materials in dielectric material layer 860 may include, for example, SiCN, SiO_2, SiN, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, or the like. P-contacts 880 and n-contacts 882 may include, for example, Cu, Ag, Au, Al, W, Mo, Ni, Ti, Pt, Pd, or the like. The top surfaces of p-contacts 880, n-contacts 882, and dielectric material layer 860 may form a bonding layer. The bonding layer may be planarized and polished using, for example, chemical mechanical polishing, where

the polishing may cause dishing in p-contacts 880 and n-contacts 882. The bonding layer may then be cleaned and activated by, for example, an ion (e.g., plasma) or fast atom (e.g., Ar) beam 815. The activated surface may be atomically clean and reactive for formation of direct bonds between wafers when they are brought into contact, for example, at room temperature.

[0117] **FIG. 8C** illustrates a room temperature bonding process for bonding the dielectric materials in the bonding layers. For example, after the bonding layer that includes dielectric regions 840 and contact pads 830 and the bonding layer that includes p-contacts 880, n-contacts 882, and dielectric material layer 860 are surface activated, wafer 850 and micro-LEDs 870 may be turned upside down and brought into contact with substrate 810 and the circuits formed thereon. In some embodiments, compression pressure 825 may be applied to substrate 810 and wafer 850 such that the bonding layers are pressed against each other. Due to the surface activation and the dishing in the contacts, dielectric regions 840 and dielectric material layer 860 may be in direct contact because of the surface attractive force, and may react and form chemical bonds between them because the surface atoms may have dangling bonds and may be in unstable energy states after the activation. Thus, the dielectric materials in dielectric regions 840 and dielectric material layer 860 may be bonded together with or without heat treatment or pressure.

[0118] **FIG. 8D** illustrates an annealing process for bonding the contacts in the bonding layers after bonding the dielectric materials in the bonding layers. For example, contact pads 830 and p-contacts 880 or n-contacts 882 may be bonded together by annealing at, for example, about 200-400 °C or higher. During the annealing process, heat 835 may cause the contacts to expand more than the dielectric materials (due to different coefficients of thermal expansion), and thus may close the dishing gaps between the contacts such that contact pads 830 and p-contacts 880 or n-contacts 882 may be in contact and may form direct metallic bonds at the activated surfaces.

[0119] In some embodiments where the two bonded wafers include materials having different coefficients of thermal expansion (CTEs), the dielectric materials bonded at room temperature may help to reduce or prevent misalignment of the contact pads caused by the different thermal expansions. In some embodiments, to further reduce or avoid the misalignment of the contact pads at a high temperature during annealing, trenches may be formed between micro-LEDs, between groups of micro-LEDs, through part or all of the substrate, or the like, before bonding.

[0120] After the micro-LEDs are bonded to the drive circuits, the substrate on which the micro-LEDs are fabricated may be thinned or removed, and various secondary optical

components may be fabricated on the light emitting surfaces of the micro-LEDs to, for example, extract, collimate, and redirect the light emitted from the active regions of the micro-LEDs. In one example, micro-lenses may be formed on the micro-LEDs, where each micro-lens may correspond to a respective micro-LED and may help to improve the light extraction efficiency and collimate the light emitted by the micro-LED. In some embodiments, the secondary optical components may be fabricated in the substrate or the n-type layer of the micro-LEDs. In some embodiments, the secondary optical components may be fabricated in a dielectric layer deposited on the n-type side of the micro-LEDs. Examples of the secondary optical components may include a lens, a grating, an antireflection (AR) coating, a prism, a photonic crystal, or the like.

[0121] **FIG. 9** illustrates an example of an LED array 900 with secondary optical components fabricated thereon according to certain embodiments. LED array 900 may be made by bonding an LED chip or wafer with a silicon wafer including electrical circuits fabricated thereon, using any suitable bonding techniques described above with respect to, for example, FIGS. 8A-8D. In the example shown in FIG. 9, LED array 900 may be bonded using a wafer-to-wafer hybrid bonding technique as described above with respect to FIG. 8A-8D. LED array 900 may include a substrate 910, which may be, for example, a silicon wafer. Integrated circuits 920, such as LED drive circuits, may be fabricated on substrate 910. Integrated circuits 920 may be connected to p-contacts 974 and n-contacts 972 of micro-LEDs 970 through interconnects 922 and contact pads 930, where contact pads 930 may form metallic bonds with p-contacts 974 and n-contacts 972. Dielectric layer 940 on substrate 910 may be bonded to dielectric layer 960 through fusion bonding.

[0122] The substrate (not shown) of the LED chip or wafer may be thinned or may be removed to expose the n-type layer 950 of micro-LEDs 970. Various secondary optical components, such as a spherical micro-lens 982, a grating 984, a micro-lens 986, an antireflection layer 988, and the like, may be formed in or on top of n-type layer 950. For example, spherical micro-lens arrays may be etched in the semiconductor materials of micro-LEDs 970 using a gray-scale mask and a photoresist with a linear response to exposure light, or using an etch mask formed by thermal reflowing of a patterned photoresist layer. The secondary optical components may also be etched in a dielectric layer deposited on n-type layer 950 using similar photolithographic techniques or other techniques. For example, micro-lens arrays may be formed in a polymer layer through thermal reflowing of the polymer layer that is patterned using a binary mask. The micro-lens arrays in the polymer layer may be used as the secondary optical components or may be used as the etch mask for

transferring the profiles of the micro-lens arrays into a dielectric layer or a semiconductor layer. The dielectric layer may include, for example, SiCN, SiO_2, SiN, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, or the like. In some embodiments, a micro-LED 970 may have multiple corresponding secondary optical components, such as a micro-lens and an anti-reflection coating, a micro-lens etched in the semiconductor material and a micro-lens etched in a dielectric material layer, a micro-lens and a grating, a spherical lens and an aspherical lens, and the like. Three different secondary optical components are illustrated in FIG. 9 to show some examples of secondary optical components that can be formed on micro-LEDs 970, which does not necessary imply that different secondary optical components are used simultaneously for every LED array.

[0123] **FIG. 10A** illustrates an example of a method of die-to-wafer bonding for arrays of LEDs according to certain embodiments. In the example shown in FIG. 10A, an LED array 1001 may include a plurality of LEDs 1007 on a carrier substrate 1005. Carrier substrate 1005 may include various materials, such as GaAs, InP, GaN, AlN, sapphire, SiC, Si, or the like. LEDs 1007 may be fabricated by, for example, growing various epitaxial layers, forming mesa structures, and forming electrical contacts or electrodes, before performing the bonding. The epitaxial layers may include various materials, such as GaN, InGaN, (AlGaIn)P, (AlGaIn)AsP, (AlGaIn)AsN, (Eu:InGa)N, (AlGaIn)N, or the like, and may include an n-type layer, a p-type layer, and an active layer that includes one or more heterostructures, such as one or more quantum wells or MQWs. The electrical contacts may include various conductive materials, such as a metal or a metal alloy.

[0124] A wafer 1003 may include a base layer 1009 having passive or active integrated circuits (e.g., drive circuits 1011) fabricated thereon. Base layer 1009 may include, for example, a silicon wafer. Drive circuits 1011 may be used to control the operations of LEDs 1007. For example, the drive circuit for each LED 1007 may include a 2T1C pixel structure that has two transistors and one capacitor. Wafer 1003 may also include a bonding layer 1013. Bonding layer 1013 may include various materials, such as a metal, an oxide, a dielectric, CuSn, AuTi, and the like. In some embodiments, a patterned layer 1015 may be formed on a surface of bonding layer 1013, where patterned layer 1015 may include a metallic grid made of a conductive material, such as Cu, Ag, Au, Al, or the like.

[0125] LED array 1001 may be bonded to wafer 1003 via bonding layer 1013 or patterned layer 1015. For example, patterned layer 1015 may include metal pads or bumps made of various materials, such as CuSn, AuSn, or nanoporous Au, that may be used to align LEDs 1007 of LED array 1001 with corresponding drive circuits 1011 on wafer 1003. In one

example, LED array 1001 may be brought toward wafer 1003 until LEDs 1007 come into contact with respective metal pads or bumps corresponding to drive circuits 1011. Some or all of LEDs 1007 may be aligned with drive circuits 1011, and may then be bonded to wafer 1003 via patterned layer 1015 by various bonding techniques, such as metal-to-metal bonding. After LEDs 1007 have been bonded to wafer 1003, carrier substrate 1005 may be removed from LEDs 1007.

[0126] For high-resolution micro-LED display panel, due to the small pitches of the micro-LED array and the small dimensions of individual micro-LEDs, it can be challenging to electrically connect the drive circuits to the electrodes of the LEDs. For example, in the face-to-face bonding techniques describe above, it is difficult to precisely align the bonding pads on the micro-LED devices with the bonding pads on the drive circuits and form reliable bonding at the interfaces that may include both dielectric materials (e.g., SiO_2, SiN, or SiCN) and metal (e.g., Cu, Au, or Al) bonding pads. In particular, when the pitch of the micro-LED device is about 2 or 3 microns or lower, the bonding pads may have a linear dimension less than about 1 μm in order to avoid shorting to adjacent micro-LEDs and to improve bonding strength for the dielectric bonding. However, small bonding pads may be less tolerant to misalignments between the bonding pads, which may reduce the metal bonding area, increase the contact resistance (or may even be an open circuit), and/or cause diffusion of metals to the dielectric materials and the semiconductor materials. Thus, precise alignment of the bonding pads on surfaces of the micro-LED arrays and bonding pads on surfaces of CMOS backplane may be needed in the conventional processes. However, the accuracy of die-to-wafer or wafer-to-wafer bonding alignment using state-of-art equipment may be on the order of about 0.5 μm or about 1μm, which may not be adequate for bonding the small-pitch micro-LED arrays (e.g., with a linear dimension of the bonding pads on the order of 1 μm or shorter) to CMOS drive circuits.

[0127] In some implementations, to avoid precise alignment for the bonding, a micro-LED wafer may be bonded to a CMOS backplane after the epitaxial layer growth and before the formation of individual micro-LED on the micro-LED wafer, where the micro-LED wafer and the CMOS backplane may be bonded through metal-to-metal bonding of two solid metal bonding layers on the two wafers. No alignment would be needed to bond the solid contiguous metal bonding layers. After the bonding, the epitaxial layers on the micro-LED wafer and the metal bonding layers may be etched to form individual micro-LEDs. The etching process may have much higher alignment accuracy and thus may form individual

micro-LEDs that align with the underlying pixel drive circuits.

[0128] **FIG. 10B** illustrates an example of a method of wafer-to-wafer bonding for arrays of LEDs according to certain embodiments. As shown in FIG. 10B, a first wafer 1002 may include a substrate 1004, a first semiconductor layer 1006, active layers 1008, and a second semiconductor layer 1010. Substrate 1004 may include various materials, such as GaAs, InP, GaN, AlN, sapphire, SiC, Si, or the like. First semiconductor layer 1006, active layers 1008, and second semiconductor layer 1010 may include various semiconductor materials, such as GaN, InGaN, (AlGaIn)P, (AlGaIn)AsP, (AlGaIn)AsN, (AlGaIn)Pas, (Eu:InGa)N, (AlGaIn)N, or the like. In some embodiments, first semiconductor layer 1006 may be an n-type layer, and second semiconductor layer 1010 may be a p-type layer. For example, first semiconductor layer 1006 may be an n-doped GaN layer (e.g., doped with Si or Ge), and second semiconductor layer 1010 may be a p-doped GaN layer (e.g., doped with Mg, Ca, Zn, or Be). Active layers 1008 may include, for example, one or more GaN layers, one or more InGaN layers, one or more AlInGaP layers, and the like, which may form one or more heterostructures, such as one or more quantum wells or MQWs.

[0129] In some embodiments, first wafer 1002 may also include a bonding layer. Bonding layer 1012 may include various materials, such as a metal, an oxide, a dielectric, CuSn, AuTi, or the like. In one example, bonding layer 1012 may include p-contacts and/or n-contacts (not shown). In some embodiments, other layers may also be included on first wafer 1002, such as a buffer layer between substrate 1004 and first semiconductor layer 1006. The buffer layer may include various materials, such as polycrystalline GaN or AlN. In some embodiments, a contact layer may be between second semiconductor layer 1010 and bonding layer 1012. The contact layer may include any suitable material for providing an electrical contact to second semiconductor layer 1010 and/or first semiconductor layer 1006.

[0130] First wafer 1002 may be bonded to wafer 1003 that includes drive circuits 1011 and bonding layer 1013 as described above, via bonding layer 1013 and/or bonding layer 1012. Bonding layer 1012 and bonding layer 1013 may be made of the same material or different materials. Bonding layer 1013 and bonding layer 1012 may be substantially flat. First wafer 1002 may be bonded to wafer 1003 by various methods, such as metal-to-metal bonding, eutectic bonding, metal oxide bonding, anodic bonding, thermo-compression bonding, ultraviolet (UV) bonding, and/or fusion bonding.

[0131] As shown in FIG. 10B, first wafer 1002 may be bonded to wafer 1003 with the p-side (e.g., second semiconductor layer 1010) of first wafer 1002 facing down (i.e., toward wafer 1003). After bonding, substrate 1004 may be removed from first wafer 1002, and first

wafer 1002 may then be processed from the n-side. The processing may include, for example, the formation of certain mesa shapes for individual LEDs, as well as the formation of optical components corresponding to the individual LEDs.

[0132] **FIG. 11** is a simplified block diagram of an example of a display device 1100 according to certain embodiments. Display device 1100 may include a display panel 1130 that includes an array (e.g., a 2-D array) of pixels 1112. Display panel 1130 may be an example of display panel 640. FIG. 11 illustrates the block diagram of one pixel 1112, which may be similar to other pixels 1112 in the array of pixels. Various functional components of each pixel 1112 may generate digital PWM signals to control a micro-LED. In the illustrated example, each pixel 1112 may include a micro-LED 1105, which may emit light at an intensity level that is controlled by the PWM signals. The circuits that control micro-LED 1105 in pixel 1112 may include a memory device 1102, a comparator 1104, a PWM latch circuit 1106, and an LED drive circuit 1108. Memory device 1102 may be a part of pixel 1112 or may be outside of pixel 1112. Memory device 1102 may include, for example, SRAM cells, and may store the intensity data for pixel 1112. Memory device 1102 may be connected to comparator 1104, which may be connected to PWM latch circuit 1106. PWM latch circuit 1106 may be connected to LED drive circuit 1108 to control LED drive circuit 1108 to provide a pulse width modulation to a drive current that may be an approximately constant current. LED drive circuit 1108 may drive micro-LED 1105 with the drive current for different periods of time based on the PWM signals to emit different amounts of light during a PWM frame (also referred to as a PWM cycle). In general, the longer micro-LED 1105 is driven at the current level within a PWM cycle, the brighter micro-LED 1105 may be perceived by an observer.

[0133] Display device 1100 may also include a row driver 1114, a column driver 1116, and a counter 1110. In some embodiments, row driver 1114, column driver 1116, and counter 1110 may be parts of the periphery circuits of display panel 1130. Row driver 1114 and column driver 1116 may be connected to pixels 1112. For example, row driver 1114 may be connected to memory device 1102, comparator 1104, and PWM latch circuit 1106. Column driver 1116 may be connected to memory device1102. Display device 1100 may further include a controller 1140, which may include a processor 1142 and a display memory device 1144. Controller 1140 may be connected to row driver 1114 and column driver 1116 to control the operations of row driver 1114 and column driver 1116. For example, processor 1142 of controller 1140 may provide control signals to row driver 1114 and column driver 1116 to operate pixels 1112. Counter 1110 may be coupled to display memory device 1144,

which may store, for example, calibration data and/or a gamma correction look-up table (LUT).

[0134] Memory device 1102 may include digital data storage cells, such as cells of SRAM or some other types of memory. For example, memory device 1102 may include multiple memory cells for storing the display data (e.g., intensity data) for pixel 1112. Each cell in memory device 1102 may be connected to row driver 1114 via a word line (WL) and may be connected to column driver 1116 via a bit line (BL) and an inverse bit line ($\overline{BL}$). Memory device 1102 may receive WL signals from row driver 1114 for memory word selection, and may receive, from column driver 1116, control words in the form of data bits for writing to the selected memory cells. The bit values of data bits define the intensity level of the pixel for a PWM frame. The number of data bits (or bitcells) in a control word may vary. In one example, each control word in memory device 1102 may include 3 bitcells storing a 3-bit value representing one of eight levels of brightness (e.g., 000, 001, 010, 011, 100, 101, 110, and 111). In another example, each control word in the memory device 1102 may include 8 bitcells storing an 8-bit value representing one of 256 levels of brightness.

[0135] Counter 1110 may be used to generate counter values (e.g., a clock cycle count) based on a clock signal. The counter value of counter 1110 may be compared with the value of a control word from memory device 1102 by comparator 1104 to generate a comparison result. For example, the comparison result may be generated based on an exclusive OR (XOR) of each data bit in the control word and the corresponding bit of the counter value. Comparator 1104 may include a dynamic comparison node that switches between a high and low level according to the comparison result, and may output the comparison result to PWM latch circuit 1106 to generate PWM signals.

[0136] LED drive circuit 1108 may include one or more LED drive transistors. One of the LED drive transistors may have a source or drain terminal connected to micro-LED 1105. One of the LED drive transistors may include a gate terminal connected to PWM latch circuit 1106 to receive the PWM signal for modulating the current flowing through the source and drain terminals of the driving transistor into micro-LED 1105.

[0137] **FIGS. 12A-12F** illustrate an example of a method of fabricating a micro-LED device using alignment-free metal-to-metal bonding and post-bonding mesa formation processes. **FIG. 12A** shows a micro-LED wafer 1202 including epitaxial layers grown on a substrate 1210. As described above, substrate 1210 may include, for example, a GaN, GaAs, or GaP substrate, or a substrate including, but not limited to, sapphire, silicon carbide, silicon, zinc oxide, boron nitride, lithium aluminate, lithium niobate, germanium, aluminum nitride,

lithium gallate, partially substituted spinels, or quaternary tetragonal oxides sharing the beta-$LiAlO_2$ structure, where the substrate may be cut in a specific direction to expose a specific plane (e.g., c-plane or a semipolar plane) as the growth surface. In some embodiments, a buffer layer 1212 may be formed on substrate 1210 to improve the lattice matching of the epitaxial layers, thereby reducing stress and defects in the epitaxial layers. The epitaxial layers may include an n-type semiconductor layer 1214 (e.g., a GaN layer doped with Si or Ge), an active region 1216, and a p-type semiconductor layer 1218 (e.g., a GaN layer doped with Mg, Ca, Zn, or Be). Active region 1216 may include multiple quantum wells or an MQW formed by quantum well layers (e.g., InGaN layer) sandwiched by barrier layers (e.g., GaN layer) as described above. The epitaxial layers may be grown layer-by-layer on substrate 1210 or buffer layer 1212 using techniques such as VPE, LPE, MBE, or MOCVD.

[0138] In the epitaxial growth processes, dopants (e.g., Mg) used to dope the p-type semiconductor layer (*e.g.*, Mg-doped GaN layer) may remain in the reactor and/or on the epitaxial surface after the introduction of Mg precursors into the reactor. For example, the source for Mg doping (*e.g.*, bis(cyclopentadienyl) magnesium (Cp_2Mg)) may be adsorbed onto reactor lines and walls and may be released in the gas phase in subsequent processes. A surface riding effect can also contribute to the residual Mg due to a Mg-rich layer formed on the surface of the p-GaN layer. Thus, if the quantum-well layers are grown on the Mg-rich p-GaN layer after the growth of the p-GaN layer using Mg dopants, the quantum-well layers may be contaminated with Mg dopants even after the Mg source is turned off, which may be referred to as the Mg-memory effect and may manifest as a slow decay tail of Mg into subsequent epitaxial layers. Mg can contaminate the MQW layers to form non-radiative recombination centers, which may be caused by Mg-related point defects, Mg interstitials, or Mg-related complexes.

[0139] In addition, for p-type GaN layers formed using, for example, MOCVD, the dopants (*e.g.*, Mg) may be passivated due to the incorporation of atomic hydrogen (which exists in the form of H^+) during growth and the formation of Mg-H complexes. Therefore, a post-growth activation of the dopants is generally performed to release mobile holes. The activation of the dopants in the p-GaN layer may include breaking the Mg-H bonds and driving the H^+ out of the p-GaN layer at elevated temperatures (*e.g.*, above 700 °C) to activate the Mg dopants. Insufficient activation of the p-GaN layer may lead to an open circuit, a poor performance, or a premature punch-through breakdown of the LED device. If p-type GaN layer is grown before the growth of the active region and the n-type layer, to drive out hydrogen, positively charged H^+ ions need to diffuse across the p-n junction and through the n-GaN layer that is

exposed. However, because of the depletion field in the p-n junction (with a direction from the n-type layer to the p-type layer), positively charged H^+ ions may not be able to diffuse from the p-type layer to the n-type layer across the p-n junction. Furthermore, hydrogen may have a much higher diffusion barrier and thus a much lower diffusivity in n-type GaN compared with in p-type GaN. Thus, the hydrogen ions may not diffuse through the n-type layer to the exposed top surface of the n-type layer. Moreover, the activation may not be performed right after the p-doping and before the growth of the active region either, because the subsequent growth may be performed in the presence of high pressure ammonia (NH_3) in order to avoid decomposition of GaN at the high growth temperatures, and thus a semiconductor layer (e.g., the p-type semiconductor layer) that was activated may be re-passivated due to the presence of ammonia.

[0140] Therefore, in general, during the growth of the epitaxial layers, n-type semiconductor layer 1214 may be grown first. P-type semiconductor layer 1218 may be grown after the growth of active region 1216 to avoid contamination of active region 1216 and facilitate activation of the dopants in the p-type semiconductor layer.

[0141] **FIG. 12B** shows a reflector layer 1220 and a bonding layer 1222 formed on p-type semiconductor layer 1218. Reflector layer 1220 may include, for example, a metal layer such as an aluminum layer, a silver layer, or a metal alloy layer, or a distributed Bragg reflector formed by conductive materials (e.g., semiconductor materials) or including conductive vias. In some embodiments, reflector layer 1220 may include one or more sublayers. Reflector layer 1220 may be formed on p-type semiconductor layer 1218 in a deposition process. Bonding layer 1222 may include a metal layer, such as a titanium layer, a copper layer, an aluminum layer, a gold layer, or a metal alloy layer. In some embodiments, bonding layer 1222 may include a eutectic alloy, such as Au-In, Au-Sn, Au-Ge, or Ag-In. Bonding layer 1222 may be formed on reflector layer 1220 by a deposition process and may include one or more sublayers.

[0142] **FIG. 12C** shows a backplane wafer 1204 that includes a substrate 1230 with electrical circuits formed thereon. The electrical circuits may include digital and analog pixel drive circuits for driving individual micro-LEDs. A plurality of metal pads 1234 (e.g., copper or tungsten pads) may be formed in a dielectric layer 1232 (e.g., including SiO_2 or SiN). In some embodiments, each metal pad 1234 may be an electrode (e.g., anode) for a micro-LED. In some embodiments, pixel drive circuits for each micro-LED may be formed in an area matching the size of a micro-LED (e.g., about 2μm × 2μm), where the pixel drive circuits and

the micro-LED may collectively form a pixel of a micro-LED display panel. Even though FIG. 12C only shows metal pads 1234 formed in one metal layer in one dielectric layer 1232, backplane wafer 1204 may include two or more metal layers formed in dielectric materials and interconnected by, for example, metal vias, as in many CMOS integrated circuits. In some embodiments, a planarization process, such as a CMP process, may be performed to planarize the exposed surfaces of metal pads 1234 and dielectric layer 1232. A bonding layer 1240 may be formed on dielectric layer 1232 and may be in physical and electrical contact with metal pads 1234. As bonding layer 1222, bonding layer 1240 may include a metal layer, such as a titanium layer, a copper layer, an aluminum layer, a gold layer, a metal alloy layer, or a combination thereof. In some embodiments, bonding layer 1240 may include a eutectic alloy. In some embodiments, only one of bonding layer 1240 or bonding layer 1222 may be used.

[0143] **FIG. 12D** shows that micro-LED wafer 1202 and backplane wafer 1204 may be bonded together to form a wafer stack 1206. Micro-LED wafer 1202 and backplane wafer 1204 may be bonded by the metal-to-metal bonding of bonding layer 1222 and bonding layer 1240. The metal-to-metal bonding may be based on chemical bonds between the metal atoms at the surfaces of the metal bonding layers. The metal-to-metal bonding may include, for example, thermo-compression bonding, eutectic bonding, or transient liquid phase (TLP) bonding. The metal-to-metal bonding process may include, for example, surface planarization, wafer cleaning (e.g., using plasma or solvents) at room temperatures, and compression and annealing at elevated temperatures, such as about 250 °C or higher, to cause diffusion of atoms. In eutectic bonding, a eutectic alloy including two or more metals and with a eutectic point lower than the melting point of the one or more metals may be used for low-temperature wafer bonding. Because the eutectic alloy may become a liquid at the elevated temperature, eutectic bonding may be less sensitive to surface flatness irregularities, scratches, particles contamination, and the like. After the bonding, buffer layer 1212 and substrate 1210 may be thinned or removed by, for example, etching, back grinding, or laser lifting, to expose n-type semiconductor layer 1214.

[0144] **FIG. 12E** shows that wafer stack 1206 may be etched from the side of the exposed n-type semiconductor layer 1214 to form mesa structures 1208 for individual micro-LEDs. As shown in FIG. 12E, the etching may include etching through n-type semiconductor layer 1214, active region 1216, p-type semiconductor layer 1218, reflector layer 1220, and bonding layers 1222 and 1240, in order to singulate and electrically isolate mesa structures 1208. Thus, each singulated mesa structure 1208 may include n-type semiconductor layer 1214,

active region 1216, p-type semiconductor layer 1218, reflector layer 1220, and bonding layers 1222 and 1240. To perform the etching, an etch mask layer may be formed on n-type semiconductor layer 1214. The etch mask layer may be patterned by aligning a photomask with the backplane wafer (e.g., using alignment marks on backplane wafer 1204) such that the patterned etch mask formed in the etch mask layer may align with metal pads 1234. Therefore, regions of the epitaxial layers and bonding layers above metal pads 1234 may not be etched. Dielectric layer 1232 may be used as the etch-stop layer for the etching. Even though FIG. 12E shows that mesa structures 1208 have substantially vertical sidewalls, mesa structures 1208 may have other shapes as described above, such as a conical shape, a parabolic shape, or a truncated pyramid shape.

[0145] **FIG. 12F** shows that a passivation layer 1250 may be formed on sidewalls of mesa structures 1208, and a sidewall reflector layer 1252 may be formed on passivation layer 1250. Passivation layer 1250 may include a dielectric layer (e.g., SiO_2 or SiN) or an undoped semiconductor layer. Sidewall reflector layer 1252 may include, for example, a metal (e.g., Al) or a metal alloy. In some embodiments, gaps between mesa structures 1208 may be filled with a dielectric material 1254. Passivation layer 1250, sidewall reflector layer 1252, and/or dielectric material 1254 may be formed using suitable deposition techniques, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced chemical vapor deposition (PECVD), atomic-layer deposition (ALD), laser metal deposition (LMD), or sputtering. In some embodiments, sidewall reflector layer 1252 may fill the gaps between mesa structures 1208. In some embodiments, a planarization process may be performed after the deposition of passivation layer 1250, sidewall reflector layer 1252, and/or dielectric material 1254. A common electrode layer 1260, such as a transparent conductive oxide (TCO) layer (e.g., an ITO layer) or a thin metal layer that may be transparent to light emitted in active region 1216, may be formed on the n-type semiconductor layer 1214 to form n-contacts and a common cathode for the micro-LEDs.

[0146] **FIG. 13** illustrates an example of a pixel 1300 of a common-cathode micro-LED display device that may be fabricated using the method described above with respect to FIGS. 12A-12F. In the illustrated example, pixel 1300 may include a digital control circuit 1310, an analog drive circuit 1320, and a micro-LED 1330. Digital control circuit 1310 may include CMOS circuits that may include memory devices (e.g., SRAM cells 1312) for storing display data, as described above with respect to memory device 1102. Digital control circuit 1310 may also include a comparator 1316, which may be similar to comparator 1104 described above and may be used to compare a clock counter value with the display data stored in

SRAM cells 1312 to generate a high or low output signal based on the comparison result. Digital control circuit 1310 may further include a PWM latch 1314, which may be similar to PWM latch circuit 1106 described above and may be used to generate PWM signals for modulating the micro-LED drive current. In some embodiments, PWM latch 1314 may terminate the PWM output pulses based on outputs signals from, for example, comparator 1316. In some embodiments, digital control circuits 1310 for the pixels of the micro-LED display device may be fabricated on a separate Si wafer and may receive power from a low-voltage (e.g., about 1 V) voltage supply or voltage regulator. Because analog drive circuits are not fabricated on the silicon wafer, there may be more room to fit more SRAM cells and/or other circuits (e.g., design-for-test circuits) for each pixel in digital control circuit 1310.

[0147] Analog drive circuit 1320 may be fabricated on the silicon wafer or a different wafer (or substrate), such as an indium–gallium–zinc–oxide (IGZO) layer. In the illustrated example, analog drive circuit 1320 may include a level shifter 1325 at the interface between low-voltage digital circuits and medium-voltage analog circuits. In some embodiments, level shifter 1325 may be implemented in digital control circuit 1310. The analog drive circuit shown in FIG. 13 may include a 2T1C pixel structure that includes two transistors T1 (1322) and T2 (1324), and a capacitor 1328 for storing an analog signal for the pixel (e.g., analog display data or analog calibration signal for the pixel). The analog signal may be stored at capacitor 1328 or the gate of transistor T2 (1324) through transistor T1 (1322) when the scan signal is active. The analog signal at the gate of transistor T2 (1324) may control the I_{DS} of transistor T2 (1324), which is supplied to micro-LED 1330 as the drive current for micro-LED 1330. In the illustrated example, transistor T2 (1324) may be a p-channel transistor. A third transistor 1326 may be controlled by the output of PWM latch 1314 (e.g., through level shifter 1325) to provide the drive current from transistor T2 (1324) to an anode 1321 of micro-LED 1330, or to disconnect anode 1321 of micro-LED 1330 from the 2T1C pixel structure. Third transistor 1326 may be a p-channel transistor or an n-channel transistor. In some embodiments, for each image frame, third transistors 1326 for micro-LEDs in a same row or column may be turned on at the same time, such that the micro-LEDs on the row or column may receive drive current and start to emit light at about the same time. Third transistors 1326 for micro-LEDs in a row or column may be turned off individually and independently by respective PWM signals generated by PWM latches 1314 and comparators 1316 based on a clock counter value and respective display data stored in SRAM cells 1312.

[0148] Micro-LED 1330 may emit red, green, or blue light in an active region (e.g., a

quantum well or a multi-quantum well). Micro-LED 1330 may share a common cathode with other micro-LEDs on the micro-LED display device. The perceived brightness of the emitted light from micro-LED 1330 may be controlled by the drive current and/or the duration of the light emission. Due to manufacture variations in the analog drive circuits and micro-LEDs 1330, the analog drive voltage at the gate of transistor T2 (and thus the drive current) to achieve a certain light emission intensity may be different from pixel to pixel. Therefore, the analog drive voltage (and thus the drive current) of each pixel in the display device may be calibrated in order to appropriately drive the micro-LEDs to achieve a uniform maximum brightness or light intensity. The calibrated maximum analog drive voltage may be stored, and may be reloaded into the pixel periodically to refresh the analog drive voltage for each pixel.

[0149] **FIG. 14** includes a simplified block diagram of an example of a common-cathode micro-LED display device 1400. Each pixel of common-cathode micro-LED display device 1400 may be controlled and driven by the circuits shown in, for example, FIG. 13. In the illustrated example, pixels drive circuits 1410 may need both a positive voltage level (e.g., Vdd of FIG. 13, which may be at or greater than about 1 V) supplied by a voltage source 1430 (e.g., a voltage regulator) and a negative voltage level (e.g., about -3 V to about -5 V) supplied by a voltage source 1440 (e.g., a voltage regulator) to the common cathode of micro-LEDs 1420 (e.g., cathode of micro-LED 1330). Thus, as shown in FIGS. 13 and 14, the drive current may flow from voltage source 1430 (e.g., Vdd), through pixel drive circuits 1410 (e.g., transistor T2 (1324) and third transistor 1326), micro-LEDs 1420 (e.g., micro-LED 1330), and voltage source 1440 connected the cathodes of micro-LEDs 1420. Therefore, the power rail design for pixel drive circuits 1410 may be complex and the efficiency of the voltage supplies may be low.

[0150] According to certain embodiments, a micro-LED display device may include common-anode micro-LEDs, and corresponding drive circuits that may include a voltage supply (e.g., a first voltage regulator) for supplying a positive voltage level to digital pixel drive circuits (e.g., timing control circuits) and another voltage supply (e.g., a second voltage regulator) for supplying a positive voltage level (and drive current) to the common anode of the micro-LEDs. In some embodiments, the micro-LED display device may include multiple arrays of micro-LEDs, where each array of micro-LEDs may emit light in a respective wavelength ranges (e.g., red, green, or blue light) and may have a common anode that receives a positive voltage level (and drive current) from a respective voltage supply. Thus, the drive circuits for the common-anode micro-LEDs may not need negative voltage levels

and can have higher efficiency. In addition, the current driving transistors in the common-anode micro-LED devices can be n-channel transistors that may have smaller sizes than p-channel transistors for driving the same current. Therefore, the common-anode pixel drive circuit can use a smaller semiconductor area and may be better suitable for, in particular, small micro-LEDs with in-pixel drive circuits.

[0151] In some embodiments, the micro-LED display device may include GaN-based micro-LEDs (e.g., including quantum wells formed by InGaN/GaN layers) and may be made, for example, by epitaxially growing a p-type semiconductor layer after growing an n-type semiconductor layer and active layers on a growth substrate, bonding a carrier substrate to the p-type semiconductor layer, removing the growth substrate to expose the n-type semiconductor layer, forming a solid metal bonding layer on the exposed n-type semiconductor layer, bonding the metal bonding layer formed on the n-type semiconductor layer to a metal bonding layer of a backplane wafer, removing the carrier substrate from the bonded wafer stack to expose the p-type semiconductor layer, etching the epitaxial layers and the metal bonding layers from the side of the p-type semiconductor layer to form mesa structures of singulated micro-LEDs, and depositing a common anode layer (e.g., a transparent conductive layer) on the p-type semiconductor layer.

[0152] In some embodiments, the micro-LED display device may include InGaP-based micro-LEDs (e.g., including quantum wells formed by InGaP/AlGaInP layers) and may be made, for example, by epitaxially growing an n-type semiconductor layer after growing a p-type semiconductor layer and active layers on a growth substrate, forming a metal bonding layer on the n-type semiconductor layer, bonding the metal bonding layer formed on the n-type semiconductor layer to a metal bonding layer of a backplane wafer, removing the growth substrate from the bonded wafer stack to expose the p-type semiconductor layer, etching the epitaxial layers and the metal bonding layers from the side of the p-type semiconductor layer to form mesa structures of singulated micro-LEDs, and depositing a common anode layer (e.g., a transparent conductive layer) on the p-type semiconductor layer.

[0153] In some embodiments, the micro-LED display device may be made, for example, by obtaining a layer stack that includes a p-type semiconductor layer, active layers, and an exposed n-type semiconductor layer as described above; etching the layer stack from the side of the n-type semiconductor layer to form individual mesa structures and expose regions of the p-type semiconductor layer; forming an array of p-contacts at the expose regions of the p-type semiconductor layer and a common anode layer (e.g., a contiguous metal layer) on the array of p-contacts; forming n-contacts on the n-type semiconductor layer of the mesa

structures; forming bonding pads that are electrically connected to the p-contacts and n-contacts; and aligning and bonding the bonding pads to bonding pads on a backplane wafer.

[0154] **FIGS. 15A-15G** illustrate an example of a process for fabricating a common-anode GaN-based micro-LED devices according to certain embodiments. It is noted that the operations and processes illustrated in FIGS. 15A-15G provide particular processes for fabricating common-anode micro-LED devices. Other sequences of operations can also be performed according to alternative embodiments. For example, alternative embodiments may perform the operation in a different order. Moreover, the individual operations illustrated in FIGS. 15A-15G can include multiple sub-operations that can be performed in various sequences as appropriate for the individual operation. Furthermore, some operations can be added or removed depending on the particular applications. In some implementations, two or more operations may be performed in parallel. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0155] **FIG. 15A** shows a first wafer 1502 (e.g., a micro-LED wafer) that may be fabricated or otherwise obtained. First wafer 1502 may be similar to micro-LED wafer 1202 describe above with respect to FIG. 12A and may be fabricated using similar epitaxial growth processes, and thus is not described again in detail in this section. In the illustrated example, first wafer 1502 may include a first substrate 1510 and epitaxial layers grown on first substrate 1510. The epitaxial layers may include an optional buffer layer 1512, an n-type semiconductor layer 1514 (e.g., an n-doped GaN layer), an active light-emitting layer 1516 (e.g., including InGaN/GaN MQW layers), and a p-type semiconductor layer 1518 (e.g., a p-doped GaN layer). First substrate 1510 may include, for example, GaN, sapphire, silicon, or other substrates described above with respect to, for example, FIG. 7A and FIG. 12A. In the illustrated example, buffer layer 1512 may be grown on first substrate 1510, and n-type semiconductor layer 1514 may be grown on buffer layer 1512, for example, using techniques discussed above such as VPE, LPE, MBE, or MOCVD. Active light-emitting layer 1516 may be grown over n-type semiconductor layer 1514, and then p-type semiconductor layer 1518 may be grown on active light-emitting layer 1516.

[0156] **FIG. 15B** shows a wafer stack 1504 including a second substrate 1520 (e.g., a temporary substrate) bonded to p-type semiconductor layer 1518 of first wafer 1502 using a temporary bonding layer 1522 in a first alignment-free bonding process. In some embodiments, second substrate 1520 may be made of a substantially same or similar material as first substrate 1510. In some embodiments, second substrate 1520 may include a material different from first substrate 1510, such as a dielectric substrate (e.g., a glass substrate, a

ceramic substrate, a SiN substrate, or a metal oxide substrate), a semiconductor substrate (e.g., a silicon substrate), or another carrier substrate (e.g., a metal plate). In some embodiments, second substrate 1520 may be perforated. Temporary bonding layer 1522 may include, for example, an adhesive (e.g., a UV-curable adhesive such as an epoxy resin) or a thermoplastic bonding material (e.g., polyimide). In some embodiments, temporary bonding layer 1522 may also include a low-surface-energy polymeric release material layer, such as a polymeric release material layer. The bonding process for bonding first wafer 1502 and second substrate 1520 may include, for example, applying (e.g., spin-coating) temporary bonding layer 1522 on second substrate 1520 and/or first wafer 1502, baking temporary bonding layer 1522, and bonding second substrate 1520 to first wafer 1502 using temporary bonding layer 1522 through thermo-compression bonding. The bonding of second substrate 1520 to p-type semiconductor layer 1518 may result in a wafer stack 1504 including first substrate 1510 and second substrate 1520 on each side of wafer stack 1504, as illustrated in FIG. 15B. The temporary bonding may advantageously enable a crack-free debonding (e.g., laser lift off) process and a high-yield thermo-compression bonding of the backplane wafer and epitaxial layers in a subsequent process.

[0157] **FIG. 15C** shows that first substrate 1510 and buffer layer 1512 of first wafer 1502 may be removed or thinned to expose n-type semiconductor layer 1514. First substrate 1510 and buffer layer 1512 may be removed or thinned using, for example, mechanical back-grinding, chemical mechanical planarization (CMP), wet etching, atmospheric downstream plasma dry chemical etching, wafer lapping, or other suitable wafer thinning techniques. Second substrate 1520 may remain bonded to p-type semiconductor layer 1518 of the epitaxial layers during the removal or thinning of first substrate 1510 to support the epitaxial layers. In some embodiments, a portion of n-type semiconductor layer 1514 may also be thinned or removed by the wafer thinning process.

[0158] **FIG. 15D** shows an example of bonding a structure 1506 that includes additional layers formed on the epitaxial layers to a second wafer 1508. In the illustrated example, a reflector layer 1524 may be deposited onto the exposed n-type semiconductor layer 1514, and a first metal bonding layer 1526 may be formed on reflector layer 1524. Reflector layer 1524 may include a suitable metal material that may have a high reflectivity for visible light, such as Al or Ag, such that it may reflect light emitted in active light-emitting layer 1516 towards the light emitting surface of the micro-LED. In some embodiments, reflector layer 1524 may include multiple interleaved layers of two different materials (having different refractive indices) that may form a DBR. In some embodiments, first metal bonding layer 1526 may

include one or more metal or metal alloy materials, such as Al, Ag, Au, Pt, Ti, Cu, Ni, TiN, or any combination thereof. In some implementations, reflector layer 1524 and first metal bonding layer 1526 may be a same layer. For example, if the electrical conductivity and reflectivity of the first metal bonding layer 1526 is sufficiently high and the absorption of the first metal bonding layer 1526 is sufficiently low, reflector layer 1524 may not be used.

[0159] Second wafer 1508 (e.g., a backplane wafer) may be bonded to first metal bonding layer 1526 on structure 1506 in a second alignment-free bonding process. Second wafer 1508 may include a CMOS backplane 1530 that includes pixel drive circuits formed on a silicon substate. Second wafer 1508 may also include interconnects 1534 (e.g., tungsten plugs or copper vias) formed in one or more dielectric layers 1532 (e.g., SiO_2 or SiN layers). In some embodiments, second wafer 1508 may include a second metal bonding layer 1536, such as a layer of Ti, Au, Al, Cu, TiN, or a combination thereof. Second metal bonding layer 1536 may be coupled to interconnects 1534. In some implementations, second metal bonding layer 1536 of second wafer 1508 may be of a substantially same or similar material (e.g., Ti) as first metal bonding layer 1526. In some implementations, second metal bonding layer 1536 of second wafer 1508 may include material(s) different from first metal bonding layer 1526. In some embodiments, first metal bonding layer 1526 and second metal bonding layer 1536 may be bonded by a thermo-compression bonding process. Second metal bonding layer 1536 and first metal bonding layer 1526 may form a metal layer that may be used to form individual electrodes (e.g., cathodes) for the micro-LEDs. In some embodiments, annealing processes or other processes may be performed such that second metal bonding layer 1536 and first metal bonding layer 1526 may form a uniform metal layer where the bonding interface may not easily detectable.

[0160] **FIG. 15E** shows that, after the bonding, second substrate 1520 and temporary bonding layer 1522 may be removed from the bonded wafer stack to expose p-type semiconductor layer 1518. Second wafer 1508 may remain bonded to the epitaxial layers via the metal-to-metal bonding of first metal bonding layer 1526 and second metal bonding layer 1536. Second substrate 1520 may be removed by a low-stress debonding process, such as chemical debonding (e.g., through perforations in second substrate 1520), thermal slide debonding (e.g., heating and sliding), laser debonding (e.g., exposing a release material layer to laser beams), or mechanical debonding (e.g., through a release material layer). In some embodiments, the debonding process may be performed as room temperature. In some embodiments, at least a portion of temporary bonding layer 1522 may remain on p-type semiconductor layer 1518. The residual temporary bonding layer 1522 on p-type

semiconductor layer 1518 may be removed by dry etching and/or wet etching.

[0161] **FIG. 15F** shows that p-type semiconductor layer 1518, active light-emitting layer 1516, n-type semiconductor layer 1514, reflector layer 1524, first metal bonding layer 1526, and second metal bonding layer 1536 in the wafer stack may be etched from the side of p-type semiconductor layer 1518 down to second metal bonding layer 1536 to form an array of mesa structures 1505. Various etching techniques, such as dry etching and/or wet etching, may be used for the etching. Dielectric layer 1532 on second wafer 1508 may be used as the etch stop layer. The etching may be performed from the side of p-type semiconductor layer 1518 using a same etch mask layer. As described above, the etch mask layer may be patterned by aligning a photomask with the second wafer 1508 (e.g., using alignment marks on second wafer 1508) such that the patterned etch mask formed in the etch mask layer may align with interconnects 1534. In some embodiments, each interconnect 1534 may be smaller than the first metal bonding layer 1526 and second metal bonding layer 1536 in each mesa structure, and may overlap laterally with an interior region of second metal bonding layer 1536 in each mesa structure 1505 as shown in FIG. 15F. For example, the center of an interconnect 1534 may be aligned with the center of first metal bonding layer 1526 or second metal bonding layer 1536 in a corresponding mesa structure.

[0162] Etching the epitaxial layers may lead to the formation of mesa sidewalls that may be orthogonal to the epitaxial layers or may be tilted. Mesa structures 1505 with myriad mesa sidewall shapes may be formed, including substantially vertical shapes, parabolic shapes, conic shapes, and the like. Light emission profiles of micro-LEDs may be different depending on the shape of the mesa structure, and hence may be adjusted by changing the shape of the mesa structure, which may in turn be adjusted by adjusting the etching processes. In some embodiments, the sidewalls of mesa structures 1505 may be treated (e.g., using KOH) to remove damaged portions of the semiconductor materials.

[0163] **FIG. 15G** shows a micro-LED device 1570 formed by p-side processes. As illustrated, one or more passivation layers 1550 (e.g., a SiO_2 or SiN layer) may be deposited on sidewalls of mesa structures 1505. One or more metal materials 1552 (e.g., including a reflective metal such as Al, Ag, or Au, a barrier material such as TiN or TaN, and a filling metal such as Au, Cu, Al, or W) may be deposited on passivation layer 1550 and/or may fill gaps between mesa structures 1505 to form mesa sidewall mirrors and a common anode. In some embodiments, a dielectric material 1554 may be deposited in gaps between mesa structures. A chemical mechanical planarization (CMP) process may be performed to planarize the top surface of mesa structures 1505. A transparent conductive layer 1560 (e.g.,

including a transparent conductive oxide such as ITO) may be formed on p-type semiconductor layer 1518 of mesa structures 1505, for example, to form a common anode layer for the array of micro-LEDs in micro-LED device 1570.

[0164] **FIGS. 16A-16F** illustrate an example of a method of fabricating a common-anode phosphide-based micro-LED display device according to certain embodiments. **FIG. 16A** shows a micro-LED wafer 1602 including epitaxial layers grown on a substrate 1610. As described above, substrate 1610 may include, for example, a GaAs substrate, a GaP substrate, or another suitable substrate, where the substrate may be cut in a specific direction to expose a specific plane (e.g., c-plane or a semipolar plane) as the growth surface. In some embodiments, a buffer layer 1612 (e.g., a GaP or GaAs layer) may be formed on substrate 1610 to improve the lattice matching of the epitaxial layers, thereby reducing stress and defects in the epitaxial layers. In phosphide-based micro-LEDs, either the n-type semiconductor layer or the p-doped semiconductor layer may be grown before the growth of the active region. In the example illustrated in FIG. 16A, the epitaxial layers may include a p-type semiconductor layer 1614 (e.g., a p-doped GaP, AlGaP, AlInP, or AlGaInP layer), an active region 1616, and an n-type semiconductor layer 1618 (e.g., an n-doped GaP, AlGaP, AlInP, or AlGaInP layer). Active region 1616 may include multiple quantum wells or an MQW formed by quantum well layers (e.g., AlGaInP or InGaAsP layers) sandwiched by barrier layers (e.g., GaInP layer) as described above. The epitaxial layers may be grown layer-by-layer on substrate 1610 or buffer layer 1612 using techniques such as VPE, LPE, MBE, or MOCVD. N-type semiconductor layer 1618 may be doped with, for example, Si. P-type semiconductor layer 1614 may be doped with, for example, Zn.

[0165] **FIG. 16B** shows a reflector layer 1620 and a bonding layer 1622 formed on n-type semiconductor layer 1618. Reflector layer 1620 may include, for example, a metal layer such as an aluminum layer, a silver layer, or a metal alloy layer, or a distributed Bragg reflector formed by conductive materials (e.g., semiconductor materials) or including conductive vias. Reflector layer 1620 may include one or more sublayers. Reflector layer 1620 may be deposited on n-type semiconductor layer 1618. Bonding layer 1622 may include a metal layer, such as a titanium layer, a copper layer, an aluminum layer, a gold layer, or a metal alloy layer. In some embodiments, bonding layer 1622 may include a eutectic alloy, such as Au-In, Au-Sn, Au-Ge, or Ag-In. Bonding layer 1622 may be formed on reflector layer 1620 by a deposition process and may include one or more sublayers.

[0166] **FIG. 16C** shows a backplane wafer 1604 that includes a substrate 1630 with electrical circuits formed thereon. The electrical circuits may include digital and analog pixel

drive circuits for driving individual micro-LEDs. A plurality of metal pads 1634 (e.g., copper pads) may be formed in a dielectric layer 1632 (e.g., SiO_2 or SiN). In some embodiments, each metal pad 1634 may be an electrode (e.g., cathode) for a micro-LED. In some embodiments, pixel drive circuits for each micro-LED may be formed in an area matching the size of a micro-LED (e.g., about 2μm × 2μm), where the pixel drive circuits and the micro-LED may collectively form a pixel of a micro-LED display panel. Even though FIG. 16C only shows metal pads 1634 formed in one metal layer in one dielectric layer 1632, backplane wafer 1604 may include two or more metal layers formed in dielectric materials and interconnected by, for example, metal vias. In some embodiments, a planarization process, such as a CMP process, may be performed to planarize the exposed surfaces of metal pads 1634 and dielectric layer 1632. A bonding layer 1640 may be formed on dielectric layer 1632 and may be in physical and electrical contact with metal pads 1634. As bonding layer 1622, bonding layer 1640 may include a metal layer, such as a titanium layer, a copper layer, an aluminum layer, a gold layer, a metal alloy layer, or a combination thereof. In some embodiments, bonding layer 1640 may include a eutectic alloy. In some embodiments, only one of bonding layer 1640 or bonding layer 1622 may be used.

[0167] **FIG. 16D** shows that micro-LED wafer 1602 and backplane wafer 1604 may be bonded together to form a wafer stack 1606. Micro-LED wafer 1602 and backplane wafer 1604 may be bonded by the metal-to-metal bonding of bonding layer 1622 and bonding layer 1640. As described above, the metal-to-metal bonding may be based on chemical bonds between the metal atoms at the surfaces of the metal bonding layers. The metal-to-metal bonding may include, for example, thermo-compression bonding, eutectic bonding, or transient liquid phase (TLP) bonding. The metal-to-metal bonding process may include, for example, surface planarization, wafer cleaning (e.g., using plasma or solvents) at room temperature, and compression and annealing at elevated temperatures, such as about 250 °C or higher, to cause diffusion of atoms. In eutectic bonding, a eutectic alloy including two or more metals and with a eutectic point lower than the melting point of the one or more metals may be used for low-temperature wafer bonding. Because the eutectic alloy may become a liquid at the elevated temperature, eutectic bonding may be less sensitive to surface flatness irregularities, scratches, particles contamination, and the like. After the bonding, buffer layer 1612 and substrate 1610 may be thinned or removed by, for example, etching, back grinding, or laser lifting, to expose p-type semiconductor layer 1614.

[0168] **FIG. 16E** shows that wafer stack 1606 may be etched from the side of the exposed

p-type semiconductor layer 1614 to form mesa structures 1608 for individual micro-LEDs. As shown in FIG. 16E, the etching may include etching through p-type semiconductor layer 1614, active region 1616, n-type semiconductor layer 1618, reflector layer 1620, and bonding layers 1622 and 1640, in order to singulate and electrically isolate mesa structures 1608. Thus, each singulated mesa structure 1608 may include p-type semiconductor layer 1614, active region 1616, n-type semiconductor layer 1618, reflector layer 1620, and bonding layers 1622 and 1640. To perform the selected etching, an etch mask layer may be formed on p-type semiconductor layer 1614. The etch mask layer may be patterned by aligning a photomask with the backplane wafer (e.g., using alignment marks on backplane wafer 1604) such that the patterned etch mask formed in the etch mask layer may align with metal pads 1634. Therefore, regions of the epitaxial layers and bonding layers above metal pads 1634 may not be etched. Dielectric layer 1632 may be used as the etch-stop layer for the etching. In some embodiments, there may be two or more metal pads 1634 under each mesa structure. Even though FIG. 16E shows that mesa structures 1608 have vertical sidewalls, mesa structures 1608 may have other shapes as described above, such as a conical shape, a parabolic shape, or a truncated pyramid shape. In some embodiments, sidewalls of the mesa structures may be treated (e.g., wet etched) to remove regions of the semiconductor materials that may have been damaged by the etching (e.g., using plasma).

[0169] **FIG. 16F** shows that a passivation layer 1650 may be formed on sidewalls of mesa structures 1608, and a sidewall reflector layer 1652 may be formed on passivation layer 1650. Passivation layer 1650 may include a dielectric layer (e.g., SiO_2 or SiN) or an undoped semiconductor layer. Sidewall reflector layer 1652 may include, for example, a metal (e.g., Al) or a metal alloy. In some embodiments, gaps between mesa structures 1608 may be filled with a dielectric material 1654. Passivation layer 1650, sidewall reflector layer 1652, and/or dielectric material 1654 may be formed using suitable deposition techniques, such as CVD, PVD, PECVD, ALD, LMD, or sputtering. In some embodiments, sidewall reflector layer 1652 may fill the gaps between mesa structures 1608. In some embodiments, a planarization process may be performed after the deposition of passivation layer 1650, sidewall reflector layer 1652, and/or dielectric material 1654. A common electrode layer 1660, such as a TCO layer (e.g., an ITO layer) or a thin metal layer that may be transparent to light emitted in active region 1616, may be formed on p-type semiconductor layer 1614 to form p-contacts and a common anode for the micro-LEDs.

[0170] **FIG. 17** illustrates an example of a common-anode micro-LED display device 1700 that may be fabricated using the method described above with respect to FIGS. 15A-15G or

the method described above with respect to FIGS. 16A-16F. In the illustrated example, common-anode micro-LED display device 1700 includes a silicon substrate 1710, drive circuits 1720 formed on silicon substrate 1710, and a plurality of micro-LEDs 1702 bonded to drive circuits 1720. Drive circuits 1720 may include CMOS circuits, a plurality of metal layers 1722 (e.g., Cu layers), metal plugs 1724 (e.g., W plugs), and a bonding layer 1726. The plurality of micro-LEDs 1702 may be formed in a layer stack that includes a bonding layer 1730, a metal reflector layer 1732, an n-type semiconductor layer 1740, active layers 1742, and a p-type semiconductor layer 1744. Each micro-LED 1702 may also include a sidewall passivation layer 1750 and a sidewall metal reflector 1752 (e.g., including a metal such as Cu, Al, or Ti). The plurality of micro-LEDs 1702 may be connected to a common anode 1760, which may include a transparent conductive layer, such as an ITO layer. Common anode 1760 may be electrically connected to a p-contact 1754 and sidewall metal reflectors 1752. P-contact 1754 may be connected to a voltage supply (e.g., a voltage regulator) in drive circuits 1720. Sidewall metal reflectors 1752 may also help to spread the drive current from p-contact 1754 and common anode 1760 to the plurality of micro-LEDs 1702. Common-anode micro-LED display device 1700 may also include a dielectric layer 1770 (e.g., a SiO_2 or SiN layer) formed on common anode 1760. One or more metal plugs 1780 (e.g., including Ti/TiN/Al layers) may be formed in dielectric layer 1770.

[0171] **FIGS. 18A** and **18B** illustrate an example of a common-anode micro-LED wafer 1800 including a plurality of mesa structures formed thereon according to certain embodiments. **FIG. 18A** is a top view of common-anode micro-LED wafer 1800. **FIG. 18B** is a cross-sectional view of common-anode micro-LED wafer 1800. Common-anode micro-LED wafer 1800 may include a two-dimensional array of micro-LEDs arranged in a plurality of columns and rows. FIG. 18A shows individual mesa structures 1840 for the micro-LEDs, two shared p-contacts 1826 near two edges of the 2-D array of micro-LEDs, and p-contacts 1828 adjacent to and between mesa structures 1840 of individual micro-LEDs. FIG. 18B shows a cross-section along a line 1804 (e.g., in the w direction).

[0172] In the example shown in FIG. 18B, common-anode micro-LED wafer 1800 may include a p-type semiconductor layer 1810 (e.g., a p-doped GaN, GaP, AlGaP, AlInP, GaInP, or AlGaInP layer), an active layer 1812 that may include one or more quantum wells, and an n-type semiconductor layer 1814. Common-anode micro-LED wafer 1800 may also include a thin ITO layer 1816 and a dielectric layer 1818 (e.g., a SiO2 layer). Dielectric layer 1818 may be patterned and used as a hard mask layer for etching mesa structures in common-anode micro-LED wafer 1800. Layers 1816, 1814, and 1812, and at least a portion of p-type

semiconductor layer 1810 may be etched to form individual mesa structures 1840 and expose regions of p-type semiconductor layer 1810. A patterned dielectric layer 1820 (e.g., SiN) may be formed on the top and sidewall surfaces of mesa structures 1840 and may function as a passivation layer or a barrier layer. P-contacts 1826 and 1828 may be formed on exposed p-type semiconductor layer 1810. P-contacts 1826 and 1828 may include, for example, Ti and/or Au for green and blue light-emitting micro-LEDs, and Pd, Au, Ga, Ti, or a combination for red light-emitting micro-LEDs. The cross-sectional view along line 1804 in FIG. 18B shows p-contacts 1828 at locations where there may be larger gaps between adjacent mesa structures 1840, such as the center of four adjacent mesa structures 1840. In embodiments where the micro-LEDs may have a large pitch, p-contacts 1828 may also be at locations between adjacent mesa structures in a same row or column.

[0173] In some embodiments, common-anode micro-LED wafer 1800 may include phosphide-based semiconductor materials, and may be fabricated by growing a layer stack including p-type semiconductor layer 1810, active layer 1812, and n-type semiconductor layer 1814 on a growth substrate (e.g., substrate 1610), and processing the layer stack from the side of n-type semiconductor layer 1814 (e.g., n-type semiconductor layer 1618) to form mesa structures 1840, before bonding common-anode micro-LED wafer 1800 to a backplane wafer. In some embodiments, common-anode micro-LED wafer 1800 may include GaN-based semiconductor layers bonded to a temporary substrate (e.g., a carrier wafer), and may be fabricated by forming a layer stack on the temporary substrate (e.g., second substrate 1520) using the method described above with respect to FIGS. 15A-15C, and then processing the layer stack on the temporary substrate from the side of n-type semiconductor layer 1814 (e.g., n-type semiconductor layer 1514) to form mesa structures 1840, before bonding common-anode micro-LED wafer 1800 to a backplane wafer.

[0174] **FIGS. 19A** and **19B** illustrate an example of a common-anode micro-LED wafer 1900 with a bonding layer for bonding to a backplane wafer according to certain embodiments. Common-anode micro-LED wafer 1900 may be fabricated by further processing common-anode micro-LED wafer 1800 to form a current spreading layer (a common anode layer), n-contacts (including n-side reflectors), and metal interconnects for connecting the p-contacts and n-contacts to the backplane wafer. **FIG. 19A** is a cross-sectional view of common-anode micro-LED wafer 1900 (e.g., in a y-z plane along a line 1802 shown in FIG. 18A). **FIG. 19B** is another cross-sectional view of common-anode micro-LED wafer 1900 (e.g., in a z-w plane along line 1804 shown in FIG. 18A).

[0175] FIGS. 19A and 19B show that a contiguous metal layer 1930 (e.g., including Al,

Au, Ag, TiN/Ti, or a combination) may be formed on dielectric layer 1820 and p-contacts 1826 and 1828. For example, metal layer 1930 may be formed on sidewalls of the mesa structures and regions between the mesa structures. Metal layer 1930 may be in electric contact with p-contacts 1826 and 1828, and may also be used as a sidewall reflector and a current spreading layer (e.g., a common anode layer) for distributing current to p-contacts 1828 that are adjacent to individual mesa structures 1840. Regions between mesa structures 1840 may then be filled with a dielectric material 1932, such as SiO_2. A dielectric layer 1936 may be deposited and patterned on metal layer 1930 and dielectric material 1932. N-contacts 1940 may be formed on n-type semiconductor layers 1814 of mesa structures 1840, through dielectric layer 1936, dielectric layer 1820, and dielectric layer 1818. N-contacts 1940 may include, for example, ITO, Al, Au, Ag, Ti, TiN, TaN, or a combination, such as ITO/Ag/TiN or ITO/Ag/TaN/Ta. N-contacts 1940 may also function as an n-side reflector for reflecting incident light. A dielectric layer 1942 (e.g., SiO_2) may then be deposited on mesa structures 1840, and metal interconnects 1948 may be formed in a dielectric layer 1942. Metal interconnects 1948 may be connected to p-contacts 1826 and n-contacts 1940, and may include, for example, Cu. A barrier and/or metal seed layer 1946 (e.g., TiN/Ti or TaN/Ta) may be used between metal interconnects 1948 and dielectric layer 1942.

[0176] Common-anode micro-LED wafer 1900 with metal interconnects 1948 for n-contact 1940 and p-contacts 1826 may be bonded to a backplane wafer using, for example, processes described above with respect to FIGS. 8A-8D. In some embodiments, light extraction structures 1970 (e.g., micro-lenses) may be formed in p-type semiconductor layer 1810. In some embodiments, an antireflective coating layer 1972 may be formed on light extraction structures 1970. In some embodiments, light extraction structures 1970 may be formed on p-type semiconductor layer 1810 after common-anode micro-LED wafer 1900 is bonded to a drive circuit fabricated on a silicon wafer as described above and below, such that the silicon wafer may be used as the handle wafer and processes can be performed from the side of p-type semiconductor layer 1810 after removing the growth substrate (e.g., substrate 1610) of phosphide-based micro-LED wafer or a temporary substrate (e.g., second substrate 1520) bonded to nitride-based epitaxial layers.

[0177] **FIG. 20** illustrates an example of a pixel 2000 of a common-anode micro-LED display device according to certain embodiments. In the illustrated example, pixel 2000 may include a control circuit 2010, a switch transistor 2020, a bias transistor 2030, and a micro-LED 2040. Control circuit 2010 may include CMOS circuits that may include memory devices (e.g., SRAM cells 2012) for storing display data, as described above with respect to

memory device 1102. Control circuit 2010 may also include a comparator 2014, which may be similar to comparator 1104 described above and may be used to compare a clock counter value with the display data stored in SRAM cells 2012 to generate a high or low output signal based on the comparison result. Control circuit 2010 may further include a PWM latch 2016, which may be similar to PWM latch circuit 1106 described above and may be used to generate PWM signals for modulating the micro-LED drive current. In some embodiments, PWM latch 2016 may terminate the PWM output pulses based on outputs signals from, for example, comparator 2014. In some embodiments, control circuits 2010 for the pixels of the micro-LED display device may be fabricated on a separate silicon wafer and may receive power from a low-voltage (e.g., about 1 V) voltage supply (e.g., a voltage regulator). Because analog drive circuits are not fabricated on the silicon wafer, there may be more room to fit more SRAM cells and/or other circuits (e.g., design-for-test circuits) for each pixel in control circuits 2010.

[0178] Switch transistor 2020 and bias transistor 2030 may be fabricated on the silicon wafer or on a different wafer or substrate, such as an IGZO layer. Bias transistor 2030 may be an n-channel device and may be controlled by a bias voltage to generate the drive current for micro-LED 2040. Switch transistor 2020 may be an n-channel device and may be controlled by PWM signals generated by control circuits 2010 to turn on or off, thereby turning on or off the drive current that passes through micro-LED 2040.

[0179] Micro-LED 2040 may emit red, green, or blue light in an active region. Micro-LED 2040 may share a common anode with other micro-LEDs on the micro-LED display device. The common anode may be connected to a voltage supply VDD. The perceived brightness of the emitted light from micro-LED 2040 may be controlled by the drive current and/or the duration of the light emission.

[0180] **FIG. 21** includes a simplified block diagram of an example of a common-anode micro-LED display device 2100 according to certain embodiments. Each pixel of common-anode micro-LED display device 2100 may be controlled and driven by the circuits shown in, for example, FIG. 20. In the illustrated example, common-anode micro-LED display device 2100 may include an array (e.g., a 2-D array) of blue light-emitting micro-LEDs 2120 that have a common anode and are controlled by common control circuits 2130 and pixel control circuits 2140 (e.g., control circuits 2010). Common control circuits 2130 and pixel control circuits 2140 may be powered by a voltage supply 2105, such as a +1 V voltage supply or voltage regulator. A pixel control circuit 2140 may generate signals (e.g., PWM signals) to control a switch 2150 (e.g., switch transistor 2020) such that switch 2150 may be turned on to

supply a drive current from a first voltage supply 2110 to a corresponding blue light-emitting micro-LED 2120 for a desired light emission duration.

[0181] Common-anode micro-LED display device 2100 may also include an array (e.g., a 2-D array) of green light-emitting micro-LEDs 2122 that have a common anode and are controlled by common control circuits 2132 and pixel control circuits 2142 (e.g., control circuits 2010). Common control circuits 2132 and pixel control circuits 2142 may be powered by voltage supply 2105. A pixel control circuit 2142 may generate signals (e.g., PWM signals) to control a switch 2152 (e.g., switch transistor 2020) such that switch 2152 may be turned on to supply a drive current from a second voltage supply 2112 to a corresponding green light-emitting micro-LED 2122 for a desired light emission duration.

[0182] Common-anode micro-LED display device 2100 may further include an array (e.g., a 2-D array) of red light-emitting micro-LEDs 2124 that have a common anode and are controlled by common control circuits 2134 and pixel control circuits 2144 (e.g., control circuits 2010). Common control circuits 2134 and pixel control circuits 2144 may be powered by voltage supply 2105. A pixel control circuit 2144 may generate signals (e.g., PWM signals) to control a switch 2154 (e.g., switch transistor 2020) such that switch 2154 may be turned on to supply a drive current from a third voltage supply 2114 to a corresponding red light-emitting micro-LED 2124 for a desired light emission duration.

[0183] **FIG. 22** includes a flowchart 2200 illustrating an example of a method of fabricating a common-anode micro-LED display device according to certain embodiments. It is noted that the specific operations illustrated in FIG. 22 provide a particular process of fabricating a GaN-based common-anode micro-LED display device as described above with respect to FIGS. 15A-15G. Other sequences of operations may be performed according to alternative embodiments. For example, alternative embodiments may perform the operations outlined above in a different order. A different sequence of operations may be performed to fabricate a phosphide-based common-anode micro-LED display device as described above with respect to FIGS. 16A-16F. Another different sequence of operations as described above with respect to FIGS. 18A-19B may be performed to fabricate a common-anode micro-LED display device by forming mesa-structures for individual micro-LEDs before bonding the micro-LED wafer to a backplane wafer. Moreover, the individual operations illustrated in FIG. 22 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual operation. Furthermore, additional operations may be added or some operations may not be performed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0184] Operations at block 2210 may include obtaining a first wafer. In some embodiments, the first wafer may include a first substrate and epitaxial layers grown on the first substrate. The epitaxial layers may include a first (e.g., n-doped GaN) semiconductor layer on the first substrate, a light-emitting region on the first semiconductor layer, and a second (e.g., p-doped GaN) semiconductor layer on the light-emitting region. Examples of the first wafer include micro-LED wafer 1202 of FIG. 12A and first wafer 1502 shown in FIG. 15A. The first wafer may be fabricated by growing the first semiconductor layer on the first substrate, growing the light-emitting region on the first semiconductor layer, and growing the second semiconductor layer on the light-emitting region, using techniques described above with respect to, for example, FIG. 12A.

[0185] Operations at block 2220 may include bonding a second substrate (e.g., a temporary substrate such as a carrier substrate) to the second (e.g., p-doped) semiconductor layer on the first wafer, as described above with respect to, for example, FIG. 15B. Operations at block 2230 may include removing the first substrate of the first wafer so as to expose the first semiconductor layer as described above with respect to, for example, FIG. 15C.

[0186] Operations at block 2240 may include forming a reflector layer on the exposed first semiconductor layer as described above with respect to, for example, FIG. 15D. In some embodiments, the reflector layer may include a reflective metal layer (e.g., a layer of Ag, Al, or Au) and/or DBR layers. Operations at block 2250 may include forming a first metal bonding layer on the reflector layer as described above with respect to, for example, FIG. 15D. The first metal bonding layer may include, for example, Al, Ag, Au, Pt, Ti, Cu, Ni, TiN, TaN, or a combination thereof.

[0187] Operations at block 2260 may include bonding a second metal bonding layer of a backplane wafer to the first metal bonding layer as described above with respect to, for example, FIG. 15D. The backplane wafer may include circuits described above with respect to, for example, FIGS. 20 and 21. Operations at block 2270 may include removing the second substrate to expose the second semiconductor layer as described above with respect to, for example, FIG. 15E. As described above, the temporarily bonded second substrate may be relatively easy to remove using, for example, a low-stress debonding process, such as chemical debonding, thermal slide debonding, laser debonding, or mechanical debonding. In some embodiments, the debonding process may be performed as room temperature.

[0188] Operations at block 2280 may include etching through the epitaxial layers, the reflector layer, and the first and second metal bonding layers to form an array of mesa structures as described above with respect to, for example, FIG. 15F. The backplane wafer

may include a plurality of metal contact pads coupled to the second metal bonding layer, and the etching may include etching the epitaxial layers, the reflector layer, and the first and second metal bonding layers using an etch mask that is aligned with the plurality of metal contact pads on the backplane wafer. The mesa structures may be etched in one or more dry and/or wet etching processes to achieve various shapes as described above. The shapes of the mesa structures may be adjusted to emit light beams with preferrable beam profiles.

[0189] Optional operations at block 2290 may include forming a passivation layer (e.g., a dielectric layer such as a SiO_2 or SiN layer) and a sidewall reflector (e.g., a layer of Al, Ag, or Au) on sidewalls of the mesa structures as described above with respect to, for example, FIG. 15G. In some embodiments, regions between the mesa structures may be filled with one or more metals, such as a reflective metal (e.g., Al, Ag, or Au,) a barrier material (e.g., TiN or TaN), and a filling metal (e.g., Au, Cu, Al, or W).

[0190] Operations at block 2295 may include forming a transparent conductive layer (e.g., an ITO layer) over the second (e.g., p-doped) semiconductor layer to form a common electrode (e.g., anode) layer, as described above with respect to, for example, FIG. 15G.

[0191] Embodiments disclosed herein may be used to implement components of an artificial reality system or may be implemented in conjunction with an artificial reality system. Artificial reality is a form of reality that has been adjusted in some manner before presentation to a user, which may include, for example, a virtual reality, an augmented reality, a mixed reality, a hybrid reality, or some combination and/or derivatives thereof. Artificial reality content may include completely generated content or generated content combined with captured (*e.g.*, real-world) content. The artificial reality content may include video, audio, haptic feedback, or some combination thereof, and any of which may be presented in a single channel or in multiple channels (such as stereo video that produces a three-dimensional effect to the viewer). Additionally, in some embodiments, artificial reality may also be associated with applications, products, accessories, services, or some combination thereof, that are used to, for example, create content in an artificial reality and/or are otherwise used in (*e.g.*, perform activities in) an artificial reality. The artificial reality system that provides the artificial reality content may be implemented on various platforms, including an HMD connected to a host computer system, a standalone HMD, a mobile device or computing system, or any other hardware platform capable of providing artificial reality content to one or more viewers.

[0192] **FIG. 23** is a simplified block diagram of an example electronic system 2300 of an example near-eye display (*e.g.*, HMD device) for implementing some of the examples

disclosed herein. Electronic system 2300 may be used as the electronic system of an HMD device or other near-eye displays described above. In this example, electronic system 2300 may include one or more processor(s) 2310 and a memory 2320. Processor(s) 2310 may be configured to execute instructions for performing operations at a number of components, and can be, for example, a general-purpose processor or microprocessor suitable for implementation within a portable electronic device. Processor(s) 2310 may be communicatively coupled with a plurality of components within electronic system 2300. To realize this communicative coupling, processor(s) 2310 may communicate with the other illustrated components across a bus 2340. Bus 2340 may be any subsystem adapted to transfer data within electronic system 2300. Bus 2340 may include a plurality of computer buses and additional circuitry to transfer data.

[0193] Memory 2320 may be coupled to processor(s) 2310. In some embodiments, memory 2320 may offer both short-term and long-term storage and may be divided into several units. Memory 2320 may be volatile, such as static random access memory (SRAM) and/or dynamic random access memory (DRAM) and/or non-volatile, such as read-only memory (ROM), flash memory, and the like. Furthermore, memory 2320 may include removable storage devices, such as secure digital (SD) cards. Memory 2320 may provide storage of computer-readable instructions, data structures, program code, and other data for electronic system 2300. In some embodiments, memory 2320 may be distributed into different hardware subsystems. A set of instructions and/or code might be stored on memory 2320. The instructions might take the form of executable code that may be executable by electronic system 2300, and/or might take the form of source and/or installable code, which, upon compilation and/or installation on electronic system 2300 (*e.g.*, using any of a variety of generally available compilers, installation programs, compression/decompression utilities, etc.), may take the form of executable code.

[0194] In some embodiments, memory 2320 may store a plurality of applications 2322 through 2324, which may include any number of applications. Examples of applications may include gaming applications, conferencing applications, video playback applications, or other suitable applications. The applications may include a depth sensing function or eye tracking function. Applications 2322-2324 may include particular instructions to be executed by processor(s) 2310. In some embodiments, certain applications or parts of applications 2322-2324 may be executable by other hardware subsystems 2380. In certain embodiments, memory 2320 may additionally include secure memory, which may include additional security controls to prevent copying or other unauthorized access to secure information.

[0195] In some embodiments, memory 2320 may include an operating system 2325 loaded therein. Operating system 2325 may be operable to initiate the execution of the instructions provided by applications 2322-2324 and/or manage other hardware subsystems 2380 as well as interfaces with a wireless communication subsystem 2330 which may include one or more wireless transceivers. Operating system 2325 may be adapted to perform other operations across the components of electronic system 2300 including threading, resource management, data storage control and other similar functionality.

[0196] Wireless communication subsystem 2330 may include, for example, an infrared communication device, a wireless communication device and/or chipset (such as a Bluetooth® device, an IEEE 802.11 device, a Wi-Fi device, a WiMax device, cellular communication facilities, etc.), and/or similar communication interfaces. Electronic system 2300 may include one or more antennas 2334 for wireless communication as part of wireless communication subsystem 2330 or as a separate component coupled to any portion of the system. Depending on desired functionality, wireless communication subsystem 2330 may include separate transceivers to communicate with base transceiver stations and other wireless devices and access points, which may include communicating with different data networks and/or network types, such as wireless wide-area networks (WWANs), wireless local area networks (WLANs), or wireless personal area networks (WPANs). A WWAN may be, for example, a WiMax (IEEE 802.16) network. A WLAN may be, for example, an IEEE 802.11x network. A WPAN may be, for example, a Bluetooth network, an IEEE 802.15x, or some other types of network. The techniques described herein may also be used for any combination of WWAN, WLAN, and/or WPAN. Wireless communications subsystem 2330 may permit data to be exchanged with a network, other computer systems, and/or any other devices described herein. Wireless communication subsystem 2330 may include a means for transmitting or receiving data, such as identifiers of HMD devices, position data, a geographic map, a heat map, photos, or videos, using antenna(s) 2334 and wireless link(s) 2332.

[0197] Embodiments of electronic system 2300 may also include one or more sensors 2390. Sensor(s) 2390 may include, for example, an image sensor, an accelerometer, a pressure sensor, a temperature sensor, a proximity sensor, a magnetometer, a gyroscope, an inertial sensor (*e.g.*, a subsystem that combines an accelerometer and a gyroscope), an ambient light sensor, or any other similar devices or subsystems operable to provide sensory output and/or receive sensory input, such as a depth sensor or a position sensor. For example, in some implementations, sensor(s) 2390 may include one or more inertial measurement units

(IMUs) and/or one or more position sensors. An IMU may generate calibration data indicating an estimated position of the HMD device relative to an initial position of the HMD device, based on measurement signals received from one or more of the position sensors. A position sensor may generate one or more measurement signals in response to motion of the HMD device. Examples of the position sensors may include, but are not limited to, one or more accelerometers, one or more gyroscopes, one or more magnetometers, another suitable type of sensor that detects motion, a type of sensor used for error correction of the IMU, or some combination thereof. The position sensors may be located external to the IMU, internal to the IMU, or some combination thereof. At least some sensors may use a structured light pattern for sensing.

[0198] Electronic system 2300 may include a display 2360. Display 2360 may be a near-eye display, and may graphically present information, such as images, videos, and various instructions, from electronic system 2300 to a user. Such information may be derived from one or more applications 2322-2324, virtual reality engine 2326, one or more other hardware subsystems 2380, a combination thereof, or any other suitable means for resolving graphical content for the user (*e.g.*, by operating system 2325). Display 2360 may use liquid crystal display (LCD) technology, light-emitting diode (LED) technology (including, for example, OLED, ILED, μLED, AMOLED, TOLED, etc.), light emitting polymer display (LPD) technology, or some other display technology.

[0199] Electronic system 2300 may include a user input/output interface 2370. User input/output interface 2370 may allow a user to send action requests to electronic system 2300. An action request may be a request to perform a particular action. For example, an action request may be to start or end an application or to perform a particular action within the application. User input/output interface 2370 may include one or more input devices. Example input devices may include a touchscreen, a touch pad, microphone(s), button(s), dial(s), switch(es), a keyboard, a mouse, a game controller, or any other suitable device for receiving action requests and communicating the received action requests to electronic system 2300. In some embodiments, user input/output interface 2370 may provide haptic feedback to the user in accordance with instructions received from electronic system 2300. For example, the haptic feedback may be provided when an action request is received or has been performed.

[0200] Electronic system 2300 may include a camera 2350 that may be used to take photos or videos of a user, for example, for tracking the user's eye position. Camera 2350 may also

be used to take photos or videos of the environment, for example, for VR, AR, or MR applications. Camera 2350 may include, for example, a complementary metal–oxide–semiconductor (CMOS) image sensor with a few millions or tens of millions of pixels. In some implementations, camera 2350 may include two or more cameras that may be used to capture 3-D images.

[0201] In some embodiments, electronic system 2300 may include a plurality of other hardware subsystems 2380. Each of other hardware subsystems 2380 may be a physical subsystem within electronic system 2300. While each of other hardware subsystems 2380 may be permanently configured as a structure, some of other hardware subsystems 2380 may be temporarily configured to perform specific functions or temporarily activated. Examples of other hardware subsystems 2380 may include, for example, an audio output and/or input interface (*e.g.*, a microphone or speaker), a near field communication (NFC) device, a rechargeable battery, a battery management system, a wired/wireless battery charging system, etc. In some embodiments, one or more functions of other hardware subsystems 2380 may be implemented in software.

[0202] In some embodiments, memory 2320 of electronic system 2300 may also store a virtual reality engine 2326. Virtual reality engine 2326 may execute applications within electronic system 2300 and receive position information, acceleration information, velocity information, predicted future positions, or some combination thereof of the HMD device from the various sensors. In some embodiments, the information received by virtual reality engine 2326 may be used for producing a signal (*e.g.*, display instructions) to display 2360. For example, if the received information indicates that the user has looked to the left, virtual reality engine 2326 may generate content for the HMD device that mirrors the user's movement in a virtual environment. Additionally, virtual reality engine 2326 may perform an action within an application in response to an action request received from user input/output interface 2370 and provide feedback to the user. The provided feedback may be visual, audible, or haptic feedback. In some implementations, processor(s) 2310 may include one or more GPUs that may execute virtual reality engine 2326.

[0203] In various implementations, the above-described hardware and subsystems may be implemented on a single device or on multiple devices that can communicate with one another using wired or wireless connections. For example, in some implementations, some components or subsystems, such as GPUs, virtual reality engine 2326, and applications (*e.g.*, tracking application), may be implemented on a console separate from the head-mounted display device. In some implementations, one console may be connected to or support more

than one HMD.

[0204] In alternative configurations, different and/or additional components may be included in electronic system 2300. Similarly, functionality of one or more of the components can be distributed among the components in a manner different from the manner described above. For example, in some embodiments, electronic system 2300 may be modified to include other system environments, such as an AR system environment and/or an MR environment.

[0205] The methods, systems, and devices discussed above are examples. Various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, in alternative configurations, the methods described may be performed in an order different from that described, and/or various stages may be added, omitted, and/or combined. Also, features described with respect to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner. Also, technology evolves and, thus, many of the elements are examples that do not limit the scope of the disclosure to those specific examples.

[0206] Specific details are given in the description to provide a thorough understanding of the embodiments. However, embodiments may be practiced without these specific details. For example, well-known circuits, processes, systems, structures, and techniques have been shown without unnecessary detail in order to avoid obscuring the embodiments. This description provides example embodiments only, and is not intended to limit the scope, applicability, or configuration of the invention. Rather, the preceding description of the embodiments will provide those skilled in the art with an enabling description for implementing various embodiments. Various changes may be made in the function and arrangement of elements without departing from the scope of the present disclosure.

[0207] Also, some embodiments were described as processes depicted as flow diagrams or block diagrams. Although each may describe the operations as a sequential process, many of the operations may be performed in parallel or concurrently. In addition, the order of the operations may be rearranged. A process may have additional steps not included in the figure. Furthermore, embodiments of the methods may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof. When implemented in software, firmware, middleware, or microcode, the program code or code segments to perform the associated tasks may be stored in a computer-readable medium such as a storage medium. Processors may perform the associated tasks. It will be apparent to those skilled in the art that substantial variations may be made in accordance with

specific requirements. For example, customized or special-purpose hardware might also be used, and/or particular elements might be implemented in hardware, software (including portable software, such as applets, etc.), or both. Further, connection to other computing devices such as network input/output devices may be employed.

[0208] Terms "and" and "or" as used herein may include a variety of meanings that are also expected to depend at least in part upon the context in which such terms are used. Typically, "or" if used to associate a list, such as A, B, or C, is intended to mean A, B, and C, here used in the inclusive sense, as well as A, B, or C, here used in the exclusive sense. In addition, the term "one or more" as used herein may be used to describe any feature, structure, or characteristic in the singular or may be used to describe some combination of features, structures, or characteristics. However, it should be noted that this is merely an illustrative example and claimed subject matter is not limited to this example. Furthermore, the term "at least one of" if used to associate a list, such as A, B, or C, can be interpreted to mean A, B, C, or any combination of A, B, and/or C, such as AB, AC, BC, AA, ABC, AAB, AABBCCC, etc.

[0209] Where devices, systems, components or modules are described as being configured to perform certain operations or functions, such configuration can be accomplished, for example, by designing electronic circuits to perform the operation, by programming programmable electronic circuits (such as microprocessors) to perform the operation such as by executing computer instructions or code, or processors or cores programmed to execute code or instructions stored on a non-transitory memory medium, or any combination thereof. Processes can communicate using a variety of techniques, including, but not limited to, conventional techniques for inter-process communications, and different pairs of processes may use different techniques, or the same pair of processes may use different techniques at different times.

[0210] The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense. It will, however, be evident that additions, subtractions, deletions, and other modifications and changes may be made thereunto without departing from the broader scope as set forth in the claims. Thus, although specific embodiments have been described, these are not intended to be limiting. Various modifications and equivalents are within the scope of the following claims.

CLAIMIS:

1. A display device comprising:

a first array of micro light-emitting diodes (micro-LEDs) characterized by a pitch less than 20 μm and including a first common anode for the first array of micro-LEDs; and

a backplane wafer including pixel drive circuits configured to individually address micro-LEDs of the first array of micro-LEDs through cathodes of the micro-LEDs, each pixel drive circuit of the pixel drive circuits including:

an analog current drive circuit connected to a cathode of a micro-LED of the first array of micro-LEDs;

a storage circuit for storing pixel data; and

a timing control circuit configured to control the analog current drive circuit based on the pixel data.

2. The display device of claim 1, wherein each micro-LED of the first array of micro-LEDs includes a mesa structure that includes:

a reflector layer electrically coupled to the cathode of the micro-LED;

an n-type semiconductor layer coupled to the reflector layer;

an active region on the n-type semiconductor layer; and

at least a portion of a p-type semiconductor layer on the active region.

3. The display device of claim 2, wherein the first common anode includes a transparent conductive layer on the p-type semiconductor layer.

4. The display device of claim 2, wherein:

the first common anode includes a metal layer in regions surrounding mesa structures of the first array of micro-LEDs; and

the first array of micro-LEDs includes a plurality of p-contacts coupling the metal layer to the p-type semiconductor layer at a plurality of locations between the mesa structures of the first array of micro-LEDs; and optionally

wherein the metal layer is on sidewalls of the mesa structures of the first array of micro-LEDs and regions between the mesa structures of the first array of micro-LEDs.

5. The display device of claim 2, wherein the active region includes GaN-based semiconductor materials or phosphide-based semiconductor materials.

6. The display device of claim 1, wherein the cathode of the micro-LED is bonded to the backplane wafer; and/or

wherein the backplane wafer includes:

a first voltage regulator configured to output a first positive supply voltage to the timing control circuit; and

a second voltage regulator configured to output a second positive supply voltage to the first common anode of the first array of micro-LEDs; and optionally

wherein:

the first array of micro-LEDs is configured to emit light in a first wavelength range;

the display device includes a second array of micro-LEDs that includes a second common anode and is configured to emit light in a second wavelength range; and

the backplane wafer further includes a third voltage regulator configured to output a third positive supply voltage to the second common anode of the second array of micro-LEDs.

7. The display device of claim 1, wherein the timing control circuit includes:

a pulse-width modulation (PWM) latch configured to generate PWM signals for controlling the analog current drive circuit; and

a comparator configured to compare the pixel data with a counter value and generate a control signal to control the PWM latch.

8. The display device of claim 1, wherein the analog current drive circuit is on a indium-gallium-zinc-oxide (IGZO) layer.

9. The display device of claim 1, wherein the backplane wafer includes a common control circuit shared by two or more micro-LED of the first array of micro-LEDs.

10. The display device of claim 1, wherein the storage circuit for storing pixel data includes an analog data storage circuit, a digital data storage circuit, or a combination.

11. The display device of claim 1, wherein a pitch of the pixel drive circuits matches the pitch of the first array of micro-LEDs.

12. A display device comprising an array of pixels characterized by a pitch less than 20 μm, each pixel of the array of pixels comprising:

a micro light-emitting diode (micro-LED); and

a pixel drive circuit electrically connected to the micro-LED, the pixel drive circuit comprising:

an analog current drive circuit connected to a cathode of the micro-LED;

a storage circuit for storing pixel data; and

a timing control circuit configured to control the analog current drive circuit based on the pixel data,

wherein anodes of micro-LEDs of the array of pixels are electrically shorted.

13. The display device of claim 12, wherein the anodes of the micro-LEDs of the array of pixels are connected to: a transparent conductive layer; and/or

a metal layer in regions between the array of pixels.

14. The display device of claim 12, wherein the micro-LED includes GaN-based semiconductor materials or phosphide-based semiconductor materials.

15. The display device of claim 12, further comprising:

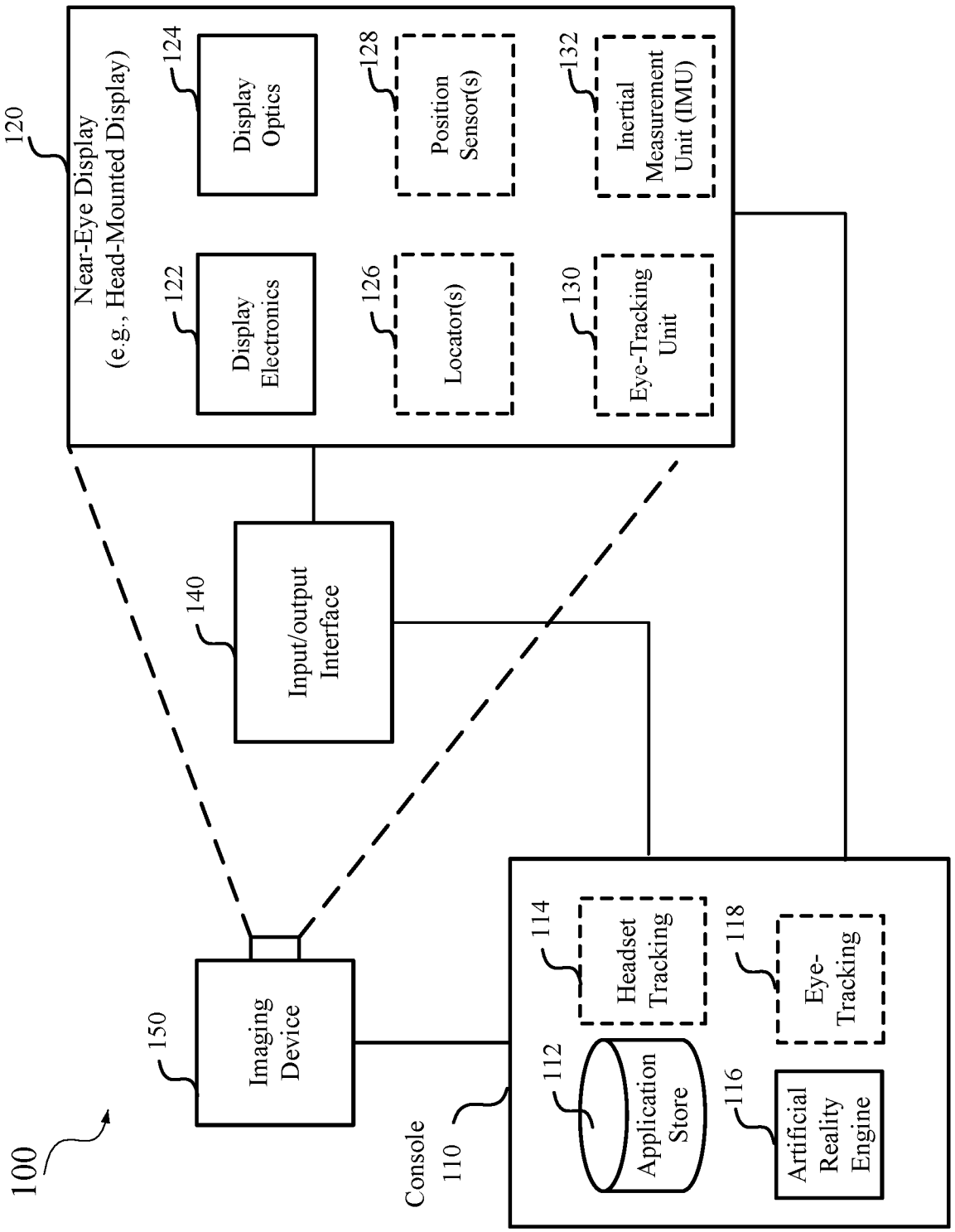
a first voltage regulator configured to output a first positive supply voltage to the timing control circuit; and

a second voltage regulator configured to output a second positive supply voltage to the anodes of the micro-LEDs of the array of pixels; and/or

wherein the timing control circuit includes:

a pulse-width modulation (PWM) latch configured to generate PWM signals for controlling the analog current drive circuit; and

a comparator configured to compare the pixel data with a counter value and generate a control signal to control the PWM latch.


100
120
Near-Eye Display
(e.g., Head-Mounted Display)
124
Display Optics
122
Display Electronics
128
Position Sensor(s)
126
Locator(s)
132
Inertial Measurement Unit (IMU)
130
Eye-Tracking Unit
140
Input/output Interface
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Imaging Device
Console
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Application Store
114
Headset Tracking
116
Artificial Reality Engine
118
Eye-Tracking

FIG. 1

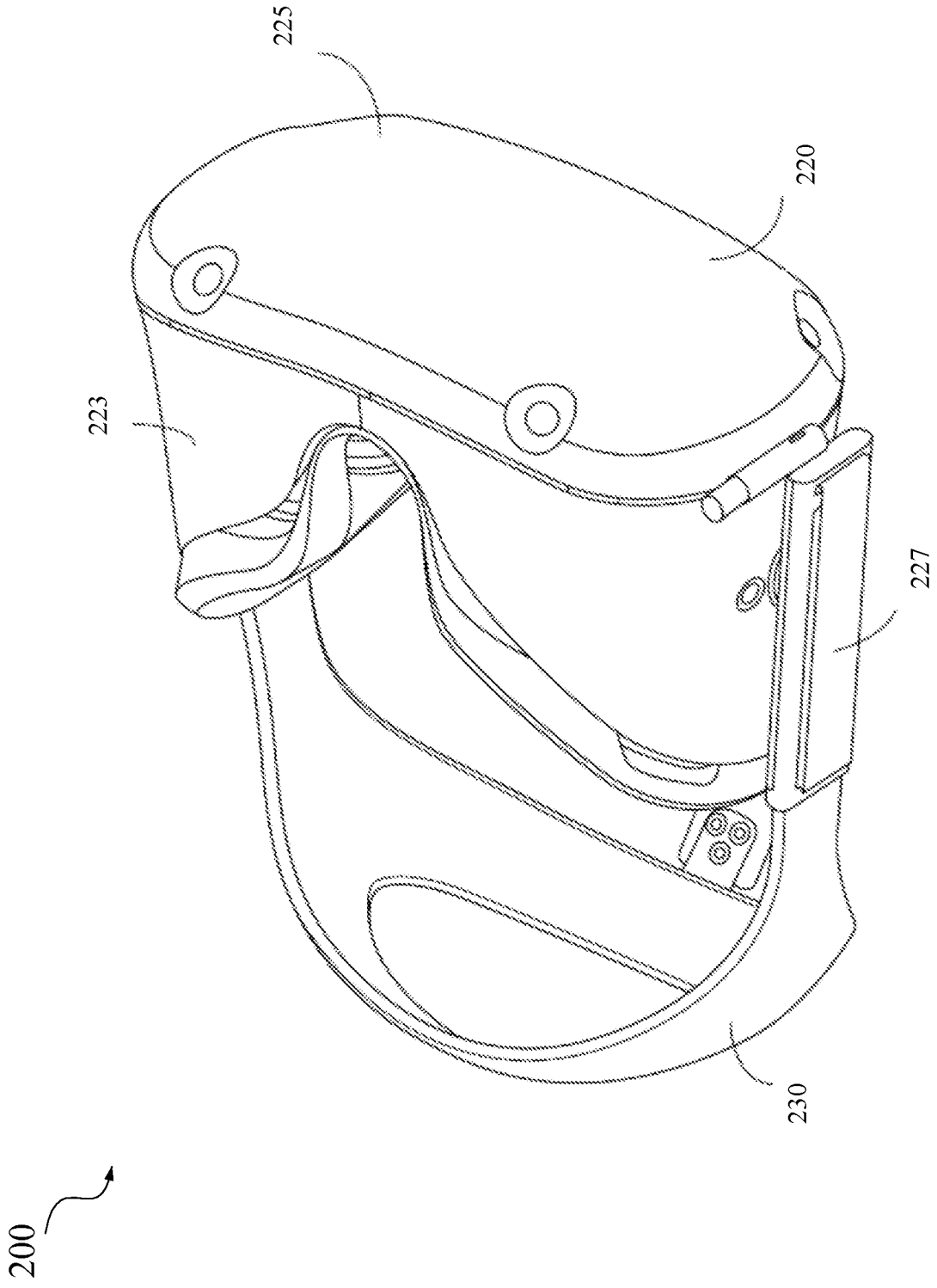

FIG. 2

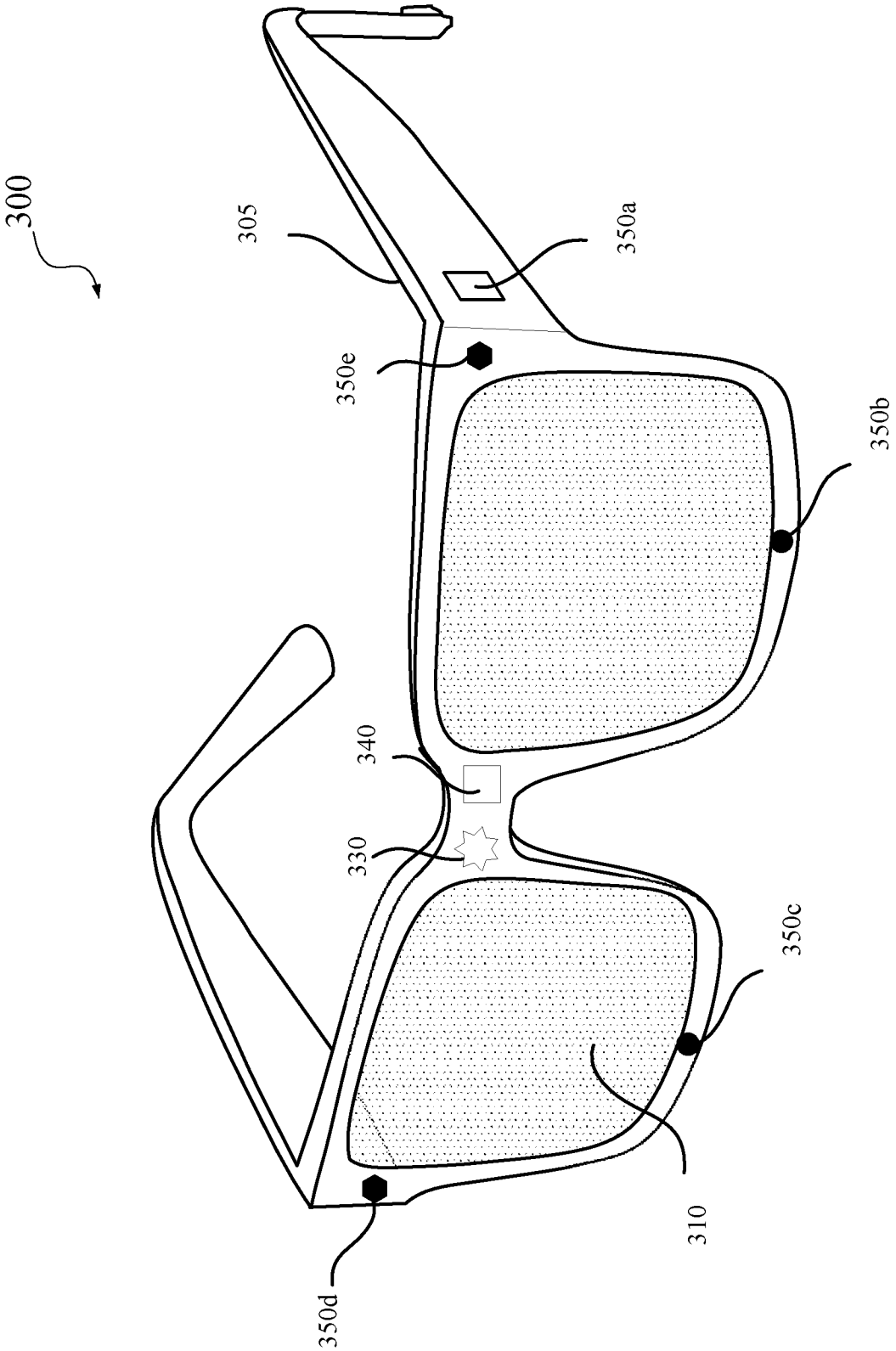

FIG. 3

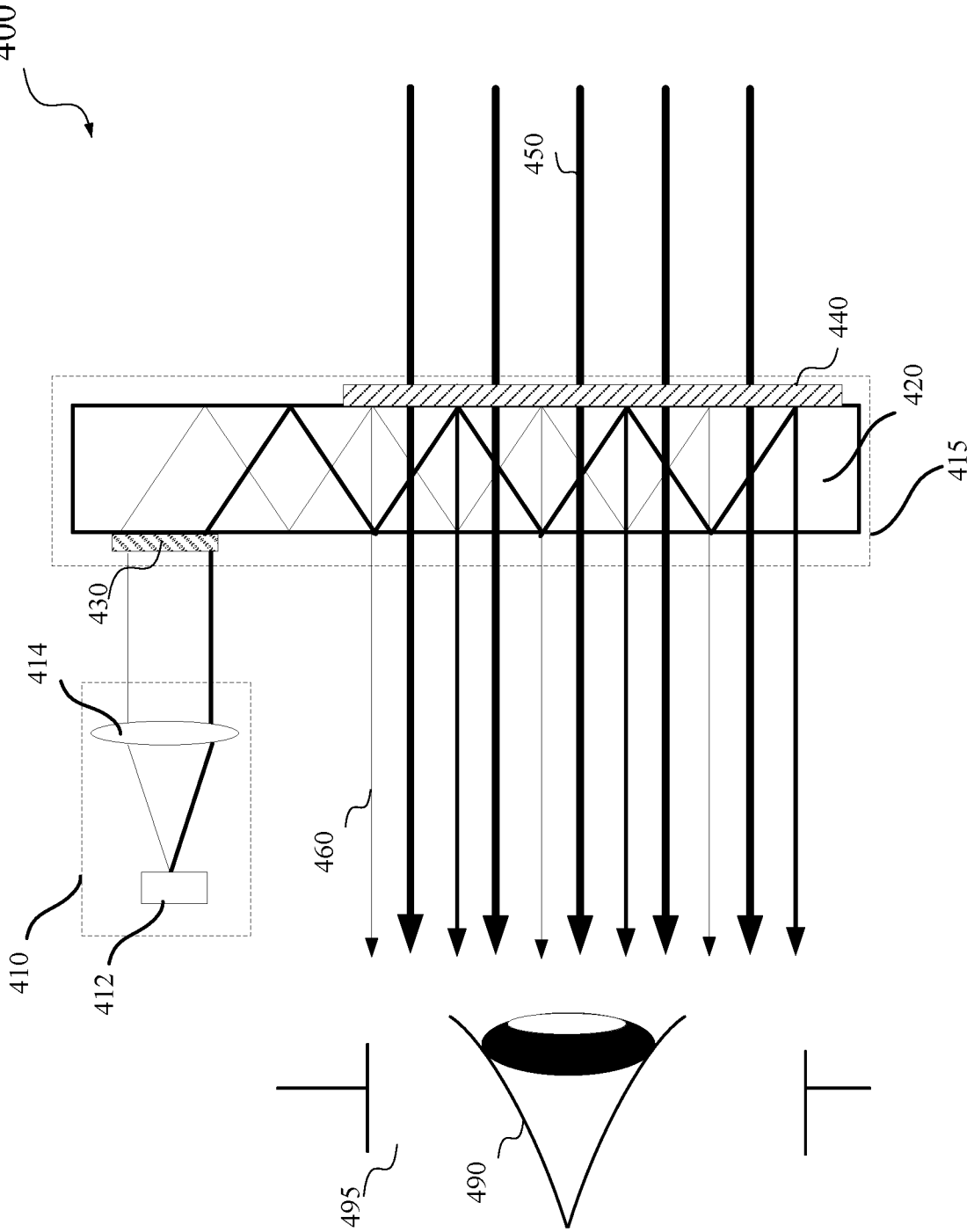

FIG. 4

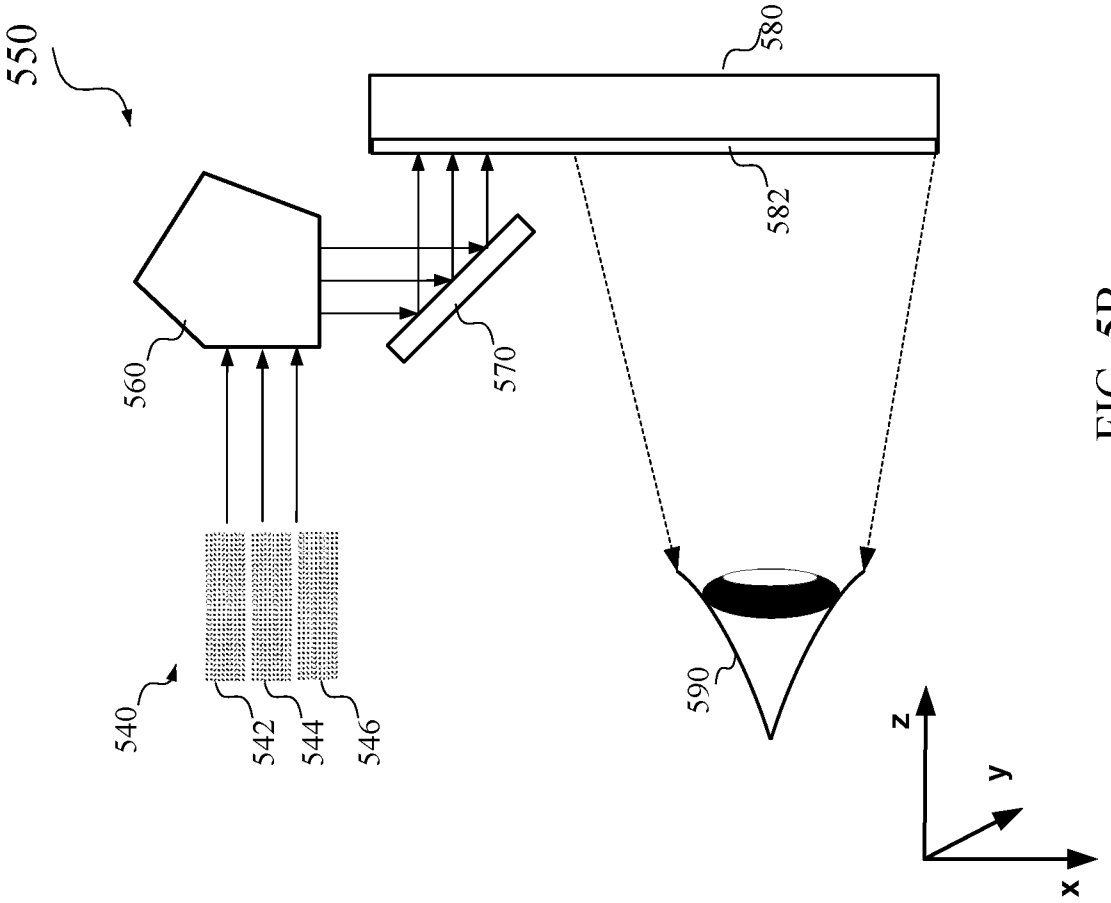
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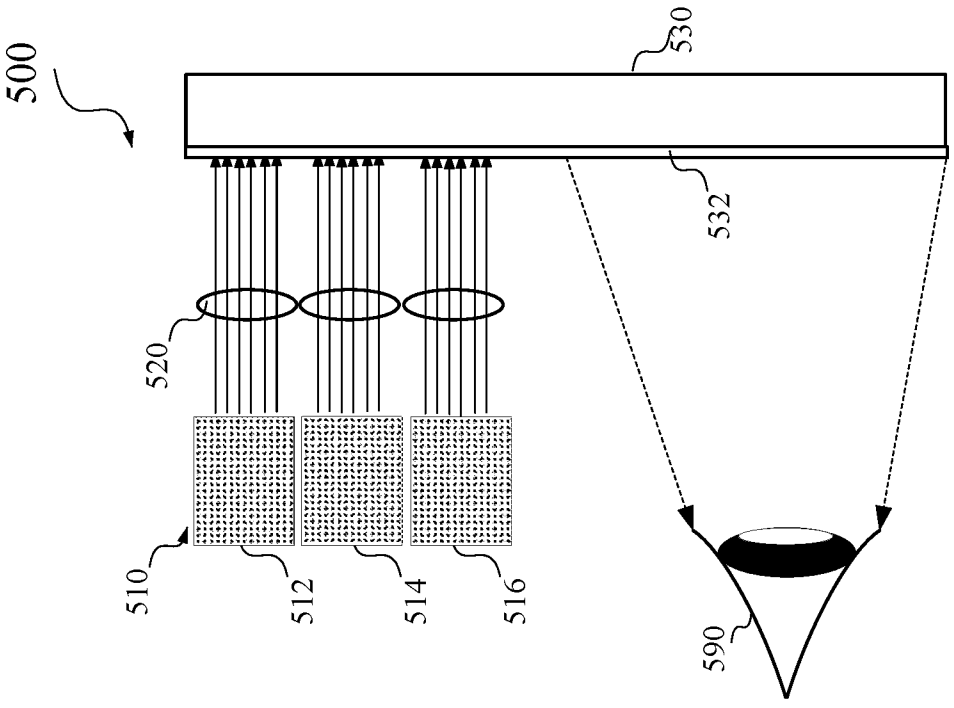
FIG. 5B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510
512
514
516
590

FIG. 5A

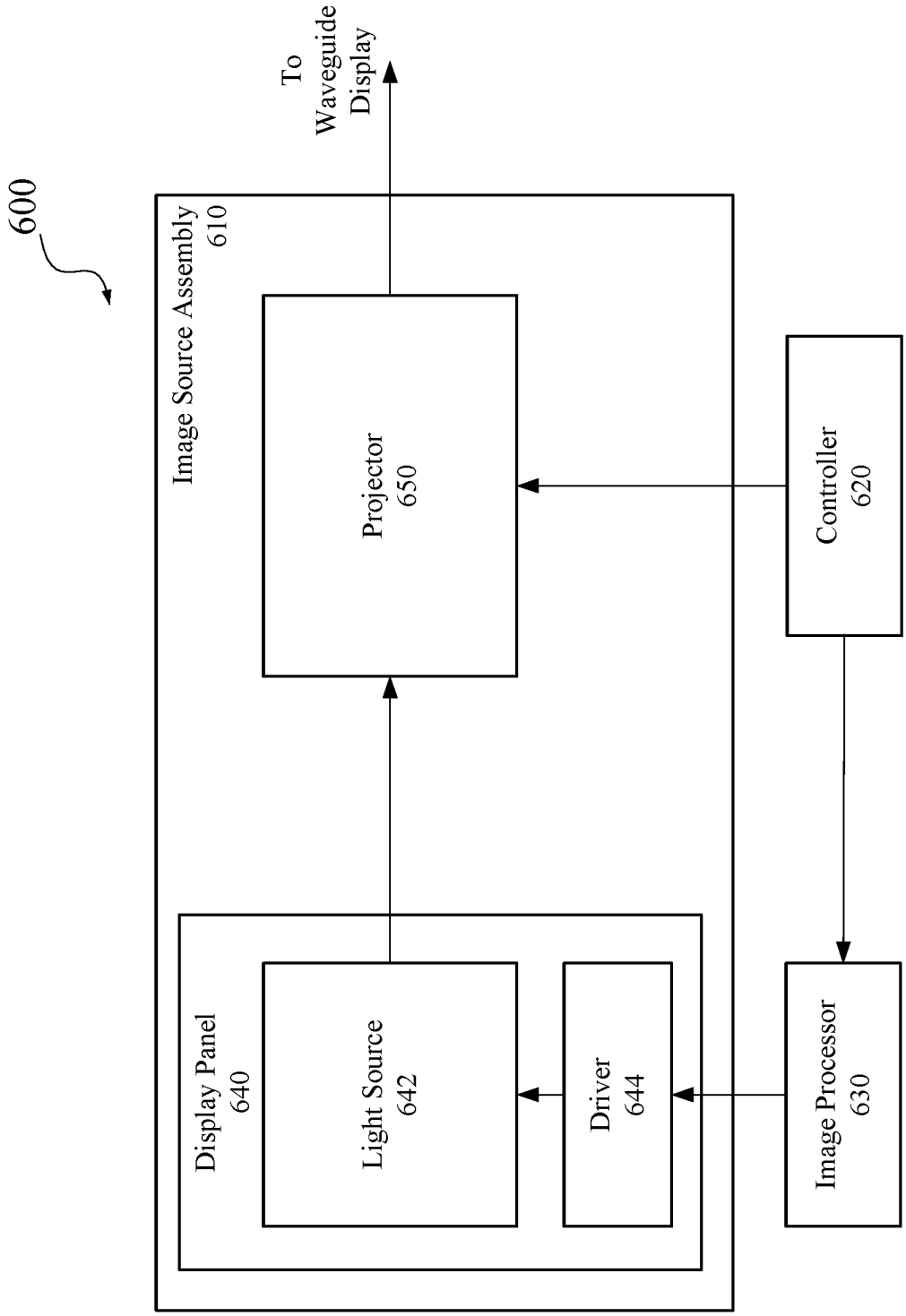
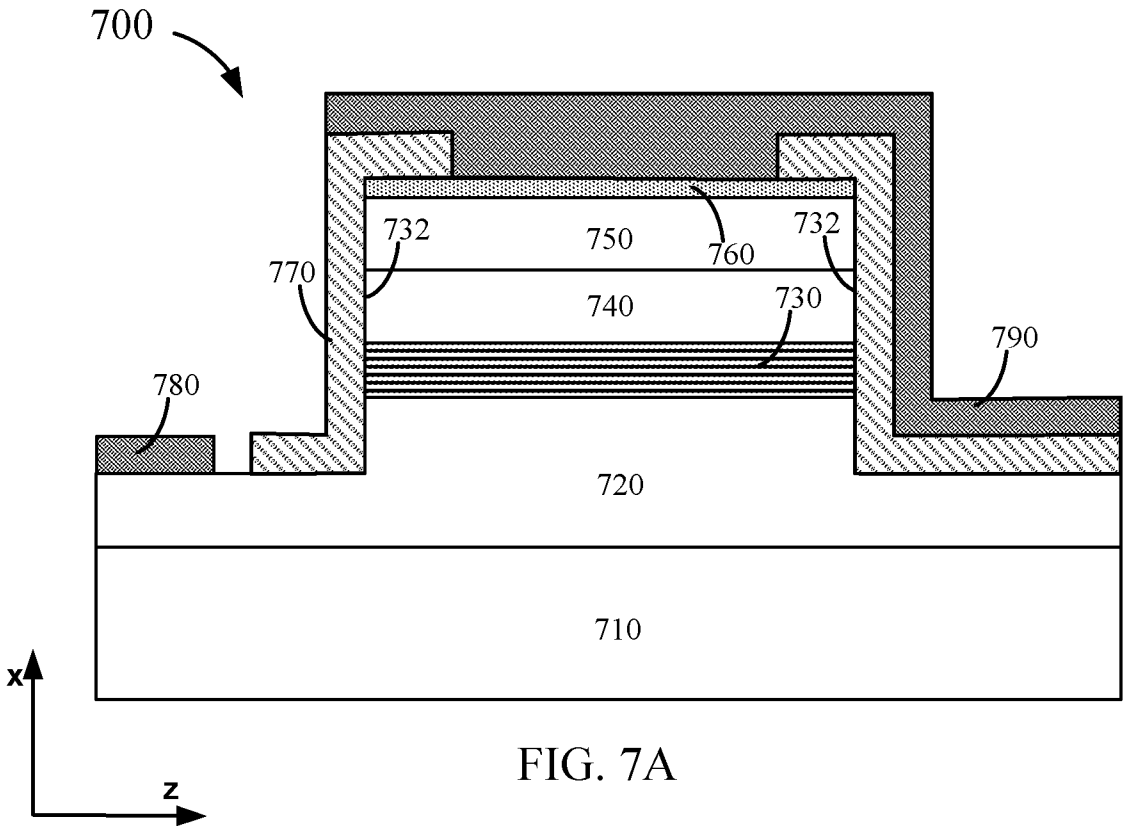

600
Image Source Assembly
610
To
Waveguide
Display
Projector
650
Controller
620
Display Panel
640
Light Source
642
Driver
644
Image Processor
630

FIG. 6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760
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770
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790
780
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710
x
z

FIG. 7A

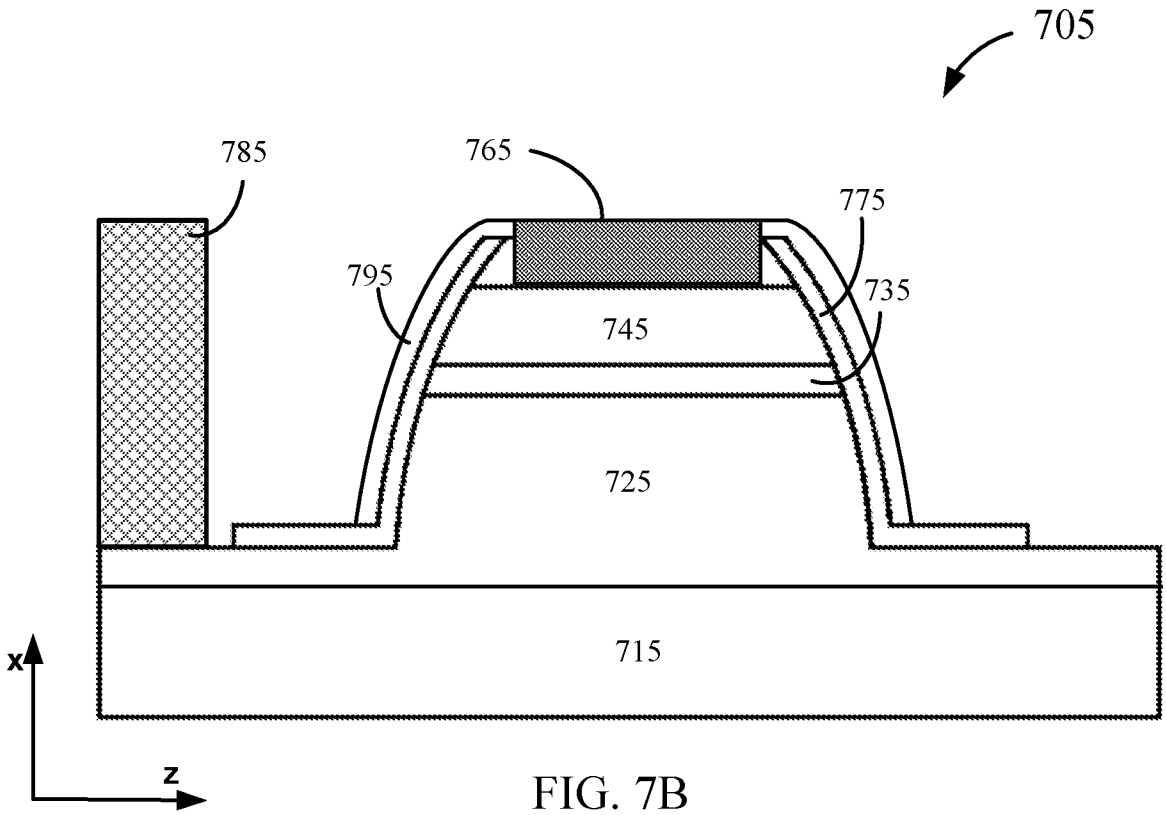
705
785
765
775
795
735
745
725
715
x
z

FIG. 7B

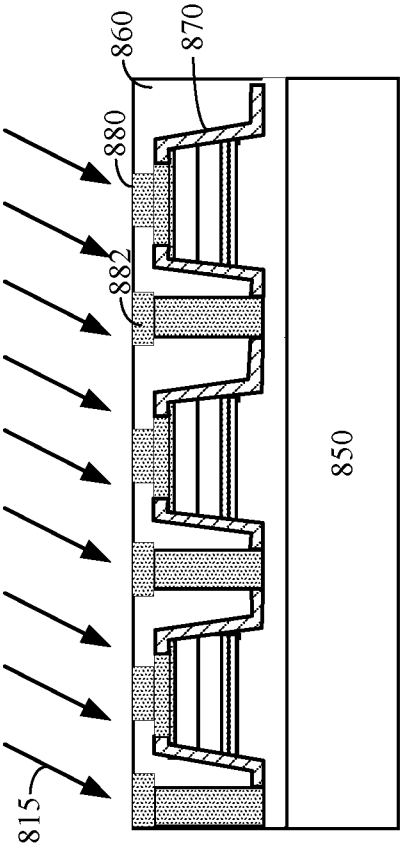

FIG. 8B

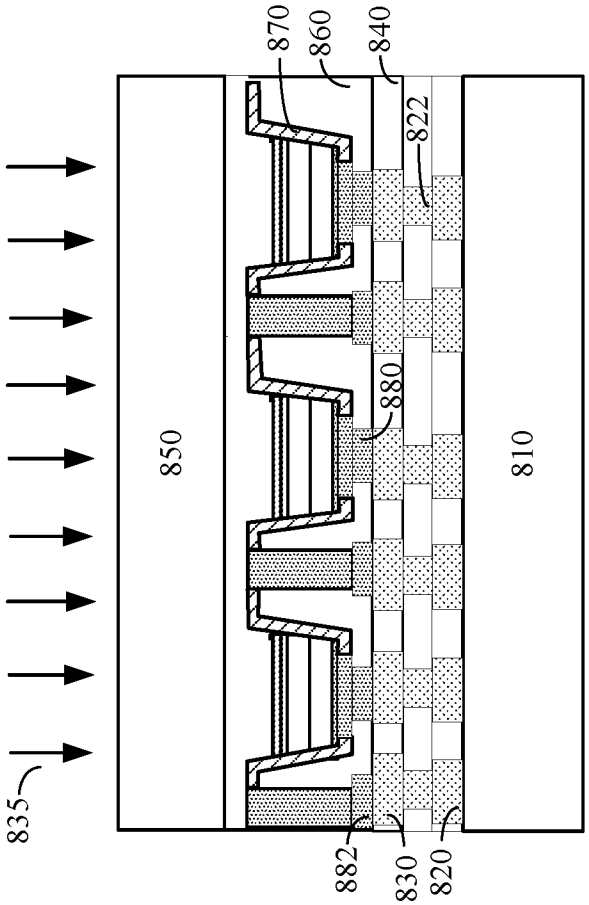

FIG. 8D

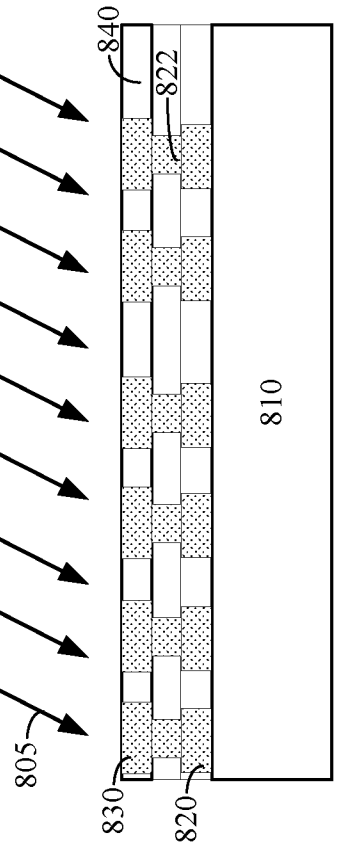

FIG. 8A

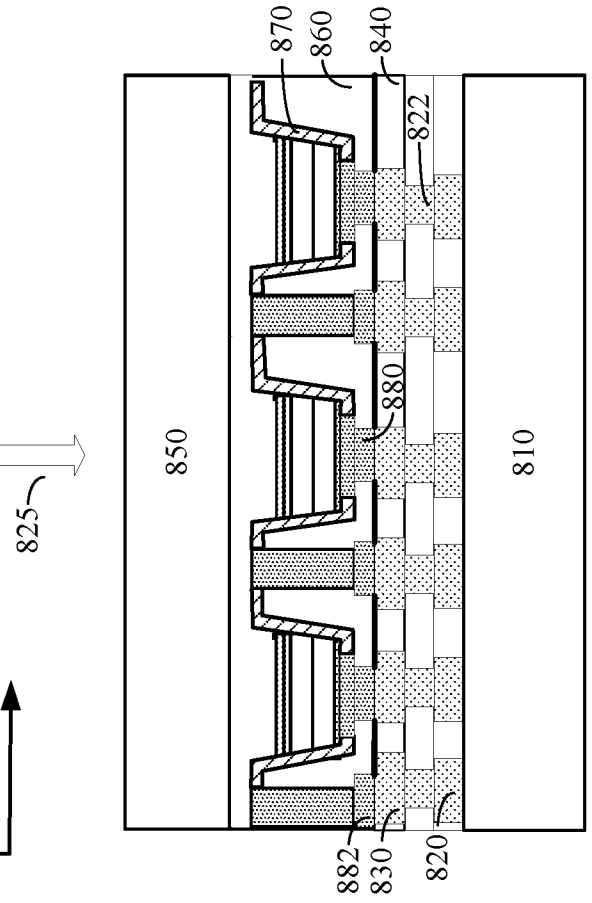

FIG. 8C

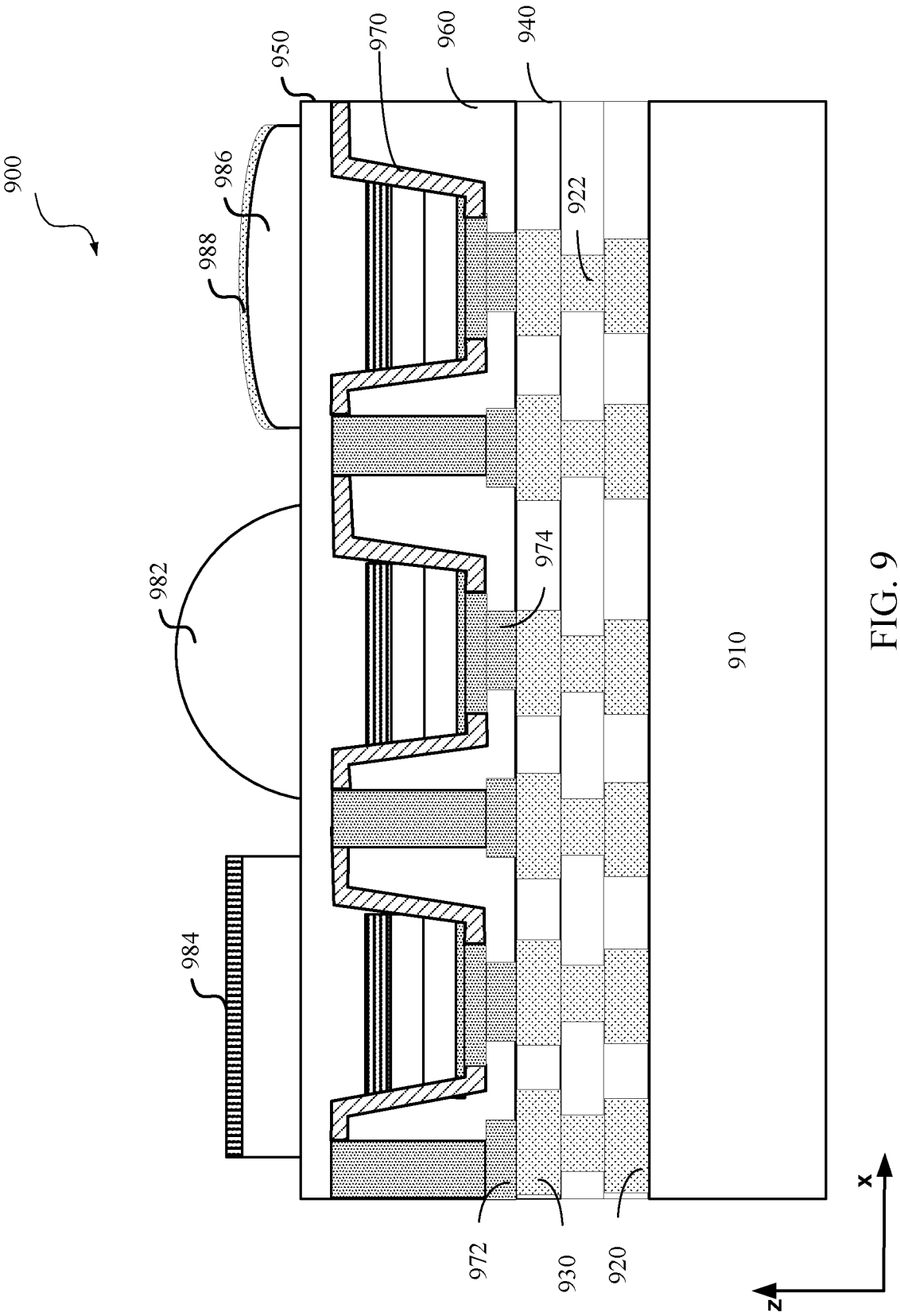

FIG. 9

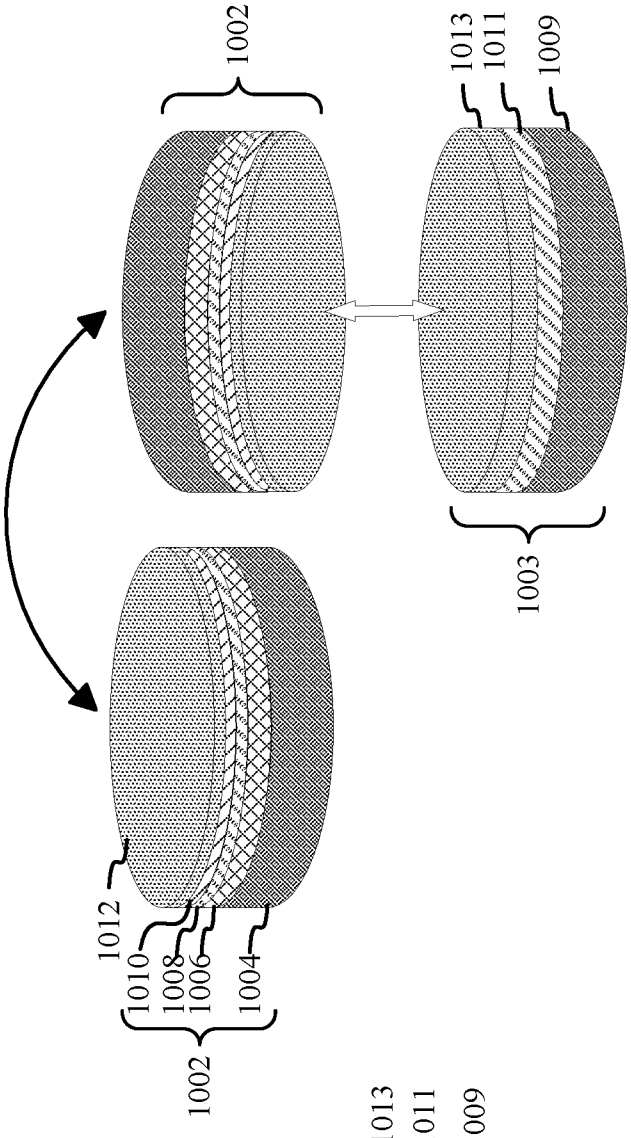

FIG. 10B

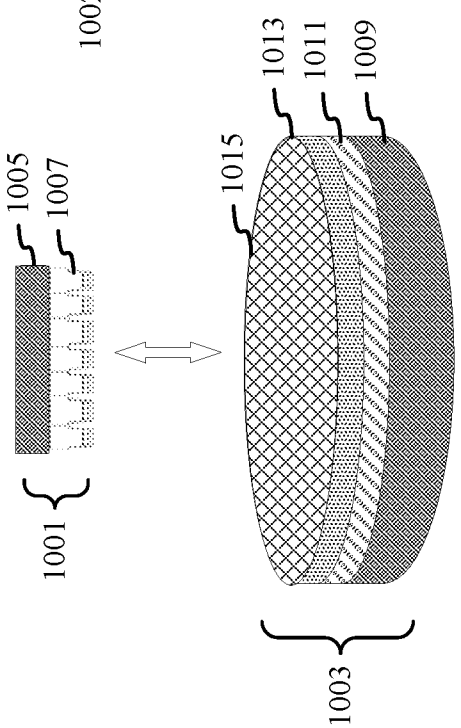

FIG. 10A

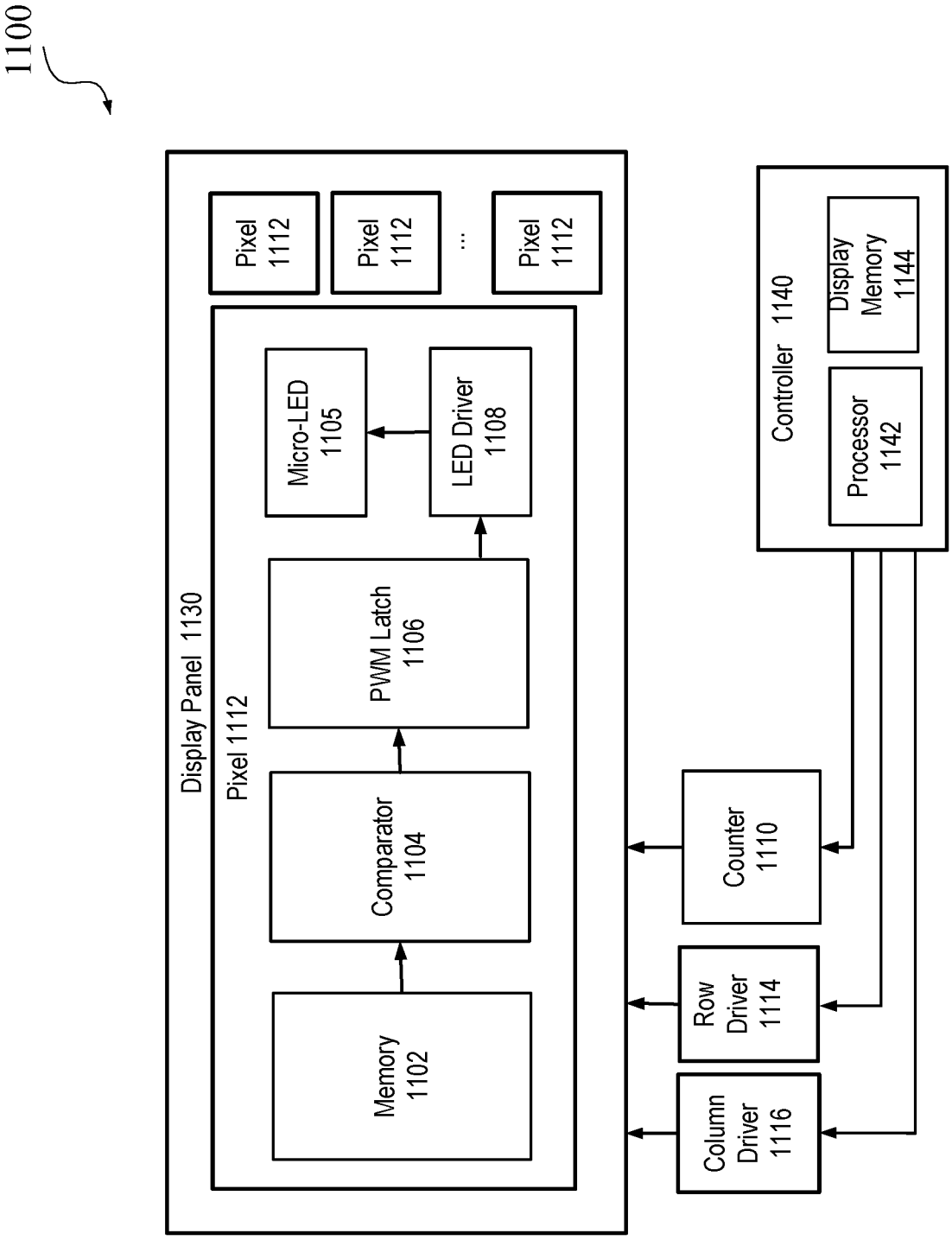
1100
Display Panel 1130
Pixel 1112
Pixel 1112
...
Pixel 1112
Pixel 1112
Micro-LED 1105
LED Driver 1108
PWM Latch 1106
Comparator 1104
Memory 1102
Counter 1110
Row Driver 1114
Column Driver 1116
Controller 1140
Display Memory 1144
Processor 1142

FIG. 11

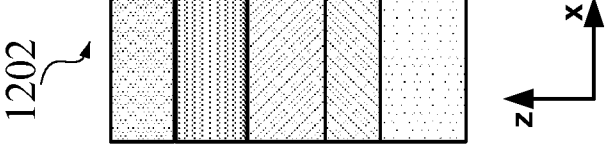

FIG. 12A

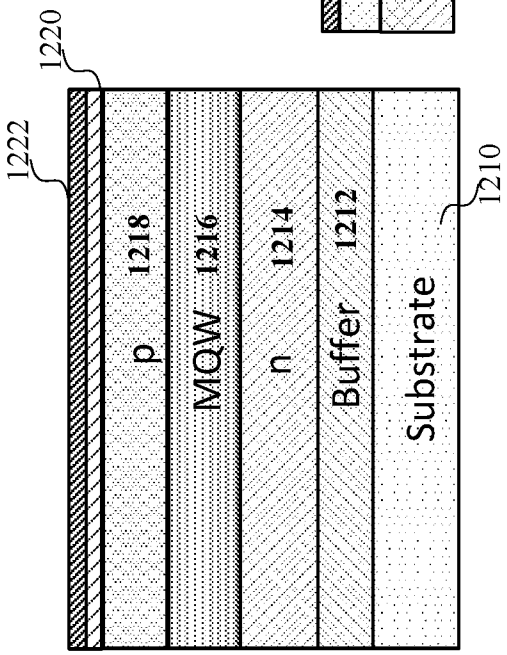

FIG. 12B

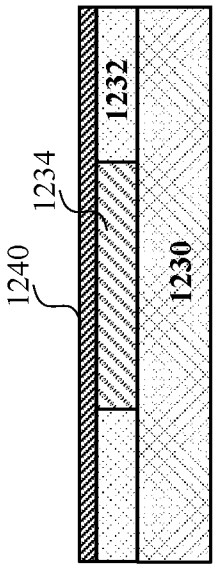

FIG. 12C

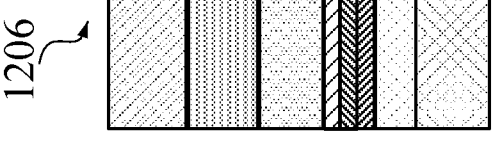

FIG. 12D

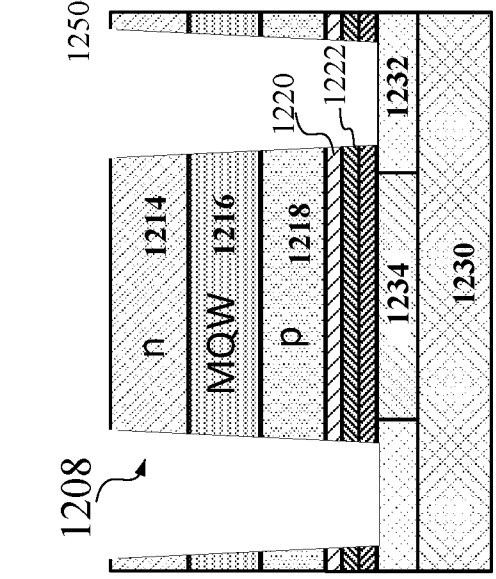

FIG. 12E

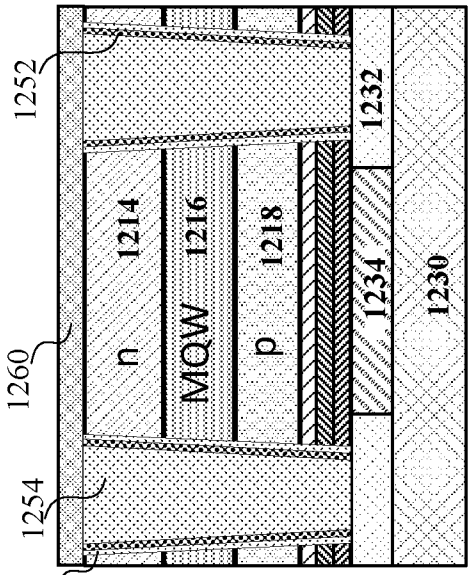

FIG. 12F

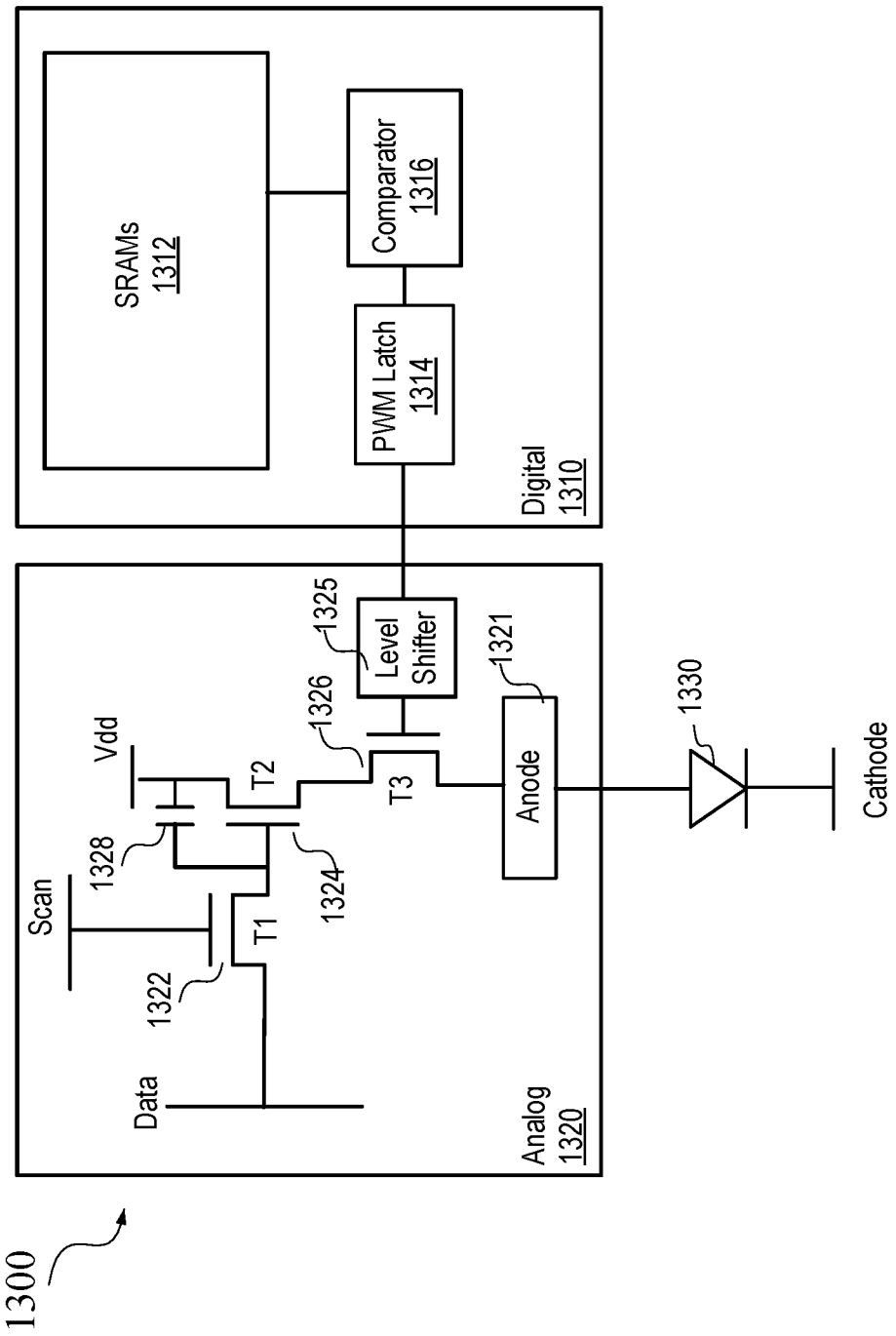
1300
Digital
1310
SRAMs
1312
Comparator
1316
PWM Latch
1314
Analog
1320
Level
Shifter
1325
1326
1321
1330
Anode
Cathode
Vdd
T2
T3
T1
1328
1324
1322
Scan
Data

FIG. 13

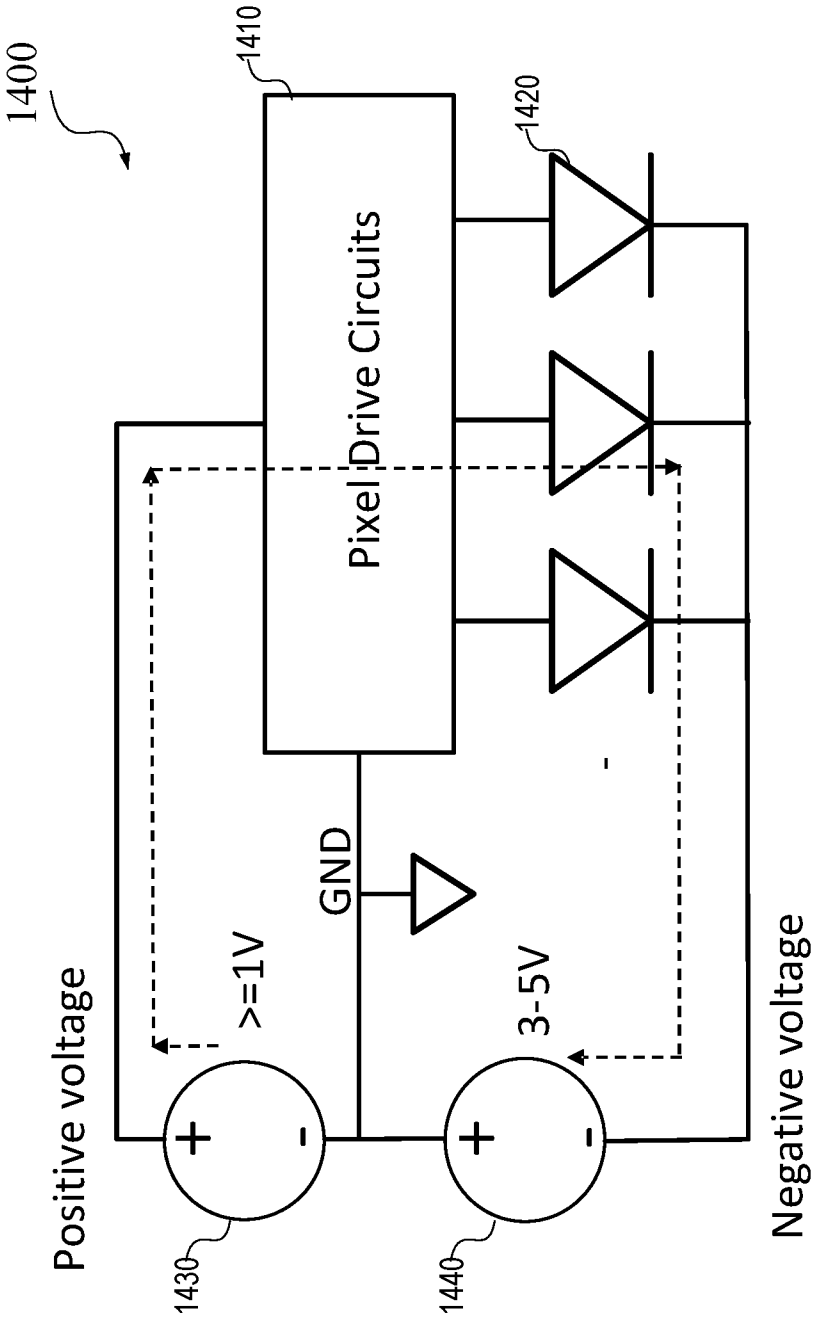
1400
1410
1420
Pixel Drive Circuits
GND
>=1V
3-5V
Positive voltage
Negative voltage
1430
1440

FIG. 14

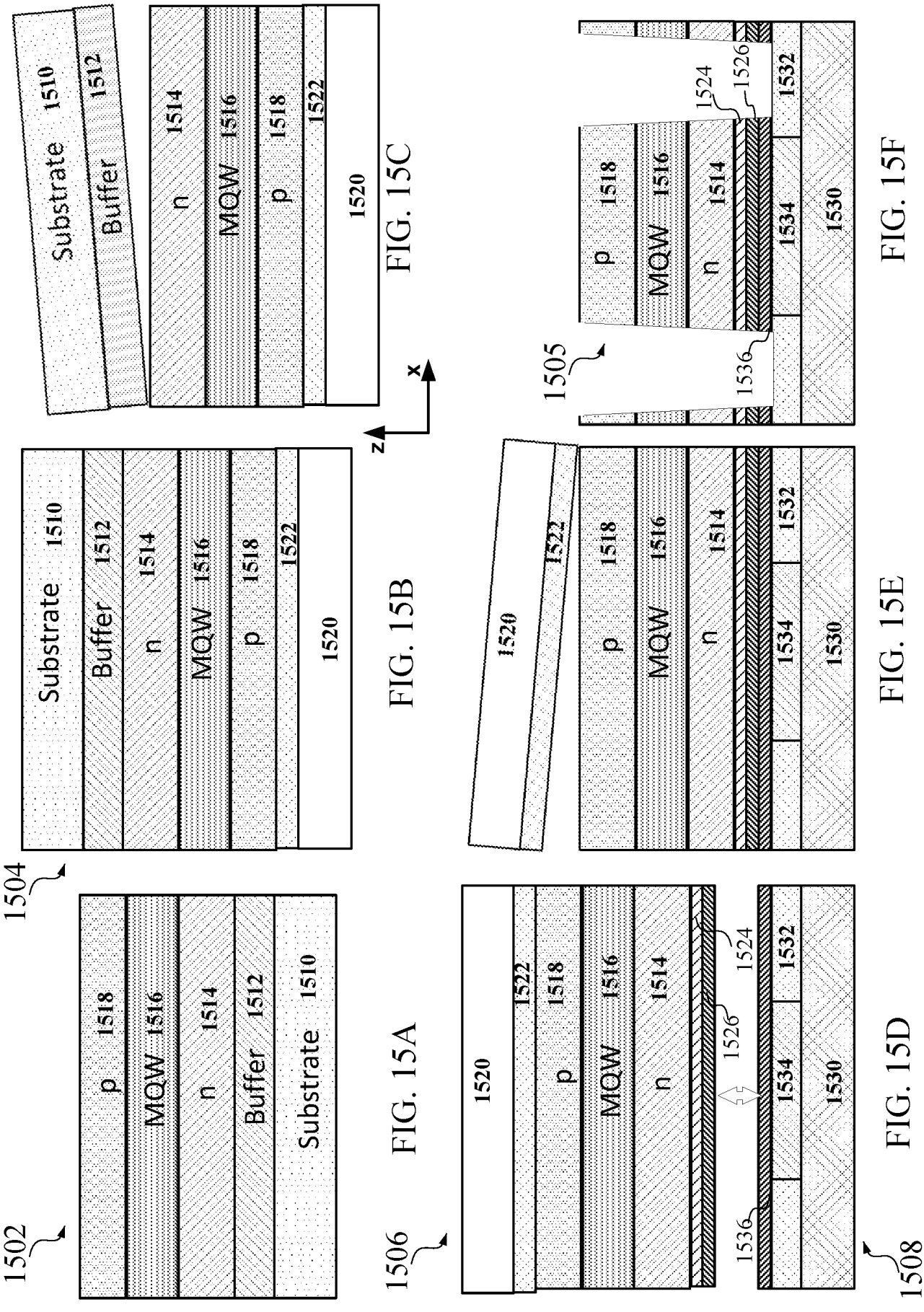

FIG. 15A FIG. 15B FIG. 15C FIG. 15D FIG. 15E FIG. 15F

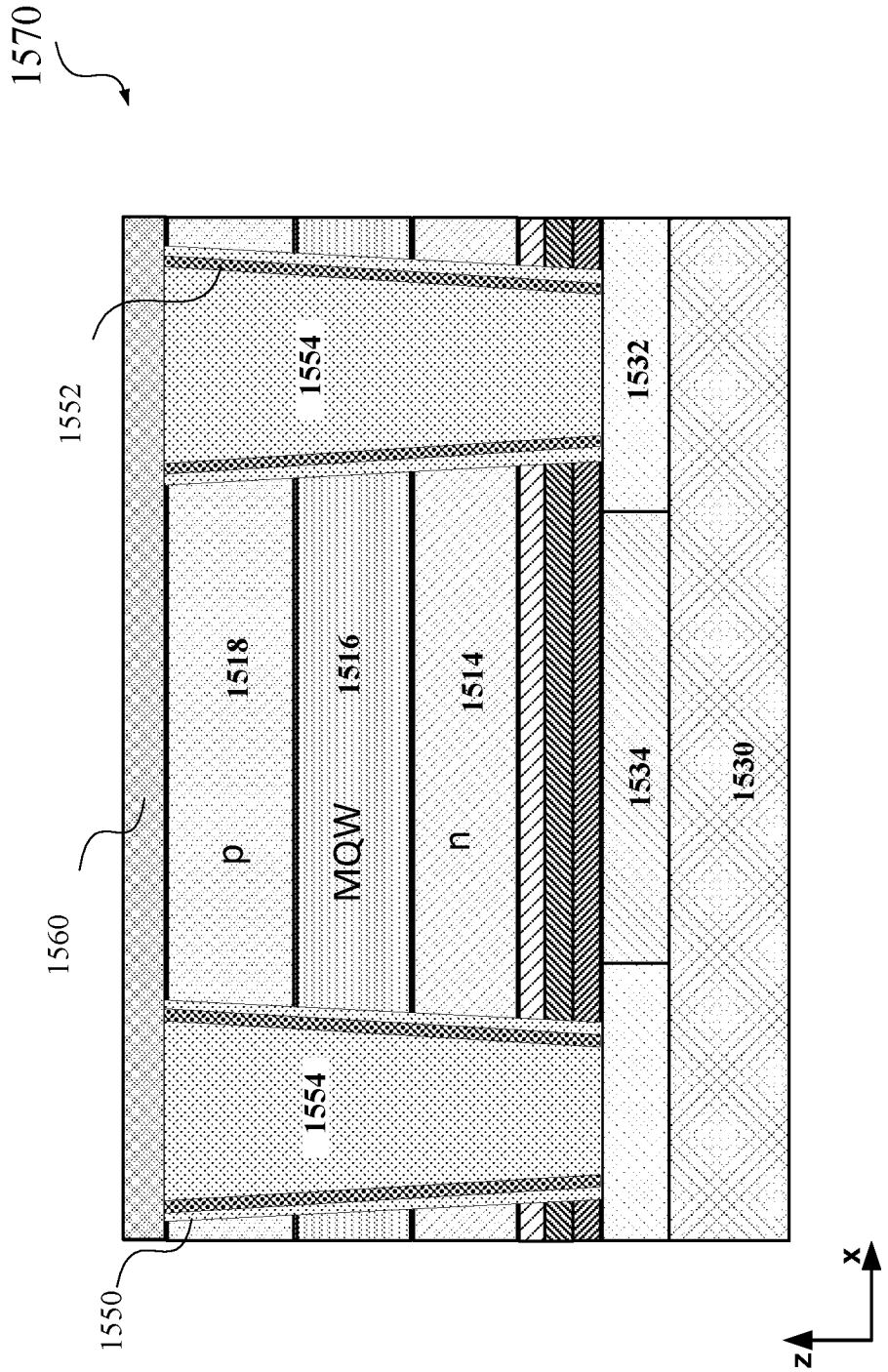
1570
1552
1554
1532
1518
1516
1514
1560
p
MQW
n
1534
1530
1554
1550
x
z

FIG. 15G

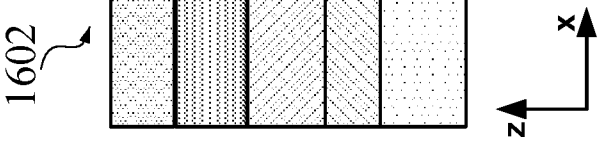

FIG. 16A

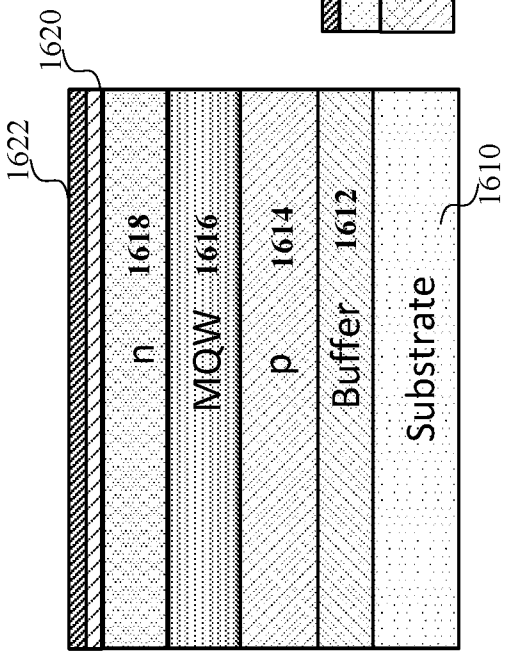

FIG. 16B

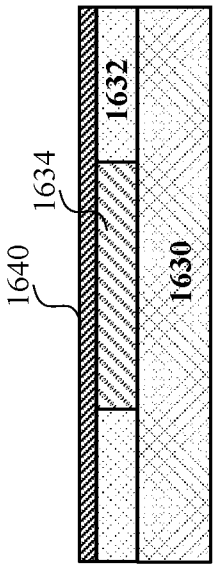

FIG. 16C

FIG. 16D

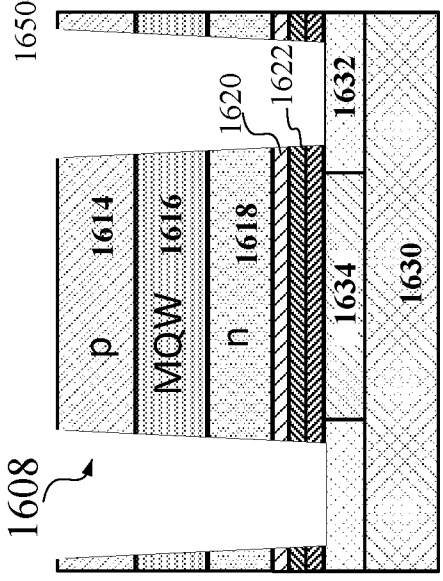

FIG. 16E

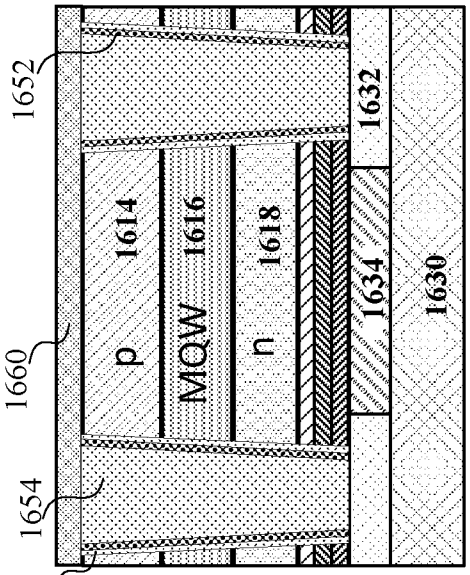

FIG. 16F

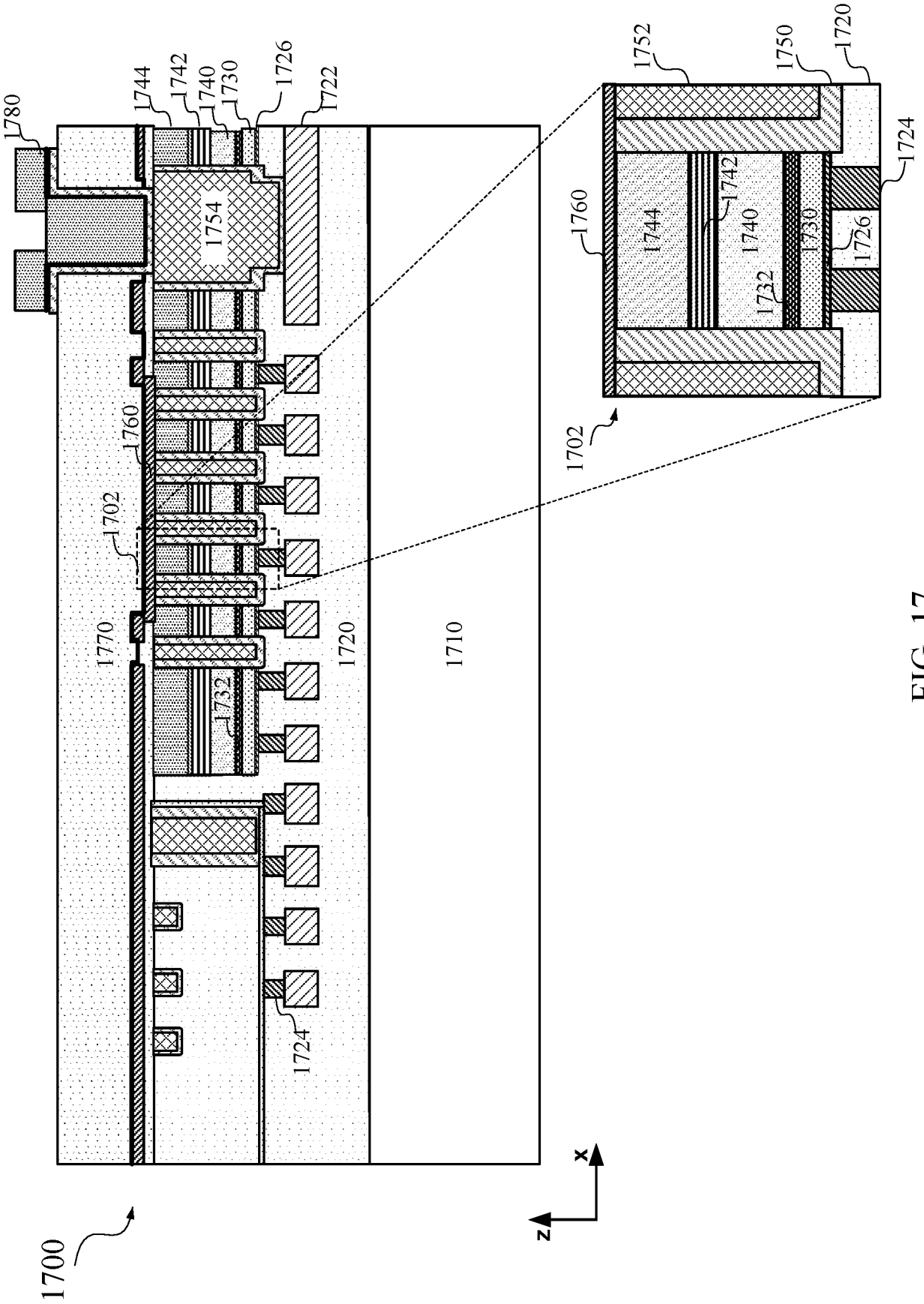
1700
1710
1720
1722
1724
1726
1730
1732
1740
1742
1744
1750
1752
1754
1760
1770
1780
1702
x
z

FIG. 17

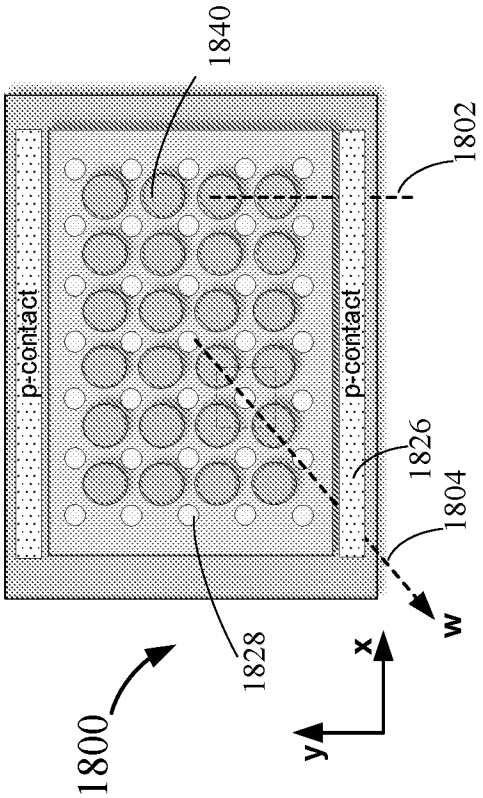

FIG. 18A

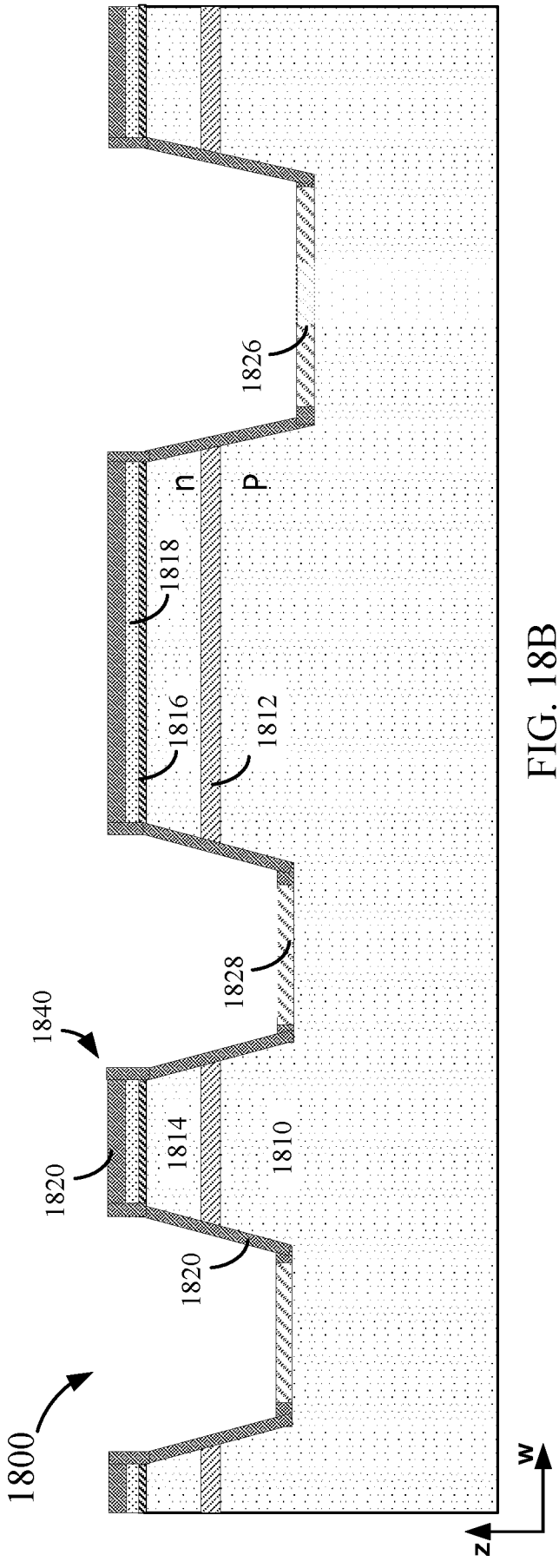

FIG. 18B

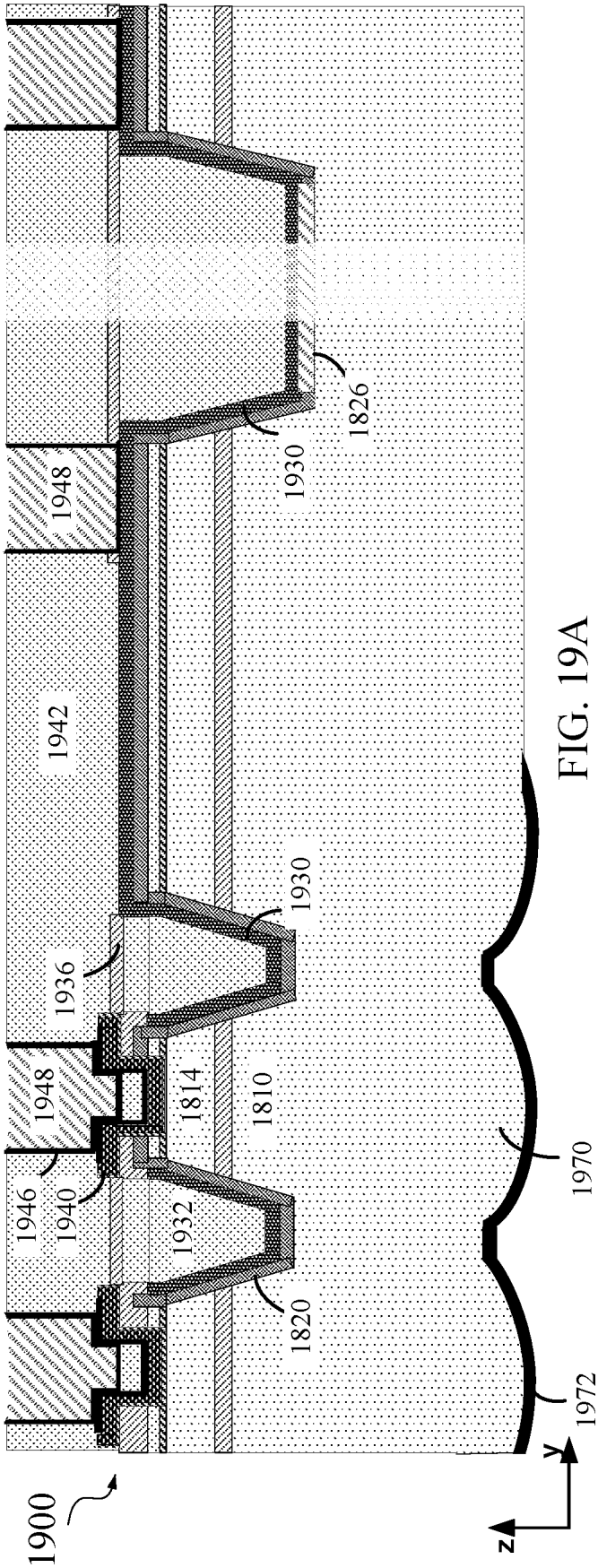

FIG. 19A

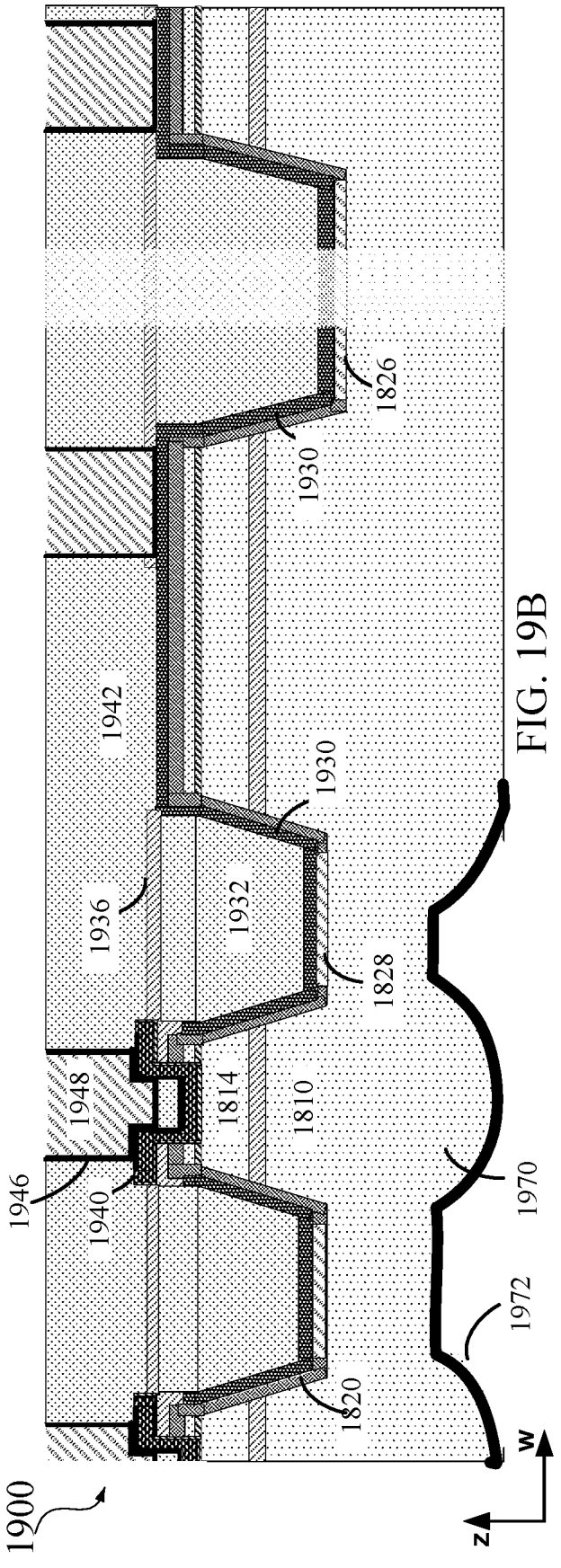

FIG. 19B

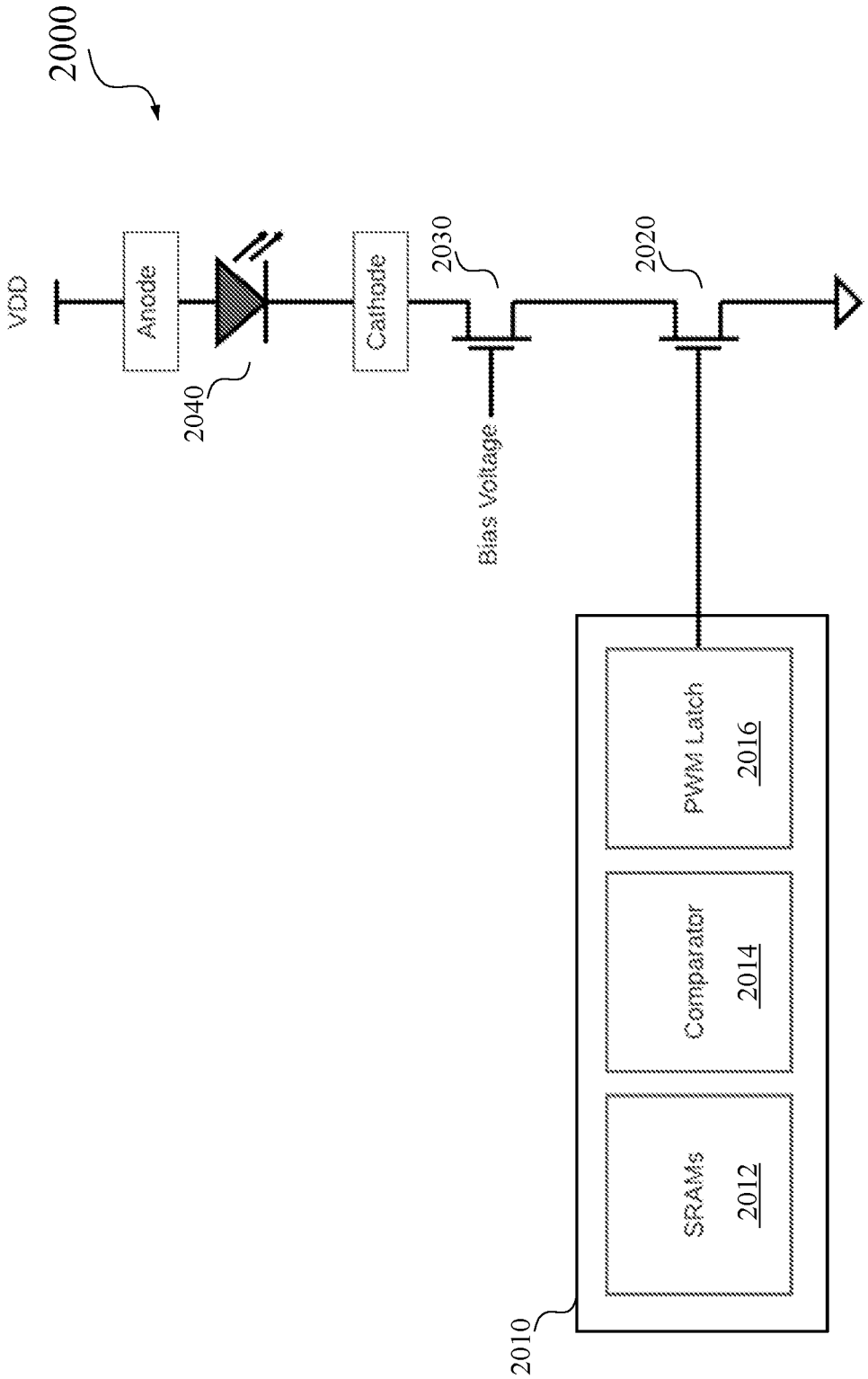
2000
VDD
Anode
2040
Cathode
2030
Bias Voltage
2020
2010
SRAMs
2012
Comparator
2014
PWM Latch
2016

FIG. 20

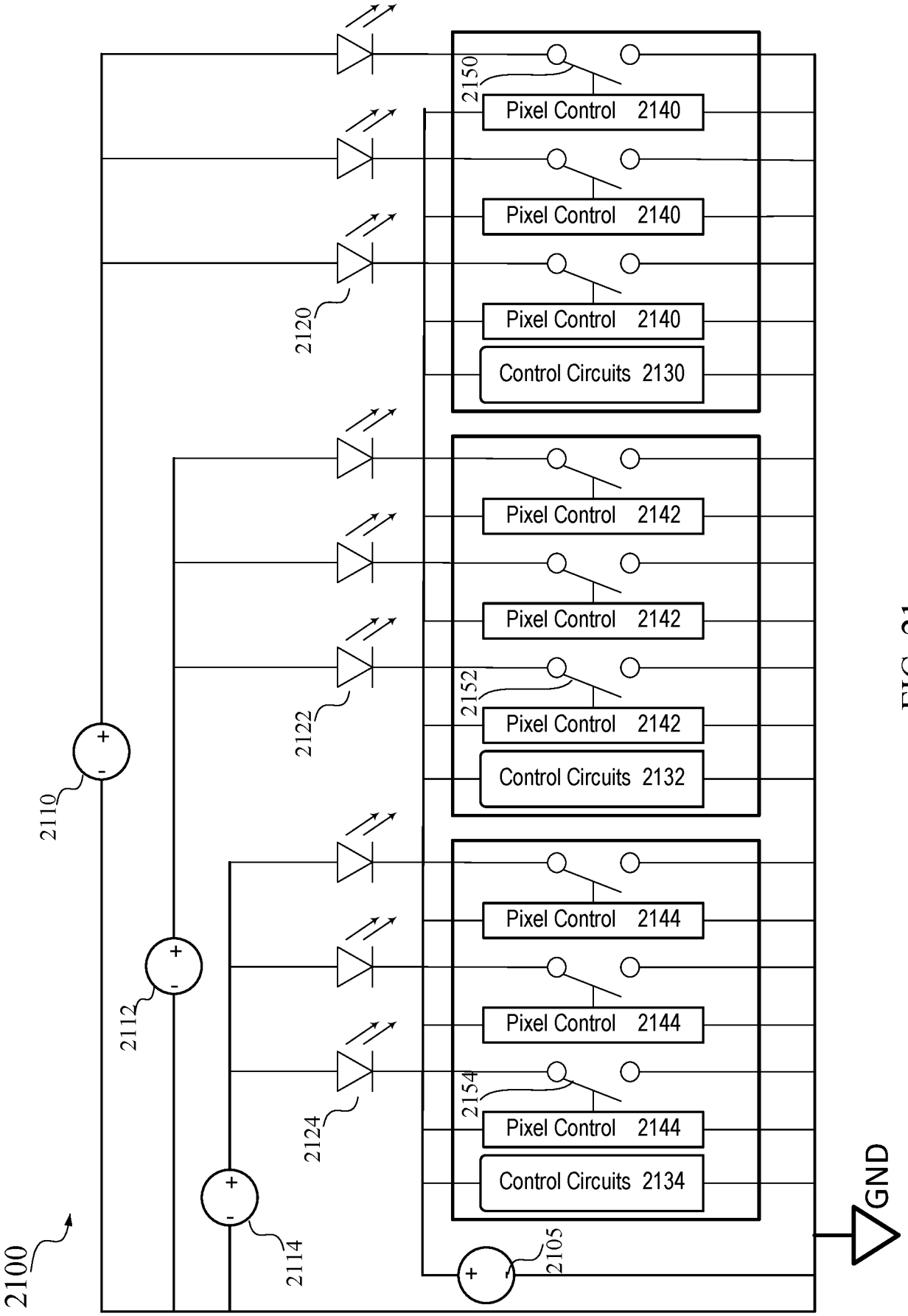
2100
2110
2112
2114
2120
2122
2124
2150
2152
2154
2105
Pixel Control 2140
Pixel Control 2140
Pixel Control 2140
Control Circuits 2130
Pixel Control 2142
Pixel Control 2142
Pixel Control 2142
Control Circuits 2132
Pixel Control 2144
Pixel Control 2144
Pixel Control 2144
Control Circuits 2134
GND

FIG. 21

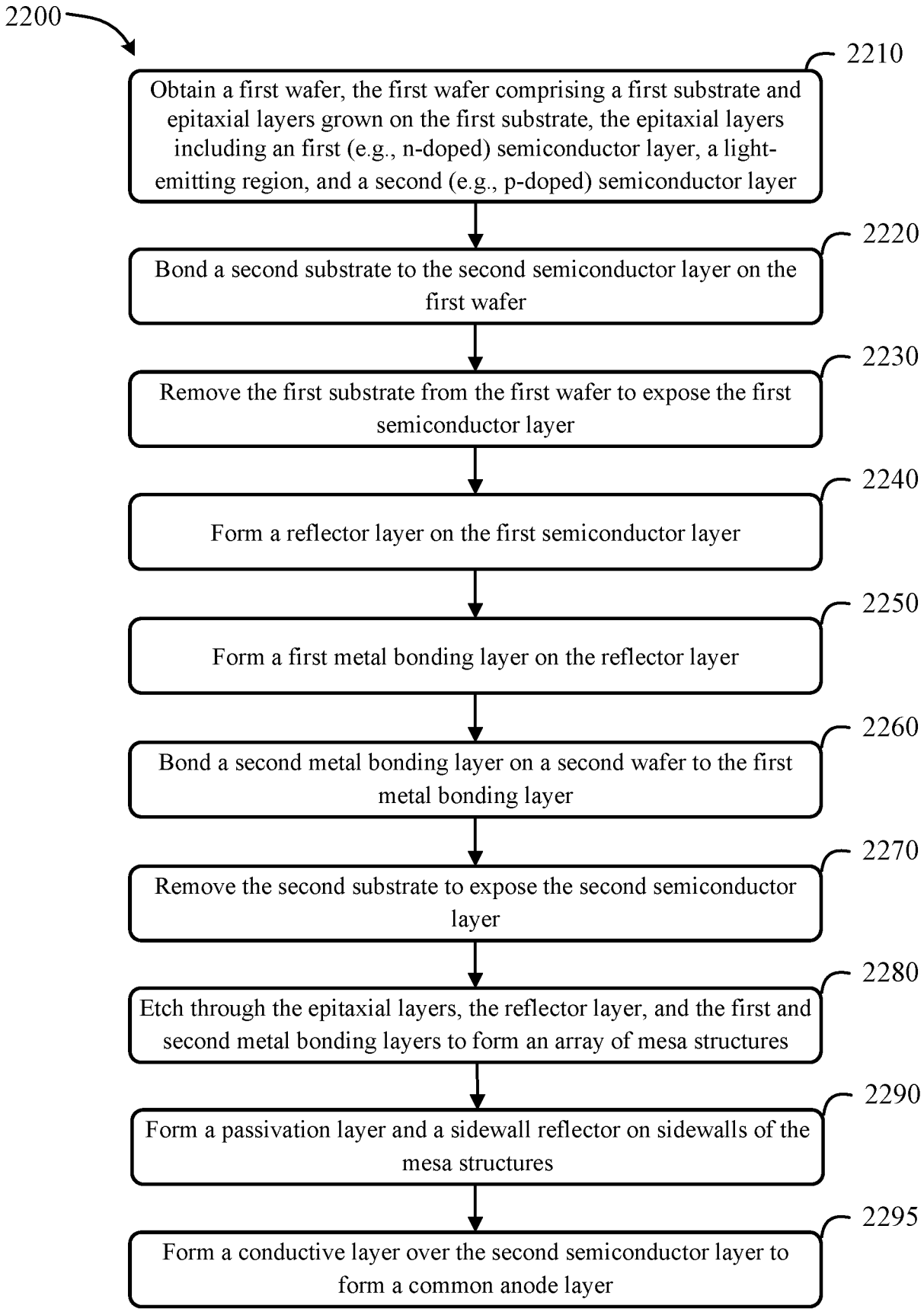
2200
2210
Obtain a first wafer, the first wafer comprising a first substrate and epitaxial layers grown on the first substrate, the epitaxial layers including an first (e.g., n-doped) semiconductor layer, a light-emitting region, and a second (e.g., p-doped) semiconductor layer
2220
Bond a second substrate to the second semiconductor layer on the first wafer
2230
Remove the first substrate from the first wafer to expose the first semiconductor layer
2240
Form a reflector layer on the first semiconductor layer
2250
Form a first metal bonding layer on the reflector layer
2260
Bond a second metal bonding layer on a second wafer to the first metal bonding layer
2270
Remove the second substrate to expose the second semiconductor layer
2280
Etch through the epitaxial layers, the reflector layer, and the first and second metal bonding layers to form an array of mesa structures
2290
Form a passivation layer and a sidewall reflector on sidewalls of the mesa structures
2295
Form a conductive layer over the second semiconductor layer to form a common anode layer

FIG. 22

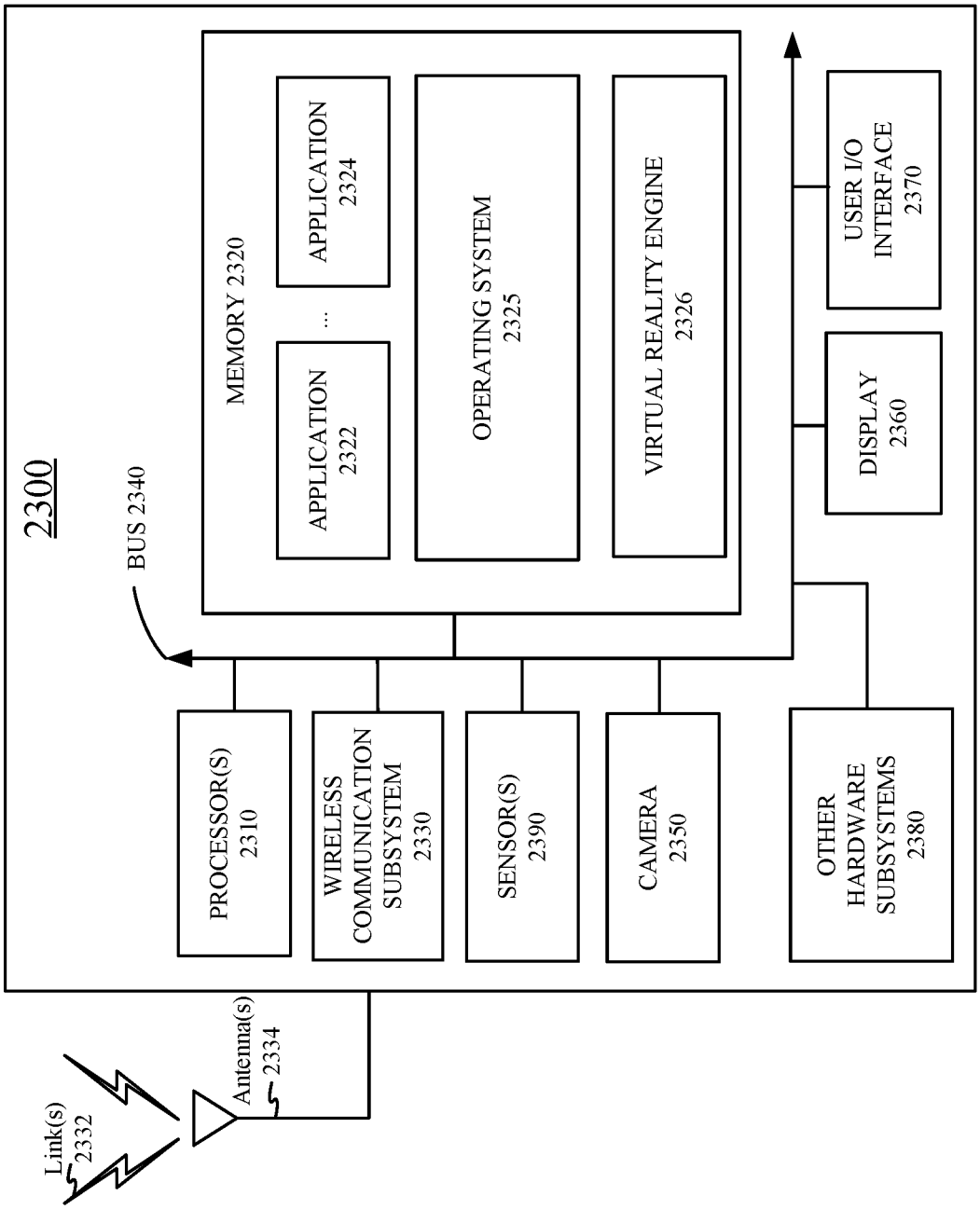
2300
BUS 2340
MEMORY 2320
APPLICATION 2322
...
APPLICATION 2324
OPERATING SYSTEM 2325
VIRTUAL REALITY ENGINE 2326
PROCESSOR(S) 2310
WIRELESS COMMUNICATION SUBSYSTEM 2330
SENSOR(S) 2390
CAMERA 2350
OTHER HARDWARE SUBSYSTEMS 2380
DISPLAY 2360
USER I/O INTERFACE 2370
Antenna(s) 2334
Link(s) 2332

FIG. 23

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2023/012358

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims;; it is covered by claims Nos.:

1-5, 8, 10-14

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2023/012358

A. CLASSIFICATION OF SUBJECT MATTER
INV. G09G3/20 G09G3/32 H01L25/16
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G09G H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2019/306945 A1 (VALENTINE GARETH JOHN [GB]) 3 October 2019 (2019-10-03)	1,12
Y	paragraph [0016] - paragraph [0053]; figures 1-6	2-5,8, 10,11, 13,14
Y	US 2020/251049 A1 (MORRIS DANIEL HENRY [US] ET AL) 6 August 2020 (2020-08-06) paragraph [0148] - paragraph [0172]; figures 1-13	2-5,8, 10,11, 13,14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 May 2023	03/07/2023

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Gartlan, Michael

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5, 8, 10-14

The display device of claim 1, wherein each micro-LED of the first array of micro-LEDs includes a mesa structure that includes:a reflector layer electrically coupled to the cathode of the micro-LED;an n-type semiconductor layer coupled to the reflector layer;an active region on the n-type semiconductor layer; andat least a portion of a p-type semiconductor layer on the active region, to solve the problem of increasing light extraction efficiency (par. 94).

---

2. claims: 6(completely); 15(partially)

The display device of claim 1, wherein the cathode of the micro-LED is bonded to the backplane wafer; and/orwherein the backplane wafer includes:a first voltage regulator configured to output a first positive supply voltage to the timing control circuit; anda second voltage regulator configured to output a second positive supply voltage to the first common anode of the first array of micro-LEDs; and optionallywherein:the first array of micro-LEDs is configured to emit light in a first wavelength range; the display device includes a second array of micro-LEDs that includes a second common anode and is configured to emit light in a second wavelength range; andthe backplane wafer further includes a third voltage regulator configured to output a third positive supply voltage to the second common anode of the second array of micro-LEDs, to solve the problem of facilitating alignment (par. 127)

---

3. claims: 7(completely); 15(partially)

The display device of claim 1, wherein the timing control circuit includes:a pulse-width modulation (PWM) latch configured to generate PWM signals for controlling the analog current drive circuit; anda comparator configured to compare the pixel data with a counter value and generate a control signal to control the PWM latch , to solve the problem of implementing a digital alternative of the timing control circuit (par. 132).

---

4. claim: 9

The display device of claim 1, wherein the backplane wafer includes a common control circuit shared by two or more micro-LED of the first array of micro-LEDs, to solve the problem of reducing area (par. 180).

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2023/012358

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2019306945 A1	03-10-2019	CN 110322829 A	11-10-2019
		US 2019306945 A1	03-10-2019
US 2020251049 A1	06-08-2020	CN 113383263 A	10-09-2021
		EP 3877803 A1	15-09-2021
		JP 2022519161 A	22-03-2022
		KR 20210124322 A	14-10-2021
		US 2020251049 A1	06-08-2020
		US 2020251638 A1	06-08-2020
		US 2022254974 A1	11-08-2022