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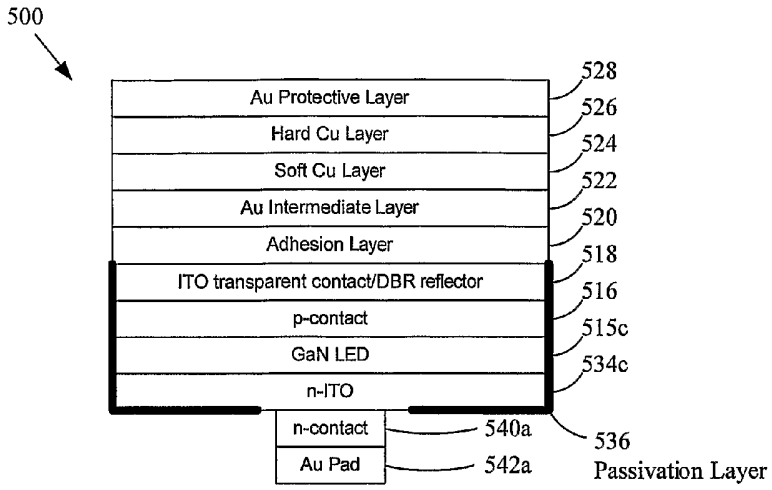

(57) Abstract: The invention provides a reliable way to fabricate a new vertical structure compound semiconductor device with improved light output and a laser lift-off processes for mass production of GaN-based compound semiconductor devices. A theme of the invention is employing direct metal support substrate deposition prior to the LLO by an electro-plating method to form an n-side top vertical structure. In addition, an ITO DBR layer is employed right next to a p-contact layer to enhance the light output by higher reflectivity. A perforated metal wafer carrier is also used for wafer bonding for easy handling and de-bonding. A new fabrication process is more reliable compared to the conventional LLO-based vertical device fabrication. Light output of the new vertical device having n-side up structure is increased 2 or 3 times higher than that of the lateral device fabricated with same GaN/InGaN epitaxial films.

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VERTICAL STRUCTURE SEMICONDUCTOR DEVICES

FIELD

[0001] The invention is related to fabricate GaN-based vertical structure semiconductor devices having a top and bottom contact structure and a method to fabricate the vertical structure devices.

BACKGROUND

[0002] Figure 1 depicts a conventional Gallium Nitride (GaN)-based semiconductor device 100 fabricated on an insulating sapphire substrate 114. This device can be for applications such as a Light Emitting Diode (LED), Laser Diode (LD), Hetero-junction Bipolar Transistor (HBT) and High Electron Mobility Transistor (HEMT). During the conventional process, the device is formed on a sapphire substrate and both electrical contacts are formed on the top side of the device. A p-contact 102 is formed on the top and mesa etching is employed to remove material to form an n-metal contact 116. The result is called a lateral structure device and tends to exhibit several problems including weak resistance to electrostatic discharge (ESD) and heat dissipation. Both of these problems limit the device yield and useful life time. In addition, the sapphire material is very hard, which creates difficulty in wafer grinding and polishing, and device separation. Device fabrication yield is dependent on post fabrication processes including lapping, polishing, and die separation.

[0003] Figure 2 depicts a second conventional technique that has become useful in building vertical structure GaN-based compound semiconductors 200. A laser lift-off (LLO) process is used to remove the sapphire substrate from the GaN epitaxial layer by applying an excimer laser having wavelength transparent to sapphire, typically in the UV range. The devices are then fabricated by substituting the insulating sapphire substrate with a conductive or semi-conductive second substrate 218 to build vertical structure devices. These processes typically employ wafer-bonding techniques for permanent bonding to the second substrate after removing sapphire substrate by laser lift-off.

[0004] However, there is still lacking a large scale laser lift-off process for the mass production of VLEDs (Vertical LED). One reason is the difficulty in large area laser lift-off due to non-uniformity of bonding adhesive layer 216 between support wafer 218 and the epitaxial layer 214 and the permanent second substrate 218 since the epitaxial layer surface is not flat over entire wafer surface after laser lift-off. Another problem associated with this wafer bonding technique is the degradation of metal contacts due to high temperature and high pressure during

eutectic metal-bonding process. Furthermore, substrates such as Si or GaAs used for the permanent wafer bonding are not optimal substrates in terms of heat dissipation compared to a Cu-based metal substrate. These problems reduce the final yield and do not provide a satisfactory solution to mass production of commercially viable devices.

[0005] Figure 3 depicts a structure 300 intended to overcome the wafer bonding problems and fabricate VLEDs. Instead of using a wafer bonding method, the fabrication of device 300 includes attaching a metal support 318 to the device. However, the yield is known to be low due to de-lamination of the bonding layer during the laser lift-off process. If the bonding is not secure against the high-energy laser shock wave, the GaN epitaxial layers may buckle or crack after laser lift-off, and then it is difficult to perform post laser lift-off processes, such as wafer cleaning, device fabrication, de-bonding and device separation. Consequently, final device process yield is low.

[0006] Another problem of a vertical devices based on the technique shown in Figure 3 is poor device performance. Since a sand blast is used on the sapphire substrate to improve uniform laser beam energy distribution, the GaN surface after laser lift-off is typically rough, which results in less light output than if it were a flat, smooth surface. In addition, the metal reflective layer formed on the n-GaN layer is not as high as non-metallic reflector material, such as ITO.

[0007] Due to these limitations of conventional techniques, a new technique is needed that can improve device performance and fabrication yield in high volume production of GaN-based semiconductor devices.

SUMMARY

[0008] The invention provides a reliable technique to fabricate a new vertical structure compound semiconductor devices with highly improved light output and the high yield laser lift-off (LLO) processes for mass production of GaN-based compound semiconductor devices. The main theme of this invention is employing direct metal support substrate deposition prior to the LLO by electro-plating method to form an n-side top vertical structure. In addition, ITO DBR layer was employed right next to p-contact layer to enhance the light output by higher reflectivity ITO layer. Perforated metal wafer carrier was also used for wafer bonding for easy handling and de-bonding. A new fabrication process is simple and more reliable process compare to the previous LLO-base vertical device fabrication. The light output of the new vertical device having

n-side-up structure was increased 2 or 3 times higher than that of the lateral device fabricated with same GaN/InGaN epitaxial films.

[0009] An exemplary embodiment of the invention is directed to a method of fabricating semiconductor devices. The invention includes the steps of forming a semiconductor layer over a substrate, forming a metal layer over the semiconductor layer, removing the substrate from the semiconductor layer, forming one or more contacts over the semiconductor layer where the substrate was removed, and separating the semiconductor layer into a plurality of individual semiconductor devices.

[0010] In one aspect, the invention includes the step of forming a buffer layer between the semiconductor layer and substrate. In one aspect, the removing step includes the step of applying a laser beam to a interface between the semiconductor layer and substrate, and inserting a diffusing media between the laser source and the substrate. In one aspect, the invention includes the step of attaching a wafer carrier to the metal layer. In one aspect, the separating step includes the step of forming a trench between each of the respective devices, passivating exposed portions of the devices, and transferring the individual semiconductor devices to a support film. In one aspect, the invention includes the step of assembling the individual semiconductor devices to a lead frame using a one-step die bonding and wire bonding technique.

[0011] Advantages of the invention include an improved technique for fabricating semiconductor devices with great yield and reliability.

DRAWINGS

[0012] The invention is described with reference to the following figures.

[0013] Figure1 depicts a lateral structure GaN-based LED with two metal contacts are formed on the topside of device, according to the prior art.

[0014] Figure 2 depicts a vertical structure GaN-based LED where a GaN thin membrane is bonded to a conductive or semi-conductive second substrate, according to the prior art.

[0015] Figure 3 depicts a vertical structure GaN-based LED where a thick metal layer is attached to a GaN thin membrane after removing original sapphire substrate, according to the prior art.

[0016] Figure 4 is a flowchart showing a method of fabricating a semiconductor device according to an embodiment of the invention.

[0017] Figure 5 depicts an epitaxial structure a vertical device where a GaN or AlN buffer layer is grown on top of the sapphire substrate, according to an embodiment of the

invention. Figure 5 also depicts an AlGaN buffer layer added as a thermal barrier, according to an embodiment of the invention.

[0018] Figure 6 depicts a p-contact metal and ITO transparent contact/DBR layer deposition on top of p-GaN epitaxial layer to form p-type contact and reflector layer, according to an embodiment of the invention.

[0019] Figure 7 depicts an adhesion layer deposition to enhance adhesion between the ITO and gold intermediate layer, according to an embodiment of the invention.

[0020] Figure 8 depicts a soft copper layer deposition using an electroplating or electro-less plating method for stress relief between the GaN LED layer and a subsequently deposited hard copper layer, according to an embodiment of the invention.

[0021] Figure 9 depicts a hard copper layer deposition using an electroplating or electro-less plating method to provide the mechanical stiffness and higher electrical and thermal conductivity, according to an embodiment of the invention.

[0022] Figure 10 depicts a copper electroplated or electro-less plated GaN LED wafer attaching to a perforated support wafer carrier using conductive adhesive glue prior to the laser lift-off, according to an embodiment of the invention.

[0023] Figure 11 depicts an eximer laser beam applied through the sapphire substrate using a diffusing media to obtain uniform laser beam energy distribution during laser lift-off process, according to an embodiment of the invention.

[0024] Figure 12 depicts the sapphire substrate removal and Ga drop cleaning after laser lift-off, according to an embodiment of the invention.

[0025] Figure 13 depicts GaN/AlGaN buffer layer removal by dry etching and GaN surface smoothing etching prior to n-contact formation, according to an embodiment of the invention.

[0026] Figure 14 depicts an n-type ITO transparent contact formation on top of the GaN LED layer, according to an embodiment of the invention.

[0027] Figure 15 depicts an n-contact formation and gold pad metallization on the n-ITO layer, according to an embodiment of the invention.

[0028] Figure 16 depicts device isolation by dry etching or mechanical methods such as mechanical scribing or laser scribing, according to an embodiment of the invention.

[0029] Figure 17 depicts a protective SiO_2 passivation layer deposition, according to an embodiment of the invention.

[0030] Figure 18 depicts support wafer carrier removal and final device structure, according to an embodiment of the invention.

[0031] Figure 19 depicts device separation by dicing or laser scribing, according to an embodiment of the invention.

[0032] Figure 20 depicts die bonding and wire bonding of vertical device on the lead frame, according to an embodiment of the invention.

DETAILED DESCRIPTION

[0033] The invention is described with reference to specific device structure and embodiments. Those skilled in the art will recognize that the description is for illustration and to provide the best mode of practicing the invention. The invention includes a number of forming and depositing steps to fabricate a semiconductor device according to the invention. The disclosure refers to depositing materials over or on other materials, which is described and depicted as representing an arbitrary frame of reference and is intended to describe and cover techniques that deposit materials over-top, on, or below other materials as explained and understood by those of skill in the art and in conjunction with the description. For example, portions of the disclosure describes semiconductors layers constructed from above and other portions describes semiconductor layers constructed from below, while in both cases, a new layer deposited over an existing layer means that it is deposited above or below the existing layer as described and illustrated. Numerous process parameters are provided herein to provide the best mode, while variations of the parameters may also result in the process, structure, and advantages as described herein. Variations of the invention are anticipated and encompassed by the claims.

[0034] A. Device Structure and Fabrication

[0035] Figure 4 is a flowchart 400 showing a method of fabricating a semiconductor device according to an embodiment of the invention. The steps depicted in the flowchart are for the purpose of demonstrating the exemplary embodiments and structures and the invention includes portions of modifications of the method and resulting structures as set forth herein. Step 402 begins the exemplary process with an epitaxial wafer as depicted in Figure 5. Reference number 500 is intended to refer to the semiconductor that may result in one or more devices. In the event of many devices, the references are provided with alphabetic suffixes such as 500a,

500b, 500c and so on. The steps are described with reference to the semiconductor structure fabrication and packaging depicted in Figures 5-20.

[0036] Figures 5-18 illustrate steps to fabricate vertical structure GaN-based LEDs, according to embodiments of the invention, using a deposition processes to form a metal substrate for mechanical support and electrical conductivity, and a laser lift-off process to remove the original substrate. The fabrication method described in this invention is not limited to LEDs but can extend to any device structures and particularly those containing GaN-based epitaxial thin films grown on an insulating substrate, such as laser diodes (LD), Hetero-junction Bipolar Transistor (HBT), High Electron Mobility Transistor (HEMT).

[0037] Figure 5 depicts an epitaxial structure a vertical device 500 formed on a substrate 502, for example, a sapphire substrate. A GaN or AlN buffer layer 504 is grown on top of the substrate. In one aspect of the invention, an AlGaN buffer layer 506 is formed over buffer layer 504 to act as a thermal barrier. The combination buffer layer is depicted as reference number 505 and may include one or both layers 504 and 506 as described below.

[0038] Next, a GaN-based LED structure 515 represented by numbers 508-514 is grown on the sapphire substrate 502 with an appropriate epitaxial growth apparatus, such as metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), vapor phase epitaxy (VPE), or other technique. A n-GaN layer 508 is formed, and then a multi-quantum well (MQW) layer 510 is formed over the n-GaN layer 508. An optional p-AlGaN layer 512 is depicted, and a P-GaN layer is depicted.

[0039] Contrary to conventional techniques where a single layer of GaN or AlN is a common buffer layer, the invention preferably employs both AlGaN buffer layer 506 in addition to the GaN or AlN buffer layer 504, but does not require both layers. The AlGaN 506 layer is useful in terms of a thermal barrier. Experiments have shown that the temperature at the interface between GaN LED layer 515 and adhesive bonding layer may increase up to 250 °C during the laser lift-off process. Therefore, a polymer-base adhesive layer may become deteriorated and may react with the GaN LED layer during laser lift-off due to heat build up, which makes it difficult to remove the thermally deteriorated adhesives during the de-bonding process. In the invention, employing AlGaN helps to reduce the bonding adhesive deterioration, hence to improve device fabrication yield. In addition, the total epitaxial layer thickness is set to certain thickness to minimize temperature increase at the GaN/adhesive interface. Beneficially, the epitaxial layer thickness is chosen to be more than 5 μm in order to maintain interfacial

temperature less than 200 °C. To achieve this, the n-GaN layer is grown more than 4 μm thick on top of GaN or AlN buffer layers.

[0040] Figure 6 depicts a p-contact metal 516 and ITO transparent contact/DBR layer 518 deposition on top of the GaN LED layer 515 to form p-type contact, deposited using thin film deposition methods, such as, electron beam evaporation or sputtering. Exemplary p-contact metals may include Ni/Au, Pd/Ni/Au, Ni/Pd/Au or Pd/Ir/Au. The thin film metal layer thicknesses can be, for example, 10 nm Ni and 20 nm for Ni/Au, 10 nm Pd and 20 nm Ni, 30 nm Au for Pd/Ni/Au, and 20 nm Ni, 10 nm Pd and 20 nm Ir, 30 nm Au for Pd/Ir/Au, and 20 nm Ni and 20 nm Pd, 100 nm Au for Ni//Pd/Au, respectively. Generally, p-contact metals are annealed in a furnace between 300 °C to 500 °C for 2 min in an oxygen ambient for Ni containing contacts, while non-nickel containing metal contacts are annealed in the nitrogen ambient.

[0041] The thin film Indium Tin Oxide (ITO) layer 518 is deposited using electron beam evaporation or sputtering to form a Distributed Bragg Reflector (DBR). Obtaining a good optical reflectivity is important to increase the light extraction in the vertical structure device. In general, oxide-base DBRs are used for the devices demanding photon recovery, such as surface emitting lasers. However, these oxide-base DBR materials are insulator. Therefore, it is useful to employ conductive DBR material for this particular vertical device having conductive metal substrate. ITO is considered the best choice of material for the reflective DBR material in the vertical device with metal substrate, but other choices are anticipated. The reflectivity of ITO is more than 90%, while the best reflectivity of metal thin film is about 50~60 %. In one aspect, the ITO thin film thickness is selected to be in the range of 75~150 nm to obtain the optimal reflectivity. The transmittances at 460 nm are over 85 % at an annealing temperature in between 300 °C to 500 °C.

[0042] Figure 7 depicts an adhesion layer 520 deposition to enhance adhesion between the ITO layer 518 and gold intermediate layer 522, according to an embodiment of the invention. To fabricate a vertical structure device having a thin, hard GaN epitaxial layer (less than 5 μm) with thick and soft metal film support (~50 μm), it is useful to form an intermediate layer between those two layers to reduce compressive stress build up at the interface between the GaN epitaxial layer and metal layers. Another reason to provide the intermediate layer is that the metallic intermediate layer makes better electroplating characteristics than depositing thick electroplated layers directly on the non-metallic ITO surface. Approximately 1-μm thick gold (Au) thin film was deposited consecutively on the ITO surface using electron beam evaporator without removing wafers from the vacuum chamber. In situ consecutive layer deposition is

useful to prevent the oxidation or contaminations, which is important to make a good thin film adhesion between the ITO and Au layers. In order to improve the adhesion between ITO and Au further, 30~50 nm-thick Cr or Ti adhesion layer is deposited in between ITO and Au layers.

[0043] In Figure 8 and 9, thick metal support layers 524, 526 are deposited by electroplating or electro-less plating. Electroplating or electro-less plating is used because it is typically fast and inexpensive for forming more than 30μm-thick metal layers, as compared to the other deposition methods. This is particularly useful for mass production of vertical devices in terms of cost effectiveness. Key functions of the metal support layer are that the support layer not only provides a good rigid mechanical support for the thin GaN epitaxial layer 515, but also provides good electrical conductivity and heat dissipation. In order to meet these requirements, graded Cu alloy layers are preferably deposited on an Au/Cr or Au/Ti adhesion layer.

[0044] A first Cu strike layer is deposited prior to the Cu alloy layer 524 in order to make a good adhesion between the thin vacuum evaporated Au layer 522 and the Cu alloy layer 524. In one aspect, initially, sulfate-base soft copper layer is plated in order to gradually soften stress build up due to thick metal layer. The initial soft Cu alloy layer thickness is set up to be about 10 μm. The plating rate is set up to 3~5 μm/hour to form a dense and uniform Cu plating layer. Another reason to choose a slow plating rate is to prevent wafer bowing after de-bonding the wafer from the support wafer carrier, described below. Due to the compressive stress build up at the interface between the GaN epitaxial layer 515 and the copper layer 524-526, the wafer may tend to bow after de-bonding. In addition to the slow rate plating, organic-based additives can be added in the electroplating solution and a sulphonate-base plating solution is used. Furthermore, the electroplating is performed at low temperature (5 °C) to minimize stress build up.

[0045] Next to the soft Cu layer 524, a hard Cu layer 526 is plated using cyanide or acid-base bath in order to provide structural stiffness. The plating rate of hard Cu plating is about 15 μm/hour. For the Cu alloy plating, the metal alloy plating solutions containing tin (Sn) and iron (Fe) were mixed with the Cu sulfate solution to improve the mechanical strength and the electrical conductivity of the Cu support layer. The total thickness of the Cu alloy support layer 522 was about 50~60 μm. At the end of the Cu alloy plating, 0.3 μm-thick Au layer was electroplated to protect Cu alloy layers from oxidation. This Au protective layer is useful to make a good adhesion between individual die and metal-base epoxy during die bonding and wire bonding process for the packaging of the vertical devices.

[0046] After the thick Cu metal support layer 526 was formed by electroplating, the sapphire surface is mechanically polished to make the sapphire surface uniform roughness. The

sapphire surface smoothness is important for to control the laser beam energy density distribution and the final surface morphology of the laser lifted GaN surface. The laser beam energy density is strongly dependent on the surface roughness of the sapphire surface. Low laser beam energy is required if the rough sapphire surface is used for LLO process. However, if the surface is rough, the laser lifted GaN surface appears rough since the sapphire surface morphology replicates to the GaN surface after laser lift-off. On the other hand, if the polished surface is used, higher laser beam energy is required. The surface morphology of laser lifted GaN surface is very similar to that of polished sapphire surface. However, higher laser beam usually results in crack generation due to excessive laser beam energy. To obtain the optimal laser lift-off result and the GaN surface morphology, the surface roughness of the sapphire surface is chosen approximately 10~20 angstrom in RMS value.

[0047] As shown in Figure 10, Sapphire/GaN/Cu/Au wafers are bonded to a perforated wafer carrier 532 using a conductive thermo-plastic epoxy 530. The perforated wafer carrier is made out of stainless steel with holes. The reason to use the metal wafer carrier is to provide the electrical and heat conduction during the inductively coupled plasma (ICP) etching, wafer probing and die isolation. By using a metal wafer carrier, there is less need to remove wafer from the carrier for post fabrication processing. In addition, the perforated wafer carrier provides bubble-free wafer bonding since air bubbles can escape easily through the holes during the bonding process. It also provides easy de-bonding between the Sapphire/GaN/Cu/Au wafer and the wafer carrier since a solvent can penetrate through the holes during de-bonding process. By using the perforated wafer carrier, the entire process is easy, reliable and simple which leads to high fabrication yield for the fabrication of the vertical devices. The exemplary thickness of wafer carrier is 1/16 inches and the diameter is 2.5 inches. The exemplary total number of holes is 21 and the through hole diameter is 20/1000 inches. The exemplary wafer carrier surface is electro-polished to make mirror like flat surface for the uniform bonding with the adhesive.

[0048] Silver-based conductive adhesives are used to bond the Sapphire/GaN/Cu/Au and the perforated wafer carrier. The conductive adhesive is used to provide the good electrical and thermal conduction for the wafer probing and die isolation etching process. The thermo-plastic epoxy has good adhesion strength and good heat resistance. Another advantage of the thermo-plastic epoxy is that it can be dissolved in the solvent, such as acetone, very easily, which is useful for the de-bonding process.

[0049] In the invention, a sheet-type thermo-plastic epoxy is employed because the film thickness of the sheet type epoxy is more uniform than that of liquid-base adhesives. The liquid-

base adhesives often result in uneven thickness uniformity and bubble formation in the previous bonding process experiences since the spin coating of the liquid-base adhesives generally leads to thicker film formation in the wafer fringe side than that of center area of the wafer. This is a common phenomena for the liquid-base adhesives to obtain thick adhesive layers by multiple spinning. For the bonding of thermo-plastic epoxy, 127 μm-thick sheet-type thermo-plastic epoxy is sandwiched in between thick metal support and perforated wafer carrier. The pressure is set to about 10~15 psi and the temperature is maintained below 200 °C in the hot iso-static press. At these conditions, the bonding time is less than 1 minute. This short bonding time has a definite advantage over to that of liquid-base adhesives, which may require more than 6 hour curing time for the complete curing of the adhesive. The short bonding process time also greatly enhance the productivity of the vertical device fabrication.

[0050] Referring to Figure 11, a 248 nm KrF ultra violet (UV) excimer laser (pulse duration of 38 ns) is used for laser lift-off. The reason for choosing this wavelength is that the laser should beneficially transmit through the sapphire but be absorbed in the GaN epitaxial layer in order to decompose the GaN into metallic Ga and gaseous nitrogen (N_2) at the GaN/sapphire interface. The laser beam size is chosen as a 7 mm x 7 mm square beam and has beam power density between 600~1,200 mJ/cm^2. It is also suggested that the laser beam energy density is dependent on the surface roughness of the sapphire substrate surface. In order to obtain smooth GaN surface after laser lift-off, the beam energy higher than 800 mJ/cm^2 was used for the mechanically polished sapphire substrate 10~20 angstrom in RMS value.

[0051] Surface roughness of the sapphire substrate is an important process parameter for obtaining a smooth GaN surface after laser lift-off. If un-polished sapphire surface is used during laser lift-off, the GaN surface is rough, which results in poor light output of the LED device due to poor reflectivity of the rough surface after forming a final device. However, if a polished surface is used, a smooth GaN surface can be obtained, hence higher light output can be obtained. However, since the laser beam is localized on the polished sapphire surface, the area irradiated with the higher laser beam power may result in cracking on the GaN surface compared to the area with less laser beam energy. Therefore, it is important to choose an optimal surface roughness of sapphire wafer in order to obtain a high yield laser lift-off process and a high device performance at the same time. According to conventional techniques, sand blasting is commonly used to obtain uniform laser beam distribution on the polished sapphire surface, however, sand blasting is unreliable and unrepeatable to obtain the identical surface roughness consistently. In the invention, a diffusing media 552 constructed from materials transparent to the 248 nm UV

laser is placed in between laser beam and sapphire substrate to obtain uniform laser beam energy distribution on the sapphire surface, hence to enhance the laser lift-off process yield. The rms (root mean square) surface roughness of the diffusing media is set up less than 30 μm and sapphire was used for the diffuser.

[0052] Referring to Figure 12, after laser lift-off, excess Ga drops 503 result from GaN decomposition during laser lift-off, and is cleaned with an HCl solution (HCl: H_2O = 1:1, at room temperature) or boiled using HCl vapor for 30 seconds. Since the Ga melts at room temperature, Ga is formed in a liquid state during the laser lift-off; hence it can be easily cleaned with chlorine-base acidic solutions.

[0053] Referring to Figure 13, in order to expose n-type GaN epitaxial layer, the buffer layer 505 (e.g. GaN or AlN and AlGaN buffer layers) are removed by dry etching; beneficially using inductively coupled reactive ion etching (ICP RIE). To make an atomically flat surface, ICP polishing is also performed on the n-GaN surface. The flat surface is important in producing high reflectivity from a reflective structure that is deposited subsequently since the light out-put can be increase with higher reflective surface.

[0054] Referring to Figure 14, in order to improve the current spreading of the vertical device, an n-type ITO transparent contact 534 is formed on the n-GaN LED surface 515. ITO composition is 10 wt% SnO_2 / 90 wt% In_2O_3, and a layer of about 75~200 nm-thick ITO film is deposited using an electron beam evaporator or sputtering system at room temperature. Annealing is carried out after the ITO film deposition in a tube furnace with N_2 ambient for 5 minutes. The annealing temperatures are varied in between 300 °C to 500 °C. The minimum resistivity of the ITO film is about low10^{-4} Ωcm at 350 °C of annealing temperature in N_2 ambient. The transmittances at 460 nm are over 85 % at the annealing temperature of above 350 °C.

[0055] Referring to Figure 15, after the ITO transparent contact formation, an n-contact 540 is formed on the n-ITO surface, comprising of Ti and Al.. Since multiple contacts are formed, they are referenced as 540a, 540b, 540c and so forth. The thickness of the n-contact metal is 5 nm for Ti, and 200 nm for Al, respectively. In order to make a good adhesion between the n-contact metal layer and a pad metal 542, 20 nm of Cr is deposited on top of the Al as an adhesion layer. For the pad metal deposition, 500 nm gold is deposited on top of the Cr consecutively in an electron beam evaporation chamber without breaking vacuum. In order to form an ohmic contact, the n-contact metal is annealed in the furnace at 250 □ for 10 minute in an N_2 ambient atmosphere.

[0056] Referring to Figure 16, after cleaningthe GaN surface, individual devices are isolated by a MICP (magnetized inductively coupled plasma) dry etching technique. The MICP can accelerate the etch rate compared with the other dry etching methods. This is useful to prevent the photo-resist mask burning during the etch process. The MICP usually provides about twice the etch rate compared to conventional ICP. Fast etch rate is recommended for the processing of the vertical devices having metal support since the metal substrate can be attacked by chemicals designed for removing metal or oxide masks. Therefore, in order to use the photo-resist mask for the die isolation etching, fast etching technique is suggested. The isolation trench dimension is 30 □ wide and 3.5 □ deep the etch depth is dependent upon epitaxial wafer thickness. Suggested MICP dry etch conditions for device isolation are as follows:

[0057] 1. Total flow rate:100 sccm

[0058] 2. Intensity of magnet field:15 gauss

[0059] 3. Substrate temperature: 70 □

[0060] 4. Gas mixture: 40%BCl_3/40%Cl_2/20%Ar

[0061] 5. Power/bias voltage: 600W/-300V

[0062] 6. Operational pressure: 30mTorr

[0063] 7. Etch depth rate: 0.4 □/min

[0064] 8. Etch mask: Photo-resist (AZ 9262) (thickness: 24 □)

[0065] The die isolation is also carried out either by mechanical dicing or laser scribing. The dicing trench for device isolation is 50 μm wide in the case of laser scribing and 40 μm in the case of mechanical dicing. The trench depth is approximately 10 μm-deep in both cases.

[0066] Referring to Figure 17, a passivation layer 536 is deposited on exposed portions of the devices. In order to protect device from the external hazardous environment and to increase the light output by modulating reflective index between the passivation layer and the GaN, the vertical device is passivated with a SiO_2 thin film 536. The film is deposited with PECVD (Plasma Assisted Chemical Vapor Deposition) at less than 250 □. The film thickness is maintained at 80 nm for the optimal reflective index.

[0067] Referring to Figure 18, after the passivation deposition, the perforated support wafer carrier is removed from the GaN/metal support wafer using solvent. The de-bonding process includes soaking of the GaN/metal wafer in acetone for 0.5~1 hour to dissolve the conductive adhesive layer from the perforated support wafer carrier. The separated GaN/metal wafers are further soaked and cleaned with isopropanol in an ultrasonic cleaner. The GaN device surface is further cleaned with DI water using rinse and dryer.

[0068] Referring to Figure 19, in order to separate individual device from the wafer, the devices are diced out by laser scribing using an Nd;YAG laser. The wafer having vertical devices with a metal substrate is placed on porous vacuum chuck. The Nd;YAG laser is focused on the 30 μm-wide trenches formed with MICP. After laser scribing is completed, the separated chips are transferred to tacky wafer grip tape. Prior to the pick and place process, the separated chips are flipped from the first wafer grip to another wafer grip 560, so that the GaN surface is located on top of the device.

[0069] Figure 20 depicts a wire bonding process with a final device 500, where reference number 570 is a lead frame, 572 is a gold bump, 574 is a gold ball, 576 is gold wire and 578 is a wire bonding device. Contrary to the conventional lateral device, the metal supported vertical device 500 is handled using a special die bonding technique. In the invention, the one-step die bonding and wire bonding technique is employed as shown in Figure 20. Instead of separating the die bonding and wire bonding processes, the separated single chip is placed on the lead frame having with gold bump on the lead frame surface. By heating and pressurizing action, the gold bump can connect together with the gold surface of the vertical device and the silver coated lead frame at once. Therefore, there is no need to perform the separate die bonding and wire bonding processes. This one-step process helps to reduce process time and provides an easy and simple packaging processes, hence reduce the fabrication cost and time. While this exemplary packaging technique is depicted, other packaging technique can be used in the invention.

[0070] B. Exemplary Points of Interest and Advantages

[0071] The points and advantages herein are intended as examples and not to limit the points or advantages of the invention.

[0072] 1. Exemplary Device Points

[0073] a. Higher light output due to better current spreading through n-GaN layer, which has higher carrier concentration than that of p-GaN. The electron concentration (carrier concentration) of the n-GaN is known to be in the range of $10^{19}/cm^3$, which is two orders of magnitude higher than that of hole concentration in p-GaN ($\sim 10^{17}/cm^3$). Therefore, more photons can be generated through the n-GaN layer upon current injection to the p-n junction. The light output of the new vertical device having n-side up structure was increased 2 or 3 times higher than that of the lateral device having p-side up structure produced with same GaN/InGaN epitaxial layers.

[0074] b. Higher heat dissipation due to metal substrate. The metal substrate of the vertical structure device gives superior electrical and heat conduction, which is useful in terms of device efficiency and reliability, i.e. device life-time.

[0075] c. Higher number of devices can be obtained since the device dimensions are shrinking because of only one metal contact pad is required with vertical device compare to the lateral structure. Vertical structure requires only one contact on top side, while the lateral device having insulating substrate requires two contacts. As a result, about 1.5 to 2 times more devices can be obtained from the vertical device than those from lateral device.

[0076] d. Higher power efficiency can be obtained from the vertical device. There is no current crowding in the vertical device; hence the light output is linear with current injection. On the other hand, the maximum light output of a lateral device is saturated earlier due to current crowding effects. This is important for the high power devices, such as white LED for solid state lighting.

[0077] e. Vertical devices can withstand a high electrostatic discharge (ESD) environment compared to lateral devices; in general the ESD resistance of a vertical device with metal substrate is higher than 10,000 V, while that of lateral device is around 100 V. This is important for devices used in automobile applications since the devices are often exposed to a high voltage environment.

[0078] 2. Exemplary Process Points

[0079] a. Due to the higher adhesion strength of the metal substrate directly attached to the GaN epitaxial layer by metal deposition, such as electro-plating, the de-bonding between the support substrate and the GaN epitaxial layer can be significantly suppressed during high energy shock wave irradiation by laser beam. As a result, crack initiation can be maintained in a minimal extent during the laser lift-off process. The result is higher laser lift-off (LLO) yield rate compared with the previous polymer-base bonding processes, such as epoxy or glue bonding, which result in higher probability of crack initiation and generation during LLO due to poor adhesion strength between the support and the GaN epitaxial layer.

[0080] b. As a result, the new invention ensures more robust and reliable LLO process compared with the previous wafer bonding or glue bonding-based LLO processes. By achieving the full wafer scale laser-lift-off processes, the invention provides the realistic production-ready technology for mass production of vertical structure devices.

[0081] c. Simple and easier device fabrication and LLO process; reduced number of mask for front fabrication process is required.

[0082] 3. Exemplary Advantages

[0083] a. Instead of metal bonding, a metal support substrate is deposited by electroplating or electro-less plating.

[0084] b. Instead of post LLO metal support layer deposition, a metal support layer is preformed prior to the LLO process.

[0085] c. No trenches are formed on the GaN epitaxial layer, which results in no crack generation during LLO process and reduce the number of fabrication steps.

[0086] d. n-contact is situated on top of the device for higher light output.

[0087] e. No transparent p-contact layer is employed; instead ITO transparent n-contact is formed on n-GaN for better current spreading.

[0088] f. ITO DBR layer is employed next to a p-contact layer to enhance the light output by higher reflectivity ITO layer.

[0089] g. Perforated metal wafer carrier is used for wafer bonding for easy handling and de-bonding.

[0090] h. A new fabrication process is straight-forward and more reliable compares to conventional LLO-base vertical device fabrication.

[0091] C. Conclusion

[0092] Advantages and exemplary embodiments of the invention have been disclosed and described herein. Accordingly, having disclosed exemplary embodiments and the best mode, modifications and variations may be made to the disclosed embodiments while remaining within the subject and spirit of the invention as defined by the following claims.

CLAIMS

1. A method of fabricating semiconductor devices, comprising the steps of:

forming a plurality of semiconductor layers over a substrate;

forming a plurality of metal layers over the semiconductor layers;

removing the substrate from the semiconductor layers;

forming one or more electrical contacts over the semiconductor layers where the substrate was removed; and

separating the semiconductor layers into a plurality of individual semiconductor devices.

2. The method of claim 1, further comprising the step of:

forming a buffer layer between the semiconductor layer and substrate.

3. The method of claim 1, wherein:

the removing step includes the step of applying a laser beam to an interface between the semiconductor layer and substrate, and inserting a diffusing media between the laser source and the substrate for uniform laser beam energy distribution.

4. The method of claim 1, further comprising the step of:

attaching a wafer carrier to the metal layer.

5. The method of claim 2, further comprising the step of:

attaching a wafer carrier to the metal layer.

6. The method of claim 3, further comprising the step of:

attaching a wafer carrier to the metal layer.

7. The method of claim 2, wherein:

the separating step includes the step of forming a trench between each of the respective devices, passivating exposed portions of the devices, and transferring the individual semiconductor devices to a support film.

8. The method of claim 2, further comprising the step of:

assembling the individual semiconductor devices to a lead frame using a one-step die bonding and wire bonding technique.

9. The method of claim 7, further comprising the step of:

assembling the individual semiconductor devices to a lead frame using a one-step die bonding and wire bonding technique.

10. A semiconductor device manufactured according to the method of claim 1.

11. A method of fabricating a light emitting semiconductor device, comprising the steps of:

forming a diode structure over a substrate;

forming a plurality of metal layers over the diode structure;

removing the substrate from the diode structure;

forming one or more contacts over the diode structure where the substrate was removed; and

separating the diode structure into a plurality of individual diodes.

12. The method of claim 11, wherein the step of forming the diode structure comprises the steps of:

depositing a first buffer layer including one of GaN and AlN over the substrate; and

depositing a n-GaN layer over the buffer layer.

13. The method of claim 11, wherein the step of forming the diode structure comprises the steps of:

depositing a first buffer layer including one of GaN and AlN over the substrate;

depositing a second buffer layer including AlGaN over the substrate; and

depositing a n-GaN layer over the buffer layer.

14. The method of claim 12, wherein:

the removing step includes the step of applying a laser beam to an interface between the semiconductor layer and substrate, inserting a diffusing media between the laser source and the substrate, and liquefying at least a portion of the buffer layer.

15. The method of claim 11, wherein:

the separating step includes the step of forming a trench between each of the respective devices, passivating exposed portions of the devices, and transferring the individual semiconductor devices to a support film.

16. The method of claim 11, further comprising the step of:

attaching a wafer carrier to the metal layer.

17. The method of claim 14, further comprising the step of:

attaching a wafer carrier to the metal layer.

18. A semiconductor device manufactured according to the method of claim 11.

19. A semiconductor structure, comprising:

a first buffer layer includes at least one of GaN and AlN;

a second buffer layer including AlGaN;

a layer including n-GaN;

a layer including AllnGaN; and

a layer including p-GaN.

20. The semiconductor structure of claim 19, further comprising:

a substrate.

21. The semiconductor structure of claim 19, further comprising:

a layer including p-AlGaN.

22. The semiconductor structure of claim 19, further comprising:

a metal layer including Cu; and

a metal layer including Au.

23. The semiconductor structure of claim 23, further comprising:

a wafer carrier coupled to the semiconductor structure.

24. The semiconductor structure of claim 22, further comprising:
a wafer carrier coupled to the semiconductor structure.

25. The semiconductor structure of claim 22, further comprising:
a layer including n-ITO.

26. The semiconductor structure of claim 25, further comprising:
a plurality of contacts.

27. The semiconductor structure of claim 26, further comprising:
a plurality of trenches disposed between individual semiconductor devices.

28. The semiconductor structure of claim 27, further comprising:
a passivation layer over exposed portions of the devices.

FIGURE 1
(prior art)

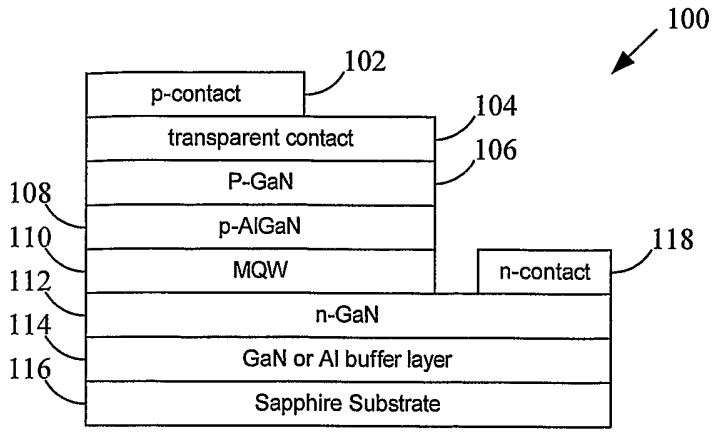


FIGURE 2
(prior art)

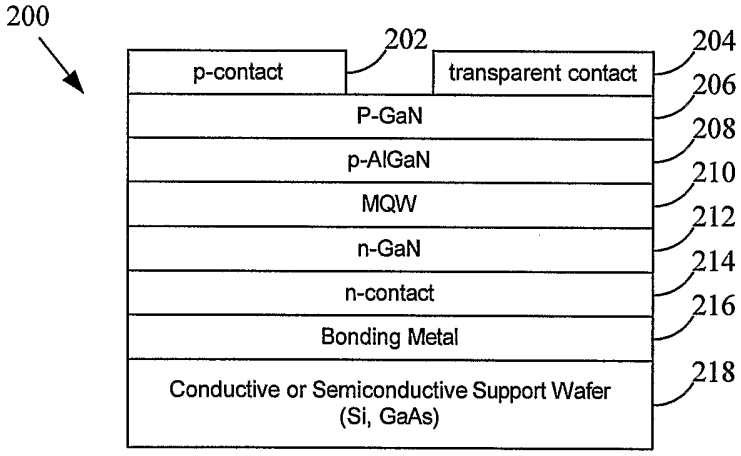
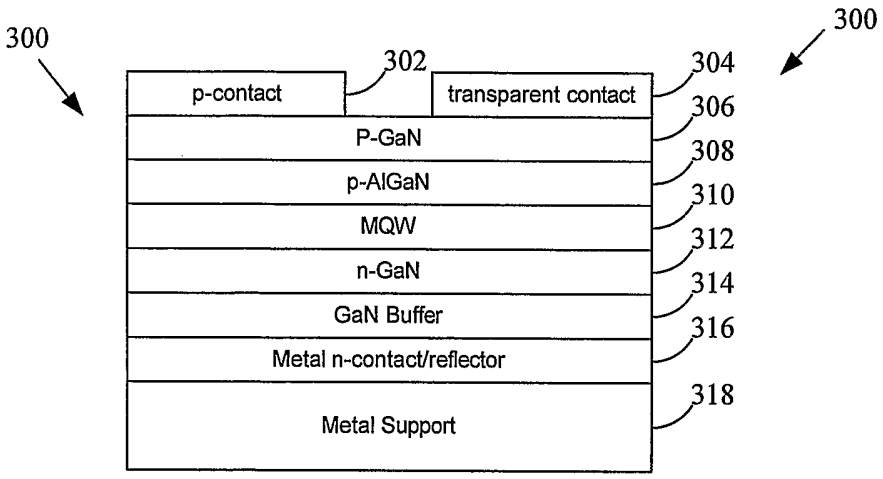


FIGURE 3
(prior art)



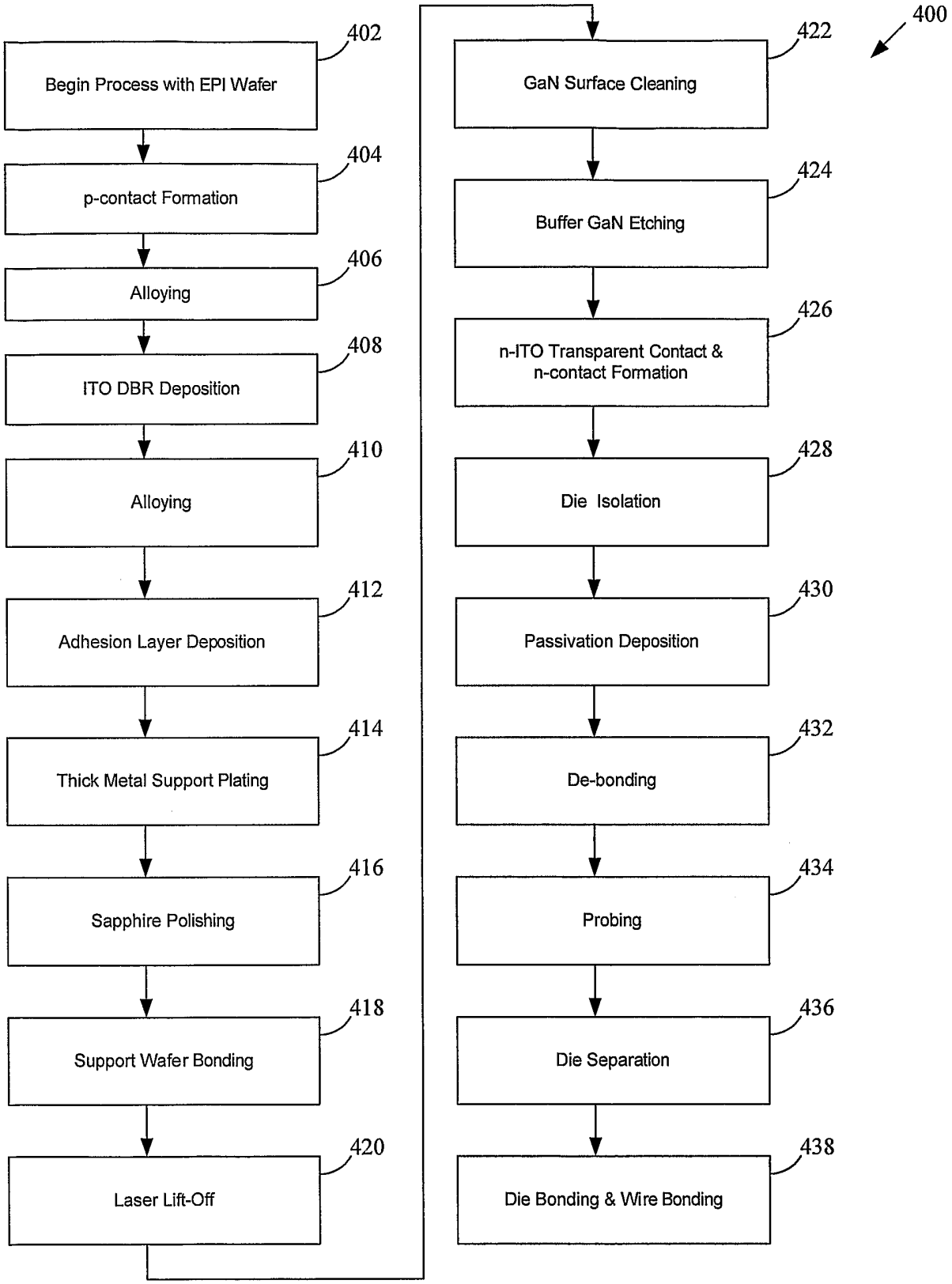

400
402
Begin Process with EPI Wafer
404
p-contact Formation
406
Alloying
408
ITO DBR Deposition
410
Alloying
412
Adhesion Layer Deposition
414
Thick Metal Support Plating
416
Sapphire Polishing
418
Support Wafer Bonding
420
Laser Lift-Off
422
GaN Surface Cleaning
424
Buffer GaN Etching
426
n-ITO Transparent Contact &
n-contact Formation
428
Die Isolation
430
Passivation Deposition
432
De-bonding
434
Probing
436
Die Separation
438
Die Bonding & Wire Bonding

FIGURE 4

FIGURE 5

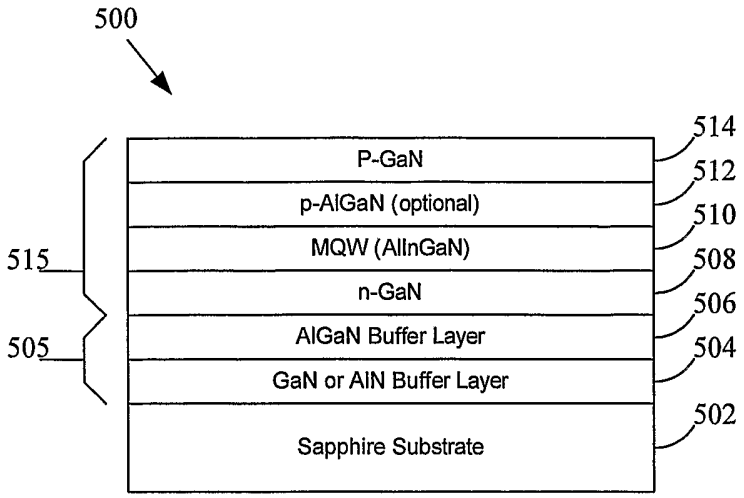


FIGURE 6

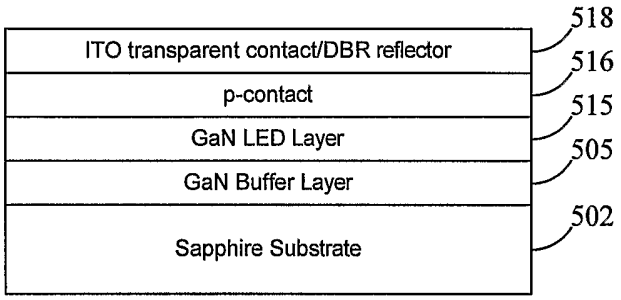


FIGURE 7

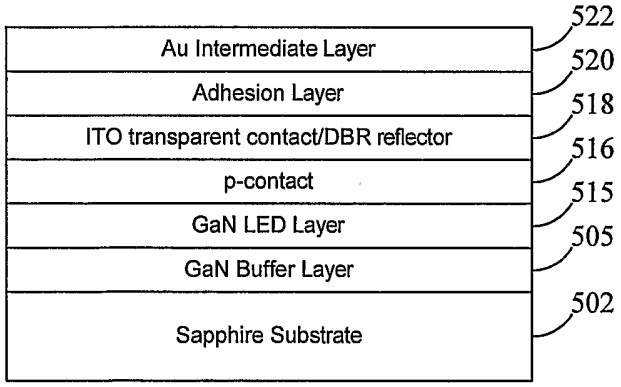


FIGURE 8

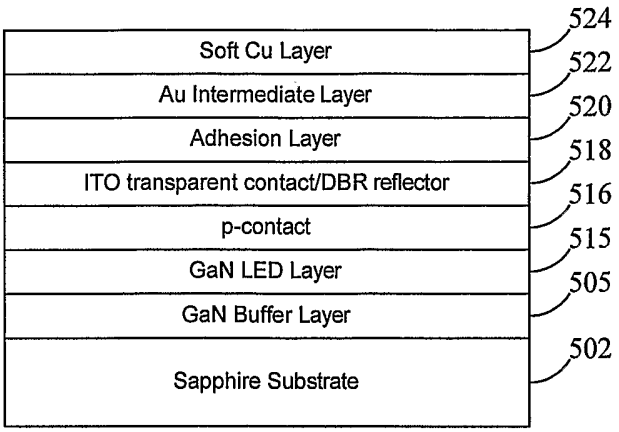


FIGURE 9

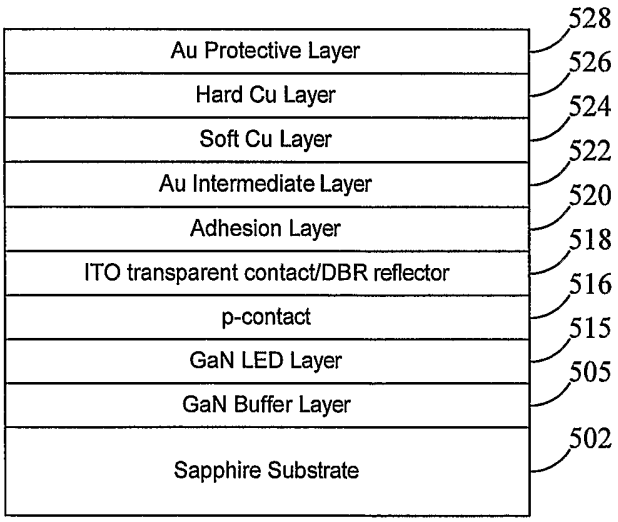


FIGURE 10

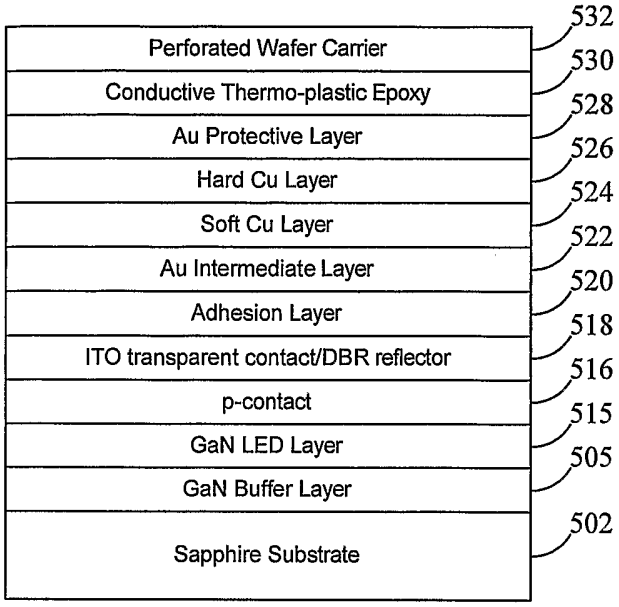


FIGURE 11

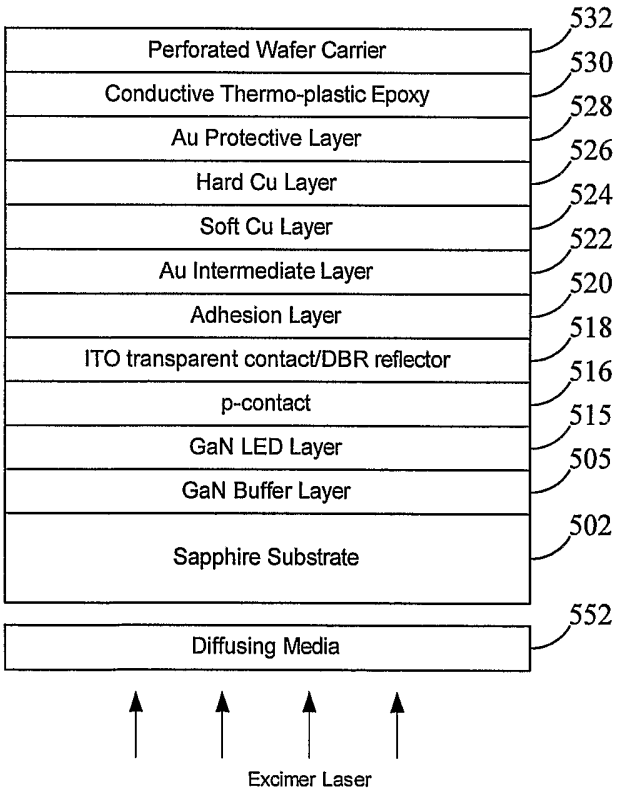


FIGURE 12

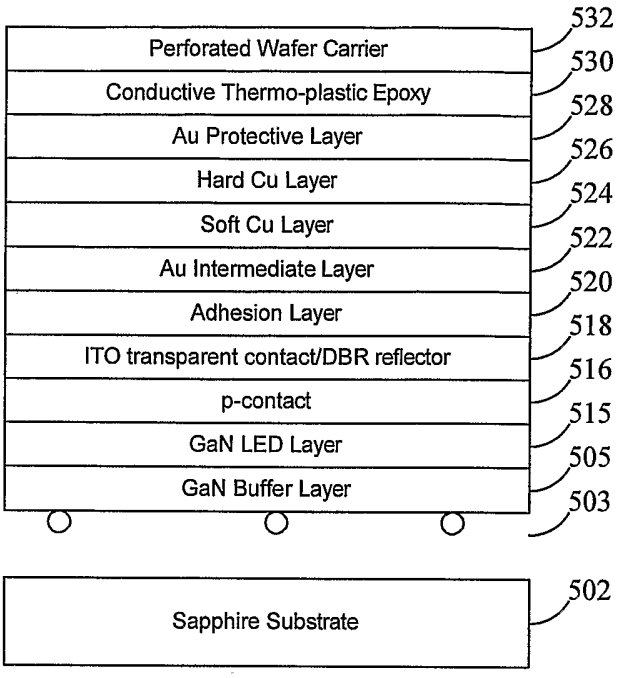


FIGURE 13

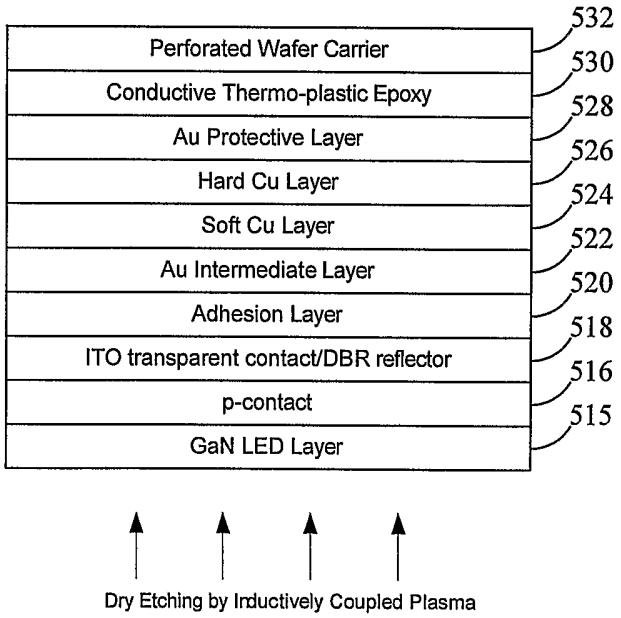


FIGURE 14

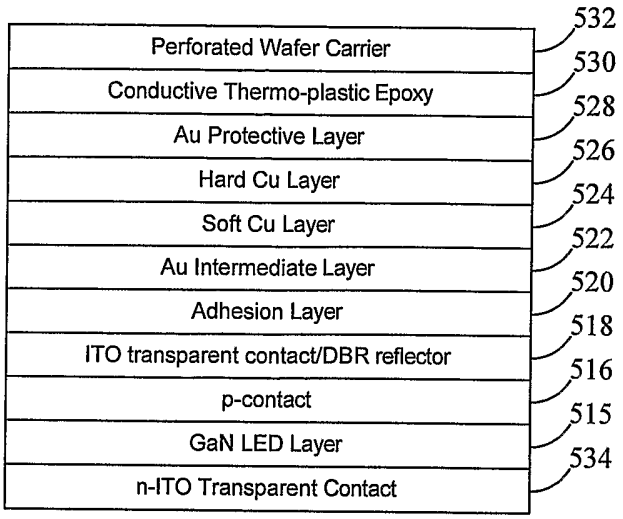


FIGURE 15

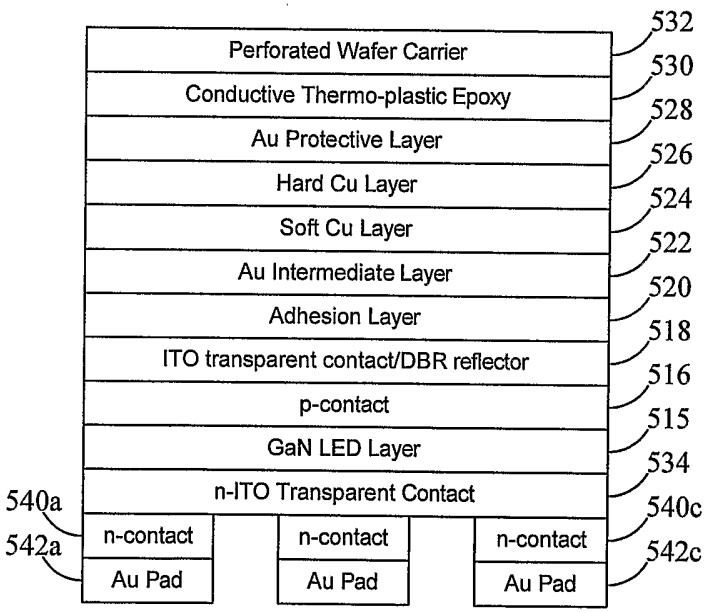


FIGURE 16

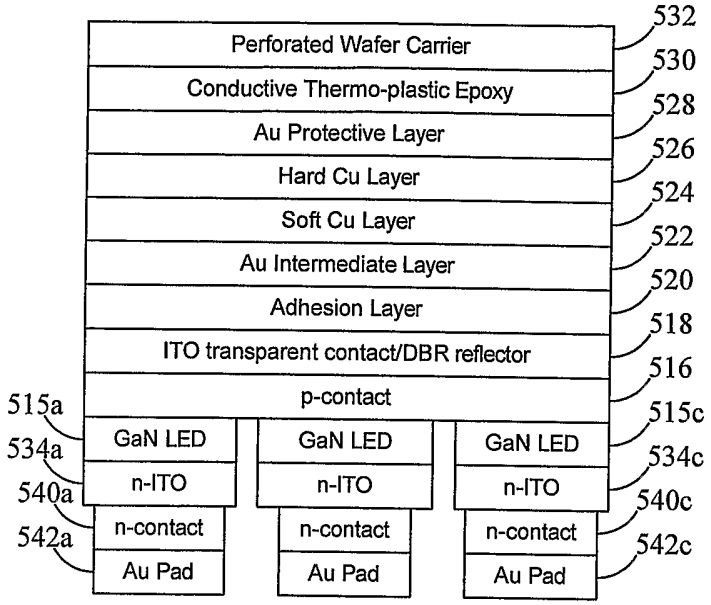


FIGURE 17

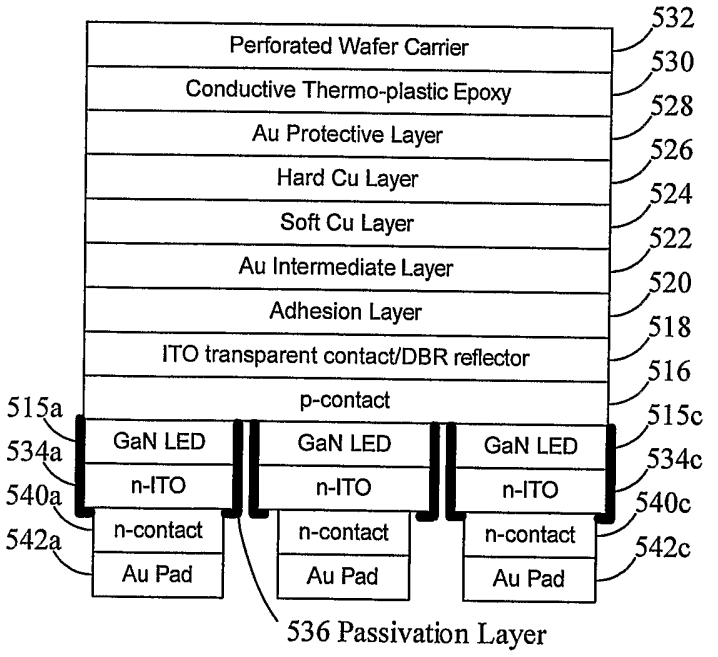


FIGURE 18

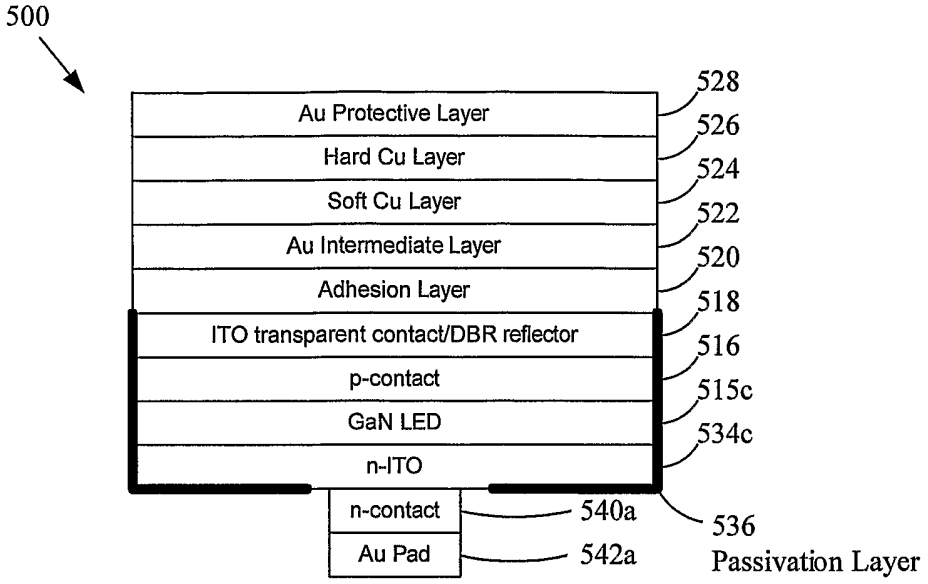


FIGURE 19

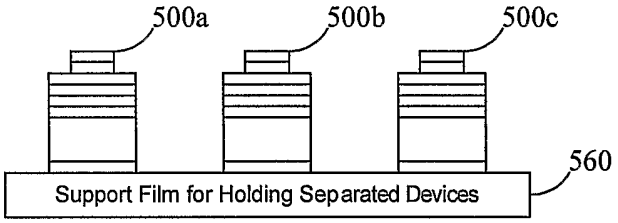
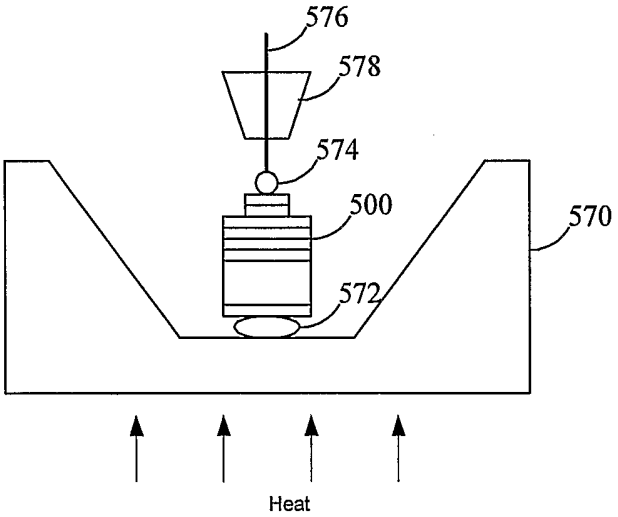



FIGURE 20