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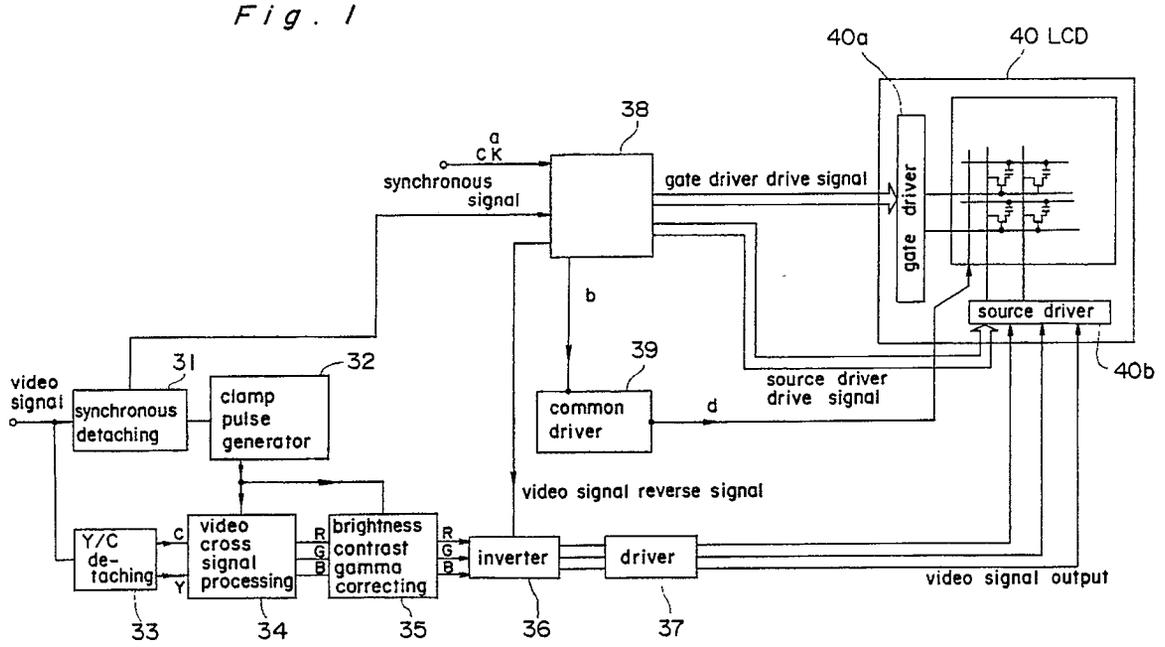
(54) Common driver circuit for a display panel.

(57) A common driver circuit for driving a load heavy in a capacitive property such as a common electrode or the like of a liquid crystal panel is composed of the simple circuit construction provided with each circuit of the voltage follower, the low-pass filter, the feedback, the control so that the variation in the direction current component which gives bad influences in the processing of the signals of this type of circuit is restrained to improve the reliability, and the direct current is not required to be cut to eliminate the direct current cutting capacitor of the large capacity.

Fig. 1



EP 0 428 250 A2

COMMON DRIVER CIRCUIT

BACKGROUND OF THE INVENTION

The present invention generally relates to a common driver circuit for driving a load heavy in a capacitive property such as a common electrode or the like of a liquid crystal panel.

Generally, a common driver circuit built into the conventional liquid crystal display apparatus of this type fed a bias through a variable resistor (2) to a buffer amplifier (1) to which a common amplitude signal (frame pulse) (FP) was inputted, the amplitude of the common amplitude signal was adjusted by the adjustment of the bias as shown in Fig. 6. The output of the buffer amplifier (1) was adapted to be removed in the direct current component by a capacitor for direct current cutting use (C1) and the common bias was adapted to be given newly by a variable resistor (3). But the above described core on amplitude signal (FP) and the common bias by the variable resistor (3) are given to the common electrode of the liquid crystal panel.

But in the conventional embodiment, in order to obtain the amplitude signal to which the common bias was added, the direct current component had to be cut by the capacitor (C1) out of the output from the buffer amplifier (1). Therefore, in order to exchange the common for each field, a capacitor of large capacity was required as a capacitor (C1). Also, as the common bias depends upon the power voltage Vcc, -Vee to be applied upon the variable resistor (3), the common bias also changes, applies bad influences upon the liquid crystal panel when these power voltages change.

As shown in Fig. 6, conventionally there was adopted a method of cutting the direct current component in the common output by the capacitor (C1) after amplifying the frame pulse, and adding the bias by the resistance division again. The amplitude of the common output was sometimes shaked as much as 8 Vpp at its maximum. Also, the -Vee connected with the bias adjustment (VR) of 3 sometimes could not be adjusted in the voltage the same as the source power voltage of the panel, depending upon the bias to be applied. Therefore, the -Vee was required to be taken from much lower voltage (-21V). Since the voltage varies independently of the variation in the source power voltage of the panel, the direct current may be added to the panel when the power is not stable. When the voltage for deciding the bias may be taken from the power line the same as the source power voltage of the panel, even the bias to be set by 3 varies in the same direction in accordance with the variation if the source power voltage receives the variation, with a disadvantage that the direct current is hard to be applied upon the panel. Also, in the speck of the panel, both the variation in the central voltage of the video signal to be applied upon the source driver and the variation in the central voltage of the common were required to be controlled even in the conditions of the signal content, the power variation and so on. In the video signal, the feedback was already applied and was stable, while in the common, the speck was not necessarily observed because of the above described causes.

SUMMARY OF THE INVENTION

Accordingly, the present invention has been developed with a view to substantially eliminating the above described drawbacks and has for its object to provide a common driver circuit, which is capable of feeding the common output provided with the stable bias, with no variation being provided in the common bias, and the capacitor of large capacity for direct current cutting use being not required.

In order to achieve the above described object, the present invention is composed of, in a common driver circuit for driving a liquid crystal panel, an output circuit composed of a buffer amplifier capable of sufficiently driving the capacitive load or of a voltage follower, a means for feeding the common signal and the common bias to the above described output circuit, a bias setting means for setting the above described common bias, a control means which detects the direct current level of the above described output circuit, so that the common bias set by the above described bias setting means may be normally retained through the use of the detection output.

According to such construction, as the common bias from the bias setting means is given to the output circuit and furthermore, when the common bias varies, the variation is compensated by the control means, so that it is normally retained.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become apparent from the following description taken in conjunction with the preferred embodiment thereof with reference to the accompanying drawings, in which;

Fig. 1 is a block diagram showing the whole

construction of a liquid crystal display apparatus into which a common driver circuit of the present invention has been built in;

Fig. 2 is a block diagram showing the schematic construction in one embodiment of a common driver circuit in accordance with the present invention;

Fig. 3 is a circuit diagram showing the concrete construction of the detailed circuit of the block diagram of Fig. 2;

Fig. 4 is a wave form chart of the respective signals to be caused in each portion of Fig. 1 and Fig. 3;

Fig. 5 is a circuit diagram showing a modified embodiment of a circuit diagram of Fig. 3; and

Fig. 6 is a circuit diagram showing the conventional embodiment of this type of common driver circuit.

DETAILED DESCRIPTION OF THE INVENTION

Before the description of the present invention proceeds, it is to be noted that like parts are designated by like reference numerals throughout the accompanying drawings.

Embodiment:

Fig. 1 is a block diagram showing the whole construction of a liquid crystal display apparatus into which a common driver circuit has been built in. Fig. 2 is a block diagram of a common driver circuit shown as one embodiment of the present invention. Fig. 3 is a circuit diagram showing the concrete circuit construction of the respective blocks of Fig. 2. Fig. 4 is a signal wave form chart of the signals in each portion of Fig. 1 and Fig. 3.

In the liquid crystal display apparatus of Fig. 1, a LCD panel 40 composed of a TFT array (Thin•Film•Transistor• Array) is provided with a gate driver 40a, a source driver 40b, and a common driver 39 so as to input a gate driver driving signal into a gate driver 40a from a liquid crystal panel controller 38, a source driver driving signal into the source driver 40b, and a signal for common signal making use into the common driver 39.

A video signal is inputted into a synchronous detaching circuit 31 and a Y/C detaching circuit 33. The synchronous signal which has been synchronously detached in the synchronous detaching circuit 31 is inserted into a liquid crystal panel controller 38 and a clamp pulse. generator 32 in a sine wave-form of 10MHz or more as shown in Fig. 4 (a). In a Y/C detaching circuit 33, the video signal is detached into a brilliance signal and a cross signal and is inputted into a video cross signal processing circuit 34. Prime color signals of R, G, B are outputted from the video cross signal processing circuit 34 and are inputted into a brightness, contrast, gamma correcting circuit 35. The clamp pulse of a clamp pulse • generator 32 is inputted into the video cross signal processing circuit 34 and the brightness, contrast, gamma correcting circuit 35. The prime color signals R, G, B of the brightness, contrast, gamma correcting circuit 35 are processed in a inverter circuit 36, and are inputted into the source driver circuit 40b as the video signal output from a driver circuit 37. A liquid crystal panel controller 38 inputs a synchronizing signal from a synchronous detaching circuit 31, and also, inputs a clock pulse ck, outputs a gate driver driving signal and a source driver driving signal as a control signal of a panel. At the same time, as a frame pulse (FP) synchronized with the signal or an inversion pulse, such a signal for common signal making use which is a horizontal periodic signal of 0 through 5V of 15MHz is outputted. The inversion pulse to be outputted from the liquid crystal panel controller 38 is inputted into an inverter 36 and a common driver 39. A horizontal periodic signal of 15KHz, which has a DC level of 0 through 5V as shown in Fig. 4 (b), as an inversion inputted into the common diver 39 is inputted into a buffer amplifier 11 as a common amplitude signal from a terminal 10 shown in Fig. 2. A control portion (12) for controlling bias, amplitude is connected with the buffer amplifier (11). The control portion (12) gives a set value established by an amplitude variable volume (13) to the buffer amplifier (11), and also, compares a bias set by a bias variable volume (14) with a direct current level feedbacked from the output circuit side by a comparator so as to vary the bias by the comparison output to give it to the buffer amplifier (11). In an operational amplifier (15) connected with the buffer amplifier, the output from the above described buffer amplifier (11) is fed into the (+) input terminal as a pulse signal having a DC level of -1V through -7 with such -4V as shown in Fig. 4 (c) being provided as a center bias. The output of the operational amplifier (15) is connected in transistors (Q1), (Q2) for buffer use as shown so that the load heavy in the capacitive property may be sufficiently driven, with the voltage feedback being effected from the output point (a) to the (-) input terminal. With this, the operational amplifier (15) and the buffer amplifiers (Q1), (Q2) compose a voltage follower 18. The voltage follower constitutes an output circuit (18), the output point (a) is connected with the common electrode of the liquid crystal panel, and the output is fed as a pulse signal which has a DC level of -1V through -7V with -4V being provided as a center bias as shown in Fig. 4 (d). It is also connected, on the one hand, with a low-pass filter (16) composed of a resistor

(R1) and a capacitor (C1). The output of the low-pass filter (16) is fed into the above described control portion (12) through a feedback circuit (17) as a signal of -4V as shown in Fig. 4 (e). The feedback circuit (17) is composed of an operational amplifier, with the output of the above described low-pass (16) being applied upon the plus input terminal, the voltage Vcc/2 whose power voltage + Vcc is divided in voltage by 1/2 being applied upon the minus input terminal. The output of the feedback circuit (17) is combined, as a signal of the -4V shown as shown in Fig. 4 (f), with one input terminal of the first, second comparators (20, 21 of Fig. 3) constituting one portion of the control portion (12). It is to be noted that the direct current voltage set by the bias variable volume (14) is given to the other input terminal of the comparator. The output of the comparator controls the bias to be given to the buffer amplifier (11) so that the direct current voltage to be given through the feedback circuit (17) from the above described low-pass filter (16) may conform to the direct current voltage from the above described bias variable volume (14) as a pulse signal varied by the VR (13), (14) in both the DC level and the amplitude as shown in Fig. 4 (g).

The block diagram of Fig. 2 is concretely composed of a circuit diagram shown in Fig. 3. The buffer amplifier 11 is composed of a working amplifier 19 and resistors R1, R2, R3, R4. The voltage follower 18 is composed of the operational amplifier 15 and a pair of transistors Q1, Q2 for buffer use. The feedback circuit 17 is composed of a working amplifier 17 and a resistor R6.

The low-pass filter circuit 16 is composed of a resistor R1 and a capacitor C1, with the direct current component thereof being inputted into the working amplifier of the feedback circuit 17. The feedback circuit 17 is composed of a working amplifier 22 and a resistor R6, with the output thereof being inputted into a first comparator 20 and a second comparator 21 of the control portion (12). The control portion 12 is composed of a first comparator 20, a second comparator 21, resistors R7, R8, R9, R10 and a capacitor C2. The amplitude variable volume (13) connected with the first comparator 21 is to adjust the amplitude of the output signal from the control portion (12). The bias variable volume 14 connected with the second comparator 20 is to adjust the center bias of the output signal from the control portion (12).

The inversion pulse inputted from the terminal (10) is amplified (or contracted) by the control signal from the control portion of the control portion (12) by the circuit 11, and at the same time, the bias is also controlled. The control signal of the bias to be made by the amplification circuit (12) is made through the comparison by the feedback circuit (17) between a reference level set by the bias variable volume (14) and a level of a signal to be made by the low-pass filter (16). The amplifier of the circuit (11) is controlled so that the output of the voltage follower (18) may become normally constant. The capacitor C3 together with the resistor R6 is provided for the smoothing use.

The inversion pulse inputted into the common driver 39 is adapted to be added into the liquid crystal panel LCD, with the amplitude stabilized by the concrete circuit of Fig. 3 and the bias being set.

The common driver circuit in accordance with the present invention is composed of a block circuit as shown in Fig. 2, and may be constructed as in the circuit diagram of Fig. 5 as a modified example in addition to the concrete circuit in Fig. 3. In the circuit shown in Fig. 5, the inversion pulse supplied to the input terminal (51) is inputted into the operational amplifier (52). The amplitude of the inputted inversion pulse is adjusted by the variable feedback resistor (53). The output of the amplifier (52) is inputted into the voltage follower (54) and is taken out as the common output. Also, the common output is taken out as the direct current output by the low pass filter composed of the resistor R17, and capacitor C12, and is inputted into the comparator (56). In the comparator (56), the level set by the comparator (57) and variable resistor (58) is compared with the above described low-pass filter output level, and the comparator output is applied to the voltage follower (55) through the low-pass filter comprising the resistor R18 and capacitor C13. The output is applied to the amplifier (52) so that the output of the low-pass filter comprising the resistor R17 and the capacitor C12 may become normally a level set by the variable resistor (58) with the direct current as shown in Fig. 4 (g). The capacitor C11 of Fig. 5 is provided for the by-pass (especially when the higher frequency is handled) of the high frequency component. The capacitor C13 smooths the output of the comparator (56), which drops to the reference voltage (the output of the (57)). The capacitor C14 provides protection against noise.

In Fig. 5, the common output is smoothed by the resistor R17, the capacitor C12, and is inputted into the comparator (56). Also, the bias set VR of the potentiometer (58) is established using both Vcc, Vee from the same power line as the source power voltage of the panel. The bias to be set by the potentiometer (58) sets the bias of the common output, and also, becomes a reference voltage of the direct current feedback, so that it may follow even the variation in the source power voltage. When the source power voltage has been varied, the variation in the voltage to be applied upon the panel becomes smaller because of the movement in accordance with the variation in the reference

voltage. Since the circuits are all directly connected in construction, the capacitor for the direct current cutting use is not required. The modified example of Fig. 5 provides the same effect as that of Fig. 3, with the stability that the feedback resistor (53) is varied with the volume in the amplitude adjustment.

As is clear from the foregoing description, the common driver circuit in accordance with the present invention is composed of the simple circuit construction provided with each of voltage follower, low-pass filter, feedback and control circuits. The variation in the direction current component which adversely affects the signal processing of this type of circuit is inhibited so as to improve reliability.

Also, D.C. cutting at the front end of the output circuit for providing a common bias is not required, so that a large capacity direct current cutting capacitor becomes unnecessary.

Although the present invention has been fully described by way of example with reference to the accompanying drawings, it is to be noted here that various changes and modifications will be apparent to those skilled in the art. Therefore, unless otherwise such changes and modifications depart from the scope of the present invention, they should be construed as included therein.

There are described above novel features which the skilled man will appreciate give rise to advantages. These are each independent aspects of the invention to be covered by the present application, irrespective of whether or not they are included within the scope of the following claims.

Claims

1. A common driver circuit for liquid crystal panel driving use, comprising an output circuit composed of a buffer amplifier capable of sufficiently driving the capacitive load or of a voltage follower, a means for feeding common signals and common biases to the above described output circuit, a bias setting means for setting the above described common bias, a control means which detects the direct current level of the above described output circuits, so that the common bias set by the above described bias setting means may be normally retained through the use of the detection output.

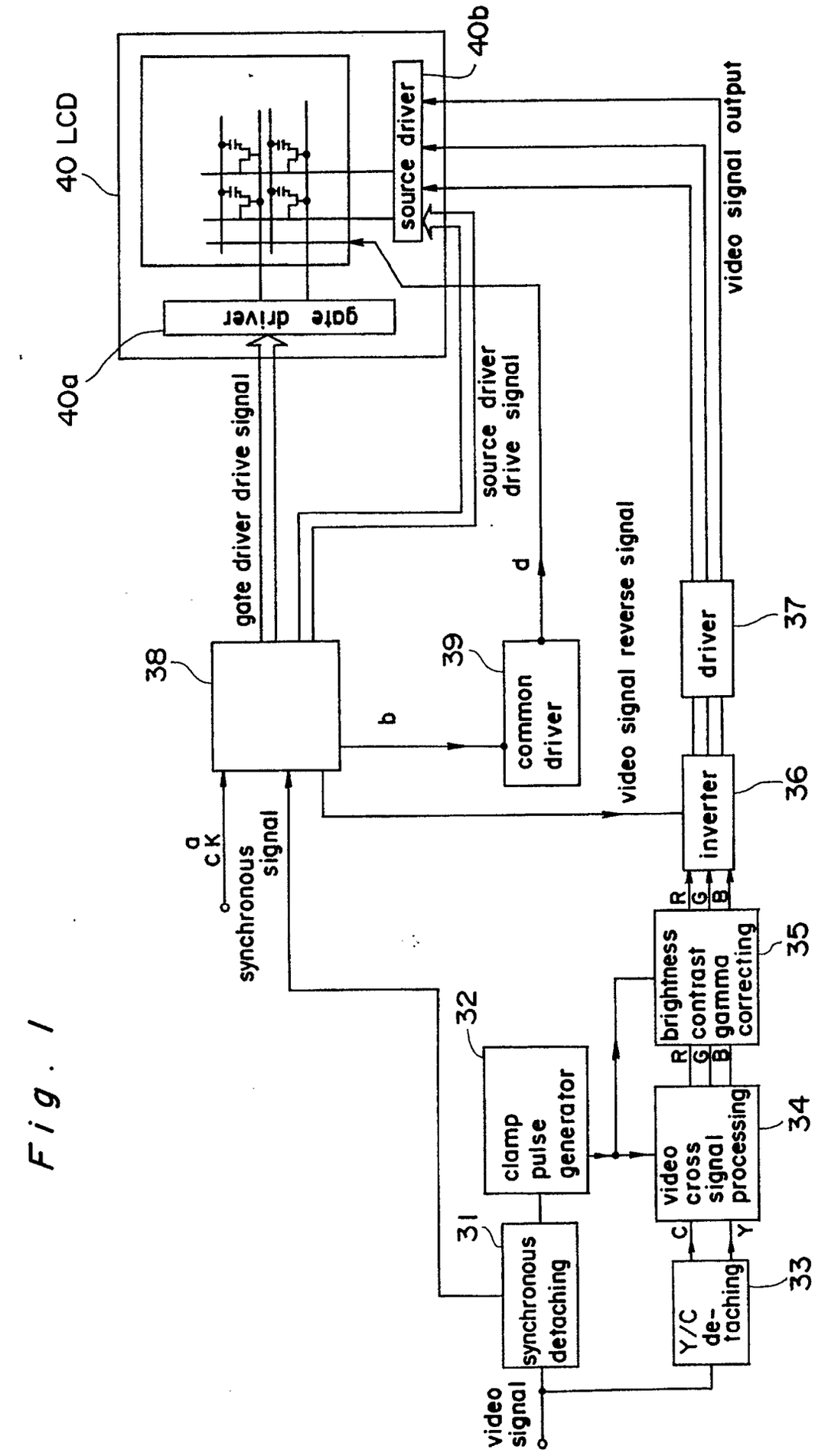
2. A driver circuit for driving a capacitive load in accordance with supplied drive signals, for example a common driver circuit for driving a liquid crystal display panel, the circuit comprising an output circuit (18; 54) adapted for driving the capacitive load, means (11) for feeding the supplied drive signals to said output circuit, means (14) for setting a desired DC bias level for the drive signals, means (R_5, C_1; R_{17}, C_{12}) for detecting the DC level of the signal from the output circuit, and control means (12) for controlling the feeding means so as to adjust the said DC bias to said desired level in response to the outputs of said setting means and said detecting means.

3. A driver circuit according to claim 2 wherein said detecting means (R_5, C_1; R_{17}, C_{12}) comprises a low-pass filter.

4. A driver circuit according to claim 2 or claim 3 wherein said feeding means comprises an operational amplifier (19; 52) receiving at a first input terminal thereof the supplied drive signals and at a second terminal thereof a controlled signal from said control means (12).

5. A driver circuit according to any preceding claim wherein said output circuit (18; 54) is a voltage follower circuit comprising an operational amplifier (15) and a buffer amplifier means (Q_1, Q_2; Q_{11}, Q_{12}) the output of said operational amplifier means being coupled to said detecting means (R_5, C_1; $R1_{17}$, C_{12}).

6. A driver circuit according to any preceding claim, wherein said control means includes a first controller (14) for DC bias level setting, and a second controller (13) for adjusting the amplitude of the control signal supplied to the feeding means.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40a
40b
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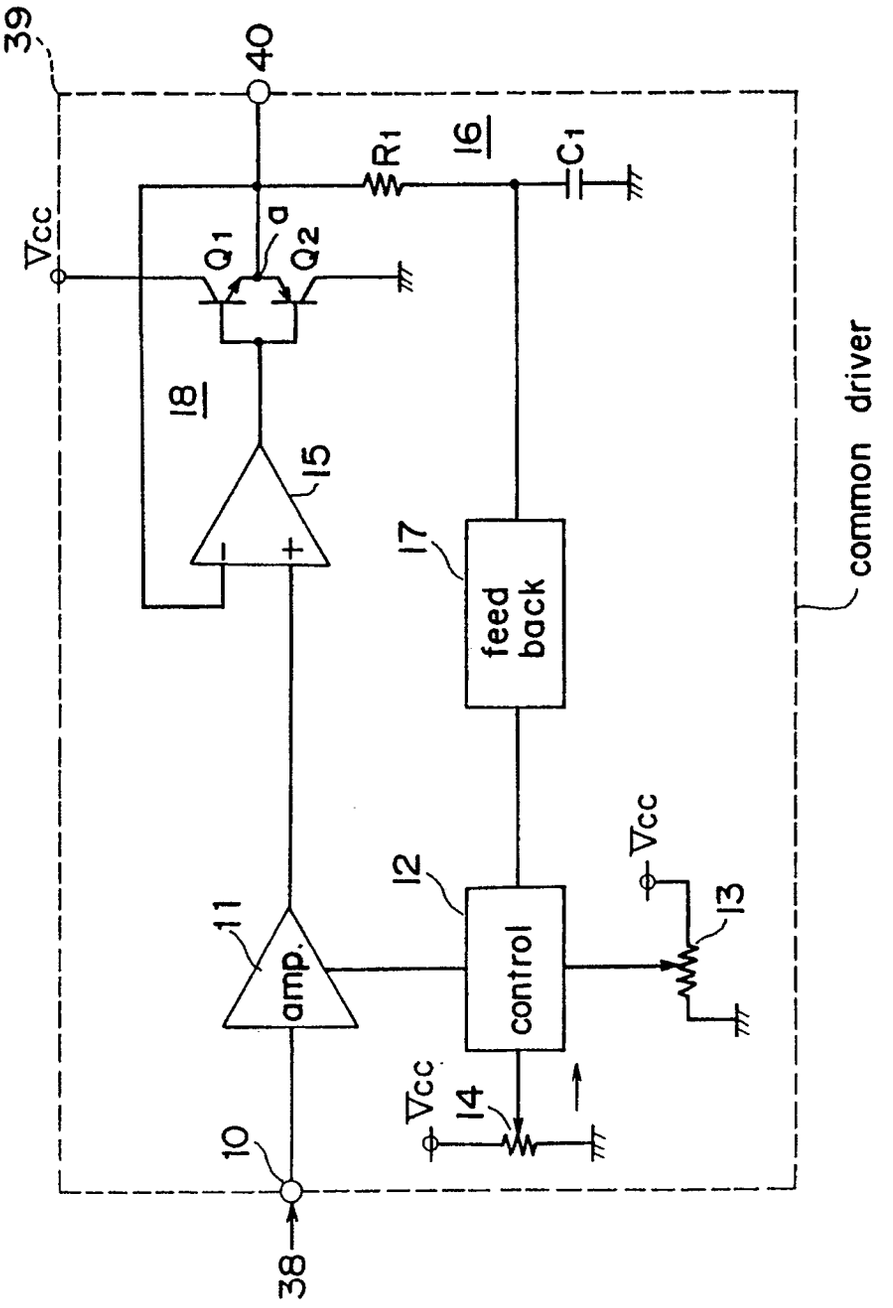
source driver
video signal output
gate driver drive signal
source driver drive signal
video signal reverse signal
38
39
common driver
37
driver
36
inverter
35
brightness contrast gamma correcting
34
video cross signal processing
33
Y/C de-taching
32
clamp pulse generator
31
synchronous detaching
synchronous signal
clock
video signal
R
G
B
C
Y
a
b
d

Fig. 1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12
Vcc
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11
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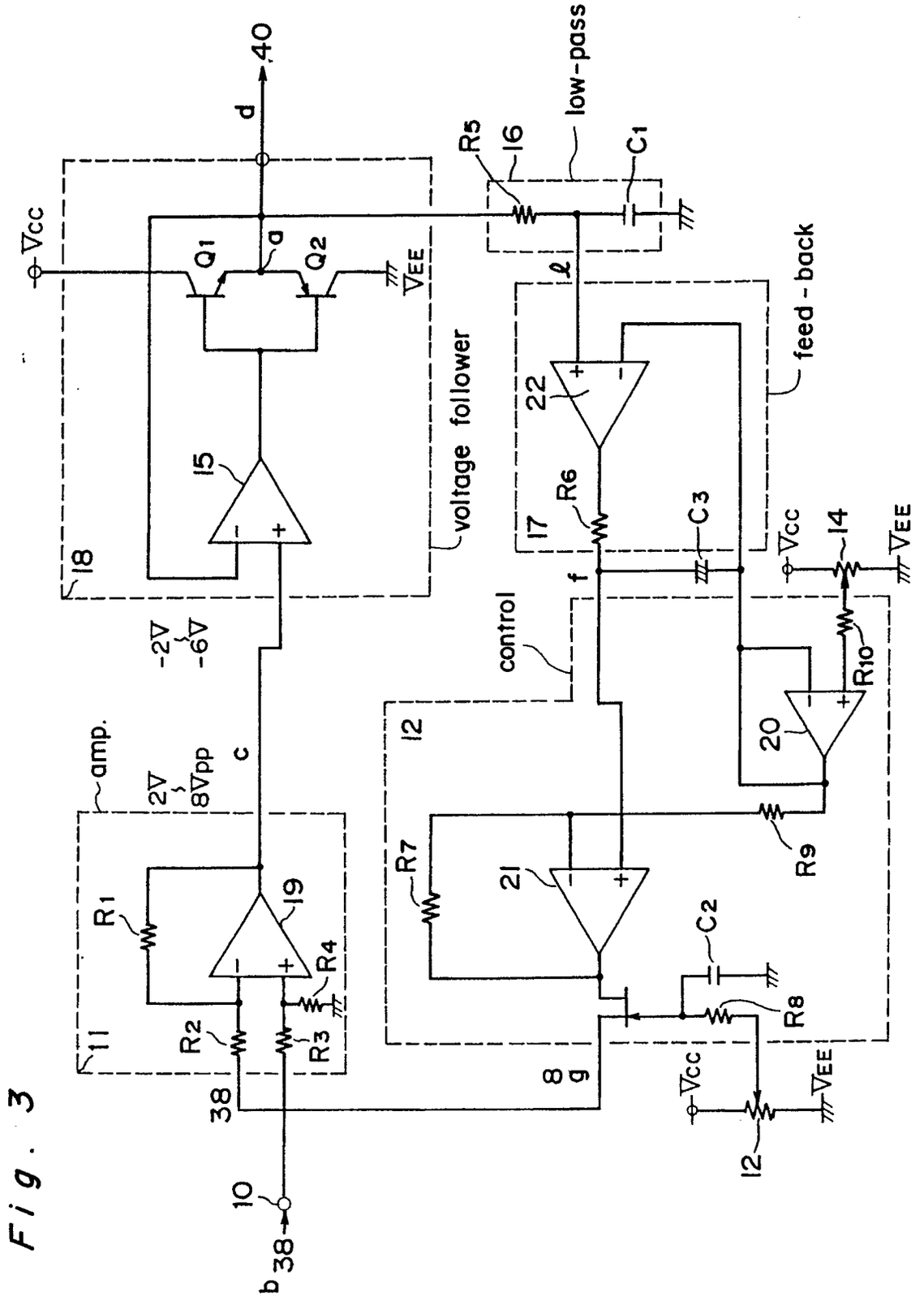
Vcc
14
10
38

Fig. 2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R5
16
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Vcc
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22
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18
Vcc
14
VEE
f
control
-2V
-6V
R10
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20
amp.
2V
8Vpp
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R7
21
R9
R1
19
C2
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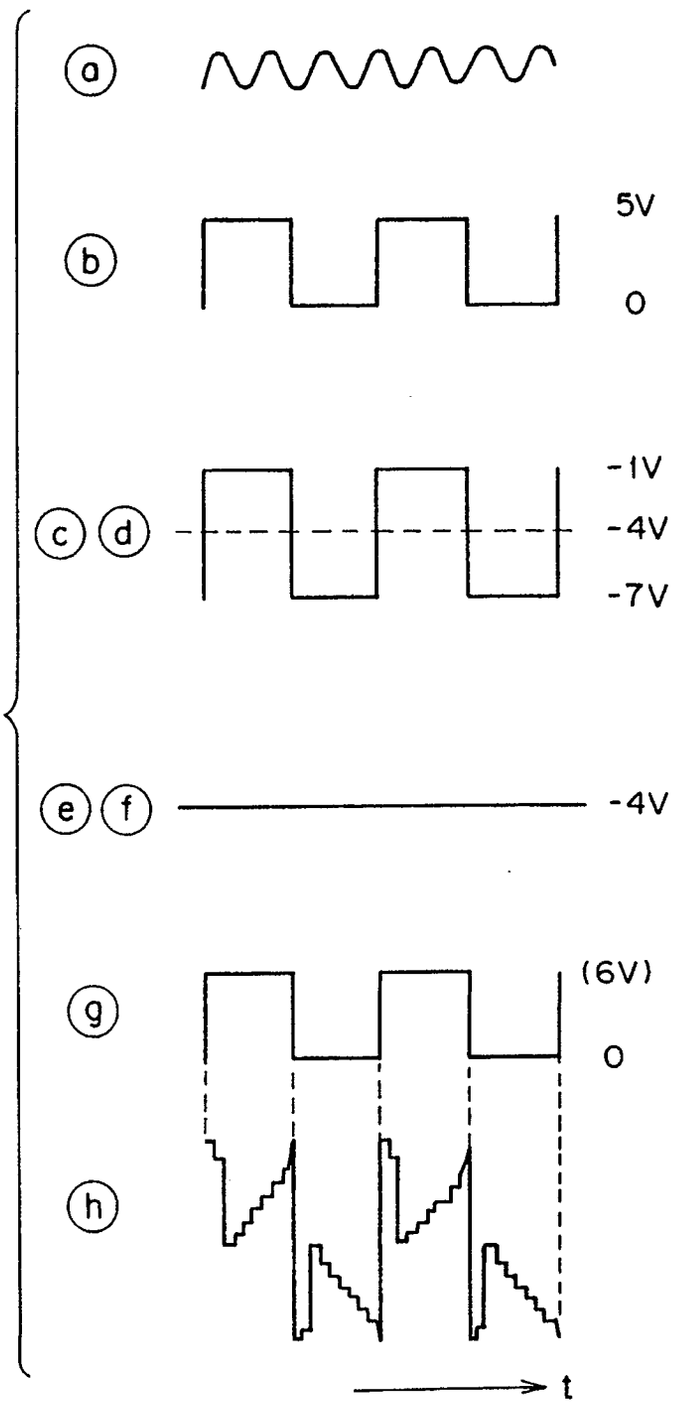
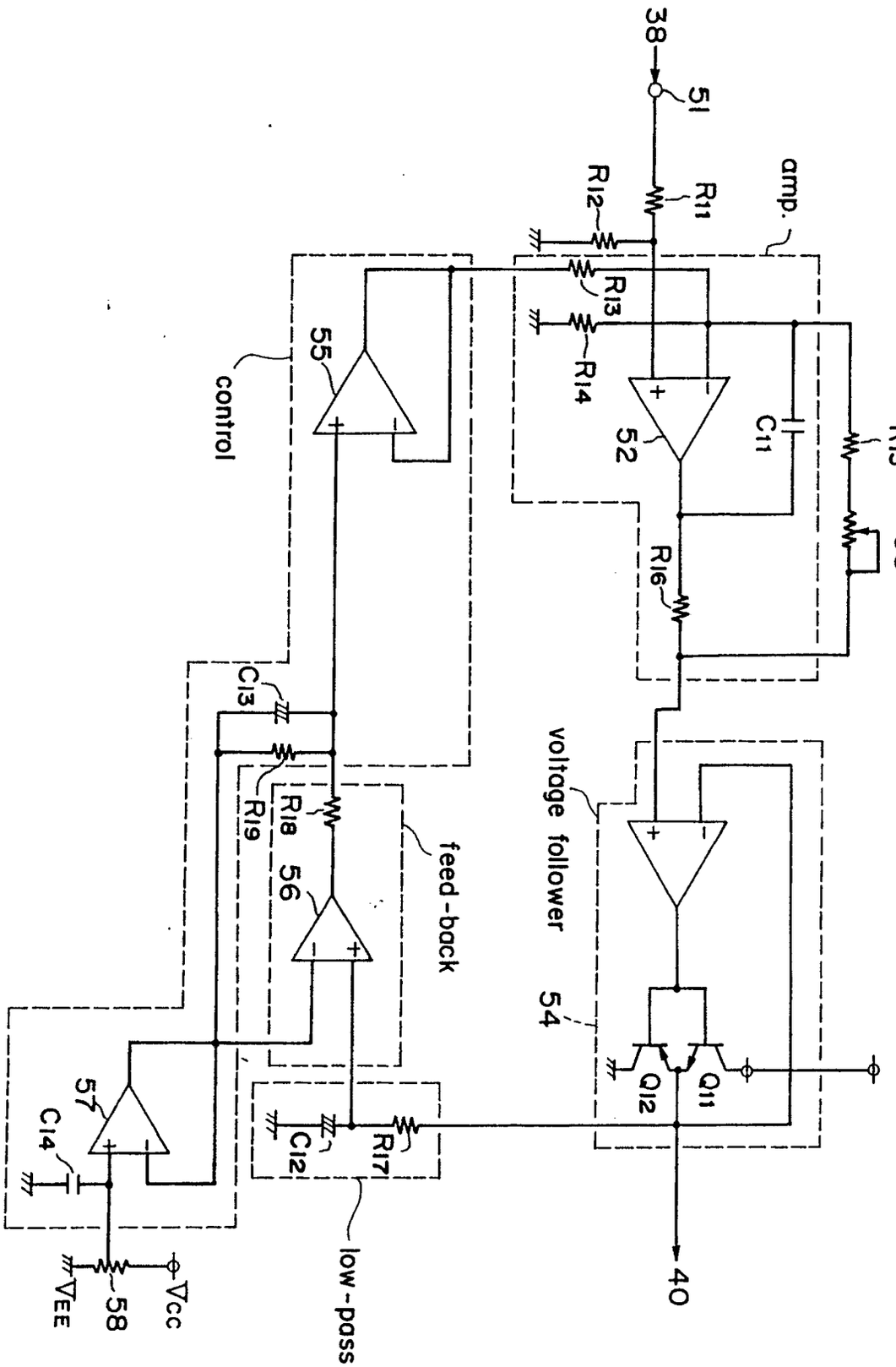
38

Fig. 3

Fig. 4

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R11
R12
amp.
R13
R14
55
control
52
C11
R15
53
R16
C13
R18
R19
56
feed-back
voltage follower
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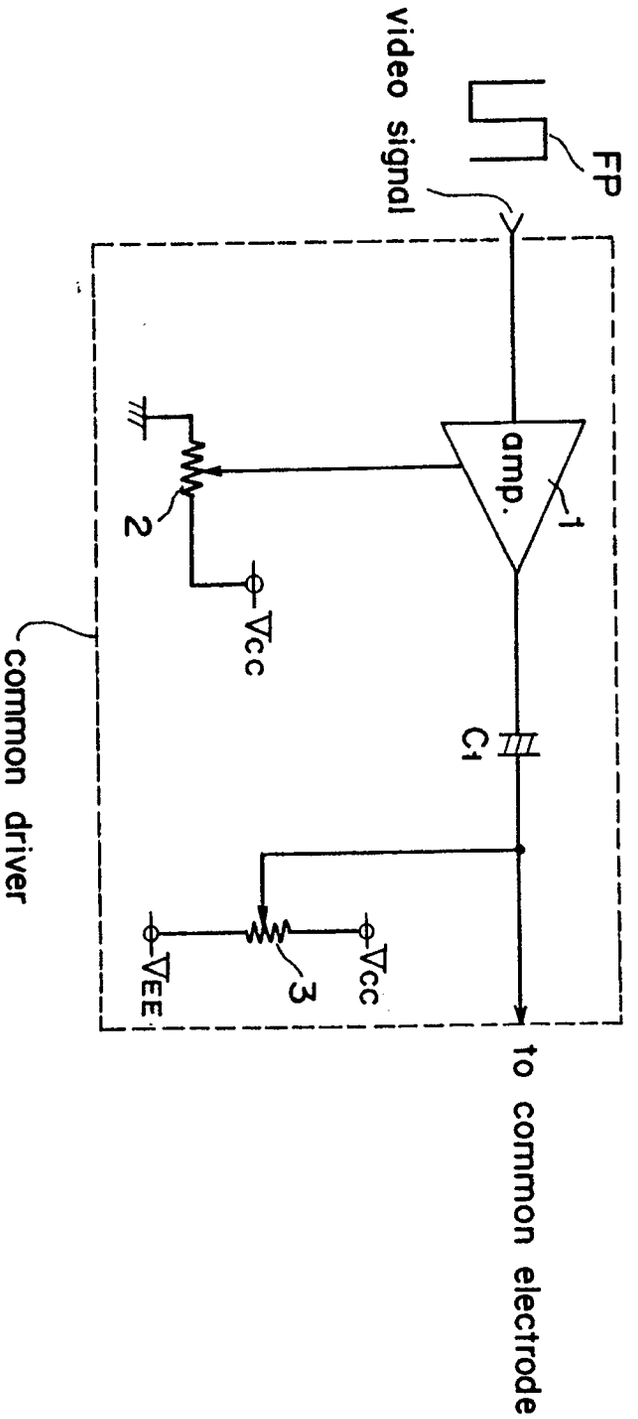
Q12
Q11
57
C14
C12
R17
low-pass
40
58
VEE
Vcc

Fig. 5

Fig. 6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amp.
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2
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C1
3
VEE
Vcc
common driver
to common electrode