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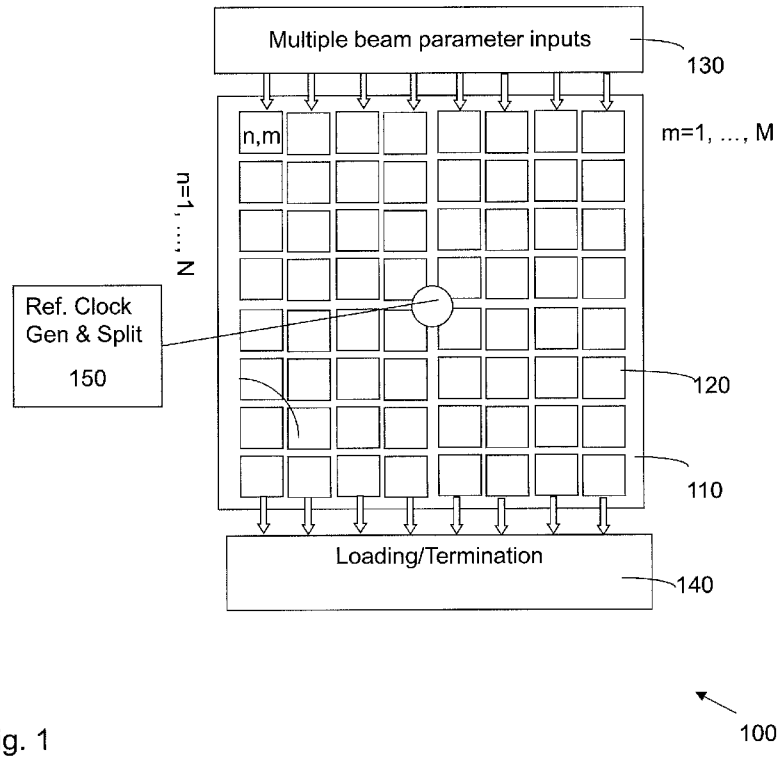

Fig. 1

(57) Abstract: A beamforming receiver 100 for receiving multiple radio signals and generating multiple output beam signals is disclosed. The beamforming receiver (100) comprises multiple beam parameter inputs (130) to receive multiple beam parameters and an element array (110) comprising a plurality of elements (120). The beamforming receiver 100 further comprises a loading unit 140 coupled to each element 120 in the element array 1 10. The beamforming receiver 100 further comprises a reference clock generating and splitting circuit 150 to generate and distribute reference clock signals for each element 120.

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A BEAMFORMING RECEIVER

TECHNICAL FIELD

Embodiments herein relate to a beamforming receiver. In particular, they relate to a beamforming receiver for receiving multiple radio signals and generating multiple output beam signals in a wireless communication system.

BACKGROUND

Beamforming is a signal processing technique for directional signal transmission or reception. This is achieved by combining antenna elements in a phased array in such a way that signals at particular angles or directions experience constructive interference while others experience destructive interference. Beamforming can be used at both the transmitting and receiving ends in order to achieve spatial selectivity. Beamforming is for instance intended to be used in the 5th generation (5G) wireless communications system. The beamforming can be performed at different parts along the signal path, such as in radio frequency (RF), in intermediate frequency (IF), in baseband (BB) frequency or in digital domain.

Digital beamforming (DBF) has many advantages, including the ability to apply multiple sets of weight vectors simultaneously to receive multiple beams. For example, in phased array receivers, multiple beams may be created from digitalized signals after analog to digital converters (ADCs) in each channel of the receiver. However, there are some drawbacks to DBF, e.g. the need to have separate receive chains from each antenna element through the ADCs. Therefore, to create multiple beams, high speed ADCs are needed which are very power hungry. Another issue is that the data rate created from each channel is very high, and data links have to be connected from chip-to-chip or die-to-die. This may require high speed field-programmable gate arrays (FPGAs) with many input/output (I/O) pins to receive the signals from the ADCs, which leads to huge data rate and complicated data interfaces. Thus, this type of configuration requires significant power, which may lead to heat dissipation issues. Further, some DBF algorithms require so much processing that large array with many elements become impractical.

It is difficult to perform multiple beam forming in RF and IF paths. There are some multiple beamforming methods performed in baseband. For example, an antenna array with analog beamforming (ABF) capability may be utilized for receiving RF signals. The ABF array

manipulates the phase and/or gain of signals arriving at each element, then sums the signals, and continues processing on the signals e.g., utilizing ADCs.

The patent application US8743914 discloses an analog beamforming receiver for forming multiple simultaneous independent beams. The analog beamforming receiver includes a first receive element for receiving a signal, where the first receive element is coupled with circuitry for sequentially adjusting at least one of a phase or a gain of the signal received by the first receive element. The analog beamforming receiver may also include a second receive element for receiving the signal, where the second receive element is coupled with circuitry for sequentially adjusting at least one of a phase or a gain of the signal received by the second receive element. The analog beamforming receiver further includes a combiner coupled with the first receive element and the second receive element for combining the phase or gain adjusted signals from the first receive element and the second receive element to form a combined analog signal. The analog beamforming receiver also includes an analog to digital converter coupled with the combiner for converting the combined analog signal from the combiner into a digital signal. The analog beamforming receiver further includes a demultiplexer coupled with the analog to digital converter for demultiplexing the digital signal from the analog to digital converter into a plurality of demultiplexed signals forming a plurality of multiple simultaneous independent beams. In this analog beamforming receiver, a number of simultaneous beams are determined by the maximum sample rate of the ADC, the sample rate per beam and the ABF switching time.

SUMMARY

Therefore it is an object of embodiments herein to provide an analog beamforming receiver for generating multiple beams. Some embodiments of the present invention are based on the inventor's insight that an obstacle to implementing such beamforming receivers, especially for relatively large arrays, is the distribution of control signals, or control parameters, for controlling e.g. the beam direction to the elements in the array.

According to embodiments herein, the object is achieved by a beamforming receiver for receiving multiple radio signals and generating multiple output beam signals. The beamforming receiver comprises multiple beam parameter inputs to receive multiple beam parameters. The beamforming receiver further comprises an element array comprising a plurality of elements. Each element comprises an antenna to receive the multiple radio signals; an amplifier to amplify the received multiple radio signals; a mixer to down-convert the amplified multiple radio signals and generate in-phase and quadrature phase signals; a

filter to filter the generated in-phase and quadrature phase signals and generate in-phase and quadrature phase input signals. Each element further comprises a plurality K of Phase Rotator and Amplitude control Units (PRAU) configured to perform phase rotation and amplitude control of the in-phase and quadrature phase input signals based on phase and amplitude control parameters and generate multiple analog output signals with individual phase shifts. Each element further comprises a parameter calculator to generate the phase and amplitude control parameters from the multiple beam parameters which are related to K directions of the multiple radio signals.

Since the beamforming receiver according to embodiments herein comprises an element array and each element comprises a number K of phase rotator and amplitude control units, all in parallel, at least K multiple output beam signals may be generated simultaneously. The phase rotator and amplitude control unit according to embodiments herein has relatively high accuracy and low power. Further, since each element comprises a parameter calculator, the phase and amplitude control parameters may be generated quickly and distributed locally to each phase rotator and amplitude control unit, therefore data interfaces are simple. Furthermore delays, noises and heating issues etc. which related to high speed data lines are reduced.

Thus, embodiments herein provide a beamforming receiver with improved performance on e.g. power consumption, accuracy etc. and which is easy to implement.

BRIEF DESCRIPTION OF THE DRAWINGS

Examples of embodiments herein are described in more detail with reference to attached drawings in which:

Figure 1 is a general block view of a beamforming receiver according to embodiments herein.

Figure 2 shows block views illustrating different element array shapes implemented in the beamforming receiver according to embodiments herein.

Figure 3 is a schematic block view illustrating an element comprised in the beamforming receiver according to embodiments herein.

Figure 4 shows signal flow charts illustrating phase rotation and amplitude control operations.

Figure 5 is a block view illustrating a Phase Rotator and Amplitude control Unit (PRAU) according to embodiments herein.

Figure 6 (a) and (b) are schematic views illustrating embodiments of a Phase Rotator and Amplitude control Circuit (PRAC).

Figure 7 (a) and (b) are block views illustrating example embodiments of a parameter calculator.

Figure 8 illustrating one example of a DC compensation unit.

Figure 9 is a schematic diagram illustrating one example of a mixer according to embodiments herein.

Figure 10 is a schematic diagram illustrating another example of a mixer according to embodiments herein.

Figure 11 is a block diagram illustrating examples of processing units comprised in the beamforming receiver.

Figure 12 is a schematic diagram showing a loading unit according to embodiments herein.

Figure 13 is a diagram showing examples of a beamforming receiver matrix.

Figure 14 is a block diagram illustrating a wireless communication device in which embodiments herein may be implemented.

DETAILED DESCRIPTION

A general block view of a **beamforming receiver 100** for receiving multiple radio signals and generating multiple output beam signals according to embodiments herein is shown in **Figure 1**. The beamforming receiver 100 comprises **an element array 110** which comprising a plurality of **elements 120**. The beamforming receiver 100 further comprises **multiple beam parameter inputs 130** to receive multiple beam parameters. The beamforming receiver 100 further comprises a **loading unit 140** coupled to each element 120 in the element array 110. The beamforming receiver 100 further comprises a **reference clock generating and splitting circuit 150** to generate and distribute reference clock signals for each element 120.

The plurality of elements 120 in the element array 110 may be arranged to form different shapes. In the example shown in Figure 1, an 8x8 element array in a square shape is shown, i.e. the element array 110 has N=8 rows and M=8 columns, or N=8 elements in each column and M=8 elements in each row. Each element 120 in the element array 110 is identified by an address index <n, m>, where n=1, ... N and m=1, ... M, which means the element is in the n-th row and m-th column of the element array 110. Although the row and

column defined here are referred to Figure 1 in its direction in a conventional way, they will not set limitations to the configuration of the element array 110. For example, the element array 110 may comprise M rows and N columns, if the element array 110 in Figure 1 is rotated 90 degree either to the right or left. The array can also be rotated in any arbitrary angle such that neither the rows nor the columns are horizontal or vertical.

According to some embodiments herein, the element array 110 may be formed in any other shape than the square shape as shown in Figure 1. For example, as shown in **Figure 2**, the element array 110 may be formed in different shapes and may comprise N rows and M columns, where N may or may not be equal to M. The element array 110 may be arranged to form a rectangle shape as shown in Figure 2 (a), where numbers of rows and columns are not equal. The element array 110 may be arranged to form a cross shape as shown in Figure 2(b), where elements at corners of the array are omitted. More generally speaking, in some embodiments, all rows do not need to include the same number of columns. Vice versa, all columns do not need to include the same number of rows. In such embodiments, the numbers N and M may be seen as the maximum number of rows (in a column) and the maximum number of columns (in a row), respectively. Thus, in such embodiments, there may be at least one row that has fewer columns than at least one other row. Conversely, there may be at least one column that has fewer rows than at least one other column. The element array 110 may be arranged to form a hexagon shape as shown in Figure 2(c), where each consecutive row has a different numbers of elements and are placed with an offset to each other, thus columns formed by the elements are not in straight lines.

Figure 3 shows an example of the element 120 according to embodiments herein. The element 120 has at least one channel or branch which comprises **an antenna 121** to receive the multiple radio signals; an **amplifier 122** to amplify the received multiple radio signals; a **mixer 123** to down-convert the amplified multiple radio signals and generate in-phase and quadrature phase signals; a **filter 124** to filter the generated in-phase and quadrature phase signals and generate in-phase and quadrature phase input signals; and a plurality K of Phase Rotator and Amplitude control Units, **PRAU<1>, ...PRAU<j>,... PRAU<K>**, which are configured to perform phase rotation and amplitude control of the in-phase and quadrature phase input signals based on the phase and amplitude control parameters and generate multiple analog output signals, **Out<1>, ... Out<j>, ...Out<K>**, with individual phase shifts, **ψ1, ... ψj, ...ψK**.

The element 120 further comprises **a parameter calculator 125** to generate the phase and amplitude control parameters from multiple beam parameters. The multiple beam

parameters are related to K directions of the multiple radio signals. In the embodiments and examples presented below, they comprise azimuth vector, **A1,..., AK**, elevation vector, **E1,..., EK**, and amplitude vector, **Amp1,..., AmpK**. However, in other embodiments, the parameters may be encoded in different form than such vectors.

Individual, or local, control parameters for the PRAUs in each element depends on the location, or position, of that element in the array. Based on knowledge of the location, which can be programmed or hardcoded into the parameter calculator 125 of each element, e.g. by the address index <n, m>, the parameter calculator can compute these individual control parameters from the multiple beam parameters. By distributing the same multiple beam parameters to several (e.g. all) elements of the array, and then utilizing the parameter calculator 125 in each element to generate the local control parameters for the PRAUs in each element locally, the overall control interface for the beamforming receiver can be simplified to a large extent. Consider for instance an alternative implementation as a reference example, where the local control parameters for all elements are generated centrally in a global control unit of the beamforming receiver, and all of these local control parameters are distributed to the elements in the array via a control interface. In this case, the number of control parameters that need to be distributed would be very large, and increases with an increasing number of elements in the array, and may limit the number of elements that can be practically implemented e.g. due to complex wire routing and control interface needed to distribute the control parameters. Using a solution with local parameter calculators 125 in each element as proposed in embodiments herein, the complexity of the control interface and wire routing can be largely reduced compared with the reference example, e.g. facilitating larger arrays.

According to some embodiments, the element 120 may have more than one channel, for instance 4 or 8 channels, which may be viewed as paralleled structures with corresponding duplications of the circuits mentioned above, of course some of the circuits may be shared. If the element 120 has more than one channel, the vector dimension for azimuth vector A1,... AK, elevation vector, E1,... EK, and amplitude vector, Amp1,..., AmpK and the address index n and m, may be duplicated, or local address may be inserted.

All elements in the element array 110 are synchronized by a reference clock. The reference clock may be, e.g. generated in the reference clock generating and splitting circuit 150, which is usually located in the centre of the element array 110. Synchronization may be achieved by matching the delays in the clock distribution networks to the different elements

The multiple beam parameters, i.e. information on azimuth and elevation angles and amplitude control for K multiple radio signals, are sent either by point-to-point or in broadcast way, or by many other means to the beamforming receiver 100, and then received by each element 120 via the multiple beam parameter inputs 130 through data bus.

According to some embodiments, each PRAU<1>, ...PRAU<j>,... PRAU<K> is configured to perform phase rotation and amplitude control of the in-phase and quadrature phase input signals and generate one output Out<j> of the multiple analog output signals Out<1>, ... Out<j>, ...Out<K> with an individual phase shift ψj.

In general, operations performed on a quadrature signal I, Q with a phase rotation of θ and amplitude control of a, to generate a phase rotated and amplitude controlled quadrature signal, OI and OQ, may be expressed as

$$\begin{bmatrix} OI \\ OQ \end{bmatrix} = \begin{bmatrix} a\cos(\theta), & a\sin(\theta) \\ -a\sin(\theta), & a\cos(\theta) \end{bmatrix} \begin{bmatrix} I \\ Q \end{bmatrix} = \begin{bmatrix} a11, & a12 \\ a21, & a22 \end{bmatrix} \begin{bmatrix} I \\ Q \end{bmatrix} \quad (2)$$

Where, the four factors a11, a12, a21, a22 are merged phase rotation and amplitude control coefficients. The operation in Eq. (2) is shown in a signal flow chart in **Figure 4** (a).

According to some embodiments herein, the four factors a11, a12, a21, a22 in Eq.(2) may be split into amplitudes A11, A12, A21, and A22, and signs, so the amplitudes are always positive, i.e. larger or equal 0. Then the sign of the function sin and cos of the phase θ are split into 4 positive sign signals pa11, pa12, pa21 and pa22, and 4 negative sign signals na11, na12, na21 and na22, so that

$$paij = \begin{cases} 1, & \text{aij} \geq 0 \\ 0, & \text{aij} < 0 \end{cases}$$

$$naij = \begin{cases} 0, & \text{aij} \geq 0 \\ 1, & \text{aij} < 0 \end{cases} \quad (3)$$

$$\text{for} \quad \text{i, j} \in [1,2]$$

Then aij may be expressed as

$$aij = paij \cdot Aij + naij \cdot Aij \quad (4)$$

As such, the operation of Eq.(2) may be implemented in a differential style as shown in the signal flow chart in Figure 4 (b), where the original structure (a) is converted into differential absolute value weighted style in (b). Thus, the operation in Eq. (2) may be expressed by partial summed differential signal forms as

$$\begin{bmatrix} OIp \\ OQp \end{bmatrix} = \begin{bmatrix} A11 \cdot pa11, & A12 \cdot pa12 \\ A21 \cdot pa21, & A22 \cdot pa22 \end{bmatrix} \begin{bmatrix} Ip \\ Qp \end{bmatrix}$$

$$+$$

$$\begin{bmatrix} OIp \\ OQp \end{bmatrix} = \begin{bmatrix} A11 \cdot na11, & A12 \cdot na12 \\ A21 \cdot na21, & A22 \cdot na22 \end{bmatrix} \begin{bmatrix} In \\ Qn \end{bmatrix}$$

$$\begin{bmatrix} OIn \\ OQn \end{bmatrix} = \begin{bmatrix} A11 \cdot pa11, & A12 \cdot pa12 \\ A21 \cdot pa21, & A22 \cdot pa22 \end{bmatrix} \begin{bmatrix} In \\ Qn \end{bmatrix}$$

$$+$$

$$\begin{bmatrix} OIn \\ OQn \end{bmatrix} = \begin{bmatrix} A11 \cdot na11, & A12 \cdot na12 \\ A21 \cdot na21, & A22 \cdot na22 \end{bmatrix} \begin{bmatrix} Ip \\ Qp \end{bmatrix} \quad (5)$$

Each PRAU<1>, …, PRAU<j>,… PRAU<K> is configured to perform operations expressed in Eq. (5) on the in-phase and quadrature phase input signals. By splitting the phase rotation and amplitude control parameters to positive amplitudes and positive and negative sign control signals, the PRAUs may be implemented easily and accurately.

Figure 5 shows a block diagram of one of the K PRAUs, e.g. the j-th PRAU<j>, denoted as **PRAU 500**, according to embodiments herein. The amplitude control coefficients may comprise a number of digital bits, e.g. N1 digital bits. To implement the PRAU 500 which may be amplitude controlled by N1 digital bits, each PRAU 500 comprises a plurality N1 of Phase Rotator and Amplitude control Circuits PRAC<1>, …PRAC<i>, …, PRAC<N1> as shown in Figure 5, using differential weighting factors, such as binary weighting

As discussed above, the phase and amplitude control parameters may be split into amplitudes and signs, so the phase and amplitude control parameters comprise sign control signals pa11, pa12, pa21, pa22, na11, na12, na21, na22 and positive amplitude coefficient signals A11, A12, A21, A22. In Figure 5, a11<j, i>, a12<j, i>, a21<j, i>, a22<j, i> are positive amplitude coefficient signals which represent one bit, i.e. the i-th bit, of the positive amplitude control coefficients A11, A12, A22, A22 respectively for the j-th PRAU, and pa11<j>, pa12<j>, pa21<j>, pa22<j>, na11<j>, na12<j>, na21<j>, na22<j> represent the positive and negative sign signals for the j-th PRAU. Each PRAC<1>, …PRAC<i>, …PRAC<N1> is configured to receive one bit of the positive amplitude coefficient signals, e.g. the i-th PRAC<i> is configured to receive the i-th bit of the positive amplitude coefficient signals a11<j, i>, a12<j, i>, a21<j, i>, a22<j, i>, where i=1, …, N1 and j=1,…K.

Figure 6 (a) shows a schematic view of one of the N1 PRACs, e.g. the i-th PRAC<i>, according to one embodiment herein. **Figure 6 (b)** shows a schematic view of one of the N1 PRACs, e.g. the i-th PRAC<i>, according to another embodiment herein.

As shown in Figure 6(a) and (b), each PRAC comprises an input port comprising in-phase and quadrature-phase inputs Ip, In, Qp, Qn to receive the in-phase and quadrature phase input signals; an output port comprising in-phase and quadrature-phase outputs OIp, OIn, OQp, OQn; and control inputs to receive the phase and amplitude control parameters.

Each PRAC further comprises a plurality of switched transconductance branches, wherein each switched transconductance branch comprises one transconductance transistor connected in series with two switching transistors. In Figure 6(a), each transconductance transistor is connected in series with its own two switching transistor. In Figure 6(b), the transconductance transistors are pairwise connected in series with the same two switching transistors.

As shown in Figure 6(a) and (b), a gate of one switching transistor is coupled to one of the sign control signals pa11, pa12, pa21, pa22, na11, na12, na21 na22, a gate of another switching transistor is coupled to one of the positive amplitude coefficient signals a11<i>, a12<i>, a21<i>, a22<i>, a gate of the transconductance transistor is coupled to one of the in-phase and quadrature-phase inputs Ip, In; Qp, Qn, and a drain of the transconductance transistor is coupled to one of the in-phase and quadrature-phase outputs OIp, OIn, OQp, OQn.

As seen from Figure 6 (a) and (b), each transconductance branch is a current branch which implements one operation and generates current to the output. For example, the first branch to the left implements $OIp = a11 \cdot pa11 \cdot Ip$, and the four branches to the left which connected to the output OIp implement operation $OIp = a11 \cdot pa11 \cdot Ip + a21 \cdot pa21 \cdot Qp + a11 \cdot na11 \cdot In + a21 \cdot na21 \cdot Qn$, i.e. the first two equations in Eq.(5), for calculating OIp. Since the drain of the transconductance transistor is coupled to one of the in-phase and quadrature-phase outputs, and it is in series with the two switching transistor, the positive amplitude coefficient signals and the sign control signals will control if it will contribute current to the outputs.

To simplify, the index j is omitted in the denotation of the positive amplitude coefficient signals and sign control signals, and they are just denoted as a11<i>, a12<i>, a21<i>, a22<i> and pa11, pa12, pa21, pa22, na11, na12, na21 na22 in Figure 6 (a) and (b).

According to some embodiments herein, each PRAU<1>, ...PRAU<j>,... PRAU<K> has independent phase and amplitude control parameters inputs and independent baseband quadrature outputs. The K outputs Out<1>, ... Out<j>, ...Out<K> from the PRAUs in each

element 120 are analog quadrature baseband signals, usually in differential form. Thus, as shown in Figure 5, each of the multiple analog output signals, e.g. the j-th output Out<j> of the j-th PRAU<j> may comprise in-phase and quadrature-phase output signals OIp<j>, OIn<j>, OQp<j>, OQn<j>. To generate the j-th in-phase and quadrature-phase output signals OIp<j>, OIn<j>, OQp<j>, OQn<j>, the in-phase outputs (OIp, OIn) from each PRAC (PRAC<1>,...PRAC<i>,...PRAC<N1>) are arranged to be combined, e.g. connected together, to generate the in-phase output signal (OIp<j>, OIn<j>) of the output signal (Out<j>), and the quadrature-phase outputs (OQp, OQn) from each PRAC (PRAC<1>,...PRAC<i>,...PRAC<N1>) are arranged to be combined, e.g. connected together, to generate the quadrature-phase output signal (OQp<j>, OQn<j>) of the output signal (Out<j>), wherein j=1,...K. For example, the outputs OIp from all PRACs are connected together to generate OIp<j>, the outputs OIn from all PRACs are connected together to generate OIn<j> etc.

It can be seen that the structure of the PRAC in each PRAU according to embodiments herein is totally different from conventional variable gain amplifiers and/or phase rotators which are built with feedback mechanism. The conventional variable gain amplifiers and/or phase rotators have limited accuracy in adjusting the phase and gain of the signals, especially at higher frequency. Further, the conventional amplifiers consume more power as the bandwidth increases. However, as described above, the PRAU in the beamforming receiver 100 comprises a plurality N1 of PRAC and each PRAC comprises a plurality of switched transconductance branches. The switched transconductance branches are controlled by the phase and amplitude control parameters which comprise sign control signals and positive amplitude coefficient signals, and each positive amplitude coefficient signal has N1 digital bits, the switched transconductance branches in the PRAU are digital controlled to generate currents to the outputs, therefore relatively high accuracy can be achieved. Further, the branches can be configured with an open drain topology, which can be selectively enabled or disabled, which facilitates an implementation with relatively low power consumption.

Below, calculations of the required phase shift ψj for each PRAU in each element and calculations of the phase and amplitude control parameters from the phase shift ψj will be described.

For the j-th PRAU <j> in the element <n, m>, the required phase shift ψj may be expressed as

$$\psi j = 2\pi fc \cdot td + m \cdot Aj + n \cdot Ej + \Delta Temp \cdot tc \qquad (6)$$

Where n and m are element address index, Aj is azimuth angle, Ej is elevation angle, fc is carrier frequency, td is local oscillator time delay error, ΔTemp is temperature difference and tc is temperature coefficient. This equation may be used to create required phase shift for the j-th output beam signals of the element in the n-th row and m-th column of the element array 110. A controller unit may be used to change index j, j=1, 2,…,K, to get K phases for the K output beam signals.

Figure 7 (a) and (b) show examples of the parameter calculator 125, denoted as **parameter calculator 700**, for calculating the phase and amplitude control parameters from the multiple beam parameters, e.g.. azimuth vector, A1,…, AK, elevation vector, E1,… EK, and amplitude vector, Amp1,…, AmpK based on Eq. (6).

As shown in Figure 7(a) and (b), the parameter calculator 700 comprises a **controller 701** to change index j for the individual phase shifts ψj, where j=1, 2…K. It means that the controller 701 at each parameter refresh period, controls the parameter calculator 700 to recalculate the phase and amplitude control parameters for j-th beam, where j=1,2,…,K.

The parameter calculator 700 further comprises a plurality of **multiplier 702** which comprising element address index inputs (n, m), multiple angel parameters inputs to receive the azimuth and elevation vectors Ak, Ek, compensation parameter inputs to receive compensation parameters fc, td, tc, ΔTemp. The multipliers perform the four multiply operations in Eq. (6) with coefficients α1, α2, α3, α4.

The parameter calculator 700 further comprises a phase rotation look-up-table (LUT) to store sinusoid values of phase shifts ψj.

The phase rotation LUT implements sinusoid functions, i.e. it stores the values of Amp<n,m,j>*sin(ψj) and Amp<n,m,j>*cos(ψj).

According to some embodiments, the phase rotation LUT is a full table comprising sinusoid values of the phases from 0 to 360 in degree or 0 to 2π in rad. In this case, ψj may be linearly mapped to the address of the phase rotation LUT. To reach high resolution, when implemented in digital Random Access Memory (RAMs), the whole phase range can be divided into Np units, where Np is 2^{np}.

As the sinusoid function of the phase shift is a periodic function, to limit the size of the LUT in one period, module operation may be needed, which is expressed as:

$$\theta j = \mathrm{mod}(2\pi fc \cdot td + m \cdot Aj + n \cdot Ej + \Delta Temp \cdot tc, \theta_{Mod}) \qquad (7)$$

where mod(y, x) is a modulus operation of a given y with modulo x, and θ_{Mod} is chosen from π/2, π, or 2π.

Therefore the parameter calculator 700 may further comprises a **modulus operator 706**. The modulus operator 706 operates based on Eq. (7).

According to some embodiments herein, the phase rotation LUT is a half table comprising sinusoid values of phases from 0 to 180 in degree or 0 to π in rad, as the **phase rotation LUT 703** shown in Figure 7 (a).

According to some embodiments herein, the phase rotation LUT may be a quart of the full table, for ψj from 0 to 90 in degree, or 0 to π/2 in rad, as the **phase rotation LUT 704** shown in Figure 7 (b). Then the size of the phase rotation LUT 704 becomes 4 times smaller than the full table. In such case the quadrature sinusoid functions need to be swapped in every phase jump of π/2. Thus the parameter calculator 700 further comprises a **swap unit 705**.

The phase and amplitude control parameters, i.e. the positive amplitude coefficient signals a11<n,m,j>, a12<n,m,j>, a21<n,m,j>, a22<n,m,j> and the positive sign control signals pa11<n,m,j>, pa12<n,m,j>, pa21<n,m,j>, pa22<n,m,j> may be calculated by the parameter calculator 700, stored in the **register bank 707** and input to the PRAUs via data bus **AP** as shown in Figure 7. The negative sign control signal na11<n,m,j>, na12<n,m,j>, na21<n,m,j> na22<n,m,j> may be generated from the positive sign control signals by inverters either in each PRAC or in PRAU (not shown).

According to some embodiments, the amplitude part Amp <n,m,j> may be separated, thus the parameter calculator 700 may further comprise an **amplitude LUT 708** to store amplitude values Amp<n, m, j> of the amplitude vectors.

According to some embodiments herein, the amplitude LUT 708 further comprises a beam mode control input **BMC** and element address index inputs n, m to control which amplitude values to output depending on element address index n, m and a beam mode. The beam mode may be, e.g. all elements 120 have the same amplitude value, or each element 120 has a different amplitude values base on weighting factors.

According to some embodiments herein, the modulus operator 706 further comprises a compensation input Ɛnm to receive phase compensation parameter and is further configured to correct phase errors caused by amplitude control at different levels.

Turning back to Figure 5, according to some embodiments, each PRAU 500 further comprises a Direct Current (DC) **compensation unit 510** to compensate a DC offset of the phase rotated signal, i.e. the output signals OIp<j>, OIn<j>, OQp<j>, OQn<j>.

As in the conventional variable gain amplifiers and/or phase rotators, there are different DC offsets at output of the amplifier/phase rotation circuitry when the phase rotation angle changes. This problem is solved by the DC compensation unit 510.

Figure 8 shows one example of the DC compensation unit 510, denoted as **compensation unit 800**. The compensation unit 800 comprises a **DC compensation calculator 801, 802** to calculate a DC compensation vector C<j,i> which comprising N1 digital bits, i=1,... N1, as shown in Figure 8 (a) and (b).

The DC compensation unit 800 further comprises a plurality of DC compensation circuits to receive the DC compensation vector. **Figure 8 (c)** shows one of the DC **compensation circuit 803** according to embodiments herein. The DC compensation circuit 803 comprises four switched transconductance branches, each switched transconductance branch comprises one transconductance transistor connected in series with two switching transistors. The sizes of transistors in the transconductance branch are matched to the sizes of transistors in the transconductance branch in the PRAC. The drains of the transconductance transistors in each DC compensation circuit 803 are coupled to the in-phase and quadrature-phase outputs OIp, OIn, OQp, OQn to inject compensation currents to the outputs of the PRAU.

As the total current in the output is proportional to $|\cos(\Psi j)|+|\sin(\Psi j)|$ and it will reach the peak of $\sqrt{2}$ at 45°, and reach the minimum of 1 at 0° and 90°. So the compensation current may be digitally calculated as:

$$C<j>=Amp<j>(\sqrt{2}-|\sin(\Psi j)|-|\cos(\Psi j)|) \qquad (8)$$

Where $Amp<j>$ is the amplitude for the j-th output beam signal. This is implemented in the DC compensation calculators as shown in Figure 8 (a) and (b), which comprise digital adder and subtractor. In Figure 8(a), the DC compensation calculator 801 is configured to generate DC compensation vector C<j> which comprising symmetric coefficients and the compensation is performed for symmetric quadrature signals, for which the reduced size of the phase rotation LUT is used. In Figure 8(b), the DC compensation calculator 802 is configured to generate DC compensation vector C<j> which comprising asymmetric coefficients, for which the full size LUT is used, where the 4 factors A11<n,m,j>, A12<n,m,j>, A21<n,m,j>, A22<n,m,j> may have different values.

Turning back to Figure 3, where the block diagram of an element 120 is shown. According to some embodiments herein, the mixer 123 in each element 120 may be a quadrature homodyne mixer, driven by quadrature local oscillator signals, LO-i, LO-q, for down-converting the amplified multiple radio signals to quadrature baseband signals, or a super heterodyne mixer for down-converting the amplified multiple radio signals to intermediate frequency signals, or a two-stage image rejection mixer where a first stage of

the image rejection mixer is a quadrature mixer which down-converts the amplified multiple radio signals into quadrature intermediate frequency signals, and a second stage of the image rejection mixer down-converts the quadrature intermediate frequency signals to quadrature baseband signals.

According to some embodiments herein, the down converted quadrature baseband signals are filtered by the filter 124, which may comprise quadrature filters Filter I and Filter Q and generate the in-phase and quadrature phase input signals Ip, In, Qp and Qn to the K paralleled PRAU<1>, ...PRAU<j>,... PRAU<K>. The filter 124 may be either passive or active filters.

Figure 9 shows one example of the mixer 123 according to embodiments herein, denoted as a **quadrature mixer 900**. The quadrature mixer 900 comprises a **quadrature mixer core 901** to receive RF signals RFinp, RFinn and LO signals LoIn, LoIp, LoQp, LoQn as in any conventional mixers. Further, the quadrature mixer 900 according to embodiments herein has four output branches. Each output branch comprises a load branch comprising one diode configured loading transistor TLD connected in series with two loading transistors TL1, TL2. The sizes of the loading transistors are matched to the sizes of the transistors in the switched transconductance branch in the PRAC as shown in Figure 6(a).

Figure 10 shows another example of the mixer 123 according to embodiments herein, denoted as a **quadrature mixer 1000**. The quadrature mixer 1000 also comprises a **quadrature mixer core 1010** comprising an **in-phase mixer 10**10 and **quadrature-phase mixer 1020** to receive the RF signals RFinp, RFinn and LO signals LoIn, LoIp, LoQp, LoQn as in any conventional mixers. The quadrature mixer 1000 has four output branches, each output branch comprises a load branch comprising one diode configured loading transistor TLD in series with an inductor Ld. Each in-phase mixer 1010 and quadrature-phase mixer 1020 comprises a tunable capacitor Cd connected between the two output branches. Each in-phase mixer 1010 and quadrature-phase mixer 1020 further comprises two loading transistors TL1, TL2 stacked on top of the two inductors Ld. The sizes of the loading transistors are matched to the sizes of the transistors in the switched transconductance branch in the PRAC as shown in Figure 6 (b).

The inductors Ld and tunable capacitor Cd form an inductive tank circuit which extends the bandwidth of the mixer 1000.

Now turning back to Figures 1 and 2, there are several ways of combining the outputs from the element array 110 to generating the multiple output beam signals. According to some embodiments, when the element array 110 is arranged to form a square, a rectangle or

a cross shape, and is configured to comprise N rows and M columns, or when the element array 110 is configured to comprise N rows, wherein each raw has a different number of elements and is arranged to form a hexagon shape, the jth output signals Out<j> from the elements in one column are combined by connecting together all jth outputs of the elements in said column to generate the jth output of the multiple output beam signals, wherein j=1...K., In these cases, only one column is used.

According to some embodiments, the beamforming receiver 100 may be configured to be in a K beam mode and generate K output beam signals. Then the j-th outputs of each element in the element array 110, i.e. the j-th outputs of all elements in the element array 110, are connected together to generate the jth output of the K output beam signals, where j=1,...K, thereby K output beam signals are generated.

According to some embodiments, the beamforming receiver, when configured in the K beam mode, may further comprise 2*K analog to digital converters connected to the outputs of the K output beam signals for further digital signal processing.

According to some embodiments, the beamforming receiver 100 may be configured to be in a K*M beam mode and generate K multiplied by M output beam signals. Then the j-th outputs of the elements in column m are connected together to generate K output analog signals for each column, where j=1,..., K and m=1,..., M. The beamforming receiver 100 may further comprise, as shown in **Figure 11**, **ADC array 1101** which comprises 2*K*M analog to digital converters to convert the generated K output analog signals for each column to K digital signals for each column.

The beamforming receiver 100 may further comprise a **synchronization unit 1102** to align the K digital signals for each column in time. The beamforming receiver 100 further comprise a **digital signal processor 1103**, **1104** to perform operations on the aligned K digital signals for each column to generate the K*M output beam signals. For example, the synchronized K digital signals are processed by **parallel DSPs 1103** which separate the K digital signal by DSP algorithms, such as 2D-FFTs, a complex weighted lattice FIR filter, or any others alike. The separated K digital signals are then processed by **baseband DSPs 1104** for de-modulating the separated K digital signals.

According to some embodiments, the loading unit 140 in the beamforming receiver 100 may comprise a plurality of switched resistor branches, as shown in **Figure 12**. Each switched resistor branch is connected to one output of a PRAU, e.g. each OIp<j>, OIn<j>, OQp<j>, OQn<j> in the j-th PRAU<j> is connected to a switched resistor branch. The

switched resistor branches are controlled so that some output signals from the PRAUs may be merged as to improve matching and reduce the noise of the PRAUs, or some of PRAUs may be disabled to save power, when a desired number of output beam signals is less than the maximum number of output beam signals available from the beamforming receiver 100.

Figure 13 shows examples of a **beamforming receiver matrix 1300**, in which the beamforming receiver 100 according to embodiments herein may be implemented. The beamforming receiver matrix comprises a plurality of beamforming receivers 100, and may be arranged to form different shapes. For example, as shown in **Figure 13 (a)**, the beamforming receiver matrix is formed in a square or rectangle shape, and may comprise Nr rows and Mc columns, where Nr may or may not equal to Mc. The beamforming receiver matrix may be arranged to form a cross shape as shown in **Figure 13(b)**, where the beamforming receivers 100 at corners of the matrix are omitted. The beamforming receiver matrix may be arranged to form a hexagon shape as shown in **Figure 13(c)**, where each consecutive row has different numbers of the beamforming receivers and is placed with an offset to each other.

According to some embodiments, the beamforming receiver matrix 1300 may further comprise output combiners to combine output signals from the beamforming receivers 100 in baseband, and may further comprise clock distribution networks comprising delay matched transmission lines and delay alignment units.

To summarize, some advantages of the beamforming receiver 100 according to embodiments herein are:

In some embodiments, the beamforming receiver 100 may be used in K-beam analog mode to generate K output beam signals.

In some embodiments, the beamforming receiver 100 may be used in hybrid analog-digital mode to generate K*M output beam signals.

The beamforming receiver 100 can be implemented with relatively low power consumption and high accuracy. For example, in some embodiments described above, the phase rotator and amplitude control unit in the beamforming receiver 100 comprises a plurality N1 of PRAC and each PRAC comprises a plurality of switched transconductance branches. The switched transconductance branches can be controlled in a way that facilitates an implementation with relatively high accuracy in phase rotation and amplitude control and low power consumption.

The beamforming receiver 100 can be implemented with ADCs separated from RF integrated circuits, which makes it easier to design and implement, and also has relatively low cost compared with pure digital beamforming.

The beamforming receiver 100 can be implemented to occupy a relatively small area.

The beamforming receiver 100 can be implemented to have relatively good linearity.

The beamforming receiver 100 and the beamforming receiver matrix 1300 according to embodiments herein may be employed in various wireless communication devices. **Figure 14** shows a block diagram for **a wireless communication device 1400**, which may be, e.g. a base station or a wireless terminal, such as a mobile phone, machine-type communication device, a computer or tablet computer or other device comprising a cellular data modem etc.. The wireless communication device 1400 may comprise other units, where **a processing unit 1410** is shown, which may interactive with the controller 701 in the parameter calculator 700 for different parameter settings or operating modes.

Those skilled in the art will understand that transistors in the PRACs, in the DC compensation circuit 803, in the quadrature mixer 900, 1000 as shown in Figures 6, 8, 9, 10, may be any types of transistors, e.g. Field-Effect Transistors (FET), Metal–Oxide–Semiconductor FET (MOSFET), Junction FET (JFET), or Bipolar Junction Transistors (BJT) etc.

When using the word "comprise" or “comprising” it shall be interpreted as non- limiting, i.e. meaning "consist at least of".

The embodiments herein are not limited to the above described preferred embodiments. Various alternatives, modifications and equivalents may be used. Therefore, the above embodiments should not be taken as limiting the scope of the invention, which is defined by the appending claims.

CLAIMS

1. A beamforming receiver (100) for receiving multiple radio signals and generating multiple output beam signals, the beamforming receiver (100) comprising:
multiple beam parameter inputs (130) to receive multiple beam parameters;
an element array (110) comprising a plurality of elements (120), wherein each element (120) comprises:
an antenna (121) to receive the multiple radio signals;
an amplifier (122) to amplify the received multiple radio signals;
a mixer (123) to down-convert the amplified multiple radio signals and generate in-phase and quadrature phase signals;
a filter (124) to filter the generated in-phase and quadrature phase signals and generate in-phase and quadrature phase input signals;
a plurality K of Phase Rotator and Amplitude control Unit, PRAU, (PRAU<1>, ...PRAU<j>,... PRAU<K>) configured to perform phase rotation and amplitude control of the in-phase and quadrature phase input signals based on phase and amplitude control parameters and generate multiple analog output signals (Out<1>, ... Out<j>, ...Out<K>) with individual phase shifts (ψ1, ... ψj, ...ψK); and
a parameter calculator (125, 700) to generate the phase and amplitude control parameters from the multiple beam parameters which are related to K directions of the multiple radio signals.

2. The beamforming receiver (100) according to claim 1, wherein the multiple beam parameters comprise azimuth vector, **A1,..., AK**, elevation vector, **E1,..., EK**, and amplitude vector, **Amp1,..., AmpK.**

3. The beamforming receiver (100) according to any one of claims 1-2, wherein the element array (110) is arranged to form a square, a rectangle or a cross shape, and is configured to comprise N rows and M columns, wherein the j-th output signals (Out<j>) from the elements in one column are combined by connecting together all j-th outputs of the elements in said column to generate the j-th output of the multiple output beam signals, wherein j=1...K.

4. The beamforming receiver (100) according to any one of claims 1-2, wherein the element array (110) is configured to comprise N rows, wherein each consecutive row has a different number of elements and is arranged to form a hexagon shape, and

wherein the j-th output signals (Out<j>) from the elements in one column are combined by connecting together all j-th outputs of the elements in said column to generate the j-th output of the multiple output beam signals, wherein j=1...K.

5. The beamforming receiver (100) according to any one of claims 1-4, wherein each PRAU (500, PRAU<1>, ...PRAU<j>,... PRAU<K>) is configured to perform phase rotation and amplitude control of the in-phase and quadrature phase input signals and generate one output (Out<j>) of the multiple analog output signals with an individual phase shift (ψj), and wherein each PRAU (PRAU<1>, ...PRAU<j>,... PRAU<K>) comprises:

a plurality N1 of Phase Rotator and Amplitude control Circuits, PRAC (PRAC<1>,...PRAC<i>,...PRAC<N1>), wherein each PRAC comprises:

an input port comprising in-phase and quadrature-phase inputs (Ip, In, Qp, Qn) to receive the in-phase and quadrature phase input signals;

an output port comprising in-phase and quadrature-phase outputs (OIp, OIn, OQp, OQn);

control inputs to receive the phase and amplitude control parameters, wherein the phase and amplitude control parameters comprises sign control signals (pa11, pa12, pa21, pa22, na11, na12, na21, na22) and positive amplitude coefficient signals (a11<i>, a12<i>, a21<i>, a22<i>), each positive amplitude coefficient signal has N1 digital bits; and each PRAC further comprises:

a plurality of switched transconductance branches, wherein each switched transconductance branch comprises one transconductance transistor connected in series with two switching transistors, and wherein

a gate of one switching transistor is coupled to one of the sign control signals (pa11, pa12, pa21, pa22, na11, na12, na21 na22),

a gate of another switching transistor is coupled to one of the positive amplitude coefficient signals (a11<i>, a12<i>, a21<i>, a22<i>),

a gate of the transconductance transistor is coupled to one of the in-phase and quadrature-phase inputs (Ip, In; Qp, Qn), and

a drain of the transconductance transistor is coupled to one of the in-phase and quadrature-phase outputs (OIp, OIn, OQp, OQn); and wherein

each PRAC (PRAC<1>,...PRAC<i>,...PRAC<N1>) is configured to receive one bit of the positive amplitude coefficient signals (a11<i>, a12<i>, a21<i>, a22<i>), and wherein

each of the multiple analog output signals (Out<j>) comprises in-phase and quadrature-phase output signals (OIp<j>, OIn<j>, OQp<j>, OQn<j>), and wherein

the in-phase outputs (OIp, OIn) from each PRAC (PRAC<1>,...PRAC<i>,...PRAC<N1>) are arranged to be combined to generate the in-phase output signal (OIp<j>, OIn<j>) of the output signal (Out<j>), and the quadrature-phase outputs (OQp, OQn) from each PRAC (PRAC<1>,...PRAC<i>,...PRAC<N1>) are arranged to be combined to generate the quadrature-phase output signal (OQp<j>, OQn<j>) of the output signal (Out<j>), wherein j=1,...K.

6. The beamforming receiver (100) according to any one of claims 1-5, wherein the parameter calculator (125, 700) comprises:

a controller (701) configured to change index j for the individual phase shifts (ψj), wherein j=1, 2...K;

a plurality of multipliers (702) comprising element address index inputs (n, m), multiple angel parameters inputs to receive the azimuth and elevation vectors (Ak, Ek) and compensation parameter inputs to receive compensation parameters (fc, td, tc, ΔTemp);

a phase rotation Look Up Table, LUT (703, 704), confiugred to store sinusoid values of the individual phase shifts (ψj);

an amplitude LUT (708) configured to store amplitude values (Amp<n, m, j>) of the amplitude vectors; and

a modulus operator (706).

7. The beamforming receiver (100) according to claim 6, wherein the phase rotation LUT (703) is a full table comprising sinusoid values of phases from 0 to 360 in degree or 0 to 2π in rad or a half table comprising sinusoid values of phases from 0 to 180 in degree or 0 to π in rad.

8. The beamforming receiver (100) according to claim 6, wherein the phase rotation LUT (704) is a quart of the full table comprising sinusoid values of phases from 0 to 90 in degree, or 0 to π/2 in rad, and wherein the parameter calculator (125, 700) further comprises a swap unit (706).

9. The beamforming receiver (100) according to any one of claims 6-8, wherein the modulus operator (706) further comprises a compensation input to receive a phase compensation parameter (Ɛnm) and is further configured to correct phase errors caused by amplitude control at different levels based on the phase compensation parameter (Ɛnm) .

10. The beamforming receiver (100) according to any one of claims 6-9, wherein the amplitude LUT (708) further comprises a beam mode control input and element address index inputs (n, m) to control which amplitude values to output depending on element address index (n, m) and a beam mode.

11. The beamforming receiver (100) according to any one of claims 1-10, wherein the mixer (123) comprises one of a quadrature homodyne mixer for down-converting the amplified multiple radio signals to quadrature baseband signals, a super heterodyne mixer for down-converting the amplified multiple radio signals to intermediate frequency signals, or a two-stage image rejection mixer where a first stage of the image rejection mixer is a quadrature mixer which down-converts the amplified multiple radio signals into quadrature intermediate frequency signals, and a second stage of the image rejection mixer down-converts the quadrature intermediate frequency signals to quadrature baseband signals.

12. The beamforming receiver (100) according to any one of claims 1-11, wherein the filter (124) comprises passive filters or active filters.

13. The beamforming receiver (100) according to any one of claims 1-12, wherein the mixer (123) comprises inductive tank circuits comprising inductors (Ld) and tunable capacitor (Cd) to extend bandwidth of the mixer (123).

14. The beamforming receiver (100) according to any one of claims 1-13, wherein the beamforming receiver (100) is configured to be in a K beam mode to generate K output beam signals, and wherein the j-th outputs of each element in the element array (110) are connected together to generate the j-th output of the K output beam signals, wherein j=1,...K, thereby K output beam signals are generated.

15. The beamforming receiver (100) according to claim 14, wherein the beamforming receiver (100) further comprises 2*K analog to digital converters connected to outputs of the K output beam signals.

16. The beamforming receiver (100) according to any one of claims 1-13, wherein the beamforming receiver (100) is configured to be in a K*M beam mode to generate K multiplied by by M output beam signals, and wherein the j-th outputs of the elements in column m are connected together to generate K output analog signals for each column, where j=1,...K and m=1,...M; and wherein the beamforming receiver (100) further comprises:

an analog to digital array (1101) comprising 2*K*M analog to digital converters to convert the generated K output analog signals for each column to K digital signals for each column;

a synchronization unit (1102) to align the K digital signals for each column in time; and

a digital signal processor (1103, 1104) to perform operations on the aligned K digital signals for each column to generate the K*M output beam signals.

17. The beamforming receiver (100) according to any one of claims 1-16, wherein the beamforming receiver (100) further comprises a loading unit (140) comprising a plurality of switched resistor branches, each connected to one output of a PRAU, wherein the switched resistor branches are controlled so that some output signals from the PRAUs may be merged as to improve mismatch and reduce the noise of the PRAUs, or some of PRAUs may be disabled to save power, when a desired number of output beam signals is less than the maximum number of output beam signals available from the beamforming receiver (100).

18. The beamforming receiver (100) according to any one of claims 1-17, further comprises reference clock generating and splitting circuit (150) to generate and distribute reference clock signals for each element (120).

19. A beamforming receiver matrix comprising multiple beamforming receivers (100) according to any one of claims 1-17, wherein the beamforming receiver matrix comprises Nr rows and Mc columns and is arranged to form a square, a rectangle or a cross shape, wherein Mc and Nr are positive integers.

20. A beamforming receiver matrix comprising multiple beamforming receivers (100) according to any one of claims 1-17, wherein the beamforming receiver matrix comprises Nr rows and Mc columns, and wherein each consecutive row has a

different numbers of beamforming receivers and is placed with an offset to each other, thereby form a hexagon shape.

21. The beamforming receiver matrix according to claims 19 or 20, further comprising output combiners to combine output signals from the beamforming receivers (100) in baseband, and clock distribution networks comprising delay matched transmission lines and delay alignment units.

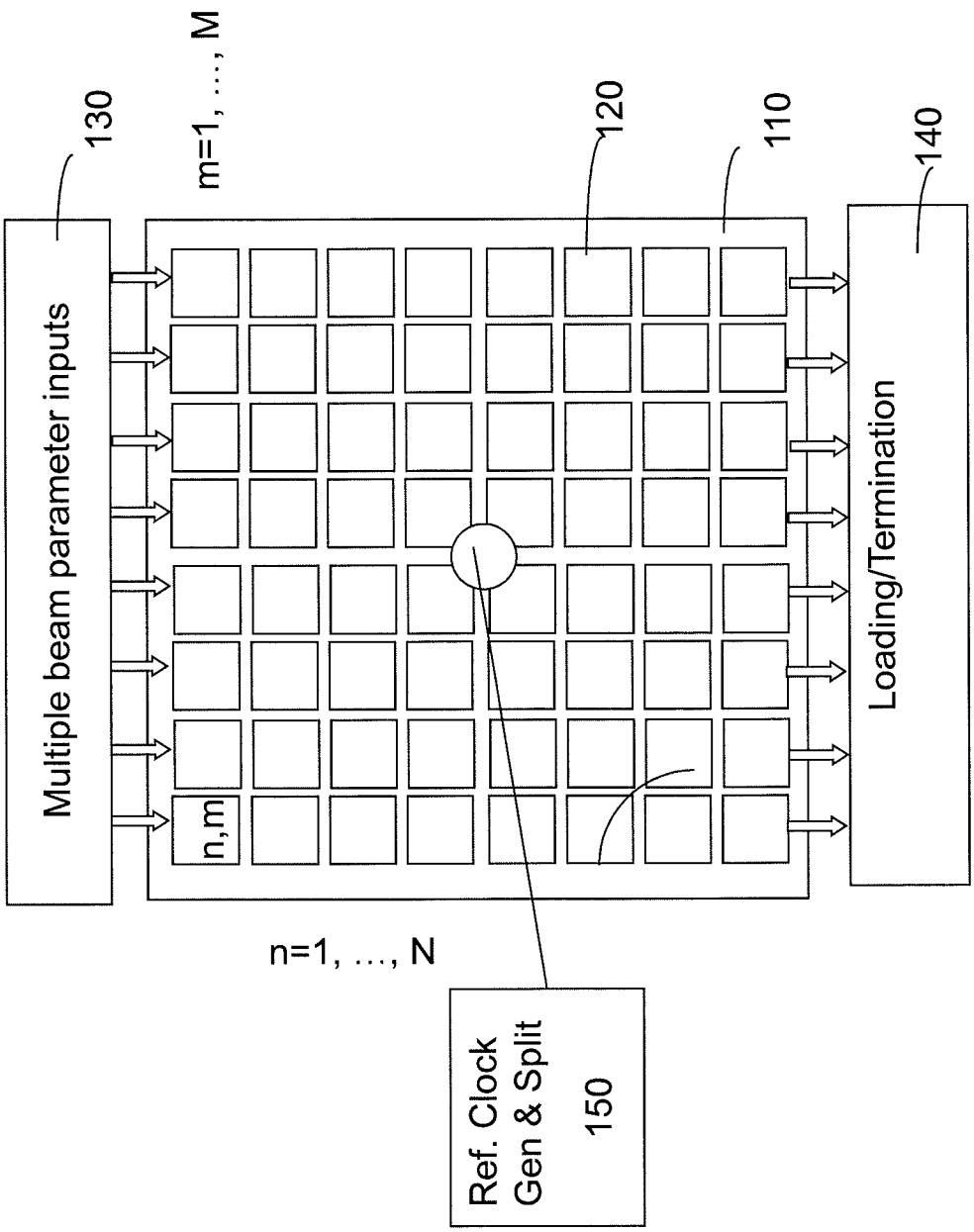

100
130
m=1, ..., M
120
110
140
Multiple beam parameter inputs
n,m
Loading/Termination
n=1, ..., N
Ref. Clock Gen & Split
150

Fig. 1

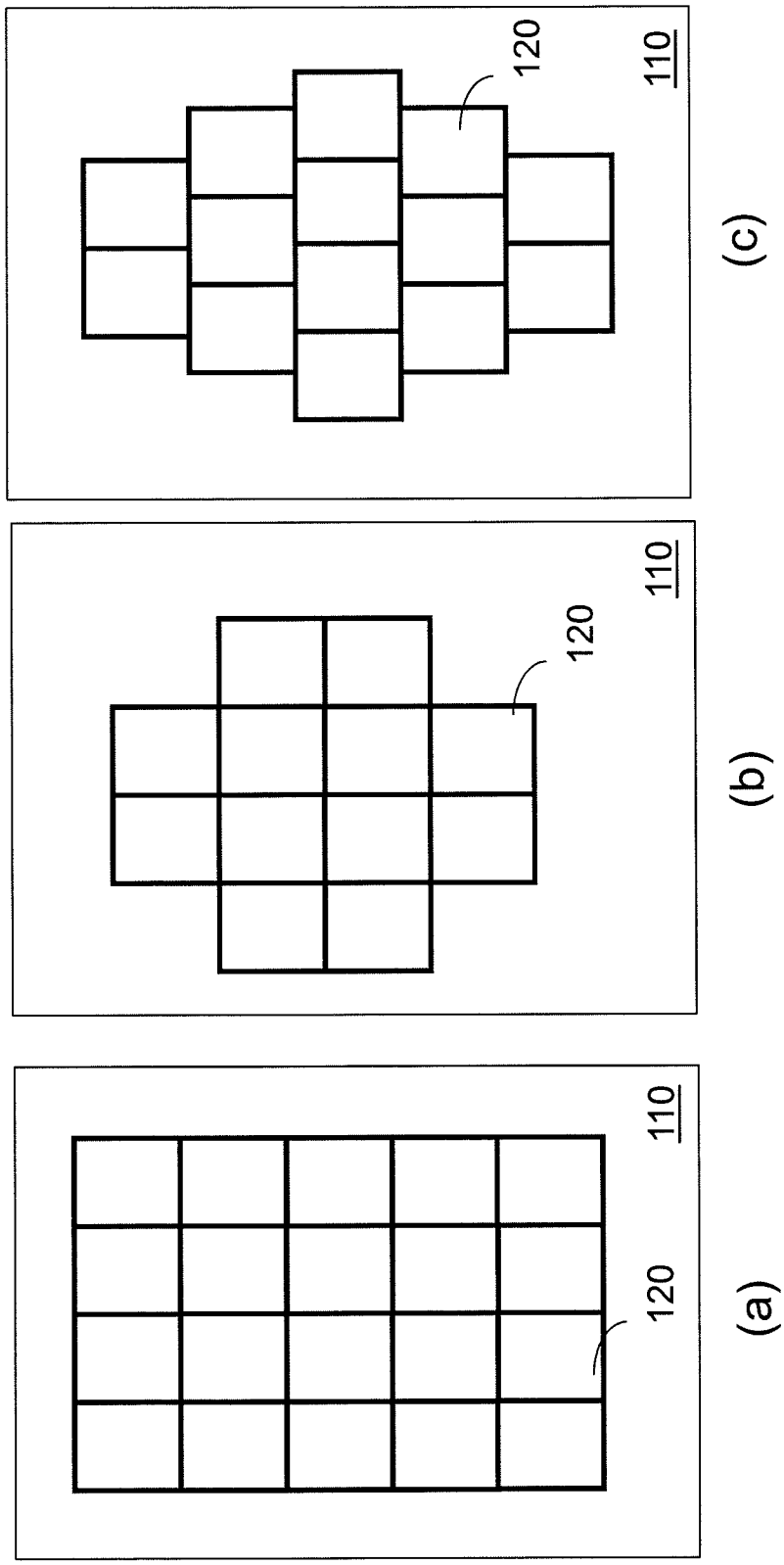
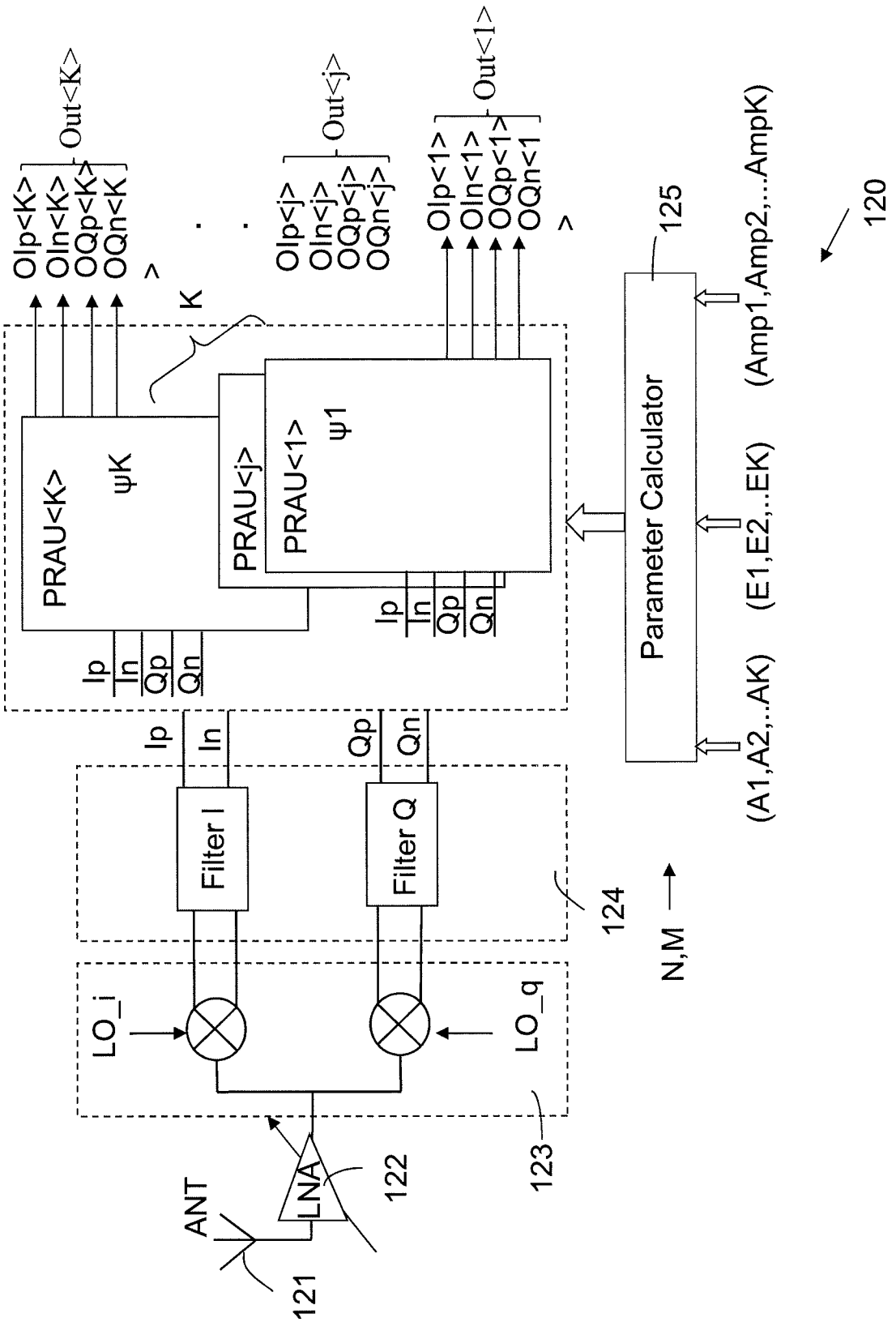


Fig. 2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LO_q
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Filter Q
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Qn
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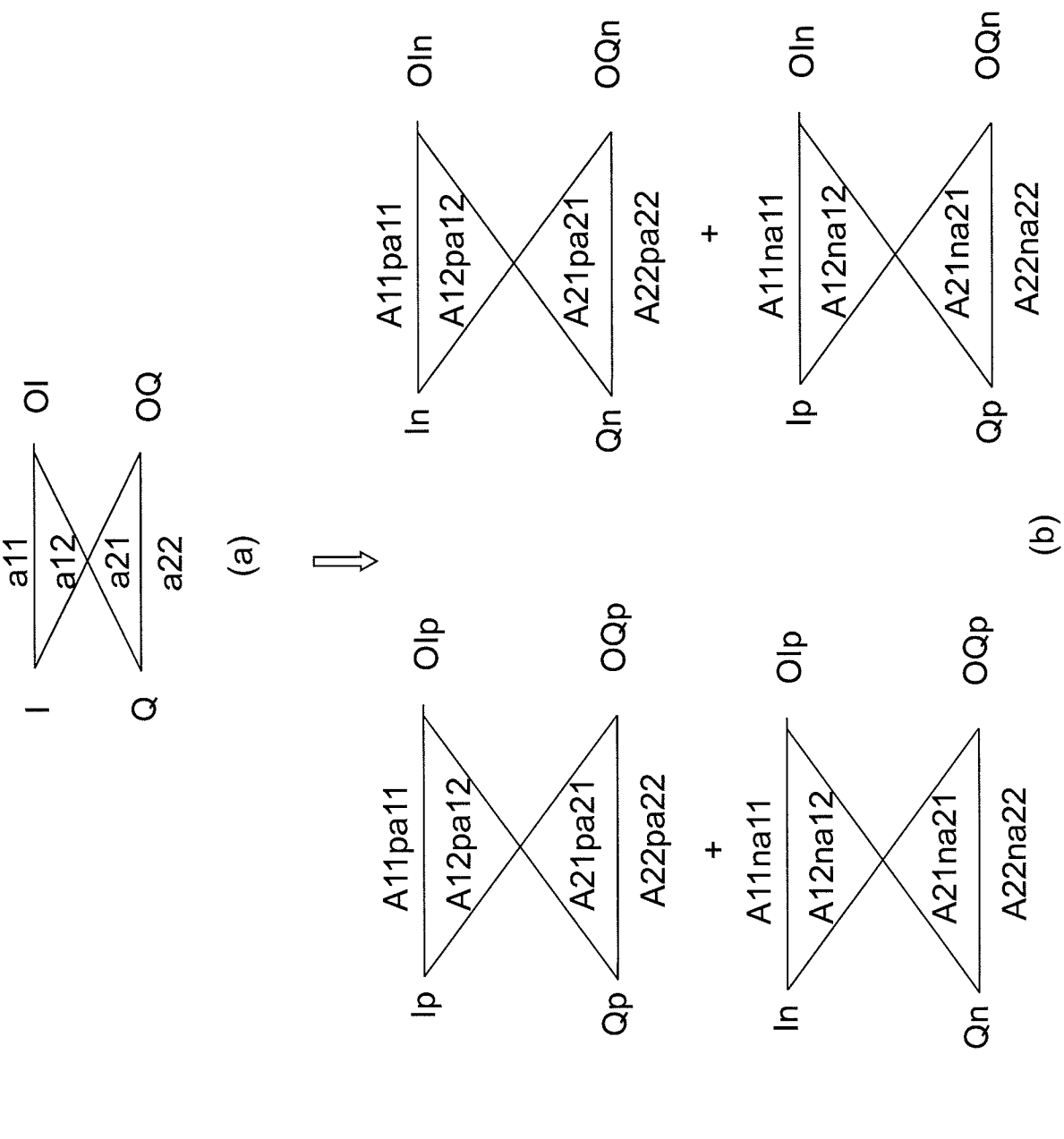
Oln<j>
OQp<j>
OQn<j>
Out<j>
Olp<1>
Oln<1>
OQp<1>
OQn<1
Out<1>
Parameter Calculator
125
120
(A1,A2,..AK)
(E1,E2,..EK)
(Amp1,Amp2,...AmpK)
N,M

Fig. 3


I
Q
OI
OQ
a11
a12
a21
a22
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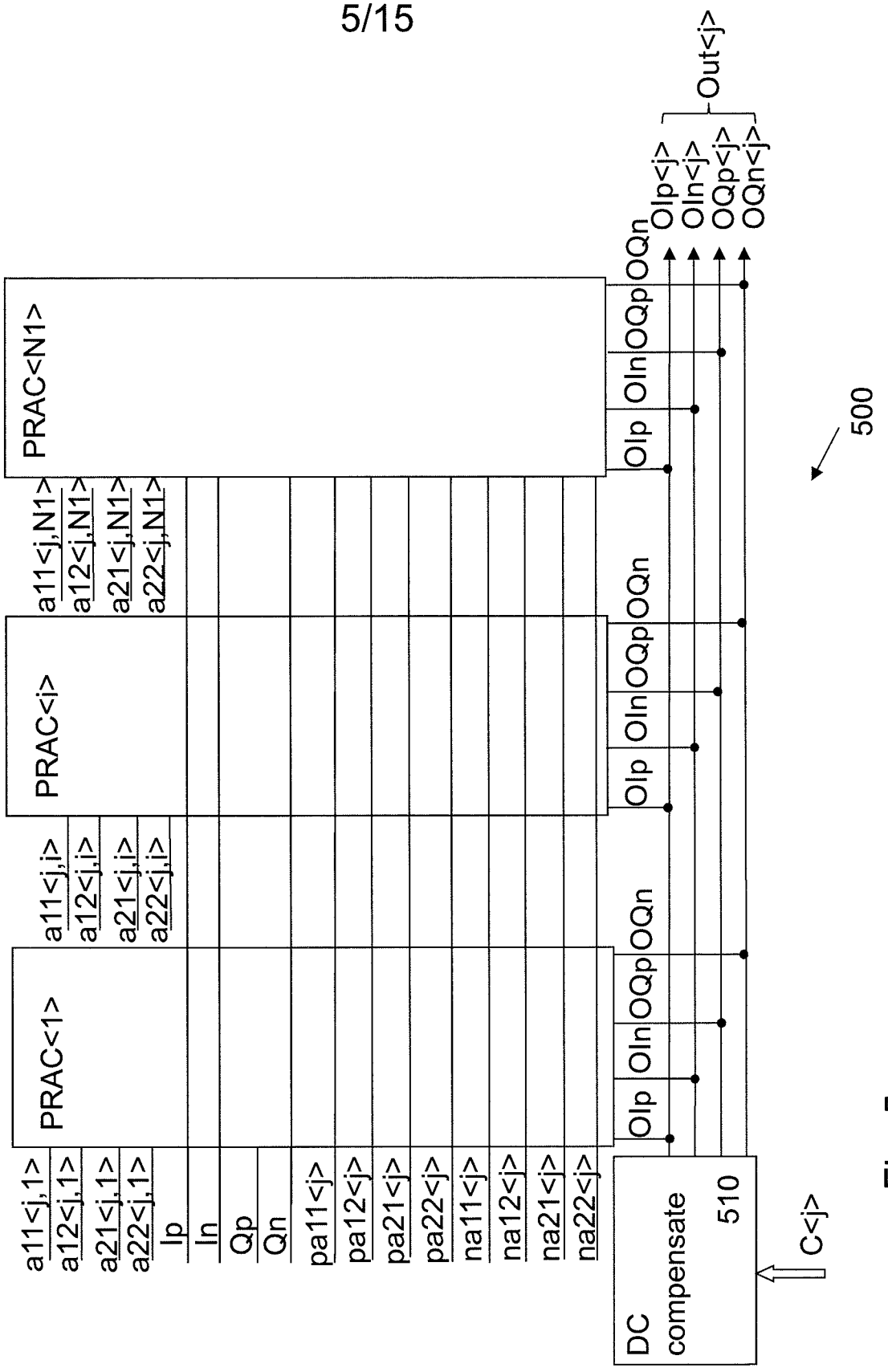
Ip
Qp
OIp
OQp
A11pa11
A12pa12
A21pa21
A22pa22
+
In
Qn
OIn
OQn
A11na11
A12na12
A21na21
A22na22
(b)

Fig. 4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a22<j,1>
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In
Qp
Qn
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pa12<j>
pa21<j>
pa22<j>
na11<j>
na12<j>
na21<j>
na22<j>
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PRAC<N1>
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a22<j,i>
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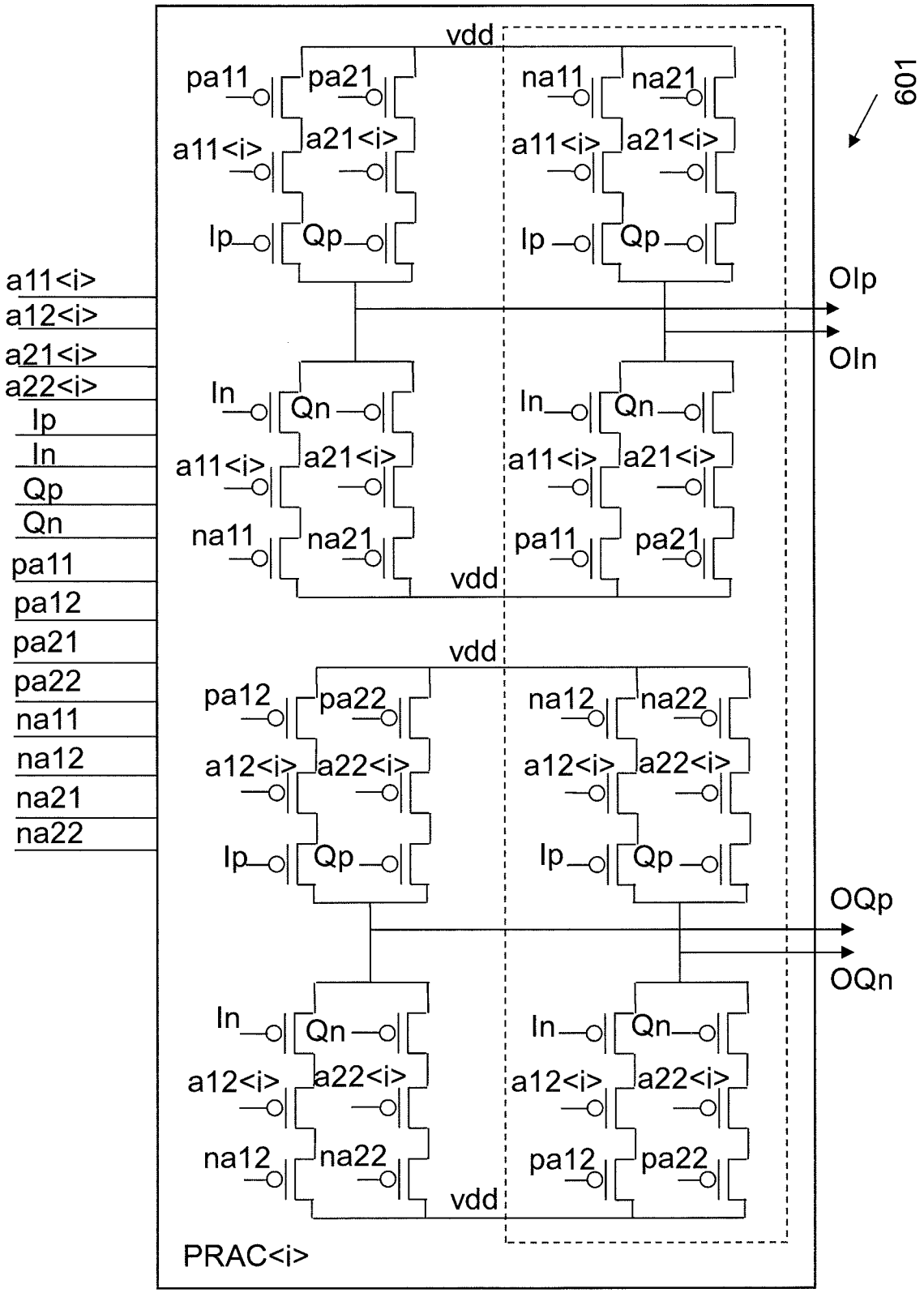
a12<j,N1>
a21<j,N1>
a22<j,N1>
OIp
OIn
OQp
OQn
Out<j>
OIp<j>
OIn<j>
OQp<j>
OQn<j>
DC compensate
510
C<j>
500

Fig. 5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pa21
na11
na21
a11<i>
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Ip
Qp
601
a11<i>
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a22<i>
Ip
In
Qp
Qn
pa11
pa12
pa21
pa22
na11
na12
na21
na22
OIp
OIn
In
Qn
na11
na21
pa11
pa21
vdd
pa12
pa22
na12
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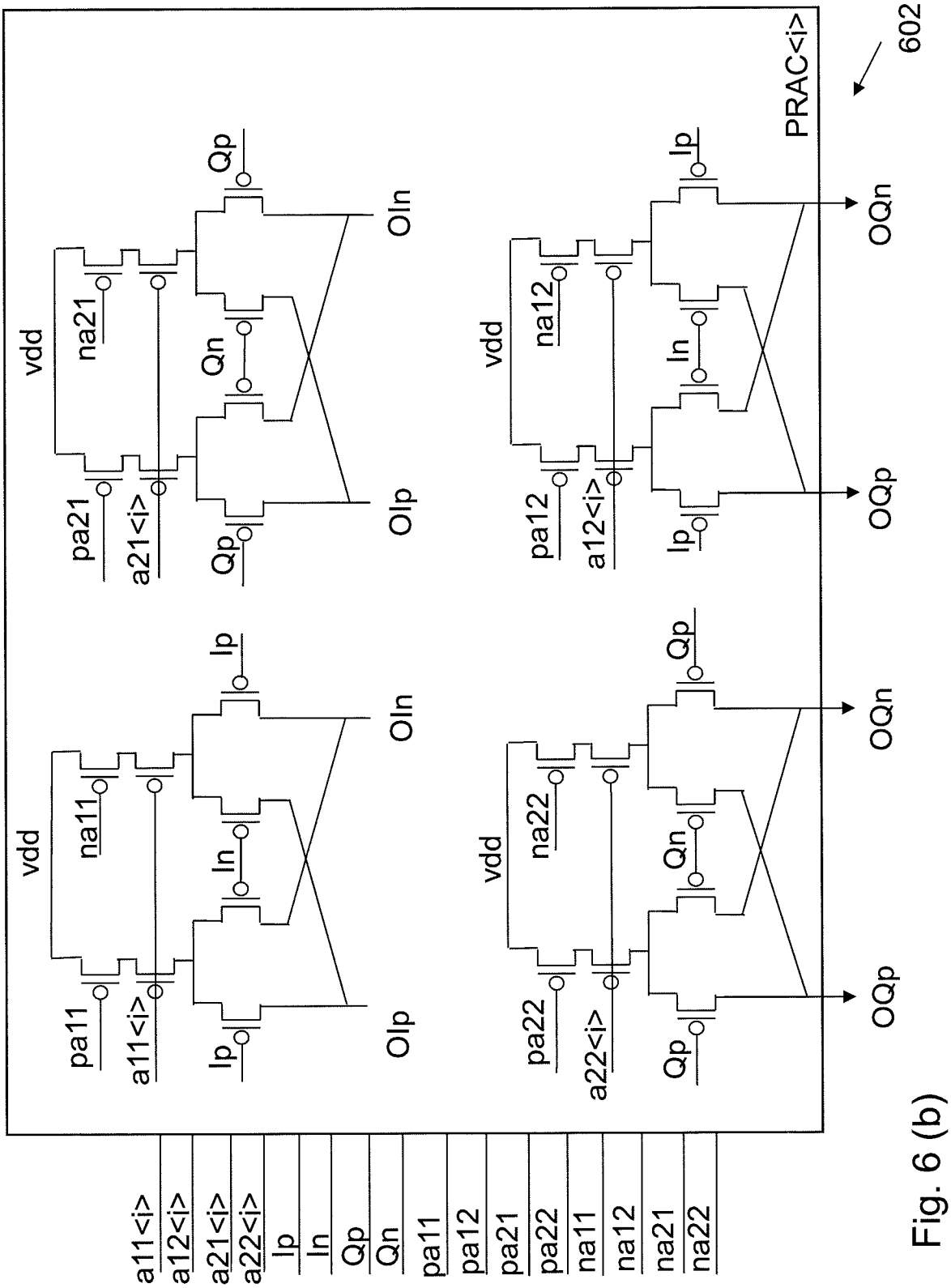
a22<i>
OQp
OQn
na12
na22
pa12
pa22
PRAC<i>

Fig. 6 (a)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a12<i>
a21<i>
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Ip
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Qn
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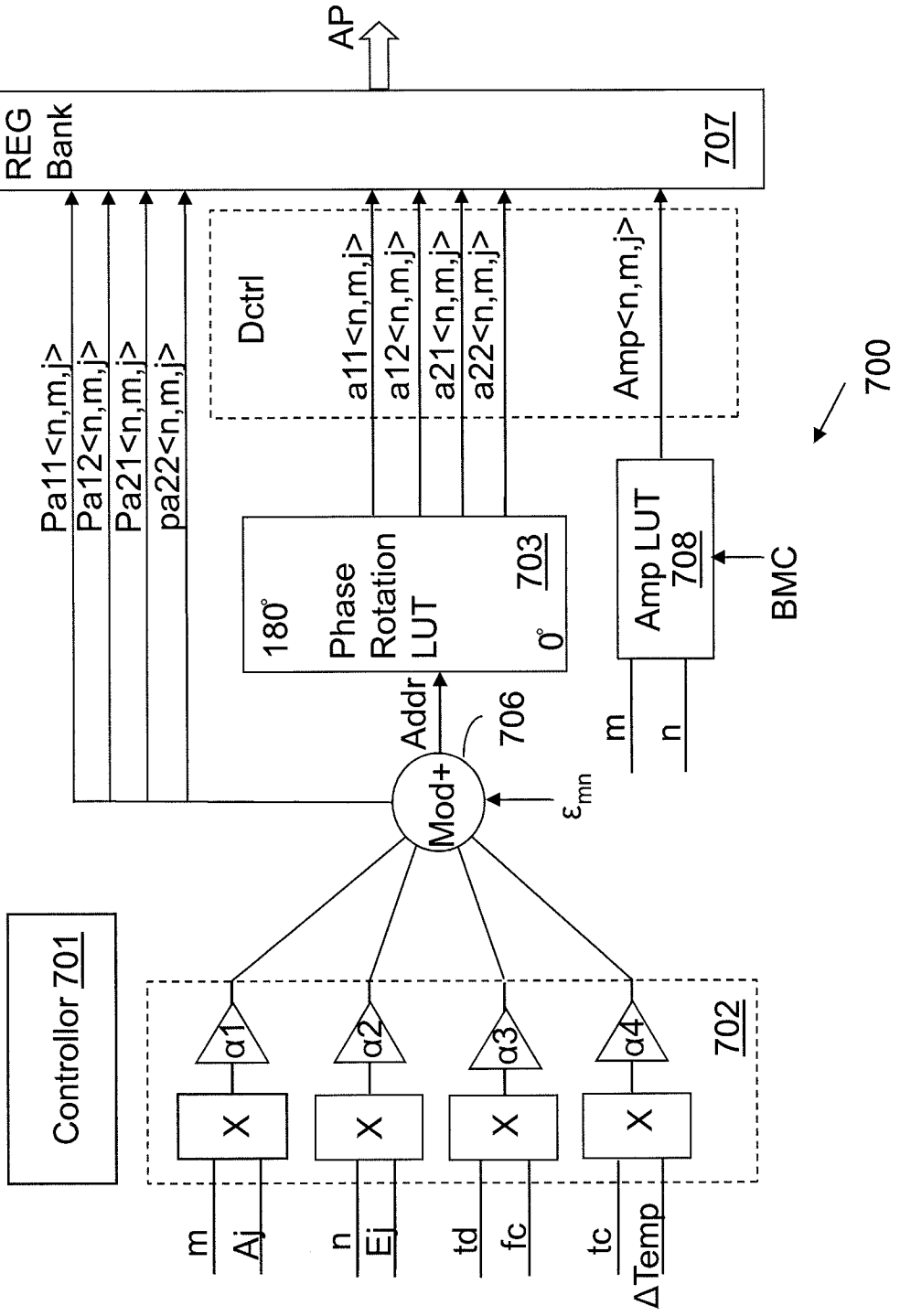
pa12
pa21
pa22
na11
na12
na21
na22
OIn
OIp
OQn
OQp

Fig. 6 (b)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REG Bank
707
Dctrl
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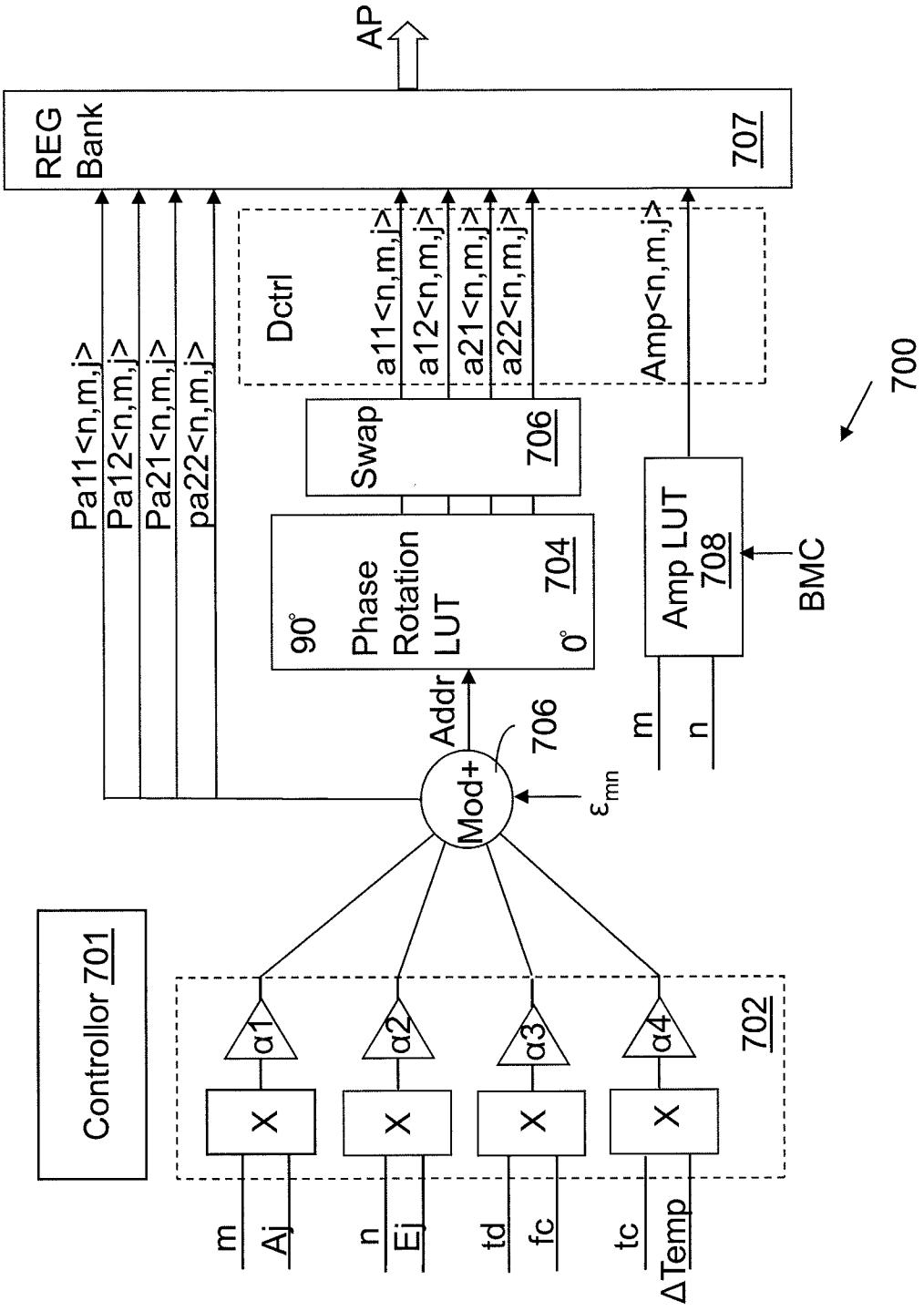
a12<n,m,j>
a21<n,m,j>
a22<n,m,j>
Amp<n,m,j>
Pa11<n,m,j>
Pa12<n,m,j>
Pa21<n,m,j>
pa22<n,m,j>
700
180°
Phase Rotation LUT
703
0°
Amp LUT
708
BMC
Addr
706
m
n
Mod+
ε_{mn}
Controllor 701
α1
α2
α3
α4
X
702
m
Aj
n
Ej
td
fc
tc
ΔTemp

Fig. 7 (a)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REG Bank
707
Dctrl
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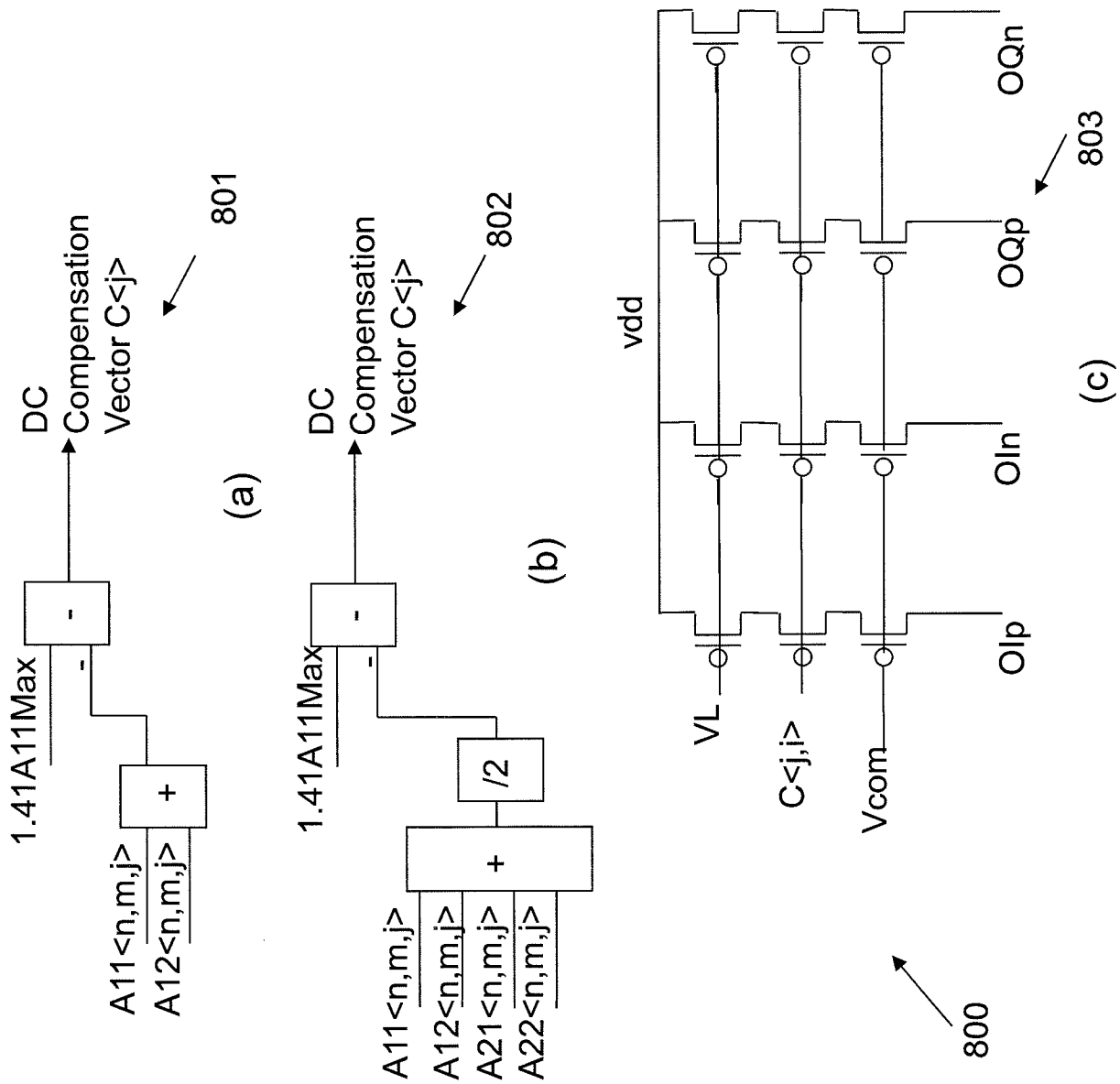
Pa12<n,m,j>
Pa21<n,m,j>
pa22<n,m,j>
Swap
706
90°
Phase Rotation LUT
704
0°
Amp LUT
708
BMC
700
Addr
706
Mod+
ε_{mn}
m
n
Controllor 701
α1
α2
α3
α4
X
X
X
X
702
m
Aj
n
Ej
td
fc
tc
ΔTemp

Fig. 7 (b)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Compensation
Vector C<j>
801
(a)
1.41A11Max
-
-
+
A11<n,m,j>
A12<n,m,j>
DC
Compensation
Vector C<j>
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(b)
1.41A11Max
-
-
/2
+
A11<n,m,j>
A12<n,m,j>
A21<n,m,j>
A22<n,m,j>
vdd
OQn
OQp
803
OIn
OIp
(c)
VL
C<j,i>
Vcom
800

Fig. 8

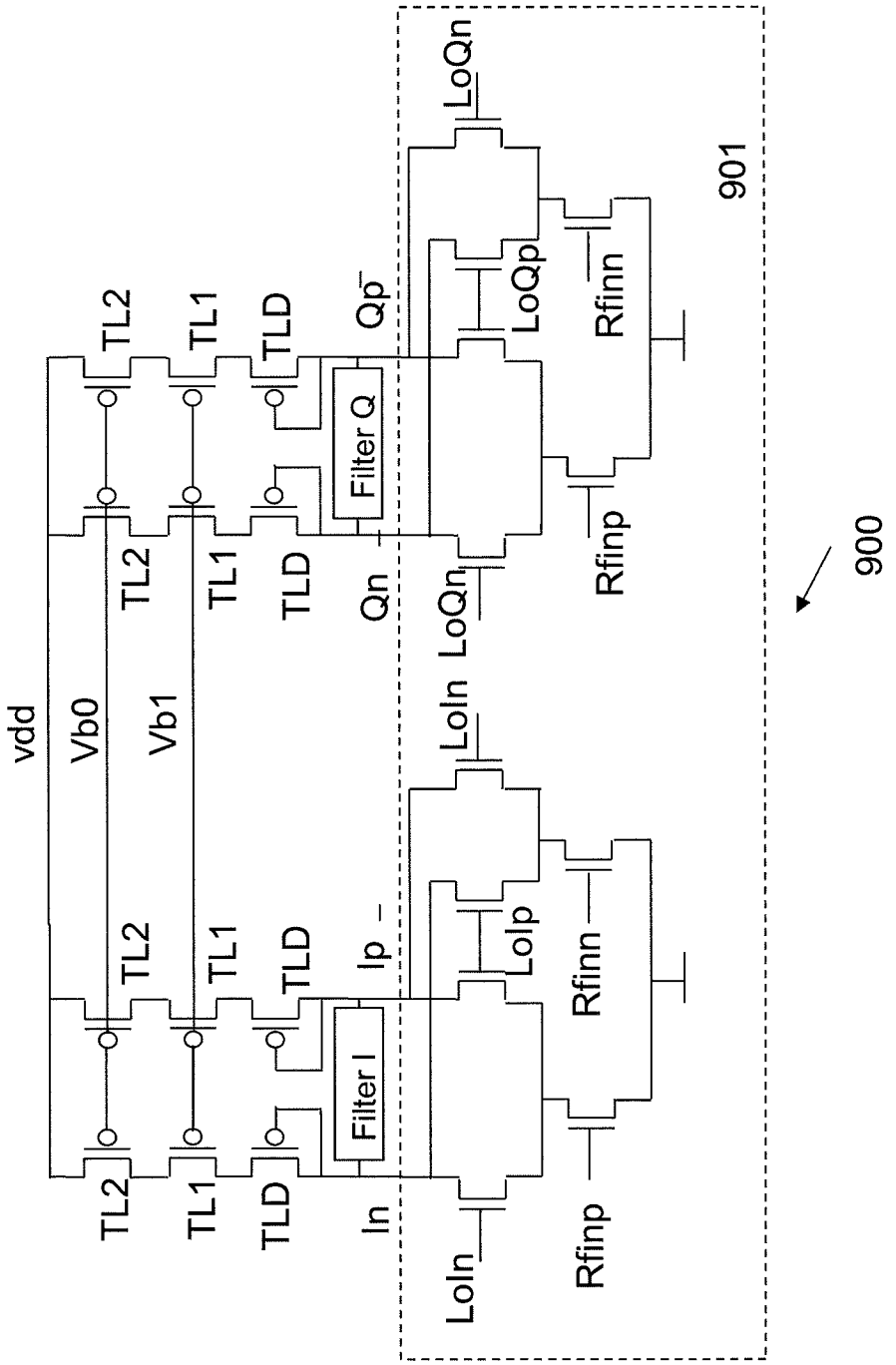
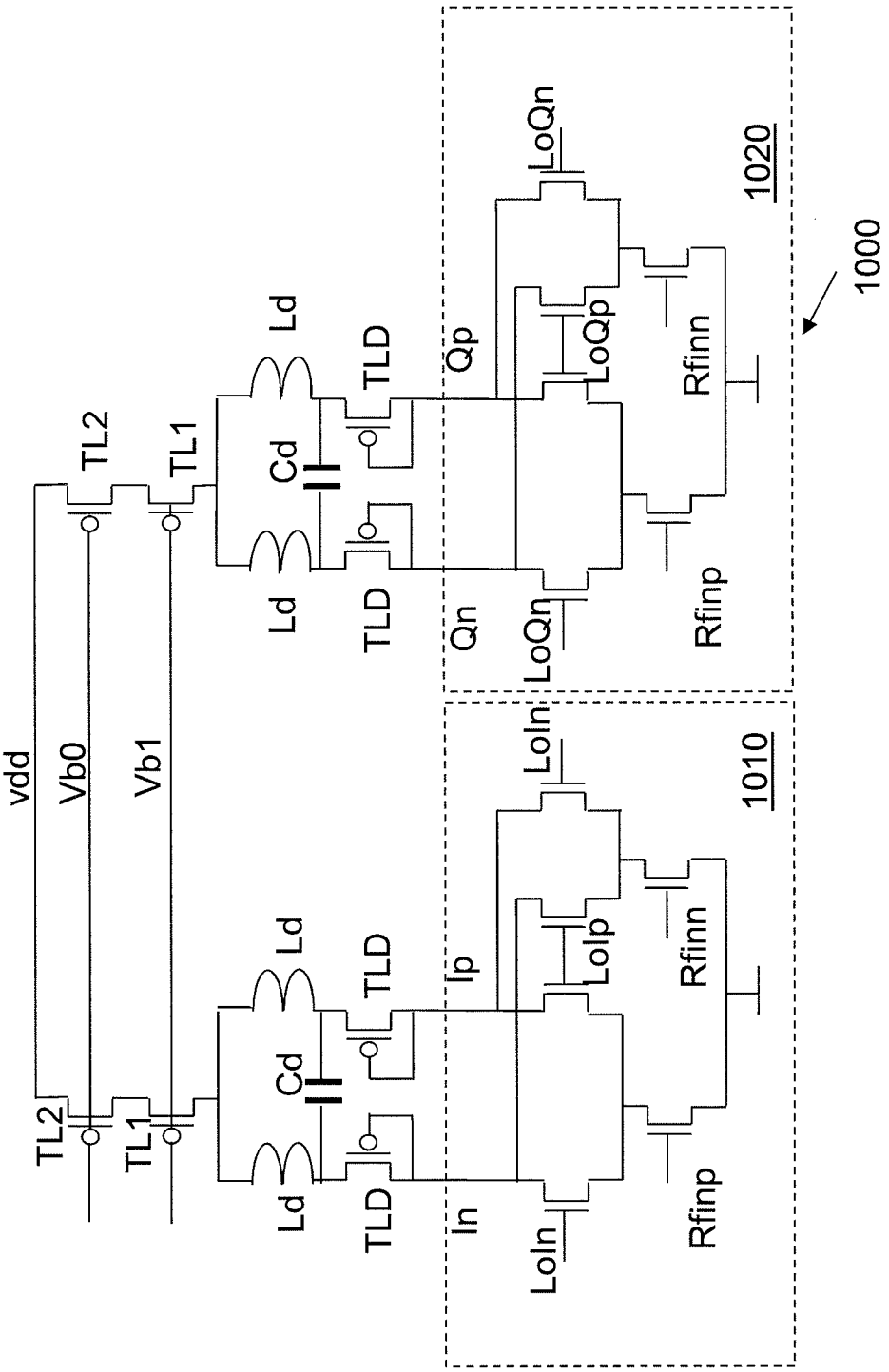

vdd
Vb0
Vb1
TL2
TL1
TLD
Filter Q
Filter I
Qp
Qn
Ip
In
LoQn
LoQp
LoIn
LoIp
Rfinn
Rfinp
901
900

Fig. 9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1020
1010
vdd
Vb0
Vb1
TL2
TL1
Ld
Cd
TLD
Qp
Qn
Ip
In
LoQp
LoQn
LoIp
LoIn
Rfinn
Rfinp

Fig. 10

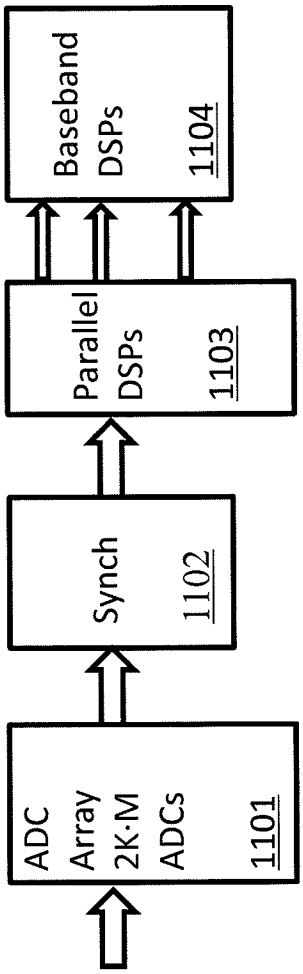
ADC
Array
2K·M
ADCs
1101
Synch
1102
Parallel
DSPs
1103
Baseband
DSPs
1104

Fig. 11

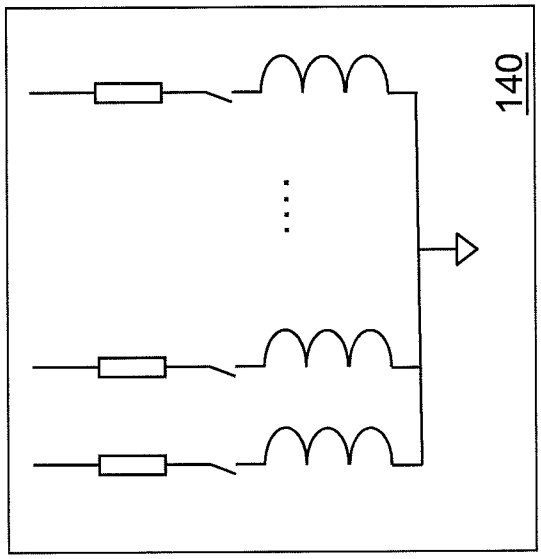
140

Fig. 12

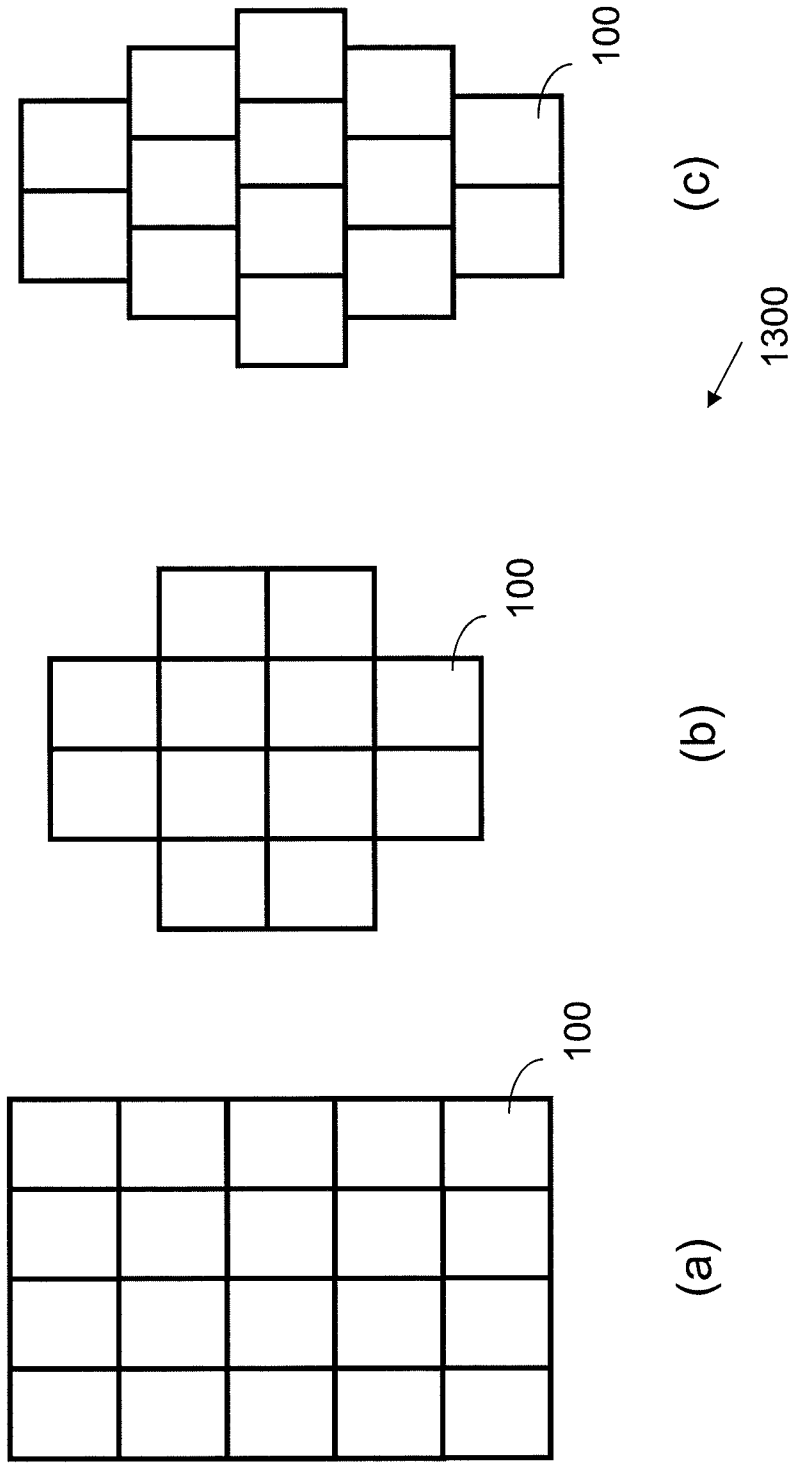

Fig. 13

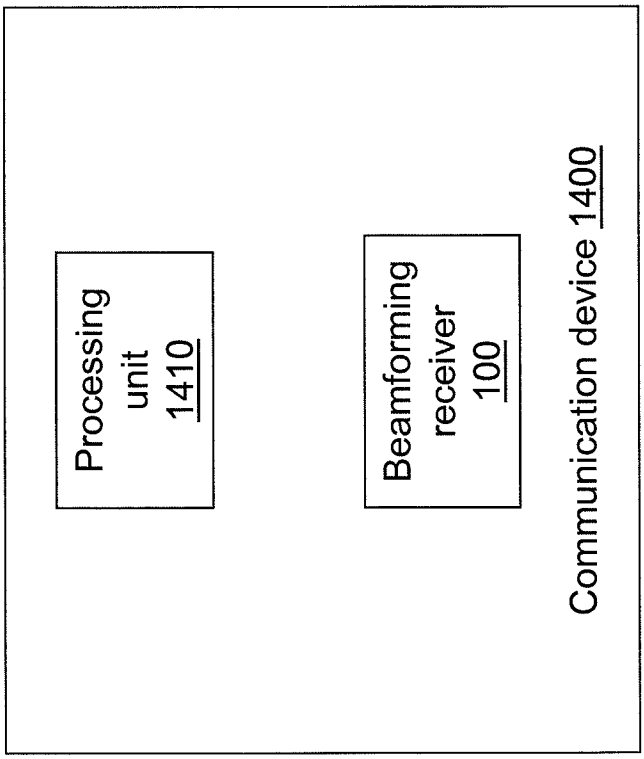
Communication device 1400
Beamforming receiver 100
Processing unit 1410

Fig. 14

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/055809

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B7/04 H04B7/08 H04B1/00 H01Q3/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B H01Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	SEONG-SIK JEON ET AL: "A Novel Smart Antenna System Implementation for Broad-Band Wireless Communications", IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 50, no. 5, 1 May 2002 (2002-05-01), XP011068529, ISSN: 0018-926X page 601 - page 602; figures 1, 2a,2b -----	1-4,12, 18-21
Y	WO 2012/098437 A1 (FREESCALE SEMICONDUCTOR INC [US]; DEHLINK BERNHARD [DE]; TROTTA SAVERI) 26 July 2012 (2012-07-26) pages 4-6; figure 6 -----	1-4,12, 18-21

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 November 2015	09/02/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Franz, Volker

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/055809

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 565 873 A (DEAN STUART J [CA]) 15 October 1996 (1996-10-15) column 5; figure 6a -----	2
Y	US 2014/354499 A1 (LEGAY HERVÉ [FR] ET AL) 4 December 2014 (2014-12-04) paragraphs [0055], [0085]; figures 1a,1b,7a,7b -----	3,4,20

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2015/055809

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-4, 12, 18-21

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-4, 12, 18-21

The receiver comprises a filter to filter the generated in-phase and quadrature phase signals and generate in-phase and quadrature phase input signals.
The multiple beam parameters comprise azimuth vector, elevation vector, amplitude vector.
The element array is arranged to form a square, a rectangle or cross shape and is configured to comprise N rows and M columns.
Each consecutive row has a different number of elements and is arranges to form a hexagon shape.

1.1. claims: 1, 12, 18, 19

The receiver comprises a filter to filter the generated in-phase and quadrature phase signals and generate in-phase and quadrature phase input signals.

1.2. claims: 2-4, 20, 21

The multiple beam parameters comprise azimuth vector, elevation vector, amplitude vector.
The element array is arranged to form a square, a rectangle or cross shape and is configured to comprise N rows and M columns.
Each consecutive row has a different number of elements and is arranges to form a hexagon shape.

---

2. claim: 5

Each Phase Rotator and Amplitude Control Circuits, PRAC, comprises
I and Q input and output ports and a plurality of switched transconductance branches comprising one transconductance transistor in series with two switching transistors.

---

3. claims: 6-10

The parameter calculator comprises a plurality of multipliers, compensation parameter inputs, phase rotation loop up table, LUT, amplitude LUT and modulus operator.

---

4. claims: 11, 13

The mixer comprises one of a quadrature homodyne mixer, super heterodyne mixer, two-stageimage rejection mixer.
The mixer comprises inductive tank circuits and tunable capacitor to extend bandwidth of the mixer.

---

5. claims: 14-17

The beamforming receiver is configured to be in a K beam mode.
The beamforming receiver is configured to be in a K x M beam mode to generate K multiplied by by M output beam signals, and wherein the j-th outputs of the elements in column m are connected together to generate K output analog signals for each column, where j=1,...K and m=1,...M; and wherein the beamforming receiver further comprises: an analog to digital array comprising 2 x K x M analog to digital converters to convert the generated K output analog signals for each column to K digital signals for each column

---

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2015/055809

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2012098437 A1	26-07-2012	CN 103329004 A	25-09-2013
		EP 2666033 A1	27-11-2013
		US 2013293411 A1	07-11-2013
		WO 2012098437 A1	26-07-2012
US 5565873 A	15-10-1996	GB 2281175 A	22-02-1995
		US 5565873 A	15-10-1996
US 2014354499 A1	04-12-2014	CA 2862729 A1	01-08-2013
		EP 2807702 A1	03-12-2014
		FR 2986377 A1	02-08-2013
		JP 2015505229 A	16-02-2015
		US 2014354499 A1	04-12-2014
		WO 2013110793 A1	01-08-2013