



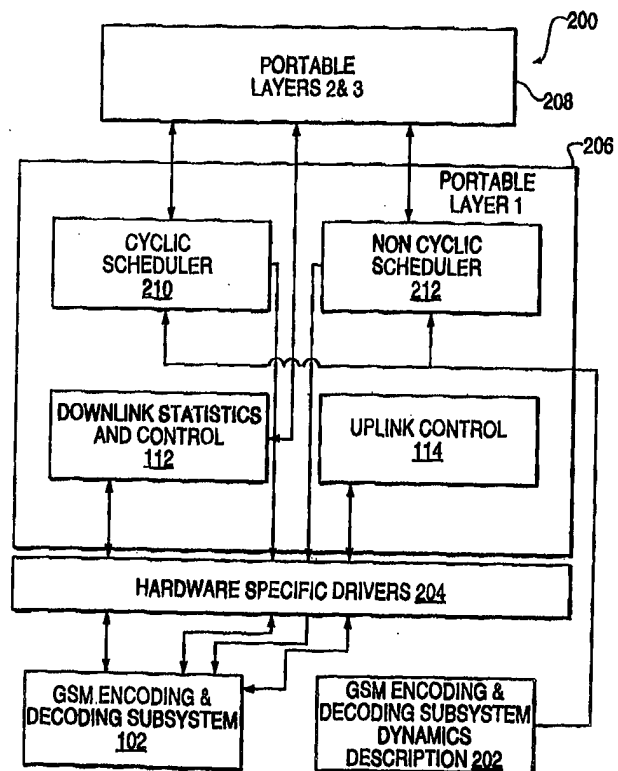
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<p>(21) International Application Number: PCT/US97/22788 (22) International Filing Date: 11 December 1997 (11.12.97) (30) Priority Data: 08/766,583 12 December 1996 (12.12.96) US (71) Applicant: OPTIMAY CORPORATION [US/US]; Jonathon R. Moore, Moore & Bruce, LLP, The Army and Navy Club Building, 1627 Eye Street, N.W., Washington, DC 20006 (US). (72) Inventor: CAGNEY, Francis; Holzstrasse 39, D-80469 Munich (DE). (74) Agent: STOUT, Donald, E.; Antonelli, Terry, Stout & Kraus, LLP, Suite 1800, 1300 North Seventeenth Street, Arlington, VA 22209 (US).</p>		<p>(81) Designated States: AL, AM, AU, AZ, BB, BG, BR, BY, CA, CN, CZ, EE, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, RO, RU, SD, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).</p> <p>Published <i>Without international search report and to be republished upon receipt of that report.</i></p>

(54) Title: GSM TRANSCEIVER WITH PORTABLE PROTOCOL STACK

(57) Abstract

A GSM transceiver unit (10), for use in a GSM network (84), having a multilayer portable protocol stack is disclosed. The multilayer protocol stack includes: a hardware layer (204) controlling communications to and from hardware (102), a first portable layer (206) configuring the hardware layer and controlling communications to and from the hardware layer and second and third portable layers (208) controlling communications to and from the first portable layer and utilizing the first portable layer for communications with the GSM network, the communications with the GSM network being time multiplexed into frames each having a fixed time duration and with each frame being divided into multiple segments each containing a plurality of bits includes, a dynamics description (202) containing at least one time delay with each time delay representing an integer multiple of the fixed time duration for a particular instruction to be scheduled in one of the frames and containing at least one time advance with each time advance representing an integer multiple of the fixed time duration for a particular instruction to be scheduled in one of the frames. The first portable layer has at least one scheduler (210, 212), with each scheduler being responsive to the dynamics description, for scheduling instructions in the frames with each instruction being either delayed or advanced by the at least one scheduler by an integer multiple of the fixed time duration for that instruction contained in the dynamics description. The hardware includes at least one processor (34, 76) for executing code implementing the at least one scheduler.



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Title**GSM TRANSCEIVER WITH PORTABLE PROTOCOL STACK****Technical Field**

The present invention relates to GSM transceiving
5 units and more particularly to portable multilayer
protocol stacks for use in GSM transceivers having
different hardware designs in which the
portable multilayer protocol stack is adaptable to
conform to different timing constraints of the different
10 hardware designs without complete rewriting thereof.

Background Art

The GSM communication system (global system for
mobile communications) is a TDMA telecommunications
system providing time multiplexed communications between
15 mobile units and base stations contained in the GSM
communication system. The GSM communication system,
including transceiver units, is defined by published
specifications which have been adopted over the years.
The totality of the GSM published specifications are
20 expressly incorporated by reference herein in their
entirety.

The functionality of a GSM transceiver in the GSM
communication system is defined by the aforementioned GSM
specifications and includes a multilayer protocol stack
25 containing software executed with a microprocessor.
A first layer of the protocol stack interfaces with the
hardware and controls communications to and from the
second and third protocol layers. The second and third
protocol layers control communications to and from the
30 first layer and utilize services provided by the first
protocol layer to communicate between the GSM network.

The communications between the GSM network and GSM transceivers are time multiplexed into GSM frames. Each GSM frame has a fixed time duration and is divided into multiple segments each containing a plurality of bits all in accordance with the aforementioned published GSM specifications.

Fig. 1 illustrates a block diagram of a prior art transceiving unit which is disclosed in a catalog entitled "ICs for Communications" published by Siemens AG and identified as Product Overview 09.95. Standard functional notations are utilized to identify the functional elements in the block diagram of Fig. 1. Only a brief overview description of Fig. 1 will be given to describe the overall design of a GSM transceiver in which the present invention may be practiced and its relationship to a GSM network.

The GSM transceiver 10 is a double conversion heterodyne PM receiver with phase shifting circuitry for I/Q demodulation. Antenna 12 is connected through filter 14 to low noise amplifier 16 which is in turn connected to filter 18. The output of filter 18 is connected to mixer 20 which shifts the received signal down to an intermediate frequency. The output of mixer 20 is connected to filter 22 and the output of filter 22 is connected to amplifier 24. The output of amplifier 24 is connected to mixer 26 which shifts the signal to the baseband. The output of mixer 26 is connected to amplifiers 28 whose I and Q outputs are respectively connected to filters 30 having outputs applied to A to D converters 32. The outputs of the A to D converters 32 are connected to a digital signal processor 34 which includes filters 36 which are connected to the outputs of the A to D converters 32, a soft equalizer 38 which is connected to the output of

the filters 36 and a speech and channel decoder 40. The output of the speech and channel decoder 40 is connected to filter 42 whose output is connected to D to A converter 44 whose output is applied to amplifier 46 which drives speaker 48 to provide audio to a user. Speech of the user is detected by microphone 50 which is connected to amplifier 52 having an output connected to A to D converter 54. The output of A to D converter 54 is connected to filter 56 having an output connected to speech and channel encoder 58. The outputs of speech and channel encoder 58 are connected to a GMSK encoder 60 having a pair of outputs which are applied to D to A converters 62 with the outputs thereof being connected to filters 64 which respectively output I and Q signals. The I and Q signals are connected to mixers 66 which are driven by RFVCO 68 to convert the signal from the baseband to the RF band. The output of mixers 66 is connected to output stage 68'. The output of output state 68 is connected to filter 70. The output of filter 70 is connected to output amplifier 72 which is controlled by a power amplifier control 74 in the form of a D to A converter. Microprocessor 76 controls the overall system including the power amplifier control 74 and provides a system interface 77. The system interface 77 generates chip select signals, internal clock signals, GSM specific control and timing signals via programmable timers for programmable interrupts on timer values and provides a chip card interface to a SIM card 78. The interface 77 also provides connectivity to a keypad 80. The microprocessor 76 is connected to a E²PROM 82, a flash memory 85, and RAM 86.

As illustrated, a GSM network 84, which is in accordance with GSM specifications including base stations and related switching architecture, transmits

and receives communications between individual transceiver units 10 via RF transmission 87. The communications are time multiplexed into GSM frames each containing 8 time slots each containing multiple bits. Base stations (not illustrated) of the GSM network 84 each have an antenna 88 which transmits and receives the aforementioned time multiplexed GSM frames.

Each GSM transceiver, such as the unit 10 illustrated in Fig. 1 in accordance with the published GSM specifications, has a multilayer protocol stack including first, second and third layers. Instructions must be issued to the hardware to allow the hardware to perform in accordance with the published GSM specifications in the GSM frames with either a frame advance or a frame delay which is required to be an integer multiple of the time duration of a GSM frame. This permits designers of hardware for implementing GSM transceivers to provide for pipeline frame delays or frame advances in terms of an integer multiple of the time duration of a GSM frame between the protocol stack and the hardware which suit the design requirements of the hardware. The first three layers of the GSM protocol stack conforms to the overall OSI network model for providing a universal multi-layer protocol stack.

In order to provide the functionality of the first three layers of the multilayer protocol stack of the GSM specifications, substantial software is required. This software requires substantial time and effort to write and is complex. Furthermore, because of the diversity of the designs used by the numerous manufacturers of chipsets used in GSM transceivers, the software required to implement the first three layers of the protocol stack of a GSM transceiver is uniquely suited to and developed for a particular chipset which

prevents the protocol stack from being portable to other chipsets and therefore usable with other chipsets without substantial rewriting of the code contained therein. A need exists in the art for a mechanism to permit the first three layers of the protocol stack in accordance with the GSM specifications to be utilized with hardware of diverse designs without requiring substantial rewriting of the software in compliance with the hardware timing requirements of the particular hardware to which the protocol stack is applied.

United States Patent 5,265,252 discloses a device driver system having a core which manages specific functions performed by a plurality of I/O devices. An operating system interface is generic to different operating systems. Each operating system has a device driver interface which is unique to the operating system. A conversion program is layered between the core and the operating system for converting communications between the device driver interface of the operating system interface of the core.

Fig. 2 illustrates a block diagram of a GSM prior art multiple layer protocol stack 100 of the type utilized with a transceiver unit 10 of Fig. 1. The overall protocol stack 100, as illustrated, may be associated with hardware 102 which is represented by the hardware 10 of Fig. 1. Layers 2 and 3 identified by reference numeral 104 are well known and comply with the published GSM specifications including timing requirements. Layer 1, which is identified by reference numeral 106, is comprised of multiple software modules which exist in diverse implementations for performing the overall functions contained in the layer 1 block diagram.

Cyclic scheduler 108 takes a GSM channel configuration description from layer 3 and arranges for

appropriate instructions to be given to the GSM encoding and decoding subsystem 102 at the required times in order for the required channel structure to be implemented. The channel configurations are described in GSM specifications 05.02, section 6.4. The cyclic scheduler 108 has software which is uniquely written for the particular GSM encoding and decoding subsystem 102 which prevents it from being portable and adaptable without substantial rewriting to be useful with other hardware configurations.

Non-cyclic scheduler 110 performs the task of scheduling instructions to be carried by out by layer 1 which do not occur on a cyclical basis. The scheduled instructions typically are requests from the layer 3 to deliver information about base stations other than the base station currently camped onto by the transceiver unit 10 which is controlled by the cyclical scheduler 108. The non-cyclical scheduler 110 finds idle GSM frames into which requests from the layer 3 can be placed without interfering with the ongoing work of the cyclic scheduler 108. The non-cyclic scheduler 110 has software which is uniquely written for the particular GSM encoding and decoding subsystem 102 which prevents it from being portable and adaptable without substantial rewriting to be useful with other hardware configurations.

Downlinked statistics and control 112 performs the task of monitoring the absolute radio frequency channel control number to determine the absolute power and reception quality as measured in accordance with GSM published specifications 05.08, chapter 8. The result is reported to the layer 3. Synchronization and MS carrier frequency are maintained as specified in GSM specifications 05.10, section 6.

Uplink control 114 functions to control the uplinked transmitted power of the MS on a frame by frame basis as ordered by the base station in accordance with published GSM specifications 05.08, section 4.7.

5 Layers 1-3 in prior art GSM transceivers 10 have specialized code which is unique to the associated particular hardware. This code typically has timing requirements for scheduling instructions which are unique to each hardware design. As a result, the programming
10 for implementing layers 1-3 for use with any particular hardware configuration of a particular chipset has little or no portability (adaptability without great reprogramming effort) to other hardware configurations.

One of the reasons, as stated above, why the prior
15 art layers 1-3 of the protocol stack are not applicable (portable) to different hardware designs is that the published GSM specifications only dictate that particular instructions are scheduled in the GSM frames in accordance with frame advances or frame delays which are
20 an integer multiple of the fixed time duration of each frame. However, because of the pipeline processing delays associated with different hardware designs and because the published GSM specifications do not specify anything more than the frame delays or frame advances for
25 scheduling instructions should be an integer multiple of the time duration of a GSM frame, each implementation of layers 1-3 has code written into it which specifies the particular frame advance or frame delay of scheduling different instructions in the GSM frames which is unique
30 to the particular frame delays and frame advances dictated by the associated hardware. As a result, code implementing layers 1-3 for a particular hardware design does not have portability to other hardware designs because the pipeline frame delays and frame advances

associated with communications between the hardware and the protocol stack are not fixed by the published GSM specifications.

5 A need exists in the art for portable GSM first, second and third protocol stack layers which may be utilized in different hardware designs without substantial rewriting of the code thereof.

Disclosure of Invention

10 The present invention is an improved GSM transceiver unit for use in a GSM network having a multilayer portable protocol stack which is adaptable to different hardware designs (processors, etc.) without substantial rewriting of the code thereof. In accordance with the invention, a generic cyclic scheduler and a generic
15 non-cyclic scheduler are adaptable to diverse hardware without rewriting of the code therein. In accordance with the invention, a subsystem dynamics description, which is a header file containing hardware specific time constants specifying a particular integer multiple of the
20 time duration of a GSM frame used for scheduling either frame advances or frame delays of particular instructions in a GSM frame, communicates with the generic portable cyclic scheduler and the generic portable non-cyclic scheduler to control execution of instructions by the
25 schedulers with the correct frame advances and frame delays required by the timing requirements of a particular hardware design. The subsystem dynamics description contains at least one frame delay and at least one frame advance with each frame delay and each
30 frame advance representing an integer multiple of the fixed time duration of a GSM frame for scheduling a particular instruction in one of the frames. As a result, the generic cyclic scheduler and non-cyclic

scheduler are portable to other hardware designs by only varying the contents of the subsystem dynamics description to specify the hardware time constants for each type of hardware design as a specified frame delay
5 or frame advance for scheduling each instruction in a GSM frame as an integer multiple of the time duration of a GSM frame. Each generic scheduler is responsive to the hardware time constants (an integer multiple of the time duration of a GSM frame) subsystem dynamics description
10 for scheduling instructions in the frames with each instruction being either delayed or advanced by an integer multiple of the fixed duration for that instruction contained in the dynamics description. At least one processor (typically, a microprocessor
15 and/or a digital signal processor) executes code implementing the at least one scheduler.

A hardware layer is provided between layer 1 of the protocol stack and the GSM encoding and decoding subsystem (system hardware, including at least one of the
20 aforementioned processors). The hardware layer is comprised of hardware specific drivers which are written specifically to provide communications to and from the specific hardware which is being interfaced to the portable layers 1-3. Each driver is not portable
25 (i.e. is not generic to all GSM transceivers) and must be written to satisfy the hardware communication requirements of each hardware design. The hardware layer controls communications between the hardware and portable layer 1. The portable layer 1 configures the hardware
30 layer and controls communications to and from the hardware layer and the second and third portable layers.

The cyclic scheduler provides a channel configuration description from layer 3 to the hardware layer to implement a channel configuration specified by

the GSM published specifications 05.02, section 6.4, under utilization of information obtained from the subsystem dynamics description and the non-cyclic scheduler schedules instructions to be executed by the hardware layer which do not occur on a cyclical basis, under utilization of information hardware specific time constants as an integer multiple of the time duration of a GSM frame for a particular instruction obtained from the dynamics description. The non-cyclic scheduler identifies segments in the frames into which the instructions may be placed without interfering with the cyclic scheduler, under utilization of information derived from the dynamics description.

As a result of the subsystem dynamics description being a file containing the required frame delay and frame advance hardware constants for scheduling of instructions into frames by both a cyclic scheduler and a non-cyclic scheduler for a particular hardware design having particular hardware specific timing requirements, generic scheduling software is provided in portable layer 1 which is applicable to diverse hardware designs. The subsystem dynamics description is varied to include scheduling hardware time constants in terms of integer multiples of a time duration of a frame for each instruction which satisfy the frame delays and frame advances associated with each hardware design. The time delays and advances are read by the cyclic and non-cyclic schedulers in the portable layer 1 such that each scheduler is responsive to the dynamics description to provide scheduling frame advances and frame delays which are an integer multiple of the fixed duration of each instruction contained in the subsystem dynamics description as executed in the cyclic and non-cyclic schedulers.

Diverse hardware constants each specifying a specified integer multiple of the fixed duration of a GSM frame for a different instruction to be scheduled are read from the subsystem dynamics description to support the functions of the cyclic scheduler and non-cyclic schedulers of the portable layer 1 for scheduling instructions in the frames. Consequently, the cyclic scheduler and non-cyclic schedulers are easily adapted to particular hardware designs without requiring a substantial rewriting of the code therein with only the subsystem dynamics description, including the hardware specific timing constants and the hardware specific drivers having to be rewritten, thus making the code of the cyclic scheduler and non-cyclic scheduler generic and portable.

Brief Description of the Drawings

Fig. 1 is a block diagram of a GSM transceiver and network in accordance with the prior art.

Fig. 2 is a block diagram of a GSM transceiver multiple layer protocol stack in accordance with the prior art.

Fig. 3 is a block diagram of a GSM transceiver multiple layer protocol stack in accordance with the present invention.

Like numbers identify like parts throughout the drawings.

Best Mode for Carrying Out the Invention

Fig. 3 illustrates an embodiment 200 of a protocol stack for a GSM transceiver in accordance with the present invention. The embodiment 200 of Fig. 3 differs from the prior art of Fig. 2 in that in accordance with the invention a GSM encoding and decoding subsystem

dynamics description 202 provides hardware time constants used for scheduling each instruction of the cyclic scheduler 210 and the non-cyclic scheduler 212 in frames to control the particular integer multiple of the fixed time duration of GSM frames which is assigned as either a frame delay or a frame advance for each instruction to be scheduled in one of the frames and further in that hardware specific drivers 204 are provided for interfacing between the specific hardware of the GSM encoding and decoding subsystem 102 and the portable layer 1. The rewriting of the dynamics description 202 and the hardware specific drivers 204 is all that is required to adapt the protocol stack to a different hardware design and requires substantially less effort than the rewriting of layers 1-3 of the prior art of Fig. 2. The generic cyclic scheduler 210 and the generic scheduler 212 and the downlink statistics control 112 and the uplink control 114 are generic to all hardware designs and do not require rewriting. The cyclic scheduler 210 and non-cyclic scheduler 212, instead of containing fixed code which is written specifically for a particular hardware configuration to be associated with the cyclic scheduler and non-cyclic scheduler, accesses the GSM encoding and decoding subsystem dynamics description 202 to obtain the hardware constants for particular instructions to be scheduled with an integer multiple of the fixed time duration of a frame which is assigned for scheduling a particular instruction in a frame as a frame delay or frame advance to make the software of the cyclic scheduler 210 and non-cyclic scheduler 212 generically operative in diverse hardware configurations having different frame advances or frame delays which are multiples of the GSM frame time interval.

The dynamics description 202 is used by the generic cyclic and non-cyclic schedulers 210 and 212 to set the particular frame advances and frame delays for the instruction set.

5 While the invention has been described in terms of its preferred embodiment, it should be understood that numerous modifications may be made thereto without departing from the spirit and scope of the invention as defined in the appended claims. For example, while
10 a preferred embodiment of the invention is a multiple layer protocol stack in a GSM transceiver, the invention is also applicable to telecommunications units having diverse applications. A telecommunications unit in accordance with the invention may be without limitation
15 a transmitter, receiver, transceiver or computer controlled device. It is intended that all such modifications fall within the scope of the appended claims.

Claims

1. A GSM transceiver unit, for use in a GSM network, having a multilayer protocol stack including a hardware layer controlling communications to and from hardware, a first portable layer configuring the hardware layer and controlling communications to and from the hardware layer and second and third portable layers controlling communications to and from the first portable layer and utilize services provided by the first portable layer for communications with the GSM network, the communications with the GSM network being time multiplexed into frames each having a fixed time duration and with each frame being divided into multiple segments each containing a plurality of bits comprising:
- 15 a dynamics description containing at least one frame delay with each frame delay representing an integer multiple of the fixed time duration for a particular instruction to be scheduled in one of the frames and containing at least one frame advance with each frame advance representing an integer multiple of the fixed time duration for a particular instruction to be scheduled in one of the frames;
- 20 the first portable layer having at least one scheduler, each scheduler being responsive to the dynamics description, for scheduling instructions in the frames with each instruction being either delayed or advanced by the at least one scheduler by an integer multiple of the fixed time duration for that instruction contained in the dynamics description; and
- 25 the hardware including at least one processor for executing code implementing the at least one scheduler.
- 30

2. A GSM transceiver in accordance with claim 1 wherein:

the at least one scheduler comprises a cyclic scheduler and a non-cyclic scheduler.

5 3. A GSM transceiver in accordance with claim 2 wherein:

the cyclic scheduler provides a channel configuration description from the third portable layer to the hardware layer to implement a channel configuration specified by GSM published specification 05.02, section 6.4, utilizing information obtained from the dynamics description.

4. A GSM transceiver in accordance with claim 2 wherein:

15 the non-cyclic scheduler schedules instructions to be executed by the hardware layer which do not occur on a cyclical basis utilizing information obtained from the dynamics description.

5. A GSM transceiver in accordance with claim 4 wherein:

the non-cyclic scheduler identifies segments in the frames into which the instructions may be placed without interfering with the cyclic scheduler, utilizing information obtained from the dynamics description.

25 6. A GSM transceiver unit, for use in a GSM network, having hardware and a multilayer protocol stack including a first portable layer controlling communications with the hardware and second and third portable layers controlling communications to and from
30 the first portable layer and services provided by the

first portable layer for communications with the GSM network, the communications with the GSM network being time multiplexed into frames each having a fixed time duration and with each frame being divided into multiple segments each containing a plurality of bits comprising:

5 a dynamics description containing at least one frame delay with each frame delay representing an integer multiple of the fixed duration for a particular instruction to be scheduled in one of the frames and

10 containing at least one frame advance with each frame advance representing an integer multiple of the fixed duration for a particular instruction to be scheduled in one of the frames;

the first portable layer having at least one

15 scheduler, each scheduler being responsive to the dynamics description, for scheduling instructions in the frames with each instruction being either delayed or advanced by the at least one scheduler by an integer multiple of the fixed duration for that instruction

20 contained in the dynamics description; and

the hardware including at least one processor for executing code implementing the at least one scheduler.

7. A GSM transceiver in accordance with claim 6

25 wherein:

the at least one scheduler comprises a cyclic scheduler and a non-cyclic scheduler.

8. A GSM transceiver in accordance with claim 7 wherein:

5 the cyclic scheduler provides a channel configuration description from the third portable layer to the hardware layer to implement a channel configuration specified by GSM published specification 05.02, section 6.4, utilizing information obtained from the dynamics description.

10 9. A GSM transceiver in accordance with claim 7 wherein:

the non-cyclic scheduler schedules instructions to be executed by the hardware layer which do not occur on a cyclical basis utilizing information obtained from the dynamics description.

15 10. A GSM transceiver in accordance with claim 9 wherein:

20 the non-cyclic scheduler identifies segments in the frames into which the instructions may be placed without interfering with the cyclic scheduler utilizing information obtained from the dynamics description.

11. A telecommunication unit, for use in a telecommunications network, having a multilayer protocol stack including a hardware layer controlling communications to and from hardware, a first portable layer configuring the hardware layer and controlling communications to and from the hardware layer and second and third portable layers controlling communications to and from the first portable layer and services provided by the first portable layer for communications with the telecommunications network, the communications with the

25

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telecommunications network being in frames each having a fixed time duration comprising:

a dynamics description containing at least one frame delay with each frame delay representing an integer multiple of the fixed time duration for a particular instruction to be scheduled in one of the frames and/or containing at least one frame advance with each frame advance representing an integer multiple of the fixed time duration for a particular instruction to be scheduled in one of the frames;

the first portable layer having at least one scheduler, each scheduler being responsive to the dynamics description, for scheduling instructions in the frames with each instruction being either delayed or advanced by the at least one scheduler by an integer multiple of the fixed time duration for that instruction contained in the dynamics description; and

the hardware including at least one processor for executing code implementing the at least one scheduler.

12. A telecommunications unit in accordance with claim 11 wherein:

the at least one scheduler comprises a cyclic scheduler and a non-cyclic scheduler.

13. A telecommunications unit in accordance with claim 12 wherein:

the cyclic scheduler provides a channel configuration description from the third portable layer to the hardware layer to implement a channel configuration utilizing information obtained from the dynamics description.

14. A telecommunications unit in accordance with claim 12 wherein:

the non-cyclic scheduler schedules instructions to be executed by the hardware layer which do not occur on a cyclical basis utilizing information obtained from the dynamics description.

15. A telecommunications unit in accordance with claim 14 wherein:

the non-cyclic scheduler identifies segments in the frames into which the instructions may be placed without interfering with the cyclic scheduler, utilizing information obtained from the dynamics description.

16. A telecommunications unit for use in a telecommunications network, having hardware and a multilayer protocol stack including a first portable layer controlling communications with the hardware and second and third portable layers controlling communications to and from the first portable layer and services provided by the first portable layer for communications with the telecommunications network, the communications with the telecommunication network being in frames each having a fixed time duration comprising:

a dynamics description containing at least one frame delay with each frame delay representing an integer multiple of the fixed duration for a particular instruction to be scheduled in one of the frames and/or containing at least one frame advance with each frame advance representing an integer multiple of the fixed duration for a particular instruction to be scheduled in one of the frames;

the first portable layer having at least one scheduler, each scheduler being responsive to the

dynamics description, for scheduling instructions in the frames with each instruction being either delayed or advanced by the at least one scheduler by an integer multiple of the fixed duration for that instruction
5 contained in the dynamics description; and

the hardware including at least one processor for executing code implementing the at least one scheduler.

17. A telecommunications unit in accordance with
10 claim 16 wherein:

the at least one scheduler comprises a cyclic scheduler and a non-cyclic scheduler.

18. A telecommunications unit in accordance with
claim 17 wherein:

15 the cyclic scheduler provides a channel configuration description from the third portable layer to the hardware layer to implement a channel configuration utilizing information obtained from the dynamics description.

20 19. A telecommunications unit in accordance with claim 17 wherein:

25 the non-cyclic scheduler schedules instructions to be executed by the hardware layer which do not occur on a cyclical basis utilizing information obtained from the dynamics description.

20. A GSM transceiver in accordance with claim 19
wherein:

the non-cyclic scheduler identifies segments in
the frames into which the instructions may be placed
5 without interfering with the cyclic scheduler utilizing
information obtained from the dynamics description.

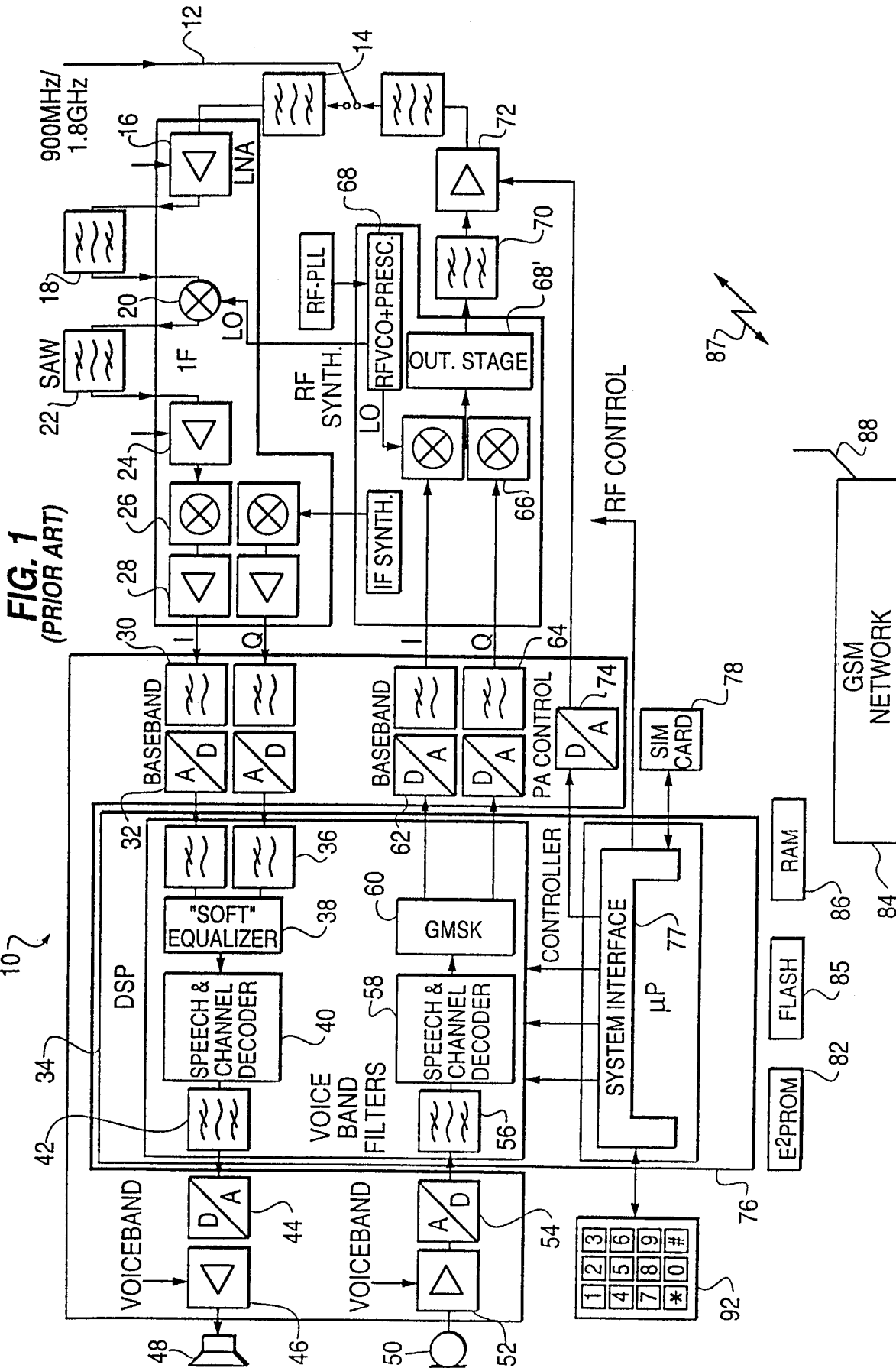


FIG. 2
(PRIOR ART)

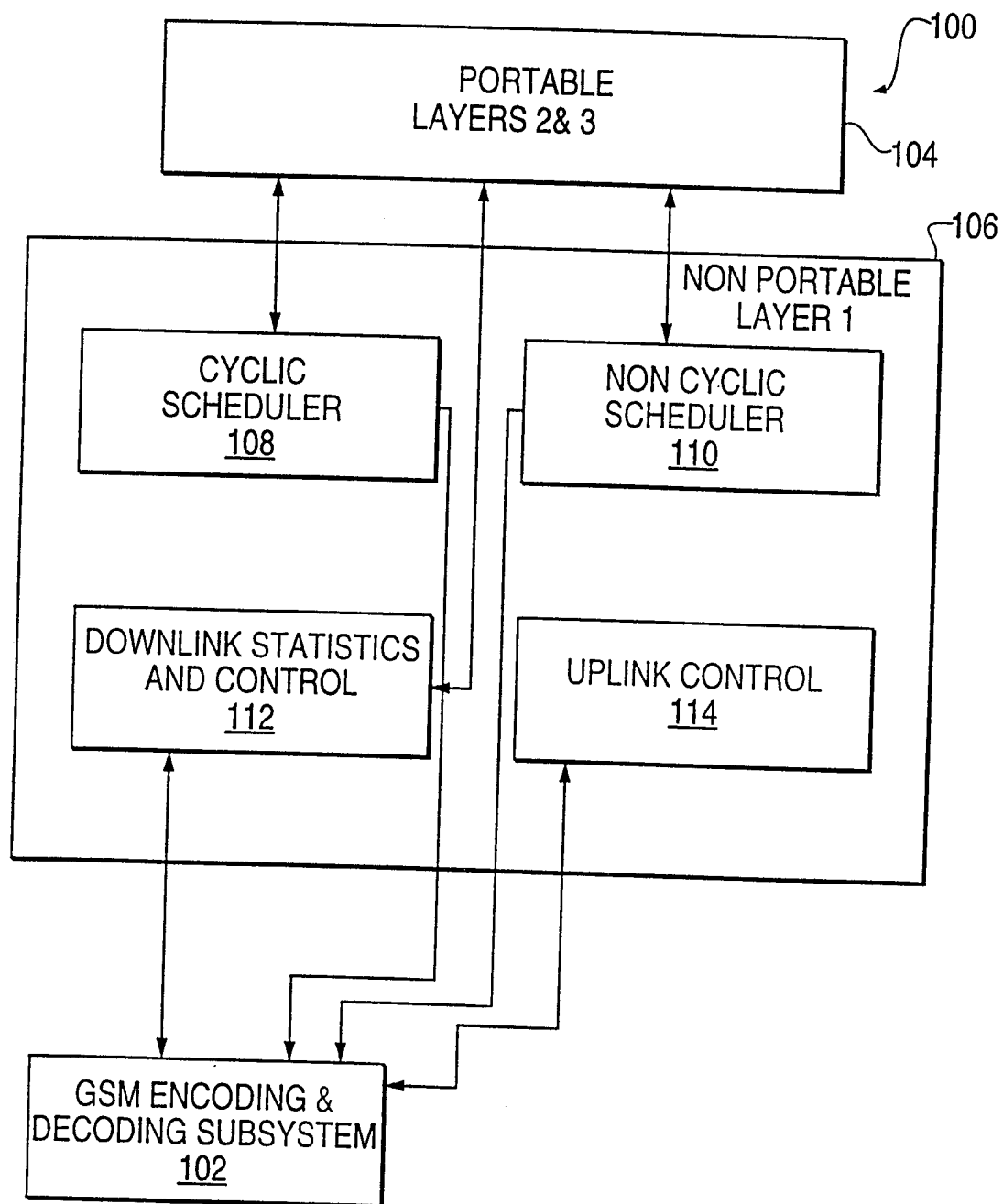


FIG. 3

