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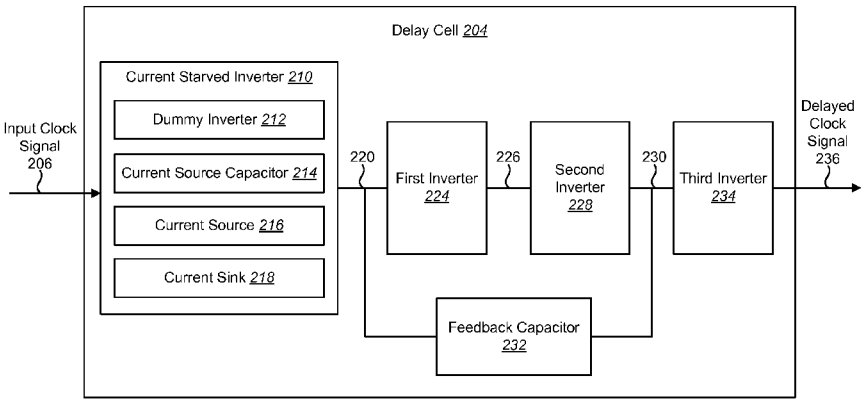

FIG. 2

(57) Abstract: An integrated circuit for delaying a clock signal using a delay cell is described. The integrated circuit includes a current starved inverter. The current starved inverter includes a switched capacitor current source with a first dummy inverter, a first amplifier coupled to the first dummy inverter and a first capacitor coupled to the first amplifier via a first switch. The current starved inverter also includes a first transistor coupled to the current source. The integrated circuit also includes a second capacitor. A delay applied to the clock signal is dependent on a ratio between the first capacitor and the second capacitor. The first capacitor and the second capacitor may be located in proximity such that process, voltage and temperature variations affect the first capacitor and the second capacitor similarly and the delay applied to the clock signal is independent of process, voltage and temperature variations

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