(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 November 2010 (25.11.2010)

PCT

(10) International Publication Number
WO 2010/135477 A1

(51) International Patent Classification:
H03K 19/177 (2006.01)

(21) International Application Number:
PCT/US2010/035487

(22) International Filing Date:
19 May 2010 (19.05.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/468,762 19 May 2009 (19.05.2009) US

(71) Applicant *(for all designated States except US)*: **SILICON STORAGE TECHNOLOGY, INC.** [US/US]; 1020 Kifer Road, Sunnyvale, CA 94086 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **SYU, Tsung-lu** [CN/US]; 203 Mission Tierra Place, Fremont, CA 94539 (US). **YEE, Wilson, Kaming** [US/US]; 4139 Angela Place, Pleasanton, CA 94566 (US).

(74) Agent: **LIMBACH, Alan, A.**; Dla Piper LLP US, 2000 University Avenue, East Palo Alto, CA 95404 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: A PROGRAMMABLE INTEGRATED CIRCUIT HAVING BUILT IN TEST CIRCUIT

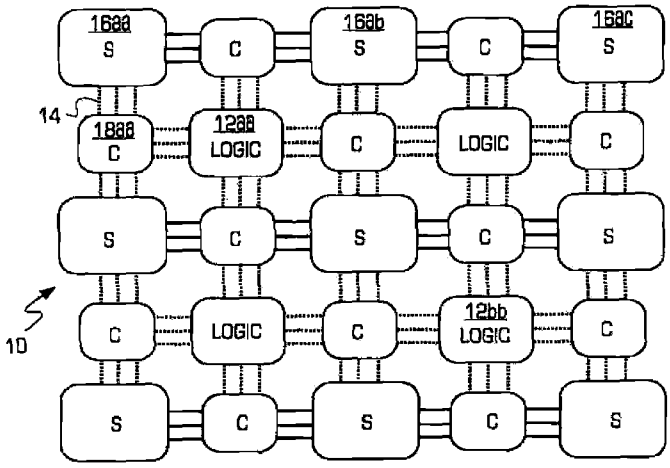


FIG. 1 (PRIOR ART)

(57) **Abstract**: A programmable integrated circuit has a plurality of logic elements with each logic element having a plurality of input leads and at least one output lead. The programmable integrated circuit further comprises a group of interconnect lines, and a first set of programmable circuits for electrically connecting the input and output leads of the plurality of logic elements to each other through the group of interconnect lines. The programmable integrated circuit further comprises a test circuit having at least one input and one output. Further the programmable integrated circuit comprises a second set of programmable circuits for electrically connecting the one output of the test circuit to the plurality of input leads of each of the plurality of logic elements and for electrically connecting the at least one output lead of each of the plurality of logic elements to the one input of the test circuit, through the group of interconnect lines.

WO 2010/135477 A1

A PROGRAMMABLE INTEGRATED CIRCUIT HAVING BUILT IN TEST CIRCUIT

TECHNICAL FIELD

[0001] The present invention relates to a programmable integrated circuit having a built in test circuit to reduce the test time of the programmable integrated circuit.

BACKGROUND OF THE INVENTION

[0002] Programmable integrated circuit devices are well known in the art. See for example U.S. Patent Re 34,363, whose disclosure is incorporated herein by reference in its entirety. Such devices can be programmed at the factory or in the field. In the case of the latter, they can be referred to as FPGA (Field Programmable Gate Array). Typically, they comprise an array of logic elements, each of which can be programmed to perform a particular logical function. In addition, a plurality of interconnect lines surround the plurality of logic elements. Each of the logic elements may be programmably connected to the plurality of interconnect lines. In addition, the interconnect lines may be programmably routed to supply signals to different logic elements.

[0003] Referring to Figure 1 there is shown a block level diagram of a programmable integrated circuit device 10 of the prior art, as disclosed in Re 34,363. The device 10 comprises an array of logic elements 12 arranged in a plurality of rows and columns. Each of the logic elements 12 can be programmed to perform a particular logic function, such as AND, OR or other logic functions. Each row of logic elements 12 is separated from one another, and each column of logic elements 12 is also separated from one another. Between the separation of the rows of logic elements 12 and the columns of logic elements 12 is a group of interconnect lines 14. The group of interconnect lines 14 comprises a plurality of lines 14. The group of lines 14 pass through a plurality of switches 16, which are also arranged in a plurality of rows and columns. Each of the switches 16 routes the connection of the interconnect lines from rows to columns or vice-versa. The group of interconnect lines 14 are also connected to a plurality of connection boxes 18. Each of the connection boxes 18 connects one or more of the group of interconnect lines 14 to an associated logic element 16.

[0004] Each of the logic element 12 has a plurality of input leads, which are connected to the group of interconnect lines 14, through an associated connection box 18. Further, each of the logic element 12 has at least one output lead, which is also connected to the group of interconnect lines 14 through an associated connection box 18. In this manner, the logic function of each logic element 12 can be changed, as well as the routing of the signals to/from each logic element 12 to other logic elements 12 can be changed.

[0005] Referring to Figure 2 there is shown in greater detail a portion of the device 10 shown in Figure 1. In particular, Figure 2 shows in greater detail the group of interconnect lines 14 as comprising a plurality of lines 14, connected to a switch 16 and to a connection box 18 and to a logic element 12.

[0006] Referring to Figure 3 there is shown in greater detail a circuit diagram of a common component of a logic element 12 in the nature of a Look-up Table (LUT). Another common component of a logic element is a D-flipflop (not shown). A plurality of input leads 21 is shown, connected to the logic element 12. The input leads 21 are "decoded" by logic gates 22. The resulting signals are used to select one of the memory elements 20 to be programmably connected to output lead 24. As previously discussed, the input leads 21 and the output lead 24 are connected to the group of interconnect lines 14, so that the signals on those input/output leads 21/24 can be routed to other logic elements 12. The set of memory elements 20 are used to configurable the LUT to the desired function. Typically, these memory elements may be SRAM cells or non-volatile cells like Flash or fuses. A logic element 12 may contain one or more LUTs and one or more D-flipflops.

[0007] The problem with the device 10 is that as the scale of integration increases, more and more logic elements 12 can be fabricated on a single integrated circuit die. For example, in 1990, a single programmable logic device may contain hundreds of LUTs, whereas it is possible today to integrate hundreds of thousand LUTs in a single die. As the number of LUTs are placed on a single integrated die increases, the testing of each of the logic elements 12 becomes increasingly time consuming. While it is very probable that not all gates or logic elements 12 will be used, once the device 10 is manufactured, nevertheless, the manufacturer of the device 10 must test each and every gate or logic element 12. Thus, increasingly, testing has become a larger cost portion of the fabrication of the device 10.

[0008] More importantly, much of the test time associated with logic elements 12 is the time it takes to write new information into the memory cells 20. For memory cells 20 that have very long write times, such as Flash memory cells, the test time will be proportionally long.

[0009] It is, therefore, an object of the present invention to reduce the test time of an integrated circuit device having a plurality of programmable logic elements.

SUMMARY OF THE INVENTION

[0010] In the present invention, a programmable integrated circuit comprises a plurality of logic elements with each logic element having a plurality of input leads and at least one output lead. The programmable integrated circuit further comprises a group of interconnect lines, and a first set of programmable circuits for electrically connecting the input and output leads of the plurality of logic elements to each other through the group of interconnect lines. The programmable integrated circuit further comprises a test circuit having at least one input and one output. Further the programmable integrated circuit comprises a second set of programmable circuits for electrically connecting the one output of the test circuit to the plurality of input leads of each of the plurality of logic elements and for electrically connecting the at least one output lead of each of the plurality of logic elements to the one input of the test circuit, through the group of interconnect lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 block level diagram of a programmable integrated circuit device of the prior art.

[0012] Figure 2 detailed block level diagram of a portion of the programmable integrated circuit device shown in Figure 1, showing the switch box for routing the interconnect lines and the connection element for connecting the interconnect lines to the input/output leads of a logic element.

[0013] Figure 3 is a detailed circuit diagram of an example of a look up table (LUT), a common component of a logic element that can be used in the programmable integrated circuit device of Figure 1.

[0014] Figure 4 is a block level diagram of a programmable integrated circuit device of the present invention.

[0015] Figure 5 is a detailed circuit diagram of a first example of a look up table, a common component of a logic element that can be used in the programmable integrated circuit device of the present invention shown in Figure 4.

[0016] Figure 6 is a detailed circuit diagram of a second example of a look up table, a common component of a logic element that can be used in the programmable integrated circuit device of the present invention shown in Figure 4.

[0017] Figure 7 is a detailed circuit diagram of a D-flipflop, another common component of a logic element that can be used in the programmable integrated circuit device of the present invention shown in Figure 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0018] Referring to Figure 4 there is shown a block level diagram of an integrated circuit device 110 of the present invention. The device 110 comprises an array of logic elements 12 arranged in a plurality of rows and columns. Each of the logic elements 12 can be programmed to perform a particular logic function, such as AND, OR or other logic functions. Each row of logic elements 12 is separated from one another, and each column of logic elements 12 is also separated from one another. Between the separation of the rows of logic elements 12 and the columns of logic elements 12 is a group of interconnect lines 14 (not shown). The group of interconnect lines 14 comprises a plurality of lines 14. The group of lines 14 pass through a plurality of switches 16 (not shown), which are also arranged in a plurality of rows and columns. Each of the switches 16 routes the connection of the interconnect lines from rows to columns or vice-versa. The group of interconnect lines 14 are also connected to a plurality of connection boxes 18 (not shown). Each of the connection boxes 18 connects one or more of the group of interconnect lines 14 to an associated logic element 16. Thus far, all of the foregoing described elements are shown and described in Figure 1, and in U.S. Patent Re 34,363, whose disclosure is incorporated herein by reference in its entirety.

[0019] The device 110 further comprises a testing circuit 120, which comprises a built-in testing circuit 122, whose output is connected to a test pattern generator circuit 124. Finally, the testing circuit 120 also comprises an Output Response Analyzer circuit 126 which receives the output from each of the logic elements 12. The test pattern generator circuit 124 generates a series or plurality of test signals. The test signals are supplied to a plurality of lines 130, which in the preferred embodiment is the same as the group of interconnect lines 14 for the device 110 to connect the logic elements 12. Alternatively, the group of lines 130 to which the test signals from the test pattern generator circuit 124 is connected may be a group of lines different from the group of interconnect lines 14. In any event, the lines 130 are supplied to all of inputs of the logic elements 12.

[0020] In the preferred embodiment, each of the logic elements 12 further comprises a multiplexer 132 to each of the LUT components. Each of the multiplexer 132 has two groups of inputs: a first group to receive the inputs 120 that are otherwise connected to the memory cells 20 and the second group of input to the multiplexer 132 is connected to the lines 130. One of the lines 134 from lines 130 is used to control the multiplexer 132, i.e. to either switch the multiplexer 132 so that the test signals from the test pattern generator circuit 124 is connected to the inputs of the logic element 12 or the signals from the memory cells 20 are supplied to the inputs to the logic element 12.

[0021] Each of the logic elements 12, as described heretofore, outputs at least one signal along the output 24, which is supplied to the group of interconnect lines 14. However, from each logic element 12, the output 24 is also supplied to the input of an AND gate 140 and to the input of an OR gate 142. The plurality of AND gates 140 from each of the logic elements 12 are connected in series. Thus, the output of an AND gate 140 from one logic element 12 is supplied as an input to an adjacent AND gate 140, with the other input to that AND gate 140 from the output 24 of that associated logic element 12. In this manner all of the AND gates 140 are connected serially in a string like configuration. The input to the first AND gate 140 is connected to a high voltage. Thus, if the output 24 of the logic element 12aa for the first AND gate 140 is high, the output of the AND gate 140 for the logic element 12aa will also be high. In this manner if the outputs 24 of all of the logic elements 12 are high, then the output of the last AND gate 140 in the string will also be high. However, if one of the logic elements 12 outputs a low output 24, indicating a failure, then the string of AND gates 12 will also be low.

[0022] The output 24 of each logic element 12 is also connected to the input of an OR gate 142. Similar to the connection of the output 24 to the AND gates 140, the plurality of OR gates 142 from each of the logic elements 12 are connected in series. Thus, the output of an OR gate 142 from one logic element 12 is supplied as an input to an adjacent OR gate 142, with the other input to that OR gate 142 from the output 24 of that associated logic element 12. In this manner all of the OR gates 142 are connected serially in a string like configuration. The input to the first OR gate 142 is connected to a low voltage. Thus, if the output 24 of the logic element 12aa for the first OR gate 142 is low, the output of the OR gate 142 for the logic element 12aa will also be low. In this manner if the outputs 24 of all of the logic elements 12 are low, then the output of the last OR gate 142 in the string will also be low. However, if one of the logic elements 12 outputs a high output 24, indicating a failure, then the string of OR gates 142 will be high.

[0023] Thus, by supplying the same test signal to all of the logic elements 12 of the device 110, all of the logic elements 12 of the device 110 can be tested simultaneously, with the need to check only one signal.

[0024] If a logic element 12 has multiple outputs 24, then multiple AND and OR gate chains can be used to implement the same function described earlier.

[0025] Referring to Figure 5, there is shown a detailed circuit diagram of the Look-up Table component of logic element 12 portion of the device 110 of the present invention. The test signals supplied on the lines 130 are supplied to the multiplexers 132 to which the memory cell outputs 20 are also supplied. The output of each multiplexer 132 is then supplied to the logic element 12 for further processing in accordance with the logic circuit 22.

[0026] Referring to Figure 6, there is shown a detailed circuit diagram of another embodiment of Look-up Table component of the logic element 12 portion of the device 110 of the present invention. The embodiment shown in Figure 6 is similar to the embodiment shown in Figure 5. The lines 130 from the test pattern generator 124 are supplied to the inputs of the multiplexer 132 to which inputs to the logic circuits 22 are also supplied,. In addition, the line that controls each of the multiplexers 132 for controlling the switching of the input signals to the logic element 12 also controls the multiplexers 132 that control the supplying of the signals 21 from the Connection Box 18 to the LUT. The enhancement allows the application of test signals 130 to all input signals of the LUT.

[0027] Referring to Figure 7 there is shown a D-flipflop 26, another common components of the logic element 12. The data input to D-flipflop 26 comes from the Connection Box 18 via signal 21. The polarity of the clock input is programmable by memory cell 20 via multiplexer 25. To enhance test time of the D-flipflop 26, multiplexers 132 are added to allow test signals 130 to replace the normal input signals 21 and signals from memory cell 20. Figure 7 illustrates another application of the same apparatus described in Figure 5 and Figure 6.

[0028] From the foregoing it is seen that although a test circuit 120 is provided in the same integrated circuit die as the integrated circuit device 110, thereby using up precious semiconductor "real estate", the addition of the testing circuit 120 actually reduces the cost of the integrated circuit die 110 because testing time is reduced.

What Is Claimed Is:

1. An integrated circuit device comprising:

a plurality of logic elements, each logic element having a plurality of input leads and at least one output lead, and having a programmable circuit to cause said logic element to perform a selected logic function;

a group of interconnect lines;

a first programmable connection circuit for programmably connecting each of said input leads of a logic element to at least one of said group of interconnect lines, and for programmably connecting said at least one output lead of a logic element to at least one of said group of interconnect lines;

a programmable switch circuit for programmably connecting each of said interconnect lines to at least one other of said interconnect lines;

whereby each of said logic elements can be programmed to perform a selected one of a plurality of logic functions, and said logic elements can be connected to each other in a selectable manner;

a testing circuit for generating at least one test signal and having a plurality of output leads and for receiving at least one input lead; and

a second programmable connection circuit for programmably connecting each of said output leads of the testing circuit to each of said input leads of each logic element, and for programmably connecting said at least one output lead of each logic element to at least one input lead of said test circuit;

whereby each of said logic elements can be tested by the testing circuit.

2. The integrated circuit device of claim 1 wherein said testing circuit further comprises:

a test pattern generator circuit for generating a plurality of different test signals supplied on said output leads.

3. The integrated circuit device of claim 2 wherein said testing circuit further comprises:

a response analyzer circuit for analyzing signals received on said at least input lead connected to said plurality of logic elements.

4. The integrated circuit device of claim 1 wherein said programmable switch circuit for programmably connecting each of said interconnect lines to at least one other of said interconnect lines comprises a non-volatile transistor.

5. The integrated circuit device of claim 4 wherein said non-volatile transistor is a split gate floating gate transistor.

6. The integrated circuit device of claim 1 wherein said programmable circuit in each logic element to cause said logic element to perform a selected logic function comprises transistors.

7. The integrated circuit device of claim 6 wherein said programmable circuit further comprises a plurality of memory cells controlling said transistors.

8. The integrated circuit device of claim 7 wherein said plurality of memory cells form at least a part of a shift register, with control signals loaded into said memory cells by being transferred through said shift register until each of said control signals is located in said memory cells.

9. The integrated circuit device of claim 1 wherein said plurality of logic elements are arranged in an array.

10. A programmable integrated circuit comprising:

a plurality of logic elements, each logic element having a plurality of input leads and at least one output lead;

a group of interconnect lines;

a first set of programmable circuits for electrically connecting said input and output leads of said plurality of logic elements to each other through said group of interconnect lines;

a test circuit having at least one input and one output; and

a second set of programmable circuits for electrically connecting said one output of said test circuit to the plurality of input leads of each of said plurality of logic elements and

for connecting said at least one output lead of each of said plurality of logic elements to said one input of said test circuit, through said group of interconnect lines.

11. The programmable integrated circuit of claim 10 wherein said test circuit further comprises:

a test pattern generator circuit for generating a plurality of different test signals supplied on said one output.

12. The programmable integrated circuit of claim 11 wherein said test circuit further comprises:

a response analyzer circuit for analyzing signals received on said at least input connected to said at least one output lead of each of said plurality of logic elements.

13. The programmable integrated circuit of claim 10 wherein said first set of programmable circuits programmably connects each of said interconnect lines to at least one other of said interconnect lines.

14. The programmable integrated circuit of claim 13 wherein said first set of programmable circuits comprises a non-volatile memory transistor.

15. The programmable integrated circuit of claim 10 wherein each of said logic elements comprises a programming circuit to cause said logic element to perform a selected logic function.

16. The programmable integrated circuit of claim 15 wherein said programming circuit further comprises a plurality of transistors, and a plurality of memory cells each memory cell controlling a corresponding transistor.

17. The programmable integrated circuit of claim 16 wherein said plurality of memory cells form at least a part of a shift register, with control signals loaded into said memory cells by being transferred through said shift register until each of said control signals is located in said memory cells.

18. The programmable integrated circuit of claim 10 wherein said plurality of logic elements are arranged in an array.

19. A programmable integrated circuit comprising:

a plurality of logic elements, each logic element having a plurality of input leads and at least one output lead, arranged in an array having a plurality of rows and a plurality of columns;

a group of interconnect lines, programmably connected to the plurality of input leads of each of said logic elements and programmably connected to at least one output lead of each of said logic elements, said group of interconnect lines arranged between rows of logic elements and between columns of logic elements;

a first set of programmable circuits for electrically routing signals supplied on said group of interconnect lines to various logic elements;

a test circuit having at least one input and one output; and

a second set of programmable circuits for electrically connecting said one output of said test circuit to the plurality of input leads of each of said plurality of logic elements and for connecting said at least one output lead of each of said plurality of logic elements to said one input of said test circuit, through said group of interconnect lines.

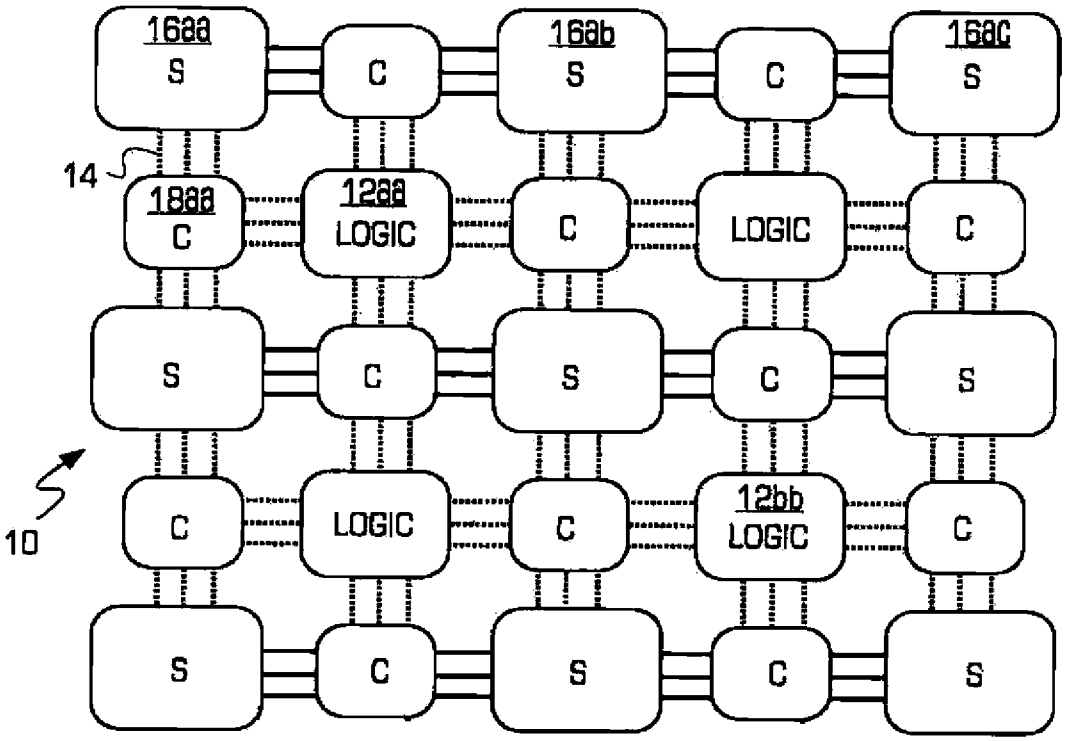


FIG. 1 (PRIOR ART)

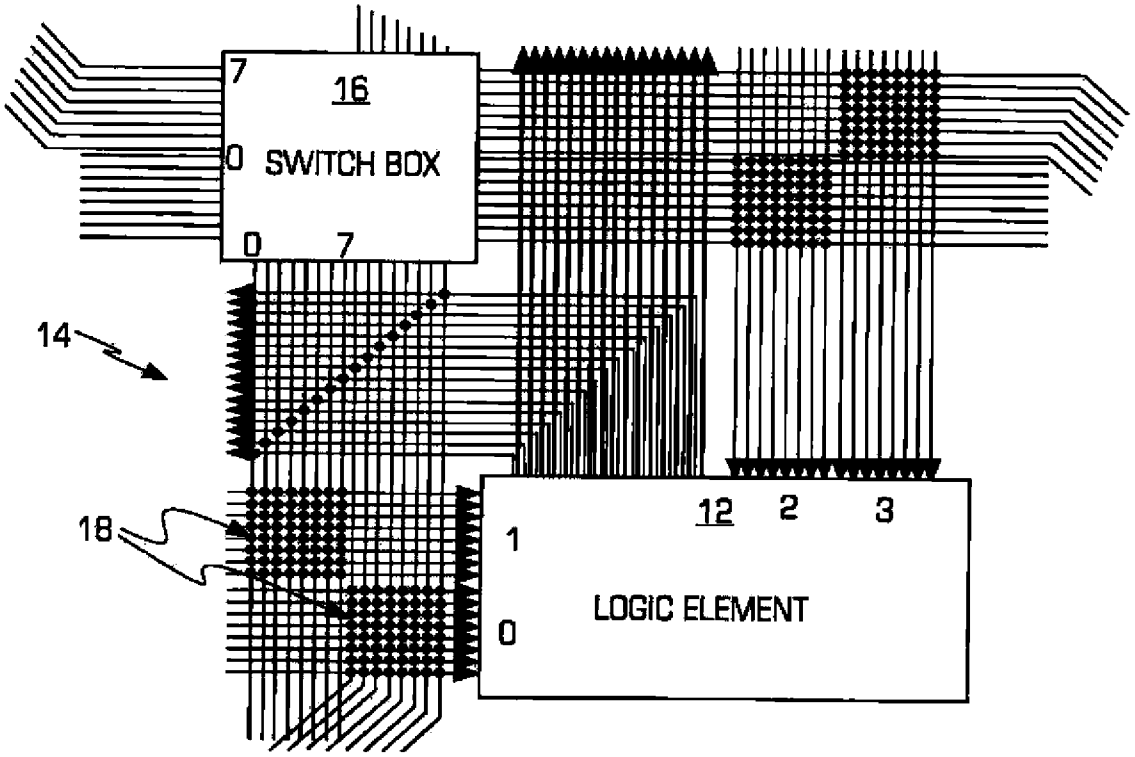


FIG. 2 (PRIOR ART)

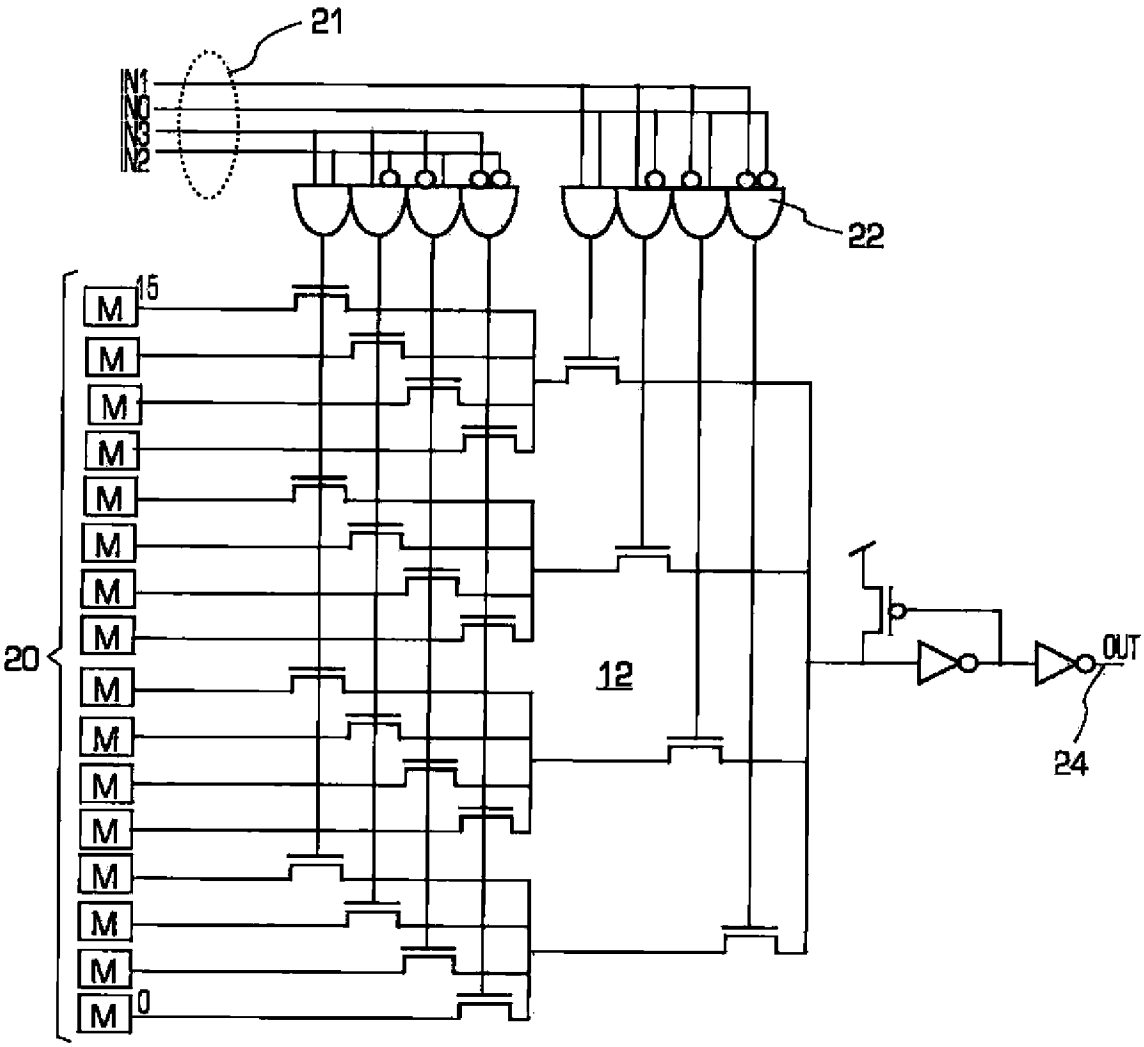


FIG. 3 (PRIOR ART)

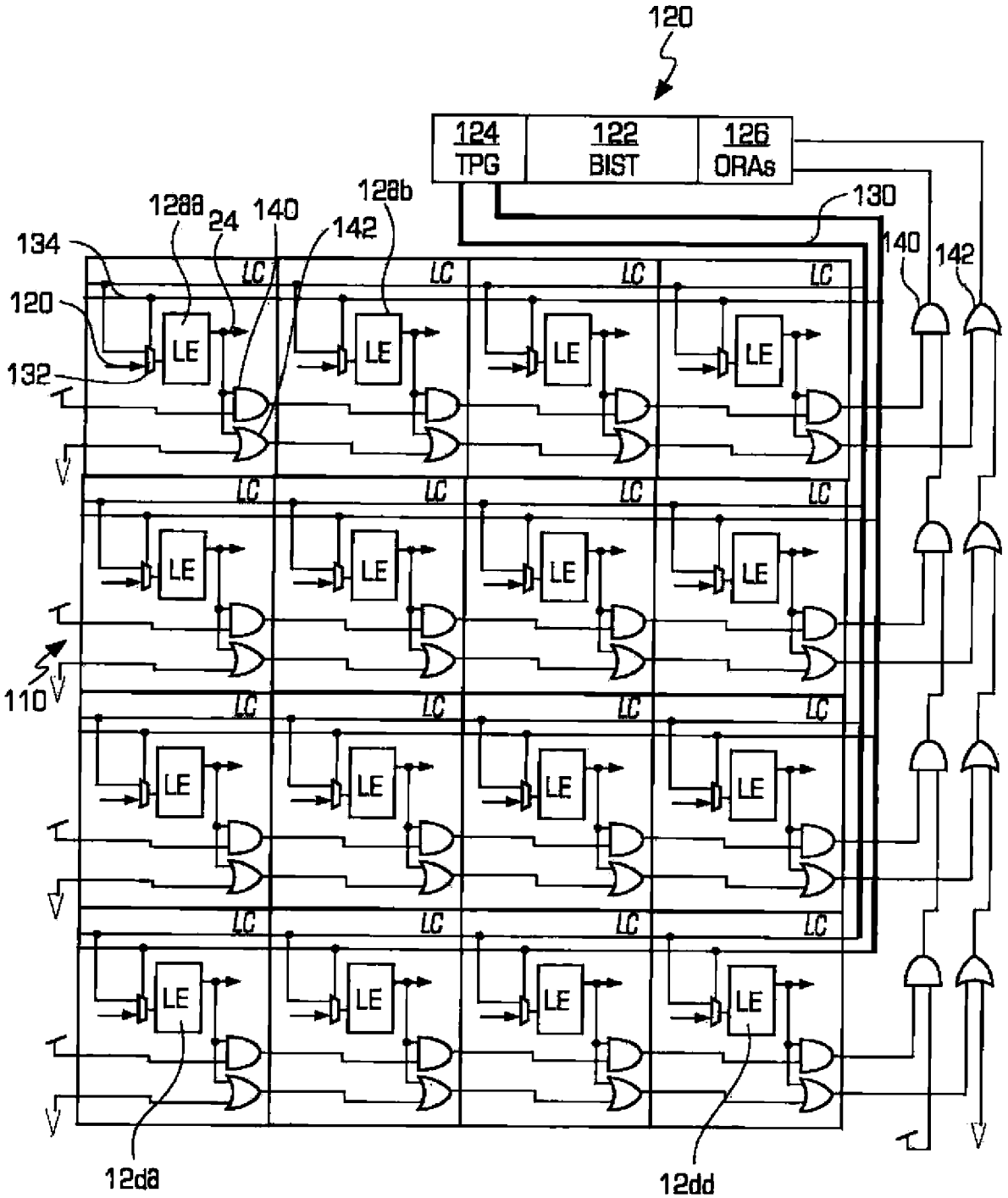

120
124
TPG
122
BIST
126
ORAs
130
128a
24
140
142
128b
134
120
132
110
LE
LC
12d8
12dd

FIG. 4

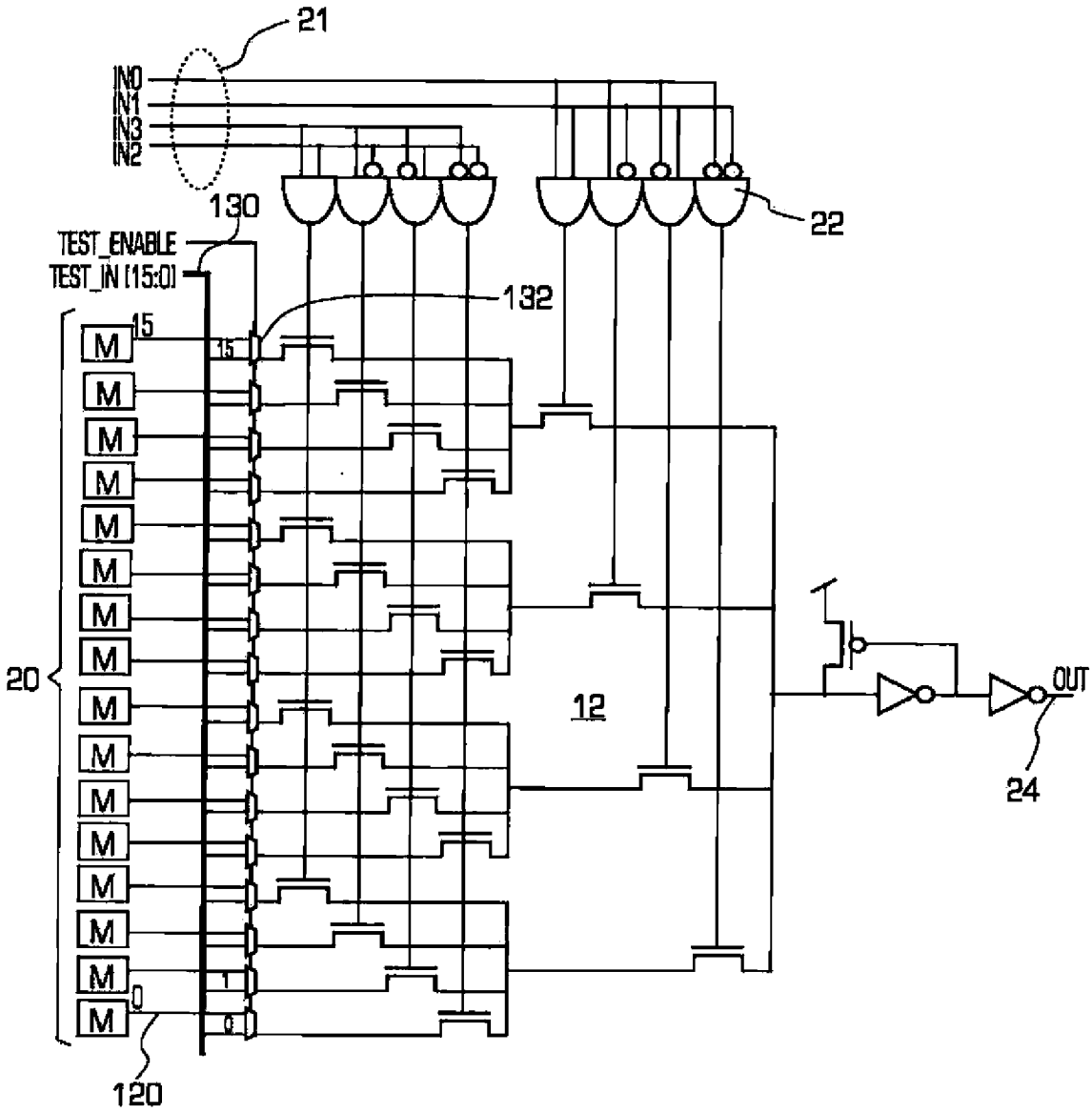

21
IN0
IN1
IN3
IN2
130
22
TEST_ENABLE
TEST_IN [15:0]
132
15
M
20
12
OUT
24
0
120

FIG. 5

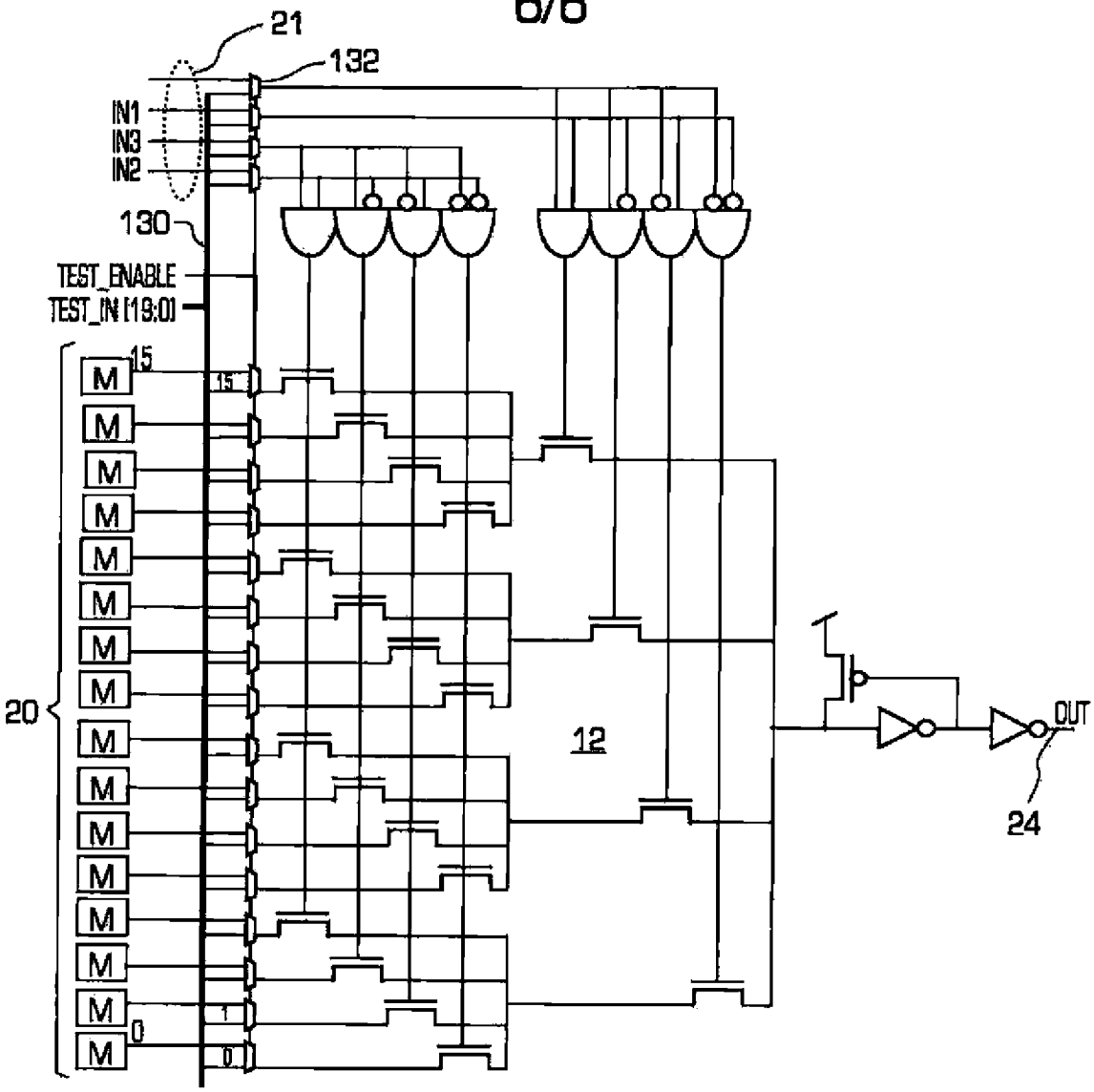

21
132
IN1
IN3
IN2
130
TEST_ENABLE
TEST_IN[1:0]
15
M
M
M
M
M
M
M
M
M
M
M
M
M
M
M
M
0
20
12
OUT
24

FIG. 6

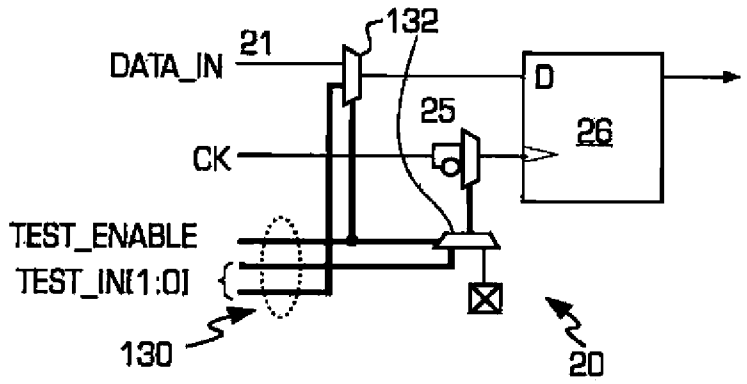

DATA_IN
21
132
D
25
26
CK
TEST_ENABLE
TEST_IN[1:0]
130
20

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US10/35487

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8): **H03K 19/177**(2006.01),**H03K 19/00**

USPC: 326/16,41
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 326/16,41,38-40,46,47

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,239,611 B1 (MATERA) 29 May 2001 (29.05.2001)	1-19
A	US 6,529,040 B1 (CARBERRY et al) 04 March 2003 (04.03.2003)	1-19

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 June 2010 (15.06.2010)	21 JUN 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No.	Authorized officer Lee Young Telephone No. 571-272-4549

Janice Ford for

Form PCT/ISA/210 (second sheet) (April 2007)

Continuation of B. FIELDS SEARCHED Item 3:
Search Text: US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT, IBM_TDB
Search Terms: mux or multiplexer, element, logic, interconnect, programmable, switch, logic, volatile, transistor,circuit, memory, cell